IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received May 6, 2022, accepted May 14, 2022, date of publication May 18, 2022, date of current version May 24, 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3176110

Reduced Voltage Stress Asymmetrical Multilevel Inverter With Optimal Components

DEVALRAJU PRASAD, (Graduate Student Member, IEEE), AND C. DHANAMJAYULU, (Senior Member, IEEE)
School of Electrical Engineering, Vellore Institute of Technology, Vellore, Tamilnadu 632014, India

Corresponding author: C. Dhanamjayulu (dhanamjayulu.c@vit.ac.in)

This work was supported by Vellore Institute of Technology, Vellore, Tamilnadu, India through the research fund Research Grant In Engineering, Management & Science (RGEMS) under VIT SEED GRANT/12439.

ABSTRACT The article presents a single phase asymmetrical multilevel inverter with a reduced components and low voltage stress which reduces the size and cost of the system. The structure provides a maximum output voltage of 23 levels with asymmetrical DC sources. There exists several reliability issues in lowering the total harmonic distortion (THD) by utilizing higher components in the design of MLI despite of its merits. Achieving reliability and lowering the THD is a challenging task for the researchers. The proposed 23-level MLI has been investigated with various performance parameters like total voltage standing (TSV), cost function (CF), power loss and efficiency analysis. The suggested MLI is compared with the existing topologies in the recent past and found that it has less voltage stress across the switches and cost-effective. The TSV calculations show that the proposed structure is more efficient in reducing the losses and increasing the efficiency. Hence, based on the evaluations and the comparisons made with the other topologies, it is found that the proposed MLI is well suited for the medium power applications such as FACTS, SVC, DSTATCOM and DVR. As the proposed architecture provides the 23 level output voltage values with asymmetrical DC sources, the configuration can be utilized for improving power quality in grid-connected renewable energy sources. The topology provides a less THD value which is under IEEE standards. The proposed architecture has been designed in MATLAB/Simulink and is implemented experimentally in hardware prototype in the laboratory environment.

INDEX TERMS Multilevel inverter, maximum blocking voltage, normalized voltage stress, cost function, TSV calculation, total harmonic distortion (THD).

I. INTRODUCTION

Multilevel inverters (MLI) have gained abundant interest in recent decades because of their benefits of reduced dv/dt stress, greater electromagnetic compatibility, lesser total harmonic distortion (THD), and superior output waveforms. As a result, these are preferred in high-voltage applications including AC drives, renewable energy, FACTS, and dynamic voltage restorer (DVR) etc., [1]. MLI was first developed in 1975 by Baker and Bannister [2]. Cascaded H-bridge type (CHB) MLI is a common name for the topology, which consists of multiple series-connected H-bridges. The flying capacitor (FC), cascaded H-bridge (CHB), and neutral point clamped (NPC) techniques are the three most common MLI topologies. CHB has captured the market's interest and is extensively utilized by sectors due to features such as simplicity and adaptability, however, have a drawback in that it is restricted by the need for separate sources [3]. Static compensators, motor drives, grid-connected RES, and photovoltaics are just a few of the many uses for MLIs [4]. Traditional MLI designs have a substantial restriction to achieve higher voltage levels because of number power switch requirements. A converter system with more semiconductor switches is bulky, expensive, and complex because of a protection unit, gate driving unit, and heat sink are generally integrated with each power switch. As a result, one of the fastest-growing study fields in MLIs is lowering the power switch count, and several topologies with fewer devices have recently been presented [5]. Seventeen level asymmetric MLI topology for medium

The associate editor coordinating the review of this manuscript and approving it for publication was Subrata Banerjee.

voltage applications with less dc sources count, less power switches, and lower dv/dt stress on switches was proposed in [6].

Novel MLIs have been presented to optimize the number of dc voltage sources and power switches [5]–[20]. The H-bridge structure was utilized to provide an alternate output voltage in the architectures presented in [7]. H-bridge switches, on the other hand, must be able to withstand large output voltages before they can be used. This issue is solved with H-type [8] and square T-type (ST-type) [9] structures, which provide alternate output voltage levels without the need for H-bridge. A new switched capacitor with single DC source and reduced components for low voltage RES applications was presented in [10] and an extended MLI topology with reduced switch and low voltage stress was presented in [11]. The topology presented in [12] employs the fewest total power electronic components. By connecting IGBT switch and diode in series/parallel. Using two dc sources and bidirectional switches coupled cross-network style, a rudimentary unit was created in [13]. As long as a full-bridge converter is used, this design may provide a multilevel output voltage on the load side while also working in asymmetrical mode. In [14], a topology is developed to minimize the maximum blocking voltage (MBV) on switches. The total standing voltage (TSV) in [15] is lower, making it a better choice for high-power applications. A unique generalized MLI configuration with optimal components, lesser power losses, and less blocking voltage is presented in [16]. The topology in [17] presents a switched capacitor MLI configuration with a low device count that has the benefits of negative polarity voltage generation without the use of an auxiliary H-bridge, the efficient voltage balancing can be done across the floating capacitors, and minimum PIV across the switches. In order to decrease the DC sources count, MLI based on switched capacitors are presented in [18] which produces nine voltage levels per DC source and also has several advantages such as enhancing the input voltage, but it suffers from a non-modularity feature.

In this work, a new MLI circuit is designed that solves all limitations and uses fewer components than similar topologies. The proposed MLI can be used to integrate distributed energy resources into medium voltage grids. The inverter's high-quality output voltage reduces the need for huge filters. The inverter reduces the size and weight along with the cost of the filters. Hence, the developed topology could be a reasonable solution for connecting PV sources in case of many DC sources are available. The proposed configuration can be employed in single-phase medium voltage applications. According to a comparison analysis, the recommended circuit uses fewer components, has reduced power loss values and increases the inverter's efficiency. However, in modern topologies, the TSV at the power switches is analyzed for the performance calculations. To test the suggested circuit's performance, both simulation and experimental conditions of the proposed 23 level inverter are examined. The following

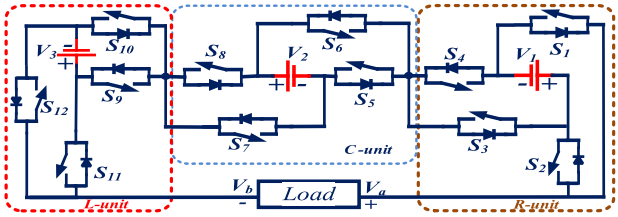


FIGURE 1. Proposed 23 level multilevel configuration.

are the most important characteristics of the suggested topology:

- Using only three sources and 12 switches, the suggested topology produces output voltage levels of 7 and 23 in both symmetrical as well as in asymmetrical configurations.
- The suggested architecture eliminates the need for an additional H-bridge circuit to produce alternate voltage levels, resulting in a considerable decrease in TSV.
- The majority of the switches have less voltage stress, allowing them to operate at medium voltages.
- The harmonic profile of proposed MLI is superior to traditional inverters, and adherence to the standard of IEEE 519.

The article is organized as follows: Section 2 presents the proposed circuit analysis as well as its general structure and also includes the selection of component value for extended topology, as well as TSV computations. Section 3 discusses comparative assessments of the suggested and other existing topologies. The proposed topology's power losses and efficiency are calculated in section 4. Cost estimation of the proposed design for medium voltage applications is discussed in Section 5. Both simulation as well as prototype experimental results with control switching approaches are provided in Section 6, and the conclusion is provided in Section 7, preceded by the references cited.

II. PROPOSED 23 LEVEL MLI TOPOLOGY

The proposed configuration comprises three dc sources namely V_1, V_2, and V_3, and twelve unidirectional switches S_1 to S_{12} are depicted in Figure 1. There are three units in the proposed topology: a left unit (L-unit), a center unit (C-unit), and a right unit (R-unit). Each unit is powered by its dc power supply. V_1, V_2, and V_3 respectively. In R-unit the switches (S_1, S_2) and (S_3, S_4), in C-unit the switches (S_5, S_6) and (S_7, S_8), in L-unit the switches (S_9, S_{10}), and (S_{11}, S_{12}) are never switched ON at the same time. In this manner a short circuit between the DC sources are prevented. Both symmetric and asymmetric combinations may be operated using the proposed topology.

A. COMPONENTS SELECTION

1) For symmetric mode, the magnitudes of DC voltage sources are fixed to be same.

$$V_1 = V_2 = V_3 = V_{dc} \tag{1}$$

The required DC sources N_{DC} are mathematically related to the number of levels N_{Lev} by using the equation:

$$N_{DC}^{Sym} = \frac{(N_{Lev} - 1)}{2} \tag{2}$$

The number of switches'N_{NS}' required may be mathematically related to the number of levels N_{Lev} by using the equation:

$$N_{SW}^{Sym} = 2(N_{lev} - 1) \tag{3}$$

The suggested topology uses unidirectional power switches for all of the switches. As a result, the required gate driver circuits N_{GDK} equals the number of IGBTs N_{SW}, and is written as:

$$N_{GDK}^{Sym} = N_{SW}^{Sym} = 2(N_{lev} - 1) \tag{4}$$

The maximum voltage output produced $V_{L,max}$ is given by:

$$V_{L,max}^{Sym} = \frac{(N_{Lev} - 1)}{2} \tag{5}$$

In symmetric mode, the proposed configuration produces 7 levels of voltage output with magnitudes of zero, $\pm 1V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$.

2) For asymmetric operation, the DC voltage sourc's magnitudes are fixed a

$$V_1 = 1V_{dc}; V_2 = 3V_{dc}; V_3 = 7V_{dc} \tag{6}$$

The required DC sources $_{ND}C$ in asymmetric mode may be mathematically related to the number of levels $N_{Le}v$ used by the equation:

$$N_{DC}^{Asym} = \frac{(N_{Lev} - 5)}{6} \tag{7}$$

The number of switches N_{SW} required in asymmetric mode may be mathematically related to the number of levels $N_{Le}v$ used by the equation:

$$N_{SW}^{Asym} = \frac{(N_{Lev} + 1)}{2} \tag{8}$$

The suggested topology uses unidirectional power switches for all of the switches. As a result, the required gate driver circuits N_{GDK} equals the number of IGBTs N_{SW}, and is written as:

$$N_{GDK}^{Asym} = N_{SW}^{Asym} = \frac{(N_{Lev} + 1)}{2} \tag{9}$$

The maximum voltage output produced $V_{L,max}$ is given by:

$$V_{L,max}^{Asym} = \frac{(N_{Lev} - 1)}{2} \tag{10}$$

In asymmetric mode, the proposed configuration produces 23 levels of voltage output with magnitudes of zero, positive ($+1$ V_{dc} to $+11$ V_{dc}), and negative (-1 V_{dc} to -11 V_{dc}). The proposed 23-level asymmetric MLI topology's switching states are tabulated in Table 1. In addition, Figure 2 shows the relevant connection diagrams for various voltage levels, while Figure 3 shows the expected output with varied switch states.

B. ANALYSIS OF TSV

Total maximum blocking voltage is one of the most important qualitative characteristics, which is referred to as the algebraic sum of the maximum voltage stress on the switches [21].

S_1 is expected to describe the TSV computation. Figure 2 is used to compute the MBV of S1 (off-state). ($+1V_{dc}$ or$+4V_{dc}$ or $+5V_{dc}$or$+8V_{dc}$or$+11V_{dc}$ or $-2V_{dc}$or $-6V_{dc}$ or $-9V_{dc}$) in which standing voltage on S_1 is created by using the R-unit dc source $V_{S1} = 1V_{dc}$.

The MBV of particular switches are calculated as follows:

$$\begin{aligned}
\text{For R-unit :} \quad & MBV_{S1} = MBV_{S4} = 1V_{dc.} \\
& MBV_{S2} = MBV_{S3} = 1V_{dc} \\
\text{For L-unit :} \quad & MBV_{S9} = MBV_{S11} = 7V_{dc.} \\
& MBV_{S10} = MBV_{S12} = 7V_{dc.} \\
\text{For C-unit :} \quad & MBV_{S5} = MBV_{S7} = 3V_{dc.} \\
& MBV_{S6} = MBV_{S8} = 3V_{dc.}
\end{aligned}$$

The term "Normalized voltage stress (NV_{strs})" refers to the ratio of V_{strs} across the switch to the maximum voltage $V_{L,max}$ [22], given by

$$NV_{strs} = \frac{\text{Vstrs}}{\text{VL, max}} \tag{11}$$

where V_{strs} is real voltage stress of the switch and corresponding values are tabulated in Table 2. Switches S_1, S_2, S_3, and S_4 experience the lowest V_{strs} and NV_{strs}, i.e. V_{dc} and 9.09% respectively, whereas switches S_5, S_6, S_7, and S_8 experience three times the lowest V_{strs} and NV_{strs}, i.e. $3V_{dc}$ and 27.27% respectively, and switches S_9, S_{10}, S_{11}, and S_{12} experience the highest V_{strs} and NV_{strs}, i.e. $7V_{dc}$ and 63.36%.

Figure 4 (a) depicts the stress distribution of each switch, Figure 4 (b) depicts the normalized voltage stress in percentage, and Figure 4 (c) depicts the voltage constraints in each level of the proposed topology. In traditional H-bridge-based MLI configurations, the blocking voltage experienced by four H-bridge switches is equal to the algebraic sum of DC sources in the circuit, i.e. $7V_{dc}$ [22]. The highest output voltage in the recommended MLI design is $11V_{dc}$, which creates a level of 23 at the output voltage, but the algebraic sum of DC sources is more than the MBV ($7V_{dc}$) encountered by the switch. Four switches S_9, S_{10}, S_{11}, and S_{12} in the proposed design are exposed to maximum voltage stress of $7V_{dc}$, even though the voltage stress across the switches in the proposed topology is spread unevenly. The minimum voltage stress is experienced by one-third of power switches, the highest voltage stress is experienced by 33.33 percent of total power switches, and the intermediate voltage stress is experienced by the remaining one-third of power switches. As a consequence, the recommended MLI topology optimizes the utilization of DC sources with minimum TSV and switches, hence the cost will be reduced.

The term TSV is stated as the algebraic sum of MBV across individual switches and is expressed in equation 11, equation

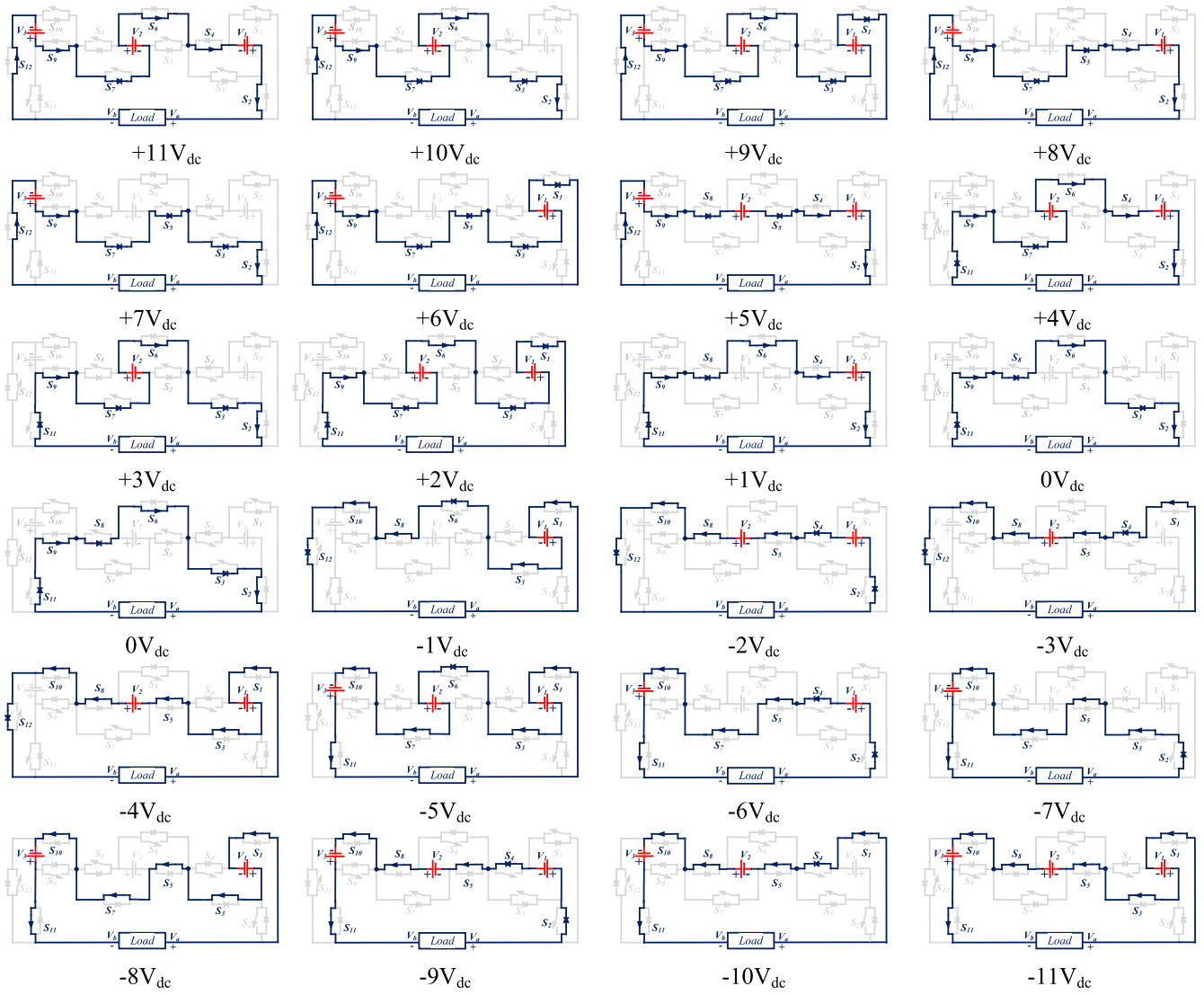


FIGURE 2. Operating modes of twenty three level MLI topology.

12 provides the TSV_{PU}.

$$TSV = MBV_{S1} + MBV_{S2} + MBV_{S3} + - - + MBV_{Sn} \tag{12}$$

$$\mathrm{TSV_{PU}} = \frac{\mathrm{TSV}}{\mathrm{V_{L,max}}} \tag{13}$$

For the proposed topology TS_{VProp} is calculated as

$$\begin{aligned} TSV^{Prop} &= MBV_{R-unit} + MBV_{C-unit} + MBV_{L-unit} \\ \mathrm{TSV^{Prop}} &= 4[\mathrm{V_{S1}} + \mathrm{V_{S5}} + \mathrm{V_{S9}}] \\ &= 4[\mathrm{V_{dc}} + 3\mathrm{V_{dc}} + 7\mathrm{V_{dc}}] \\ &= 4[11\mathrm{V_{dc}}] \\ \mathrm{TSV^{Prop}} &= 44\mathrm{V_{dc}} \end{aligned} \tag{14}$$

$$\text{And} \quad \mathrm{TSV_{PU}^{Prop}} = \frac{44\mathrm{V_{dc}}}{11\mathrm{V_{dc}}} = 4 \tag{15}$$

The proposed MLI's Peak Inverse Voltage (PIV) is determined from Figure 2 and is expressed a

$$PIV^{Prop} = (N_{lev} - 1) = 22V_{dc} \tag{16}$$

C. EXTENDED STRUCTURE FOR N LEVELS

At the output waveform, the proposed structure may generate 23 levels. An expanded architecture is developed for the higher voltage levels, as illustrated in Figure 5. The C-unit in extended topology is made up of '' number of subunits connected in sequence from C_1, C_2, C_3, ... , and Cn. Each subunit has four IGBTs that are powered by DC sources V_{c1}, V_{c2}, V_{c3}, and V_{cn}. The R-unit source magnitude is $V_R = 1V_{dc}$, the L-unit $V_L = 7V_{dc}$, and the C-subunit are $V_{C1} = V_{C2} = \ldots\ldots\ldots = V_{Cn} = 3V_{dc}$.

The required DC sources N_{DC} in extended structure may be mathematically related to the number of levels N_{Lev} used

TABLE 1. Switching conditions of the proposed the MLI.

Levels	Switch States S_1S_2----------$S_{11}S_{12}$	Current conducting path	Active sources	Output Voltage (Volts)
L_1	010101101001	V_3-S_9-S_7-V_2-S_6-S_4-V_1-S_2-L-S_{12}-V_3	V_3+V_2+V_1	+11V_{dc}
L_2	011001101001	V_3-S_9-S_7-V_2-S_6-S_3-S_2-L-S_{12}-V_3	V_3+V_2	+10V_{dc}
L_3	101001101001	V_3-S_9-S_7-V_2-S_6-S_3-V_1-S_1-L-S_{12}-V_3	V_3+V_2-V_1	+9V_{dc}
L_4	010110101001	V_3-S_9-S_7-S_5-S_4-V_1-S_2-L-S_{12}-V_3	V_3+V_1	+8V_{dc}
L_5	011010101001	V_3-S_9-S_7-S_5-S_3-S_2-L-S_{12}-V_3	V_3	+7V_{dc}
L_6	101010101001	V_3-S_9-S_7-S_5-S_3-V_1-S_1-L-S_{12}-V_3	V_3-V_1	+6V_{dc}
L_7	010110011001	V_3-S_9-S_8-V_2-S_5-S_4-V_1-S_2-L-S_{12}-V_3	V_3-V_2+V_1	+5V_{dc}
L_8	010101101010	V_2-S_6-S_4-V_1-S_2-L-S_{11}-S_9-S_7-V_2	V_2+V_1	+4V_{dc}
L_9	011001101010	V_2-S_6-S_3-S_2-L-S_{11}-S_9-S_7-V_2	V_2	+3V_{dc}
L_{10}	101001101010	V_2-S_6-S_3-V_1-S_1-L-S_{11}-S_9-S_7-V_2	V_2-V_1	+2V_{dc}
L_{11}	010101011010	V_1-S_2-L-S_{11}-S_9-S_8-S_6-S_4-V_1	V_1	+1V_{dc}
L_{12}	011001011010	L-S_{11}-S_9-S_8-S_6-S_3-S_2-L	-	0V_{dc}
L_{13}	101001010101	V_1-S_3-S_6-S_8-S_{10}-S_{12}-L-S_1-V_1	-(V_1)	-1V_{dc}
L_{14}	010110010101	V_2-S_8-S_{10}-S_{12}-L-S_2-V_1-S_4-S_5-V_2	-(V_2-V_1)	-2V_{dc}
L_{15}	100110010101	V_2-S_8-S_{10}-S_{12}-L-S_1-S_4-S_5-V_2	-(V_2)	-3V_{dc}
L_{16}	101010010101	V_2-S_8-S_{10}-S_{12}-L-S_1-V_1-S_3-S_5-V_2	-(V_2+V_1)	-4V_{dc}
L_{17}	101001100110	V_3-S_{11}-L-S_1-V_1-S_3-S_6-V_2-S_7-S_{10}-V_3	-(V_3-V_2+V_1)	-5V_{dc}
L_{18}	010110100110	V_3-S_{11}-L-S_2-V_1-S_4-S_5-S_7-S_{10}-V_3	-(V_3-V_1)	-6V_{dc}
L_{19}	011010100110	V_3-S_{11}-L-S_2-S_3-S_5-S_7-S_{10}-V_3	-(V_3)	-7V_{dc}
L_{20}	101010100110	V_3-S_{11}-L-S_1-V_1-S_3-S_5-S_7-S_{10}-V_3	-(V_3+V_1)	-8V_{dc}
L_{21}	010110010110	V_3-S_{11}-L-S_2-V_1-S_4-S_5-V_2-S_8-S_{10}-V_3	-(V_3+V_2-V_1)	-9V_{dc}
L_{22}	100110010110	V_3-S_{11}-L-S_1-S_4-S_5-V_2-S_8-S_{10}-V_3	-(V_3+V_2)	-10V_{dc}
L_{23}	101010010110	V_3-S_{11}-L-S_1-V_1-S_3-S_5-V_2-S_8-S_{10}-V_3	-(V_3+V_2+V_1)	-11V_{dc}

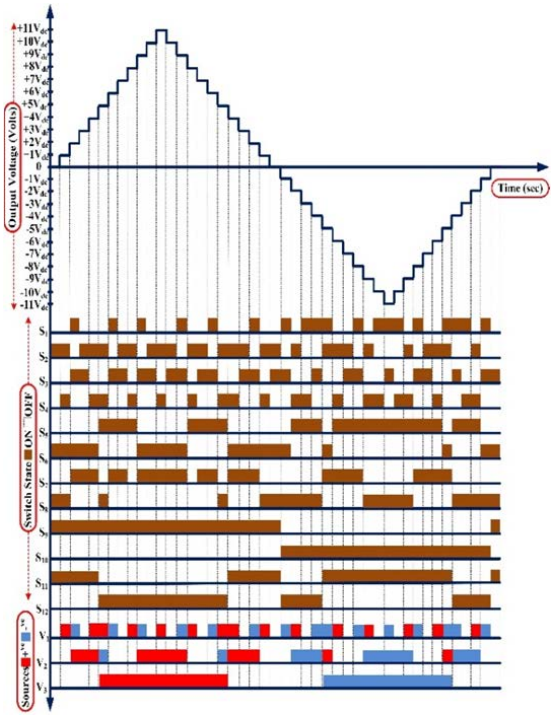


FIGURE 3. The expected output of 23 level MLI.

by the equation:

$$N_{DC}^{Extd} = \frac{(N_{Lev} - 5)}{6} \tag{17}$$

TABLE 2. Voltage and normalized voltage stress across power switches.

Switch	Voltage Stress (V_{strs})	Normalized Voltage Stress (NV_{strs})
S_1	1$V_{dc.}$	(1$V_{dc.}$/11V_{dc}) = 9.09 %
S_2	1$V_{dc.}$	(1$V_{dc.}$/11V_{dc}) = 9.09 %
S_3	1$V_{dc.}$	(1$V_{dc.}$/11V_{dc}) = 9.09 %
S_4	1$V_{dc.}$	(1$V_{dc.}$/11V_{dc}) = 9.09 %
S_5	3$V_{dc.}$	(3$V_{dc.}$/11V_{dc}) = 27.27 %
S_6	3$V_{dc.}$	(3$V_{dc.}$/11V_{dc}) = 27.27 %
S_7	3$V_{dc.}$	(3$V_{dc.}$/11V_{dc}) = 27.27 %
S_8	3$V_{dc.}$	(3$V_{dc.}$/11V_{dc}) = 27.27 %
S_9	7$V_{dc.}$	(7$V_{dc.}$/11V_{dc}) = 63.63%
S_{10}	7$V_{dc.}$	(7$V_{dc.}$/11V_{dc}) = 63.63%
S_{11}	7$V_{dc.}$	(7$V_{dc.}$/11V_{dc}) = 63.63%
S_{12}	7$V_{dc.}$	(7$V_{dc.}$/11V_{dc}) = 63.63%

The number of switches N_{SW} required in extended structure may be mathematically related to the number of levels N_{Lev} used by the equation:

$$N_{SW}^{Extd} = \frac{(N_{Lev} - 1) + 2n}{2} \tag{18}$$

The suggested topology uses unidirectional power switches for all of the switches. As a result, the required gate driver circuits N_{GDK} equals the number of IGBTs N_{SW}, and is written as

$$N_{GDK}^{Extd} = N_{SW}^{Extd} = \frac{(N_{Lev} - 1) + 2n}{2} \tag{19}$$

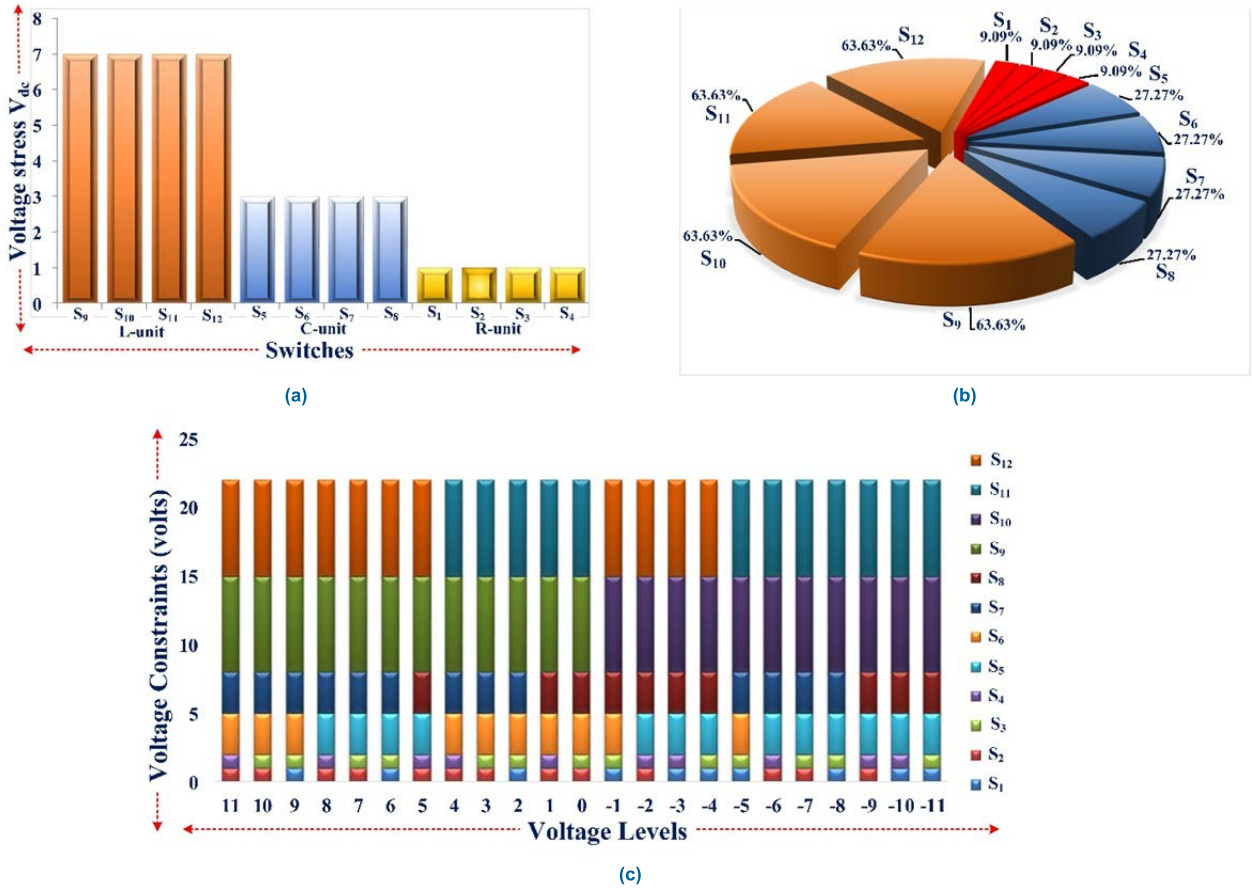


FIGURE 4. (a) Voltage stress distribution, (b) normalized voltage stress in %, and (c) voltage constraints different switches in each level.

The maximum voltage output produced $V_{L,max}$ is given by

$$V_{L,max}^{Extd} = \frac{(N_{Lev}-1)}{2} \tag{20}$$

MBV of individual switches are given a

$$\begin{aligned}
&\text{For R-unit}: MBV_{S1} = MBV_{S4} = V_R \\
&\qquad MBV_{S2} = MBV_{S3} = V_R \\
&\text{For L-unit:} MBV_{S9} = MBV_{S11} = V_L \\
&\qquad MBV_{S10} = MBV_{S12} = V_L \\
&\text{For C-unit}: \sum_{n=1}^{i} MBV_{Si5} = \sum_{n=1}^{i} MBV_{Si7} \\
&\qquad = \sum_{n=1}^{i} V_{Cn} \\
&\qquad \sum_{n=1}^{i} MBV_{Si6} = \sum_{n=1}^{i} MBV_{Si8} \\
&\qquad = \sum_{n=1}^{i} V_{Cn}
\end{aligned}$$

Therefore for the extended topology, TSV_{Extd} is calculated as

$$\begin{aligned}
TSV^{Extd} &= MBV_{R-unit} + MBV_{C-unit} + MBV_{L-unit} \\
TSV^{Extd} &= 4[V_R + V_L] + 4\sum_{n=1}^{i} V_{Cn}
\end{aligned} \tag{21}$$

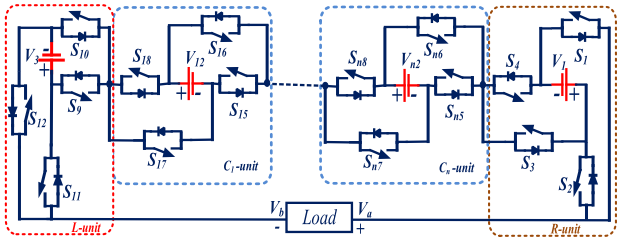


FIGURE 5. Extended structure for n levels.

III. COMPARISONS

To evaluate the benefits and capabilities of the suggested topology, a comparison is made with other recent topologies. Quantitative and qualitative evaluations of similar and different asymmetrical MLI configurations are carried out to showcase the benefits of the suggested topology. For both the same number of output voltage level topologies [21]–[28] and different numbers of output voltage level topologies [6], [9], [16], [20], [29]–[31], a comparison has been made per level concerning the required driver circuits, dc sources, switches, the factor of the component count, maximum conducting devices, TSV_{PU}, and cost factor are tabulated in Table 3.

TABLE 3. Comparisons of the proposed 23-level MLI with recent topologies.

Topologies		Quantitative analysis						Qualitative analysis					
	Ref	N_{lev}	N_{SW}	N_{DC}	N_{GDK}	N_{Var}	MCD	CC/N_{Lev}	TSV_{PU}	% THD	CF/N_{Lev}		Negative level
											$\alpha = 0.5$	$\alpha = 1.5$	
Similar	[21]	23	12	6	12	0	6	1.30	5.81	2.59	1.43	1.68	H-Bridge
	[23]	23	12	1	12	3	6	1.21	-	4.38	-	-	H-Bridge
	[24]	23	14	5	14	0	7	1.43	-	5.47	-	-	Inherent
	[25]	23	10	5	10	2	4	1.17	6.09	-	1.39	1.65	Inherent
	[26]	23	12	8	12	0	7	1.39	-	4.09	-	-	H-Bridge
	[27]	23	12	5	12	0	4	1.26	4.4	3.6	1.35	1.54	Inherent
	[28]	23	12	5	9	5	3	1.34	-	4.17	-	-	H-Bridge
Proposed		23	12	3	12	0	6	1.17	4.0	3.23	1.26	1.43	Inherent
Other	[5]	11	8	3	7	0	4	1.63	4.4	-	1.83	2.23	H-Bridge
	[9]	17	12	4	10	2	5	1.64	5	3.06	1.61	1.91	Inherent
	[16]	17	10	4	10	-	5	1.41	4.5	6.17	1.54	1.80	Inherent
	[20]	17	14	4	16	4	6	3.05	5	4.23	3.38	4.02	H-Bridge
	[29]	25	12	4	10	0	10	1.04	5	-	1.14	1.34	H-Bridge
	[30]	17	10	3	10	0	5	1.35	4.0	5.17	1.52	1.76	H-Bridge
	[31]	19	11	5	10	2	4	1.47	5.55	5.62	1.61	1.91	H-Bridge

Several parameters, such as the switch count N_{SW}, source count N_{DC}, driver circuit count N_{GDK}, diode count ND, capacitor count N_C, and total standing voltage TSV can be used to calculate the cost factor (CF). The cost factor is calculated with the following formula:

$$CF = (N_{SW} + N_{DC} + N_{GDK} + N_D + N_C + \alpha TSV_{PU}) \tag{22}$$

In practice, the value of'α' should be larger than and less than unity, respectively. For the optimal assessment of the cost function, the respective values of 'α' are approximated as 0.5 (<1) and 1.5 (>1) in the designed MLI.

The component count per level is calculated as.

$$\mathrm{CF}/N_{Lev} = \frac{N_{SW} + N_D + N_C + N_{GDK} + N_{DC}}{N_{Lev}} \tag{23}$$

Figure 6 presents the display of several performance characteristics to assess the suggested topology. The suggested topology has a significantly higher performance in terms of required switches for producing the desired output levels, as shown in Figure 6a. However, the design in [25] requires fewer switches than the proposed MLI, but more DC sources. The topology in [25], [28] has better values than proposed, however, the demand for DC sources is considerable. As a result, as illustrated in Figure 6d, the total number of components per level is less as compared to other topologies. According to Figure 6e, the THD value is lower than the high TSV_{PU} design [21], and the TSV_{PU} of the suggested topology is lower than that of recent topologies, as shown in Figure 6f. Finally, from Figure 6g, the suggested topology has the lowest cost factor when compared to recent topologies.

IV. POWER LOSS AND EFFICIENCY CALCULATION

Inmultilevel inverters, there are two significant power losses. They are conduction power losses (PC) and switching power losses (P_{Swi}). Overall conduction loss is calculated by adding the conduction losses of both IGBTs (PC_{SW}) and anti-parallel diodes (P_{CD}) in the current path and is expressed as

$$P_C(t) = P_{CSW}(t) + P_{CD}(t) \tag{24}$$

$$P_C(t) = \left(\left[V_{SW} + R_{SW} i_m^{\beta}(t)\right] + \left[V_D + R_D i_m(t)\right]\right) i_m(t) \tag{25}$$

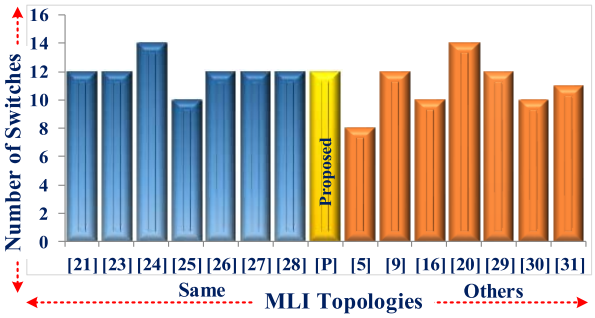
where i_m is the peak output current. V_{SW}, V_D is the power switch and diode threshold voltages, R_{SW}, R_D are the ON-state switch resistance and diode resistance, and β is a switch specification constant provided by datasheet.

If N_{SW} and N_D are the switches and diodes conducting at the same time (t) to produce each level then, the average conduction loss is

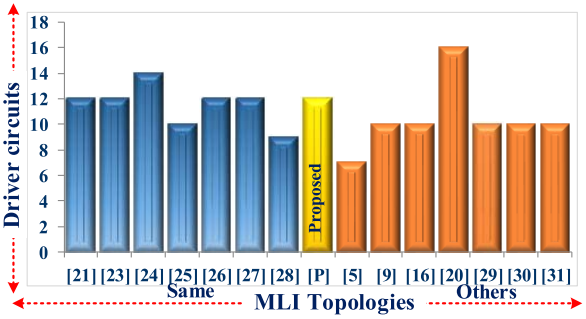
$$P_C = \frac{1}{2\pi}\int_0^{2\pi} \left[N_{SW}(t) P_{CSW}(t) + N_D(t) P_{CD}(t)\right] dt \tag{26}$$

The power consumed at the instant of the switch turn ON and turn OFF is known as switching loss (P_{Swi}). For both the switch and the antiparallel diode, this loss is estimated. The following formula can be used to determine turn-on and turn-off energy loss (E_{on}, E_{off})

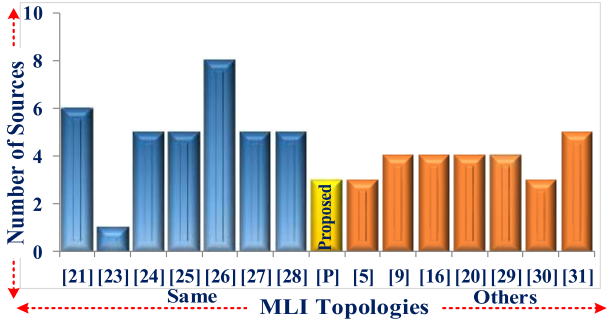
$$\begin{aligned} E_{offq} &= \int_0^{t_{off}} (v(t)\, i(t))\, dt \\ &= \int_0^{t_{off}} \left[\left(\frac{V_{SWq}}{t_{off}} t\right)\left(-\frac{I}{t_{off}}(t - t_{off})\right)\right] dt \\ E_{offq} &= \frac{1}{6} V_{SWq} I t_{off} \end{aligned} \tag{27}$$



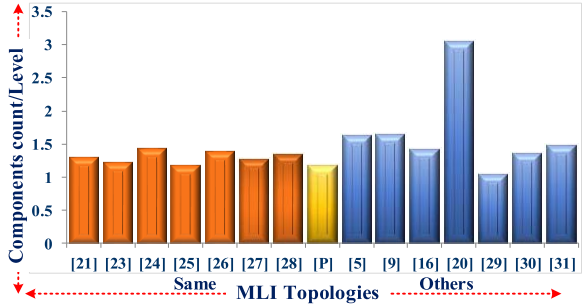
(a)



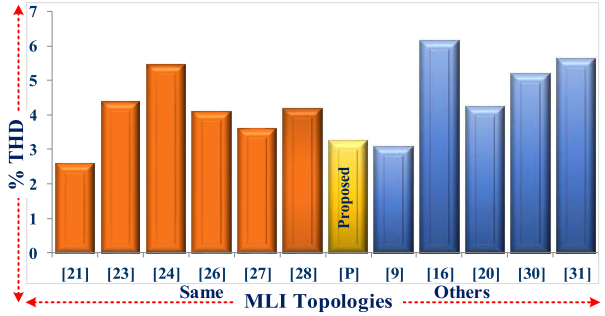
(b)



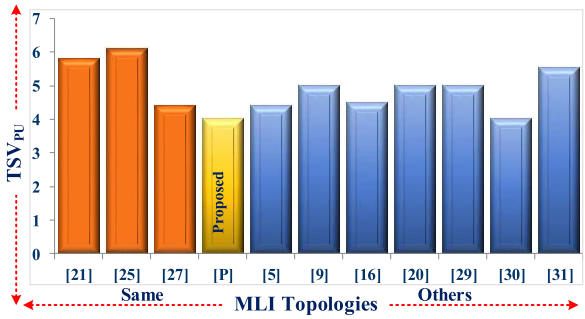
(c)



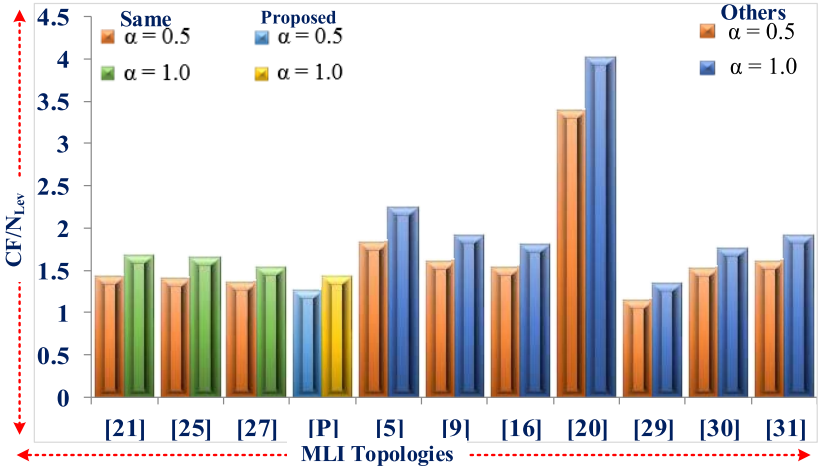
(d)



(e)



(f)



(g)

FIGURE 6. Performance comparisons between proposed and recent MI topologies. (a) N_{sw}, (b) N_{DGK}, (c) N_{DC}, (d) CC/N_{lev}, (e) % THD, (f) TSV_{PU}, (g) CF/N_{lev}.

Similarly,

$$E_{onq} = \int_0^{t_{on}} (v(t)\, i(t))\, dt$$
$$= \int_0^{t_{on}} \left[\left(\frac{V_{SW\,q}}{t_{on}} t \right) \left(-\frac{I'}{t_{on}} (t - t_{on}) \right) \right] dt$$
$$E_{onq} = \frac{1}{6} V_{SW\,q} I' t_{on} \quad (28)$$

where time to turn OFF and ON, and loss of the switch q are t_{off}, t_{on} and E_{offq}, $E_{on\ q}$ respectively. I and I^I are the switch current before turn OFF and after turn ON and V_{swq} is the OFF state switch voltage. Thus

$$P_{Swi} = f \left[\sum_{q=1}^{N_{SW}} \left(\sum_{i=1}^{N_{onq}} E_{onqi} + \sum_{i=1}^{N_{offq}} E_{offqi} \right) \right] \quad (29)$$

where fundamental frequency is f, $N_{on,q,}$ and $N_{off,q}$ is the number of times q^{th} switch turn ON or turn OFF in one fundamental cycle. Thus, total power losses are

$$P_T = P_C + P_{Swi} \quad (30)$$

The total efficiency (η) can be calculated as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_T} \quad (31)$$

The output and input powers are P_{out} and P_{in}.

The output power can be calculated as

$$P_{out} = V_{rms} * I_{rms} \quad (32)$$

Table 4 summarizes the power losses and efficiency of the proposed 23-level MLI and the efficiency at different loads are shown in Figure 7.

TABLE 4. Summary of power loss and efficiency.

Resistive load (ohms)	100	200	320	400	500
Vrms (Volts)	282.84	282.84	282.84	282.84	282.84
Irms (Amps)	2.82	1.414	0.88	0.707	0.565
Output power Pout (Watts)	797.6	400	250	200	160
Conduction loss Pc (Watts)	58.47	19.77	10.05	7.48	5.6
Switching loss Pswi (Watts)	0.365	0.182	0.114	0.09	0.073
Total loss PT (Watts)	58.83	19.95	10.164	7.57	5.673
Input power Pin (Watts)	856.43	419.95	260.16	207.57	165.67

V. COST EVALUATION

It is necessary to compute the proposed MLI's maximum working voltage in order to determine its greater cost-benefit when it is utilized for medium voltage applications. Considering that the maximum standard commercial voltage of a switch is $V_{SW\ ccv}$, therefore the proposed multilevel inverte's

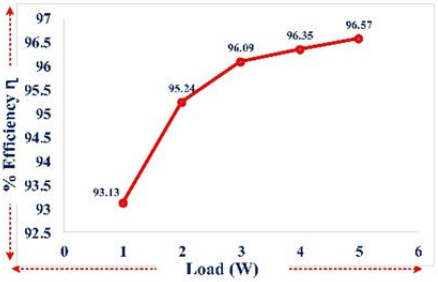


FIGURE 7. Efficiency of proposed MLI at various loads.

maximum operating voltage is equal to $\sqrt{1.5}V_{SWccv}/\gamma$ and γ is a safe operating factor of the switch, which is generally assumed to be 1:7. As a result, the suggested topology's operation voltage may be determined by determining the maximum switch voltage. For medium voltage applications, the switch voltage is calculated by assuming the 3-phase operating RMS voltage as 2.3 kV, if the maximum switch voltage is 3.3kV. For 1-φ, the operating RMS voltage will be 1328V, with a maximum voltage of 1878V. As a result, the voltage magnitudes of 23-level MLI will be V_1 = 170.72V, V_2 = 512.18V, and V_3 = 1195.04V for an RMS voltage of 1328V. Thus the switch rated voltage for the recommended topology is determined using Table 2 and $V_{SW\ ccv}$ is considering from Table 5. Table 6 calculates and compares the costs of needed IGBTs and driver circuits for 1-φ proposed 23-level MLIs and existing 13-level and 11-level MLIs [34], [33].

TABLE 5. Voltage rating of the switches in the proposed topology.

Switches	Voltage		IGBTs Rating	IGBT model number
	Standard	Normal		
S_1	170.72 V	600 V	600V, 400A	CM20MD-12H
S_2	170.72 V	600 V	600V, 400A	
S_3	170.72 V	600 V	600V, 400A	
S_4	170.72 V	600 V	600V, 400A	
S_5	518.16 V	1200 V	1200V, 400A	CM400HA-24A
S_6	518.16 V	1200 V	1200V, 400A	
S_7	518.16 V	1200 V	1200V, 400A	
S_8	518.16 V	1200 V	1200V, 400A	
S_9	1209.04 V	2500 V	2500 V, 400A	CM400DY-50H
S_{10}	1209.04 V	2500 V	2500 V, 400A	
S_{11}	1209.04 V	2500 V	2500 V, 400A	
S_{12}	1209.04 V	2500 V	2500 V, 400A	

The MITSUBISHI Companyproduces a nominal current of 400A commercial IGBTs. As a role example [32], the costs

TABLE 6. Cost comparison between the proposed topology and existing topologies.

IGBT and Driver model number	Voltage and Current Rating	Unit Cost	Proposed		[33]		[32]	
			Units	Cost	Units	Cost	Units	Cost
CM400DY-66H	3300 V, 400A	$773	-	-	2	$1546	4	$3092
CM400DY-50H	2500 V, 400A	$550	4	$2200	-	-	1	$550
CM400DU-34KA	1700V, 400A	$516	-	-	6	$3096	1	$516
CM400HA-24A	1200V, 400A	$118	4	$472	6	$708	1	$118
CM20MD-12H	600V, 400A	$60.77	4	$243.08	-	-	-	-
1SC0450V2A0-65	Up to 6500V	$267.62	4	$1070.48	1	$267.62	3	$802.86
SKYPER-32PRO2	Up to 1700V	$92.71	8	$741.68	6	$556.26	1	$92.71
844-SD303C25S20C	2500V, 350A	$102:50	-	-	-	-	3	$307.50
Overall cost			$4727.24		$6173.88		$5479.07	
Number of voltage output levels			23		13		11	

Courtesy: www.nevonexpress.com, www.yaspro.com, * Prices may vary.

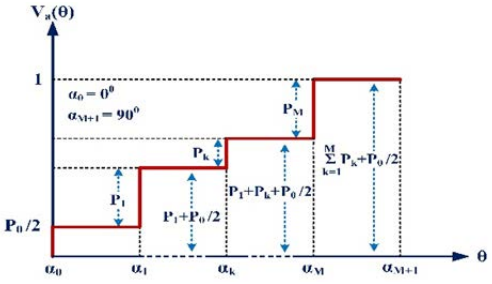


FIGURE 8. Generalized representation of a quarter-wave staircase waveform.

of power diode (single pack, Mouser Electronics) and IGBTs (single pack), as well as the driver circuits (Semikron, dual pack), are in USD. From the price comparison the proposed MLI is less expensive.

VI. RESULTS AND DISCUSSION

A. CONTROL SCHEME

The gate pulses are generated in MATLAB/Simulink using the round-robin condition (staircase modulation approach). Because of its primary advantages, such as less complexity and lower switching losses, the staircase Modulation technique is preferred over the classic PWM technique. This is true for both high-rated MLIs with higher voltage levels (N) and low-rated MLIs with lower voltage levels (N). This is the most frequent and well-known method for multilevel inverters going forward. In addition, with its lower losses for MLIs with higher ratings, this technique is the greatest alternative to the sine PWM switching technique. While symmetric MLIs are the most prevalent, using asymmetric MLIs with a cascaded H-Bridge reduces total harmonic distortion (THD) even further.

Figure 8 depicts the waveform generated by the staircase modulation method as a generalized quarter-wave representation, with M desired steps per quarter-wave and an optional extra half-step appearing at the origin. For every k^{th} step appearing at the phase switching angle α_k, consists of a normalized width and height concerning the DC supply voltage ratio of P_k. $\alpha = \{\alpha_1, \alpha_2 \ldots \alpha_k \ldots \alpha_M\}$ and P $=\{P_1, P_2, P_k \ldots P_M\}$ are the phase switching angle and the DC supply voltage ratio expressed in in degrees and per unit values respectively. In order to provide even values of N, an extra half-step with a value of $p_{0/2}$, appearing at the 0^{th} phase angle, which is $\alpha_0 = 0$. M = (N-1)/2 excluding α_0, is the total phase switching angles per quarter-wave which is related to N [34].

The generalized voltage of staircase modulation waveform can be represented as

$$V(\theta) = \sum_{k=1}^{M} P_k u(\theta - \alpha_k) + f_{tg} P_0 \tag{33}$$

where θ and α_k is lies in between 0 to 90 degrees, unit step function $u(\theta - \alpha_k)$ is zero if $\theta < \alpha$ whereas its value is unity if $\theta \geq \alpha$ and the toggle function f_{tg} is zero for odd and 0.5 for even.

The normalized fundamental component of voltage at modulation index MI is given by

$$V_1 = m_a = \frac{4}{\pi}\left(\sum_{k=1}^{M} (P_k \cos\left(\frac{\pi \alpha_k}{180}\right)) + f_{tg} P_0 \right) \tag{34}$$

The range of voltage is given by

$$\frac{4}{\pi} f_{tg} P_0 \leq m_a \leq \frac{4}{\pi} \tag{35}$$

The expected staircase waveform for the proposed topology is shown in figure 9. The variation of modulation index (M) with respect to the number of levels (NL) is shown in TABLE 7.

B. SIMULATION RESULTS

The performance of the suggested configuration has been evaluated through simulation experiments using MATLAB/Simulink software. TABLE 8 lists the many parameters that were used in the analysis. A carrier frequency of 5 kHz is used to produce the pulses in simulation, and the design is

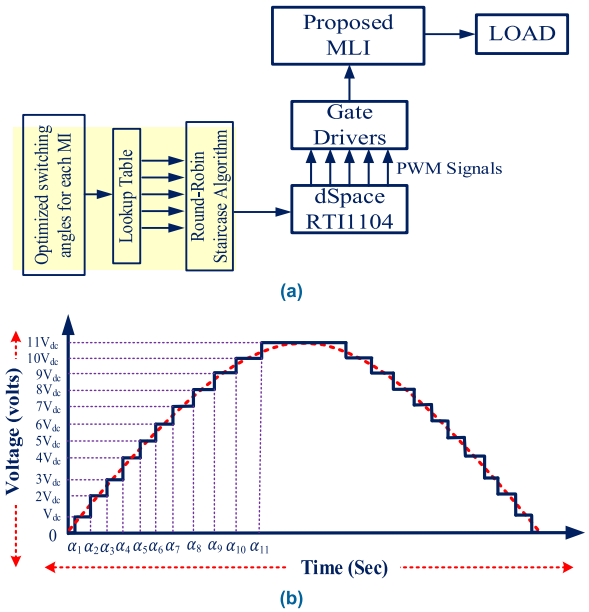


FIGURE 9. (a) Control block diagram (b) Expected staircase waveform for the proposed topology.

TABLE 7. Variation of MI with levels of proposed 23 level MLI.

Modulation Index	Number of Levels
0.09	3
0.18	5
0.27	7
0.36	9
0.45	11
0.55	13
0.64	15
0.73	17
0.82	19
0.91	21
1.00	23

TABLE 8. List of parameters used for proposed 23 level MLI.

Parameters	Simulation	Experimental
Voltage Sources	V_1= 35V, V_2= 110, V_3= 255V	V_1= 35V, V_2= 110, V_3= 255V
Load values	100Ω	100Ω
	187mH	187mH
Motor load	Single phase 230V, 0.5 HP	Single phase 230V, 0.5 HP
Switching frequency	5KHz	5KHz
IGBTs	CM75DU-12H	CM75DU-12H

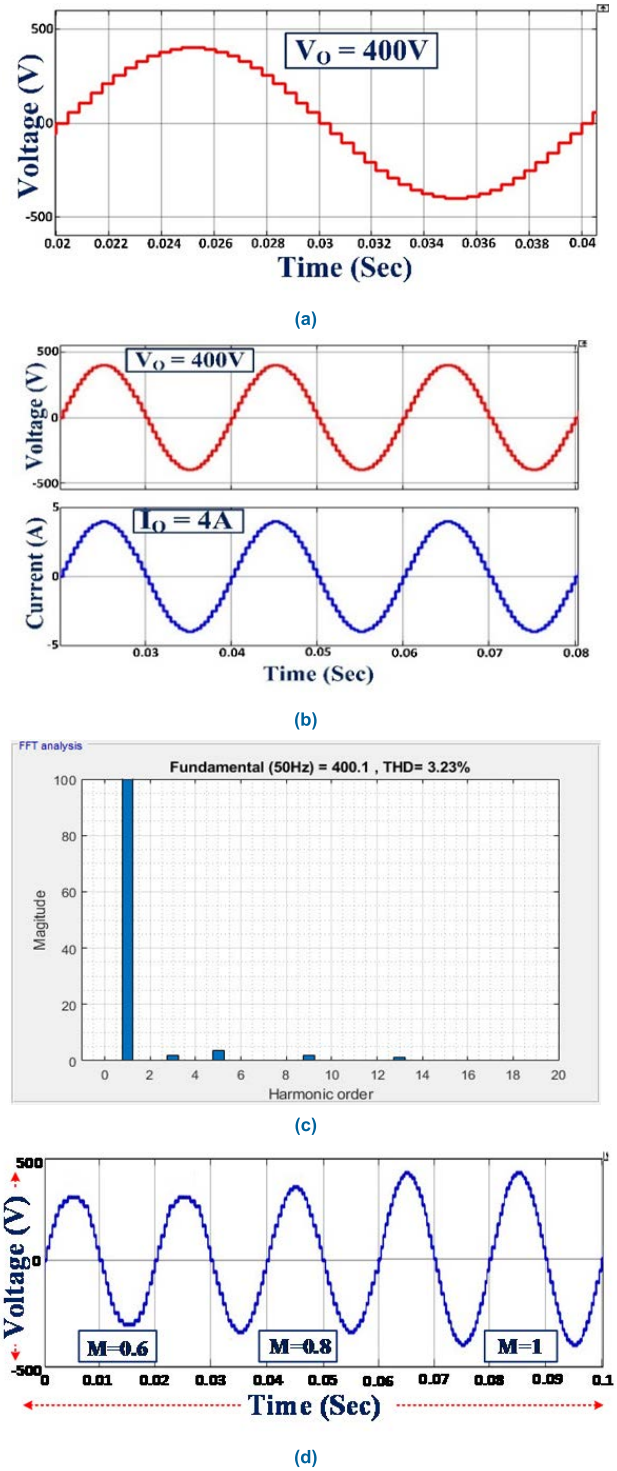


FIGURE 10. Simulation output of 23 level MLI (a) voltage waveform (b) voltage and current waveform (c) voltage THD (d) variation of output with modulation index.

evaluated with resistive and inductive loads of 100 ohms 187mH respectively. Figure 10(a) shows the simulated output voltage, while Figure 10(b) displays the simulation output voltage and current waveforms. The magnitude of source voltages in asymmetric source configuration is considered as V_1=35V, V_2=110V, and V_3=255V. At 400V peak voltage and 4 A load current, the inverter can produce 23 levels of output. Figure 10(c) shows the enhanced output waveform with a THD of 3.23 %. The simulation output waveform of the modulation index for M = 0.6 consists of 15 levels, M = 0.8 with 19 levels and M = 1 with 23 levels are represented in FIGURE 10(d).

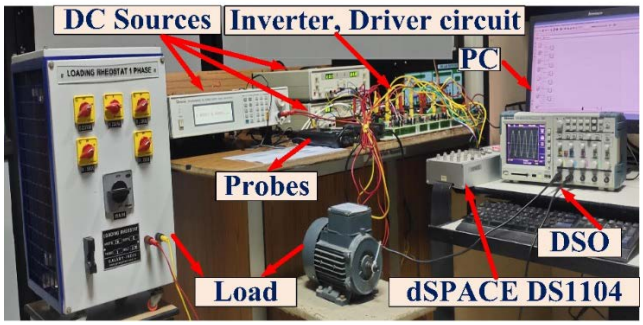


FIGURE 11. Experimental setup of the proposed topology.

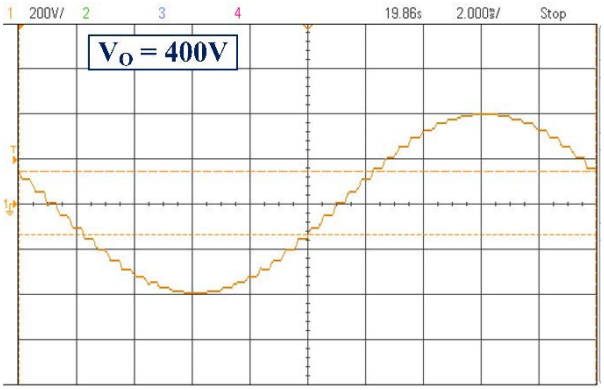


FIGURE 12. Experimental voltage output of proposed 23 level MLI.

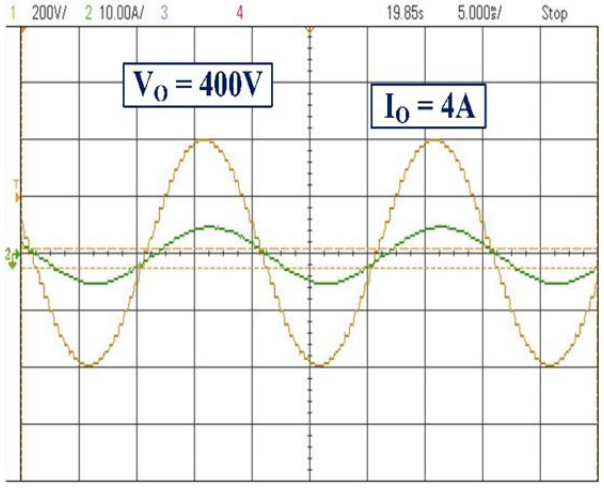


FIGURE 13. Experimental current and voltage output with R load.

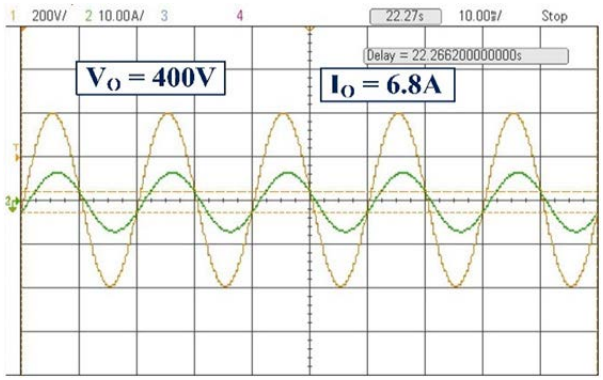


FIGURE 14. Experimental current and voltage output with motor load.

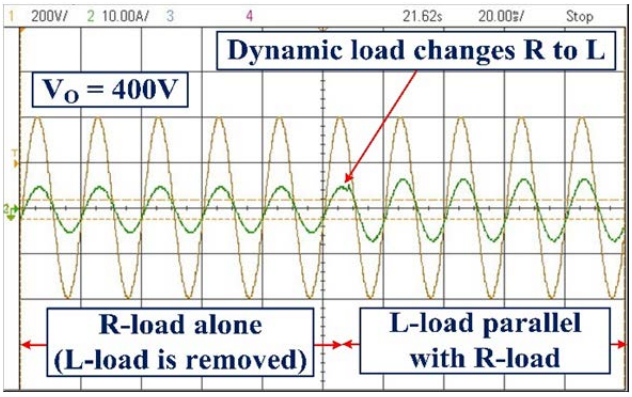


FIGURE 15. Experimental current and voltage output with dynamic RL load.

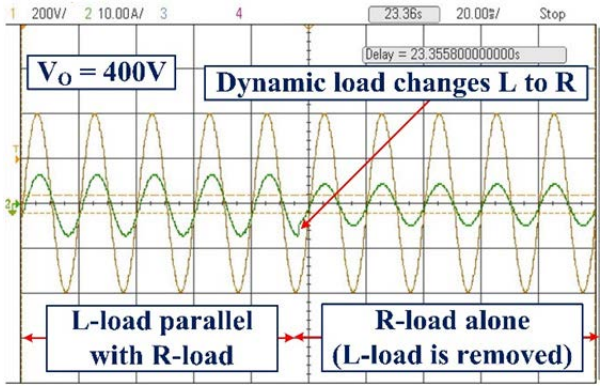


FIGURE 16. Experimental current and voltage output with dynamic LR load.

C. EXPERIMENTAL RESULTS

As illustrated in Figure 11, a single-phase prototype is built in the lab to evaluate the proposed MLI technology. The prototype is made up of 12 IGBT switches (CM75DU-12H) that are activated by optocouplers (MCT2E), and a dual dc supply provides input dc sources. The load parameters are 100 resistive load and 187mH inductive load. The real-time controller dSPACE1104 is used to build the switching control scheme and DSO is used to observe the voltage and current waveforms. Figures 12 and Figures 13 show the experimental results with resistive load at a steady-state output voltage V_0 = 400V (282.84 V_{rms}) and load current I_0=4A (2.82 I_{rms}) respectively. With motor load, the output voltage V_0 = 400V and the load current I_0 = 6.8A equivalent to 4.8A I_{rms} are shown in Figure 14. As illustrated in Figures 15 and 16, the dynamic response of the proposed MLI is accomplished by adding an inductive load parallel to resistive load or contrariwise. With a power analyzer, the total voltage harmonic spectrum of 3.23% is measured and is displayed in Figure 17.

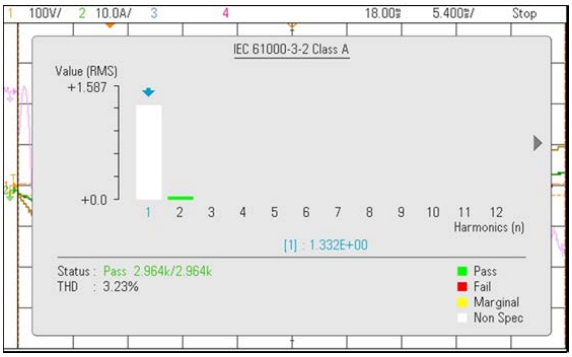


FIGURE 17. Hardware voltage THD of proposed 23 level MLI.

D. APPLICATIONS

Due to the wide range of operation with the modulation index, the proposed reduced switch count MLI is an alternative to traditional MLIs in industrial requirements. Individual photovoltaic panels with varying ratings are fed into each of the three input sources of proposed MLI, which correspond to the ratings of the DC sources [35]. To accomplish this, several control objectives must be met, including the inverter maintaining optimal power quality within grid constraints, minimizing harmonic distortions in the output ac voltage waveform, and extracting the maximum amount of energy possible from solar panels under varying irradiance conditions in order to provide an efficient and stable output throughout its operation. Additionally, to ensure reliability, the extracted power has been transferred to the output with a power factor of unity. Due to the fact that different solar panel ratings are used for different DC sources, an efficient maximum power extraction method is used to harvest energy in a variety of irradiance conditions. In this regard Power factor control is critical to transferring solar power to the grid, which is closer to a power factor of 0.95. Because the inverter rating is low according to IEC 929-2000 and IEC 62109-2 standards, reactive power consideration is not required in these systems. Furthermore, the suggested MLI is more suitable for solar PV applications in terms of fault ride-through capability and power balance because it has redundant switching states [36].

VII. CONCLUSION

An asymmetrical reduced component 23 level single-phase multilevel inverter configuration was proposed for medium voltage applications. Twelve switches and three DC sources are used in the proposed topology to produce eleven positive voltage levels and can be expanded to produce n voltage levels by adding a few devices. According to the findings of the proposed MLI and the comparisons with existing MLIs, the suggested MLI requires a lower component count per level to generate more output voltage levels. For 23-level MLI, several characteristics are examined, including cost function (CF), total standing voltage (TSV), and total harmonic distortion (THD) which is under IEEE standards. The proposed MLI is compared with other existing topologies and found to be superior among various parameters and found that it is cost-effective and compatible with the TSV and component count per level factor. As the proposed MLI has an asymmetrical sources, it can be widely utilized in hybridized energy sources where the various types of sources are interfaced. Hence the proposed MLI is well suited for medium-power and grid-connected FACTS devices such as DSTATCOM, and DVR.

REFERENCES

[1] E. Babaei and S. Laali, "A multilevel inverter with reduced power switches," *Arabian J. Sci. Eng.*, vol. 41, no. 9, pp. 3605–3617, 2016.
[2] R. H. Baker and H. L. Bannister, "Electric power converter," U.S. Patent 3 867 643, Feb. 18, 1975.
[3] M. D. Siddique, M. Rawa, S. Mekhilef, and N. M. Shah, "A new cascaded asymmetrical multilevel inverter based on switched DC voltage sources," *Int. J. Electr. Power Energy Syst.*, vol. 128, Jun. 2021, Art. no. 106730.
[4] V. Anand and V. Singh, "Implementation of cascaded asymmetrical multilevel inverter for renewable energy integration," *Int. J. Circuit Theory Appl.*, vol. 49, no. 6, pp. 1776–1794, Jun. 2021.
[5] M. D. Siddique, S. Mekhilef, N. M. Shah, and M. A. Memon, "Optimal design of a new cascaded multilevel inverter topology with reduced switch count," *IEEE Access*, vol. 7, pp. 24498–24510, 2019.
[6] S. Nyamathulla and C. Dhanamjayulu, "Design of 17-level inverter with reduced switch count," in *Proc. Innov. Power Adv. Comput. Technol. (i-PACT)*, Nov. 2021, pp. 1–8.
[7] E. Babaei, S. Laali, and Z. Bayat, "A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 922–929, Feb. 2015.
[8] P. L. Kamani and M. A. Mulla, "A home-type (H-type) cascaded multilevel inverter with reduced device count: Analysis and implementation," *Electric Power Compon. Syst.*, vol. 47, nos. 19–20, pp. 1691–1704, Dec. 2019.
[9] E. Samadaei, A. Sheikholeslami, S. A. Gholamian, and J. Adabi, "A square T-type (ST-type) module for asymmetrical multilevel inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 987–996, Feb. 2018.
[10] M. D. Siddique, J. S. M. Ali, S. Mekhilef, A. Mustafa, N. Sandeep, and D. Almakhles, "Reduced switch count based single source 7L boost inverter topology," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 12, pp. 3252–3256, Dec. 2020.
[11] M. D. Siddique, S. Mekhilef, M. Rawa, A. Wahyudie, B. Chokaev, and I. Salamov, "Extended multilevel inverter topology with reduced switch count and voltage stress," *IEEE Access*, vol. 8, pp. 201835–201846, 2020.
[12] S. A. A. Ibrahim, A. Palanimuthu, and M. A. J. Sathik, "Symmetric switched diode multilevel inverter structure with minimised switch count," *J. Eng.*, vol. 2017, no. 8, pp. 469–478, Aug. 2017.
[13] M. T. Khosroshahi, "Crisscross cascade multilevel inverter with reduction in number of components," *IET Power Electron.*, vol. 7, no. 12, pp. 2914–2924, Dec. 2014.
[14] K. K. Gupta and S. Jain, "A novel multilevel inverter based on switched DC sources," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3269–3278, Jul. 2014.
[15] M. S. B. Arif, U. Mustafa, S. B. M. Ayob, J. Rodriguez, A. Nadeem, and M. Abdelrahem, "Asymmetrical 17-level inverter topology with reduced total standing voltage and device count," *IEEE Access*, vol. 9, pp. 69710–69723, 2021.
[16] J. S. M. Ali, R. S. Alishah, N. Sandeep, S. H. Hosseini, E. Babaei, K. Vijayakumar, and U. R. Yaragatti, "A new generalized multilevel converter topology based on cascaded connection of basic units," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 4, pp. 2498–2512, Dec. 2019.
[17] M. D. Siddique, S. Mekhilef, N. M. Shah, J. S. M. Ali, and F. Blaabjerg, "A new switched capacitor 7L inverter with triple voltage gain and low voltage stress," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 7, pp. 1294–1298, Jul. 2020.
[18] A. Iqbal, M. D. Siddique, B. P. Reddy, and P. K. Maroti, "Quadruple boost multilevel inverter (QB-MLI) topology with reduced switch count," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7372–7377, Jul. 2021.

[19] D. Prasad, C. Dhanamjayulu, S. Padmanaban, J. B. Holm-Nielsen, F. Blaabjerg, and S. R. Khasim, "Design and implementation of 31-level asymmetrical inverter with reduced components," *IEEE Access*, vol. 9, pp. 22788–22803, 2021.
[20] C. Dhanamjayulu, D. Prasad, S. Padmanaban, P. K. Maroti, J. B. Holm-Nielsen, and F. Blaabjerg, "Design and implementation of seventeen level inverter with reduced components," *IEEE Access*, vol. 9, pp. 16746–16760, 2021.
[21] K. Thakre, K. B. Mohanty, A. Chatterjee, and V. S. Kommukuri, "A modified circuit for symmetric and asymmetric multilevel inverter with reduced components count," *Int. Trans. Electr. Energy Syst.*, vol. 29, no. 6, Jun. 2019, Art. no. e12011.
[22] B. Mahato, S. Majumdar, and K. C. Jana, "Single-phase modified T-type–based multilevel inverter with reduced number of power electronic devices," *Int. Trans. Electr. Energy Syst.*, vol. 29, no. 11, Nov. 2019, Art. no. e12097.
[23] K.-R. Sorto-Ventura, M. Abarzadeh, K. Al-Haddad, and L. A. Dessaint, "23-level single DC source hybrid PUC (H-PUC) converter topology with reduced number of components: Real-time implementation with model predictive control," *IEEE Open J. Ind. Electron. Soc.*, vol. 1, pp. 127–137, 2020.
[24] M. T. Khosroshahi, A. Ajami, A. O. Mokhberdoran, and M. J. Oskuee, "Multilevel hybrid cascade-stack inverter with substantial reduction in switches number and power losses," *TURKISH J. Electr. Eng. Comput. Sci.*, vol. 23, pp. 987–1000, May 2015.
[25] M. A. Hosseinzadeh, M. Sarbanzadeh, E. Sarbanzadeh, M. Rivera, and P. Wheeler, "New asymmetric cascaded multi-level converter with reduced components," in *Proc. IEEE Int. Conf. Electr. Syst. Aircr., Railway, Ship Propuls. Road Vehicles Int. Transp. Electrific. Conf. (ESARS-ITEC)*, Nov. 2018, pp. 1–6.
[26] R. R. Karasani, V. B. Borghate, P. M. Meshram, and H. M. Suryawanshi, "A modified switched-diode topology for cascaded multilevel inverters," *J. Power Electron.*, vol. 16, no. 5, pp. 1706–1715, Sep. 2016.
[27] S. T. Meraj, N. Z. Yahaya, K. Hasan, and A. Masaoud, "A hybrid T-type (HT-type) multilevel inverter with reduced components," *Ain Shams Eng. J.*, vol. 12, no. 2, pp. 1959–1971, Jun. 2021.
[28] A. Thiruvengadam, "An enhanced H-bridge multilevel inverter with reduced THD, conduction, and switching losses using sinusoidal tracking algorithm," *Energies*, vol. 12, no. 1, p. 81, Dec. 2018.
[29] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, A. Iqbal, and M. A. Memon, "A new multilevel inverter topology with reduce switch count," *IEEE Access*, vol. 7, pp. 58584–58594, 2019.
[30] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, and M. A. Memon, "A new single-phase cascaded multilevel inverter topology with reduced number of switches and voltage stress," *Int. Trans. Electr. Energy Syst.*, vol. 30, no. 2, Feb. 2020, Art. no. e12191.
[31] B. H. Montazer, J. Olamaei, M. Hosseinpour, and B. Mozafari, "A generalized diode containing bidirectional topology for multilevel inverter with reduced switches and power loss," *Int. J. Circuit Theory Appl.*, vol. 49, no. 9, pp. 2959–2978, Sep. 2021.
[32] E. Samadaei, M. Kaviani, and K. Bertilsson, "A 13-levels module (K-type) with two DC sources for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5186–5196, Jul. 2019.
[33] E. Barbie, R. Rabinovici, and A. Kuperman, "Analytical formulation and minimization of voltage THD in staircase modulated multilevel inverters with variable DC ratios," *IEEE Access*, vol. 8, pp. 208861–208878, 2020.
[34] M. A. Hosseinzadeh, M. Sarebanzadeh, M. Rivera, E. Babaei, and P. Wheeler, "A reduced single-phase switched-diode cascaded multilevel inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 3556–3569, Jun. 2021.
[35] J. Huang and K. A. Corzine, "Extended operation of flying capacitor multilevel inverters," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 140–147, Jan. 2006.
[36] M. N. Hamidi, D. Ishak, M. A. A. M. Zainuri, and C. A. Ooi, "An asymmetrical multilevel inverter with optimum number of components based on new basic structure for photovoltaic renewable energy system," *Sol. Energy*, vol. 204, pp. 13–25, Jul. 2020.

DEVALRAJU PRASAD (Graduate Student Member, IEEE) received the B.Tech. degree in electrical and electronics engineering and the M.Tech. degree in electrical power systems from JNTUA, Andhra Pradesh, India, in 2009 and 2015, respectively. He is currently pursuing the Ph.D. degree in power electronics with the Vellore Institute of Technology, Vellore, India. His research interests include multilevel inverters, power converters, and active power filters and power quality.

C. DHANAMJAYULU (Senior Member, IEEE) received the B.Tech. degree in electronics and communication engineering from JNTU University, Hyderabad, India, the M.Tech. degree in control and instrumentation systems from the Indian Institute of Technology Madras, Chennai, India, and the Ph.D. degree in power electronics from the Vellore Institute of Technology, Vellore, India. He was invited as a Visiting Researcher with the Department of Energy Technology, Aalborg University, Esbjerg, Denmark, funded by the Danida Mobility Grant, Ministry of Foreign Affairs of Denmark on Denmark's International Development Cooperation. He was a Postdoctoral Fellow with the Department of Energy Technology, Aalborg University, from October 2019 to January 2021. Since 2010, he has been a Senior Assistant Professor with the Vellore Institute of Technology. His research interests include multilevel inverters, power converters, active power filters, power quality, grid connected systems, smart grid, electric vehicle, electric spring, and tuning of memory elements and controller parameters using soft switching techniques for power converters, average modelling, steady-state modelling, and small-signal modelling stability analysis of the converters and inverters. He is an Academic Editor of the journal *International Transactions on Electrical Energy Systems* (Wiley-Hindawi).