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# Active Damping of VSC-MTDC Grid Equipped With Interline Power Flow Controller

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**ABSTRACT** To ensure the secure operation of a multiterminal high-voltage DC (MTDC) grid, power flow controllers (PFCs) are deployed to regulate current distribution among different transmission lines. Besides power flow management, PFCs are envisioned to provide a range of functionalities such as stability enhancement, oscillation damping, and ancillary services to the host MTDC grid. This paper extends the functionality of PFC to provide active damping of MTDC grid current oscillations caused by dc-side resonance. Three simple and effective active compensators integrated with the control scheme of the PFC are proposed. A comprehensive small-signal model of the MTDC grid is developed. Eigenvalue and sensitivity analyses are conducted to evaluate the damping capability of the proposed compensators and assess their dynamic coupling with PFC control loops. Based on a detailed model of a five-terminal high-voltage dc grid, simulation results are provided to evaluate the performance and effectiveness of the proposed active compensators. The results showed the effectiveness of the proposed compensation schemes in increasing the damping of the MTDC grid and enhancing its dynamic response.

**INDEX TERMS** Active compensators, eigenvalue and sensitivity analysis, MTDC grid, power flow controllers, small-signal model, voltage-source converter.

## I. INTRODUCTION

Over the last decade, high-voltage direct current (HVDC) transmission systems based on voltage-source converters (VSCs) have gained higher momentum in bulk power transmission and gird-interconnection of renewable energy resources, particularly offshore wind power plants. The HVDC-VSC technology offers a wide range of merits, such as the independent control of active and reactive power, the capability to connect to a weak ac grid, and the ease of power reversal [1], [2]. As of 2019, more than 35 HVDC-VSC links have been installed worldwide with a capacity exceeding 20 GW, and these figures are expected to continue increasing in the future [3]. With the increase in HVDC-VSC links, the idea of interconnecting those links to form a multiterminal HVDC (MTDC) grid is gaining considerable attention. A MTDC grid offers several benefits compared to point-to-point links, such as enhanced system reliability, operation flexibility, better robustness, and higher power transfer capability [4], [5]. Examples of MTDC grids currently in their planning stage include the European "SuperGrid" envisioned in the North Sea to tap the abundant wind power of the region and the connection of three primary interconnects (WECC, EI, ERCOT) in the USA [6], [7]. However, MTDC grids impose several technical challenges for large-scale deployments, such as grid protection, power flow control, and dynamic stability [8].

One problem that challenges the realization of a MTDC grid is power flow regulation among different transmission lines. In a meshed MTDC grid, current can circulate in different paths only depending on the voltage difference and line resistance. In this case, with uncontrolled power flow, network congestion and cable overloading may arise, which could challenge the proper operation of the grid. Moreover, uncontrolled power flow can lead to higher system losses and may even degrade the stability of the whole system. Therefore, a new power electronic device called a power flow controller (PFC) is proposed to enhance MTDC grid controllability [9]–[16]. Generally, PFCs can be classified into three categories depending on their connection to the MTDC grid: parallel-connected [9]–[11], series-connected [12]–[14] and parallel-series connected PFCs [15], [16]. Among these

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categories, series-connected PFCs offer several advantages, such as compact size and lower cost, as they are floating at the positive or negative pole of the transmission line. Hence, series-connected PFCs are not required to withstand the rated grid voltage. Multi-port PFC topologies that allow power regulation to any number of lines were proposed in [17], [18]. On the other hand, the idea of deploying multiple simple PFCs, referred to as distributed PFCs, and their selective operation was discussed in [19], [20]. To reduce the cost of PFCs, some research proposed the integration of the power flow control functionality in a dc circuit breaker [21], [22]. Finally, the impact of PFCs on MTDC grid stability and potential dynamic interaction with VSC stations are discussed in [23], [24].

The work in [25] suggested a wide range of futuristic functionalities of PFCs, including the provision of ancillary services to the host grid, oscillation damping, stability improvement, and pole balancing. However, limited studies have addressed the potential of PFCs to achieve these functionalities. The study in [26] explored the oscillation damping functionality of PFC to mitigate dc power oscillation caused by an unbalanced AC grid. In this study, an active damping loop based on a band-pass filter and proportional resonance controller was integrated within the control scheme of the PFC. Another problem that challenges the secure and safe operation of an MTDC grid is the current oscillations originating from MTDC grid resonance. The negative impacts of dc-side resonance on the stability of an HVDC grid were presented in [27], [28]. To solve this problem, active compensators were incorporated with the voltage droop control loop as in [28], [29]. Other studies proposed virtual synchronous generator control to enhance the damping of the MTDC grid and mitigate oscillation caused by dc-side resonance [30], [31]. Despite the effectiveness of these compensation schemes to some extent, they should be implemented in each VSC station which complicates and increases the burden of its control scheme, particularly in the case of modular multi-level VSCs.

This paper extends the functionality of the PFC beyond regulating the lines currents to provide active damping of dc oscillations caused by MTDC grid resonance. Three simple and effective active damping schemes incorporated with the control methodology of PFC are proposed. These schemes depend on modifying the transmission line impedance by injecting an active damping signal at the outer and inner control loop of the PFC. First, a comprehensive linearized state-space model that captures the dynamics of all subsystems of the MTDC grid is developed. Then, based on the developed state-space model, eigenvalue analysis is applied to evaluate the performance of the proposed compensators and assess their impact on the stability of the MTDC grid. Moreover, sensitivity analysis is conducted to study the effect of the proposed compensators on the current tracking capability of the PFC. Finally, time-domain simulations are presented to validate the theoretical analysis and the effectiveness of the proposed damping schemes.

The contributions of this paper to the research field are as follows:

1) Analyzing oscillations originating from dc-side resonance in an MTDC grid with PFCs using a comprehensive small-signal model.
2) Developing three simple active compensators incorporated with the control scheme of the PFC to enhance the dynamic response of the MTDC grid, and
3) Comparing and assessing the performance of the proposed active compensators.

The rest of this paper is organized as follows. The next section describes the modeling of each subsystem in the analyzed MTDC grid and presents validation results of the developed small-signal model. Section III discusses dc oscillations in the MTDC grid. In Section IV, the proposed active compensators are described. Section V provides a comparative study of the proposed damping schemes. Simulation results are presented in Section VI. Finally, in Section VII, conclusions are drawn.

## II. SYSTEM DESCRIPTION AND MODELING

Fig. 1 shows the single-line diagram of the analyzed MTDC grid. Each terminal is interfaced to the ac system via a central VSC that is regulated in either constant power control mode or constant power with voltage droop control mode. The VSC is connected to the PCC through the ac side filter ($R_f - L_f - C_f$). The ac system is represented by a stiff three-phase voltage source, $V_{gabc}$, and its strength at the PCC is represented by the grid impedance ($R_g + j\omega L_g$). A dc-link capacitor ($C_{dc}$) is used to interface the VSC to the dc grid. Five transmission lines are connected between the VSC terminals to allow active power exchange. The modeling details of all system components are discussed in the following sections.

### A. VSC AND AC GRID-SIDE DYNAMICS

Using the ac system d-q reference synchronous frame, where the d-axis of the reference frame is aligned with the ac system stiff voltage $V_g$, the AC-side dynamics can be described in the $s$-domain as follows:

$$\left(R_f + sL_f\right) I_{sd} = V_{td} - V_{sd} + \omega_g L_f I_{sq} \quad (1)$$

$$\left(R_f + sL_f\right) I_{sq} = V_{tq} - V_{sq} - \omega_g L_f I_{sd} \quad (2)$$

$$\left(R_g + sL_g\right) I_{gd} = V_{sd} - V_{gd} + \omega_g L_g I_{gq} \quad (3)$$

$$\left(R_g + sL_g\right) I_{gq} = V_{sq} - V_{gq} - \omega_g L_g I_{gd} \quad (4)$$

$$sC_f V_{sd} = I_{sd} - I_{gd} + \omega_g C_f V_{sq} \quad (5)$$

$$sC_f V_{sq} = I_{sq} - I_{gq} - \omega_g C_f V_{sd} \quad (6)$$

where $V_{tdq}$ and $I_{sdq}$ are the VSC output terminal voltage and current in the grid d-q reference frame, respectively. $V_{gdq}$ and $I_{gdq}$ are $d$-$q$ components of ac system voltage and current. $V_{sdq}$ are the $d$-$q$ components of the PCC voltage. $\omega_g$ is the ac system voltage angular frequency.

The active and reactive power exchanged between the VSC, and the ac system at the PCC are described as follows:

$$P_s = 1.5(V_{sd} I_{sd} + V_{sq} I_{sq}) \quad (7)$$

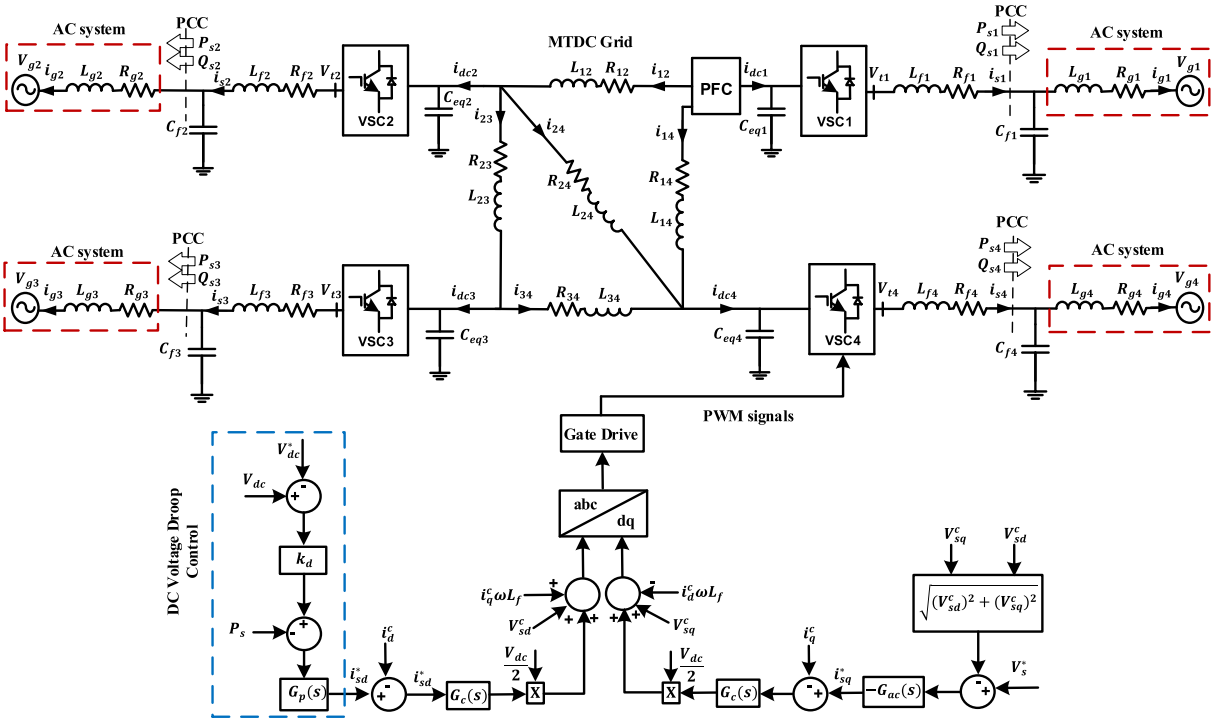


**FIGURE 1.** Analyzed MTDC grid and VSC control scheme.

$$Q_s = 1.5(-V_{sd}I_{sq} + V_{sq}I_{sd}) \tag{8}$$

The dc-link voltage dynamic can be described as

$$\frac{1}{2}C_{dc}sV_{dc}^2 = V_{dc}I_{dc} - 1.5(V_{td}I_{td} + V_{tq}I_{tq}) \tag{9}$$

The VSC control objective is to regulate the dc-link voltage and the PCC AC voltage to their reference values. This can be achieved by adjusting the active and reactive power change between the VSC and the ac system. Therefore, a nested control structure consisting of outer and inner control loops is typically applied, as shown in Fig. 1. In this study, droop voltage control is implemented to regulate the grid voltage due to its simplicity and effectiveness in regulating dc voltages in an MTDC grid. The outer and inner control loops can be described as follows:

$$I_{sd}^* = \left[-\left(V_{dc}^* - V_{dc}\right)k_d - P_s\right]G_p(s) \tag{10}$$

$$I_{sq}^* = -\left(V_{sd}^* - V_{sd}^c\right)G_{ac}(s) \tag{11}$$

$$V_{td}^c = \frac{V_{dc}}{2}m_d^c + V_{sd}^c - \omega_g L_f I_{sq}^c \tag{12}$$

$$V_{tq}^c = \frac{V_{dc}}{2}m_q^c + V_{sq}^c + \omega_g L_f I_{sd}^c \tag{13}$$

where $k_d$ is the droop voltage controller gain. $G_p(s)$ and $G_{ac}(s)$ are the transfer function of the power and AC voltage PI controllers, respectively. The superscript "$c$" signifies that the variables are represented in the converter $d$-$q$ reference frame. $m_{dq}^c$ are the $d$-$q$ components of the VSC duty ratios, which are given by

$$m_d^c = (I_{sd}^* - I_{sd}^c)G_c(s) \tag{14}$$

$$m_q^c = (I_{sq}^* - I_{sq}^c)G_c(s) \tag{15}$$

where $G_c(s)$ is the transfer function of the VSC PI current controller.

A $d$-$q$ Phase-locked loop (PLL) is typically deployed in the VSC control structure to synchronize with the PCC voltage. The PLL extracts the angle of the PCC voltage ($\delta$), which relates the electrical quantities in the converter reference frame to the ac system reference as [32]

$$F_{dq}^c = F_{dq}e^{-j\delta} \tag{16}$$

where $F_{dq}^c$ and $F_{dq}$ represent measured quantities in the converter and ac system reference frame, respectively. The PLL uses a PI controller ($G_{pll}(s)$) to track the angle $\delta$ and its dynamics can be described by

$$\delta = \frac{1}{s}G_{pll}(s)V_{sd}^c \tag{17}$$

### B. PFC DYNAMICS

The topology of the interline PFC implemented in this study is shown in Fig. 2 [12]. The PFC is deployed between lines $L_{12}$ and $L_{14}$ to regulate their current flow by allowing power exchange between the two lines. A detailed discussion of the PFC operation principle is presented in [33]. The PFC is primarily a dc-dc converter that inserts dc voltage into transmission lines to adjust their currents to a reference value. For example, with the current flow configuration in Fig. 2, switching S1 while S5 is ON applies a mean positive dc voltage between terminals 1 and 2 and a negative dc voltage between terminals 1 and 4. Thus, current $I_{12}$ decreases, while current $I_{14}$ increases. The generated voltages by the PFC can be described as

$$V_{12} = (1 - D)\,V_{pfc}, \quad V_{14} = -D.V_{pfc} \tag{18}$$

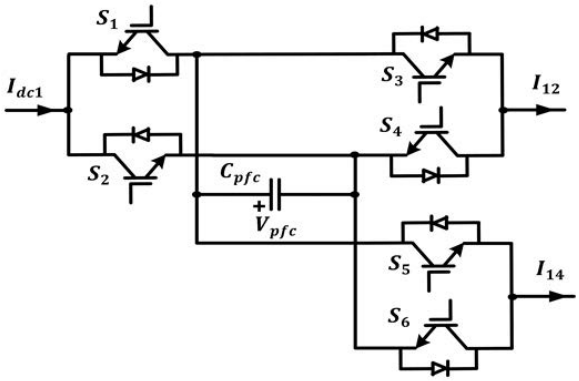


**FIGURE 2.** PFC topology.

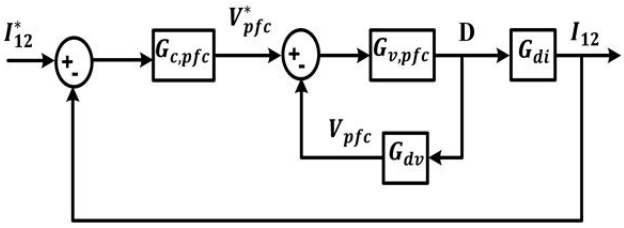


**FIGURE 3.** PFC control scheme.

where $V_{12}$ and $V_{14}$ are the voltages inserted by the PFC into lines L12 and L14, respectively. The control scheme of the PFC is shown in Fig. 3. A nested control structure that resembles the vector control methodology of VSC is implemented. Two control loops are employed; the outer loop regulates the line current using a current compensator ($G_{c,pfc}(s)$) composed of a PI regulator and a low-pass filter to provide gain damping at higher frequencies [33]. The inner loop uses a PI compensator ($G_{v,pfc}(s)$) to adjust the PFC capacitor voltage to its reference. The PFC control loop dynamics can be described as

$$V_{pfc}^* = (I_{12}^* - I_{12})G_{c,pfc}(s) \tag{19}$$
$$D = (V_{pfc}^* - V_{pfc})G_{v,pfc}(s) \tag{20}$$

where $I_{12}^*$ and $V_{pfc}^*$ are the PFC reference current and voltage, respectively. $D$ is the PFC duty ratio. The PFC capacitor voltage dynamics can be obtained as

$$C_{pfc}sV_{pfc} = (1 - D)\, I_{12} - DI_{14} \tag{21}$$

where $C_{pfc}$ is the PFC capacitance. $C_{pfc}$ should be selected so that the peak-to-peak ripple voltage on the PFC is within permissible limits.

### C. MTDC GRID EQUIPPED WITH PFC DYNAMICS

The dc transmission lines are modeled using a single $\pi$ section equivalent circuit. The single $\pi$ model is sufficiently accurate to model the dynamics of the dc line up to 100 Hz [34]. Considering the equivalent dc voltage applied by the PFC on lines L12 and L14, the MTDC grid dynamics can be described by

$$(R_{12} + sL_{12})\, I_{12} = V_{dc1} - V_{dc2} - (1 - D)V_{pfc} \tag{22}$$
$$(R_{14} + sL_{14})\, I_{14} = V_{dc1} - V_{dc4} + DV_{pfc} \tag{23}$$
$$(R_{23} + sL_{23})\, I_{23} = V_{dc2} - V_{dc3} \tag{24}$$

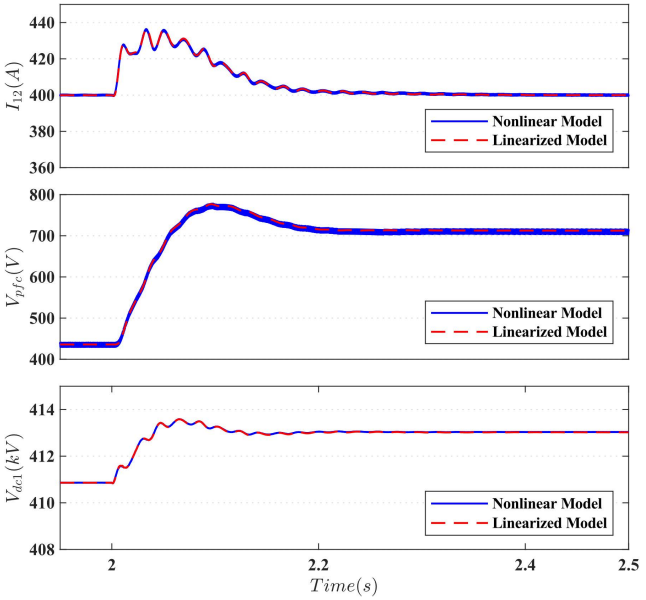


**FIGURE 4.** Small-signal model validation results.

$$(R_{24} + sL_{24})\, I_{24} = V_{dc2} - V_{dc4} \tag{25}$$
$$(R_{34} + sL_{34})\, I_{34} = V_{dc3} - V_{dc4} \tag{26}$$

### D. SMALL-SIGNAL MODEL VALIDATION

Equations (1) – (26) describe the large-signal dynamics of each subsystem of the grid-connected MTDC grid equipped with PFC. To investigate the dynamic stability of the system, (1) – (26) are linearized (see Appendix), and the overall system linearized state-space model can be described as

$$\dot{\tilde{X}} = A\tilde{X} + B\tilde{U} \tag{27}$$
$$\tilde{Y} = C\tilde{X} + D\tilde{U} \tag{28}$$

where $A$, $B$, $C$, and $D$ are the characteristic matrix, control matrix, output matrix, and feedforward matrix, respectively. $\tilde{X}$, $\tilde{Y}$, and $\tilde{U}$ denote the small-signal state vector, output vector, and input vector.

To verify the accuracy of the developed small-signal model of the analyzed system, the linearized state-space model (27 and 28) is numerically solved in the MATLAB environment. Its response is compared with the detailed nonlinear time-domain system model built in the MATLAB/Simulink. The response of $V_{pfc}$ is shown in Fig. 4. Initially, the system is at a steady-state, whereas the PFC regulates the line current $I_{12}$ at 400 A. Then, at $t = 2$ s, the power injection of VSC1 is increased by 50 MW. The results show the close matching between the small-signal and large-signal models responses. Thus, verifying the accuracy of the developed linear model.

## III. DC OSCILLATIONS AND RESONANCE ANALYSIS IN MTDC GRID

The MTDC grid is a complex system prone to instability due to system resonance and controllers' interactions. Instabilities originating from the dc-network resonances have been reported in [27], [28]. The dc-link capacitor is a critical component in VSC stations which is designed considering

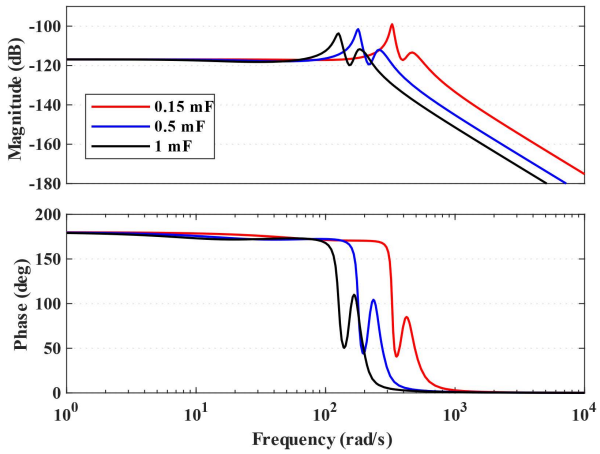


**FIGURE 5.** Frequency response of the TF $I_{12}/P_1^*$ for varying $C_{dc}$.

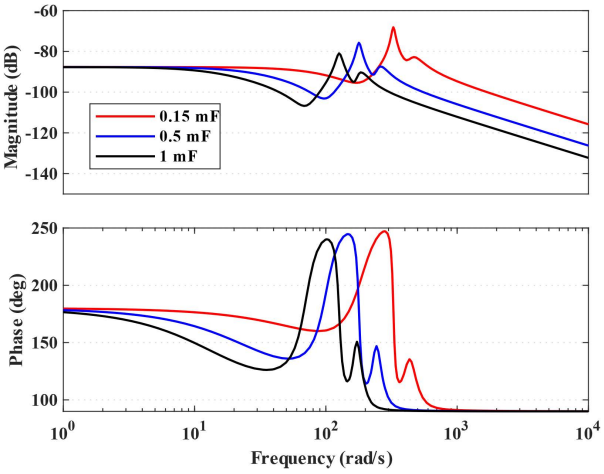


**FIGURE 6.** Frequency response of the TF $V_{dc1}/P_1^*$ for varying $C_{dc}$.

the voltage ripple limit requirement and acceptable controller dynamics. The VSC dc-link capacitance and the capacitance and inductance of the MTDC grid lines/cables form lightly damped LC circuits that give rise to current and power resonances. These resonances lead to degraded transient system response and eventually instability. Therefore, damping the resonance modes in the system is essential to ensure its efficient and reliable operation.

Using the linearized state-space model (27 and 28), the transfer function relating the current $I_{12}$ to the active power injection $P_1$ and is obtained. The frequency response of this transfer function under varying the dc link capacitance is shown in Fig. 5. It can be noted that as the dc link capacitance increases, the resonance frequency and amplitude decrease. Similar behavior can be obtained from the transfer function relating the voltage $V_{dc1}$ to $P_1$ as depicted in Fig. 6. This result implies that to mitigate the resonance in MTDC grid, the dc-link capacitance should be increased. However, increasing the capacitance will increase the system footprint and costs. Therefore, active suppression of dc resonance should be implemented.

The critical eigenvalues of the MTDC grid based on the detailed model in (27) are depicted in Fig. 7 and Table 1.

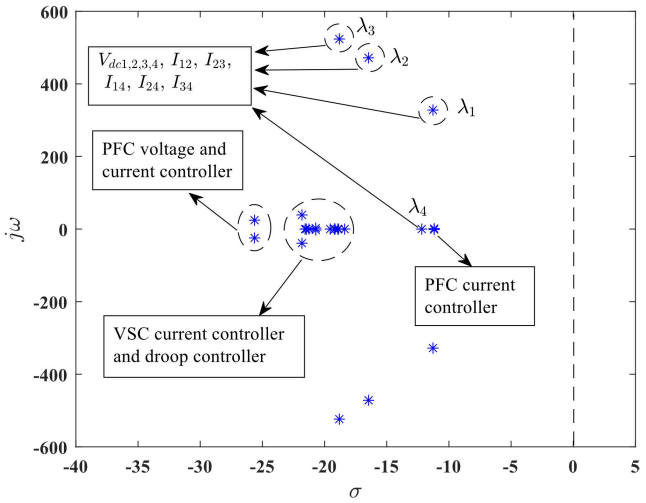


**FIGURE 7.** MTDC grid critical eigenvalues.

**TABLE 1.** Critical eigenvalue analysis.

| Mode | Eigenvalue | f, Hz | ζ | Influencing states |
|---|---|---|---|---|
| $\lambda_1$ | -11.78 ± j327.95 | 52.19 | 0.036 | DC grid |
| $\lambda_2$ | -16.57 ± j471.63 | 75.06 | 0.035 | DC grid |
| $\lambda_3$ | -18.72 ± j523.23 | 83.27 | 0.036 | DC grid |
| $\lambda_4$ | -12.18 | 0 | 1 | DC grid |
| $\lambda_5$ | -11.18 ± j1.43 | 0.23 | 0.992 | PFC control |

The participation factor analysis is applied to determine the root states that affect these eigenvalues. It has been found that modes ($\lambda_1 - \lambda_4$) are mainly affected by the dc network. These modes ($\lambda_1 - \lambda_3$) have a damping ratio lower than 0.05. Therefore, they are regarded as poorly damped modes, which may give rise to low-frequency oscillations and can even lead to system small-signal instability. Hence, increasing the damping ratio of these modes would lead to improved dynamic system response and enhance the system's relative stability. Other critical modes in the system are related to PFC controllers, VSC current controllers, and droop voltage controllers. These modes are well-damped compared to dc grid-related modes.

## IV. PROPOSED ACTIVE DAMPING COMPENSATORS

This section introduces three simple dc oscillation damping schemes to improve the performance and dynamic response of the MTDC grid. The proposed schemes are internal model-based active compensators, wherein an active damping signal is injected at the outer and inner loop of the PFC.

### A. PFC OUTER LOOP-BASED COMPENSATION

This scheme injects a damping signal at the outer current control loop of the PFC. The damping signal is a modified version of the line current obtained using a linear compensator and a scaling gain. Two compensators are proposed to generate the outer loop damping signal; one is a band-limited derivative compensator (high-pass filter (HPF)), and

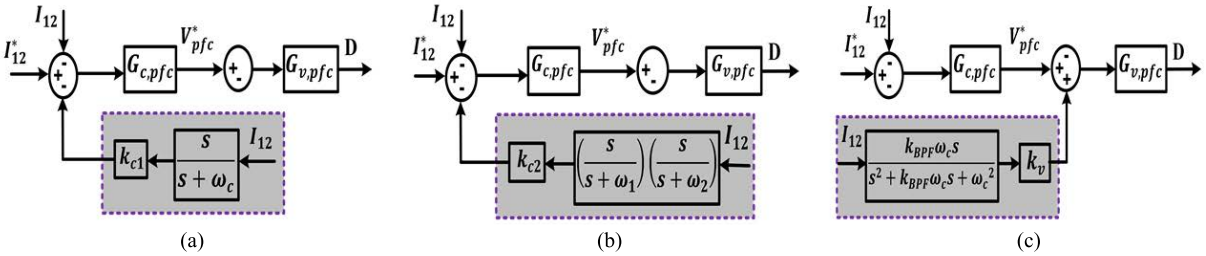


**FIGURE 8.** Proposed active compensators. (a) Outer loop-based HPF (b) outer loop-based DHPF (c) inner loop-based BPF.

the second is a double high-pass filter (DHPF) based compensator. The schematic diagram of the HPF- and DHPF-based outer compensation loops is shown in Fig. 8(a) and (b), respectively. The transfer functions of the two-outer loop-based compensators are as follows:

$$c_1(s) = k_{c1}\frac{s}{s+\omega_c} \tag{29}$$

$$c_2(s) = k_{c2}\left(\frac{s}{s+\omega_1}\right)\left(\frac{s}{s+\omega_2}\right) \tag{30}$$

where; $k_{c1}$ and $k_{c2}$ are the compensators' scaling gains. $\omega_c$, $\omega_1$ and $\omega_2$ are the cut-off frequencies.

### B. PFC INNER LOOP-BASED COMPENSATION

This method injects an active damping signal at the inner voltage control loop of the PFC. The proposed compensator is based on a band-pass filter that generates a scaled version of the line current disturbance. The damping signal is added to the PFC reference voltage. A schematic diagram of the inner loop-based active compensator is depicted in Fig. 8(c). The compensator transfer function can be described as

$$c_3(s) = k_v\frac{k_{BPF}\omega_c s}{s^2+k_{BPF}\omega_c s+\omega_c^2} \tag{31}$$

where; $k_v$ is the compensator gain, $k_{BPF}$ and $\omega_c$ are the BPF gain and cut-off frequency, respectively.

## V. PERFORMANCE COMPARISON AND DAMPING CAPABILITIES OF PROPOSED COMPENSATORS

Eigenvalue analysis is applied to evaluate the damping capabilities of the proposed active compensation schemes and determine their optimal parameters. Using the developed small-signal model (27) and adding the dynamics for the proposed damping schemes (29, 30, and 31), the impact of varying the compensators' design parameters, cut-off frequency, and scaling gain on the system dominant eigenvalues is shown in Fig. 9. The optimal parameters for each compensator can be obtained by varying the cut-off frequency and scaling gain to achieve maximum possible damping while minimizing the dynamic interactions with the PFC control loops. As shown in Fig. 9, adding the active compensation loop enhances the system stability margin by shifting the critical poorly damped modes to the LHP. As the compensator gain increases at each cut-off frequency, the system eigenvalues are shifted to the LHP until a certain value at which further increase in the gain moves the dominat eigenvalue to the RHP. The impact of

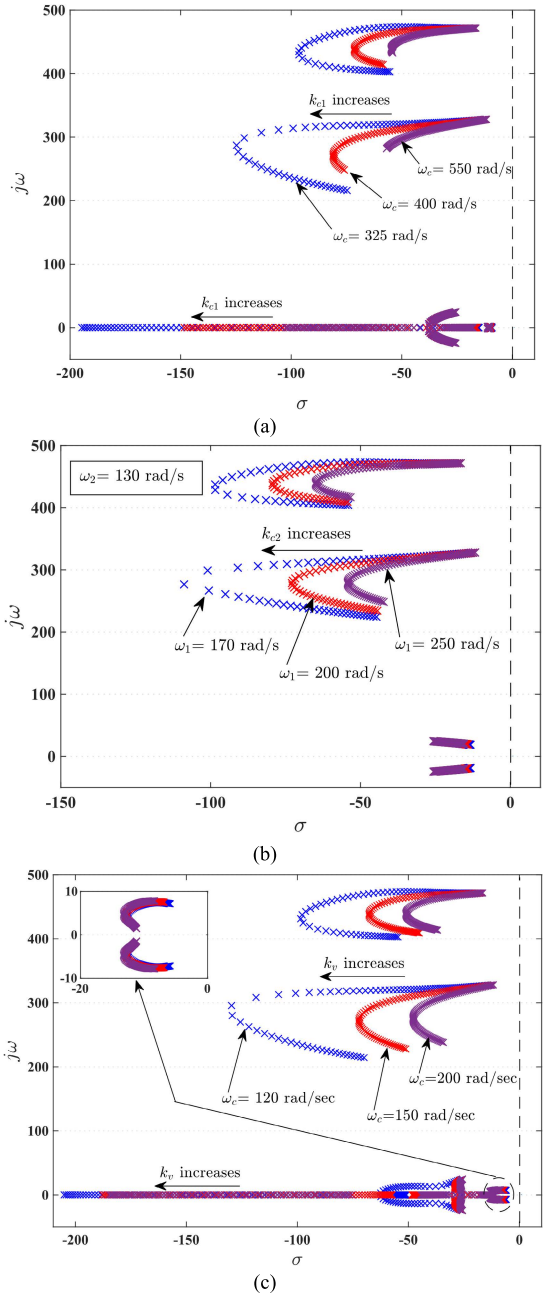


**FIGURE 9.** Damping impact of proposed compensators. (a) Outer loop HPF (b) outer loop DHPF (c) inner loop (d) all loops.

the three compensation loops on the damping of the critical modes is presented in Table 2. As shown in Fig. 10 and

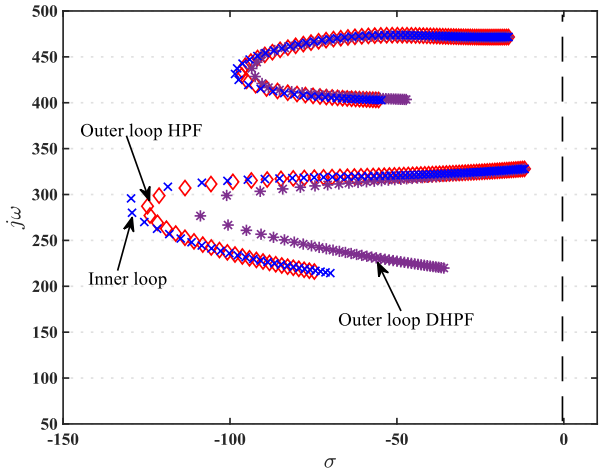


**FIGURE 10.** Comparison between the three compensators.

**TABLE 2.** Damping impact of the proposed compensators.

| Case | Damping ratio ($\lambda_1 = -11.78 \pm j327.95$) | Damping ratio ($\lambda_2 = -16.57 \pm j471.63$) |
|---|---|---|
| No compensation | 0.0359 | 0.0351 |
| Outer loop HPF | 0.3982 | 0.2164 |
| Outer loop DHPF | 0.3529 | 0.1941 |
| Inner loop | 0.4014 | 0.2183 |

Table 1, the three compensators have comparable damping capability. The inner loop compensator provides the most damping, and the DHPF outer loop compensator has the lowest damping performance.

An important aspect that should be considered when assessing the performance of the proposed compensators is their impact on the line current tracking capability of the PFC. Using the system small-signal model (27 and 28) and adding the compensators' dynamics, the closed-loop transfer function relating the line current and its reference under each of the three compensators is obtained. Fig. 11 shows a comparison between the frequency response of the uncompensated and compensated PFC current tracking transfer function. The uncompensated PFC current loop is designed with a bandwidth of 30 rad/s. It can be noted that the HPF outer loop compensator and the inner loop compensator yield the strongest dynamic coupling resulting in a decrease of current loop bandwidth to 12.3 rad/s and 16.7 rad/s, respectively. On the contrary, The DHPF outer loop-based compensator shows a highly decoupled performance, with the current bandwidth only reduced to 27 rad/s.

## VI. SIMULATION RESULTS AND DISCUSSIONS

A detailed model of the MTDC grid, depicted in Fig. 1, is implemented in the MATLAB/Simulink environment to assess the performance of the proposed active compensators. The grid operates at a dc-voltage of 400 kV with droop voltage control carried out by VSC2 and VSC4, whereas VSC1 and VSC3 operate on the constant power control mode. The MTDC grid and PFC parameters, VSC stations parameters, and VSC and PFC control parameters are provided in the Appendix and Tables 3 to 5. The designed compensators parameters are presented in Table 6. The eigenvalue analysis discussed in Section V is used to determine the compensators' parameters. Three simulation scenarios are discussed; the uncompensated system, actively compensated system, and performance of the proposed compensators under a single line to ground fault.

### A. UNCOMPENSATED SYSTEM RESPONSE

The response of the MTDC grid line currents is shown in Fig. 12(a). Several disturbance events are applied to evaluate the grid response. Initially, the system is operated in a steady-state, whereas the power injection by VSC1 and VSC3 are 350 MW and 0 MW, respectively, and the PFC maintains current $I_{12}$ at 400 A. Then, at $t = 2$ s, VSC3 injects 150 MW into the AC grid. Due to this disturbance, the MTDC grid currents suffer transient oscillations that are not properly damped. At $t = 2.5$ s, the power injection from VSC1 is increased to 400 MW. It can be noted that the PFC properly maintains the current $I_{12}$ at its reference value. Finally, at $t = 3$ s, the PFC reference current is increased to 450 A. The response of the terminals' voltage and PFC voltage is shown in Fig. 12(b). The results show the effectiveness of the voltage droop controller in maintaining the dc grid voltage within permissible limits by regulating the power injection of VSC2 and VSC4 to share the power deviation. Moreover, the PFC capacitor voltage is appropriately regulated to maintain the line current at its reference value.

### B. COMPENSATED SYSTEM RESPONSE

The proposed active compensators are implemented in the simulation model, and the response of the system under the sequence of disturbances described in the previous sub-section is obtained. The response of the currents $I_{12}$ and $I_{23}$ under each of the three compensators is depicted in Fig. 13. The results show the effectiveness of the proposed compensators in mitigating the grid currents oscillation due to increased damping. It can be noted that the three compensators have close damping capability, whereas the HPF outer loop-based and inner loop-based compensators provide the strongest damping and the DHPF compensator has the least damping of the three compensators. However, as it can be clearly noted, when a step-change in the PFC reference current is applied at $t = 3$ s, the HPF outer loop compensator and inner loop compensator show high coupling with the PFC current tracking capability resulting in a noticeable slowdown of the current tracking response. On the other hand, the DHPF outer loop compensator shows a strong decoupled response and does not affect the current tracking dynamics, as depicted in Fig. 13(b). The simulation results confirm the damping capability and dynamic interaction analysis presented in Section V. It is important to highlight that the proposed compensators have a damping impact on all transmission lines currents but only $I_{12}$ and $I_{23}$ are presented for comparison. Fig. 14 shows the dc voltage of VSC 1 and

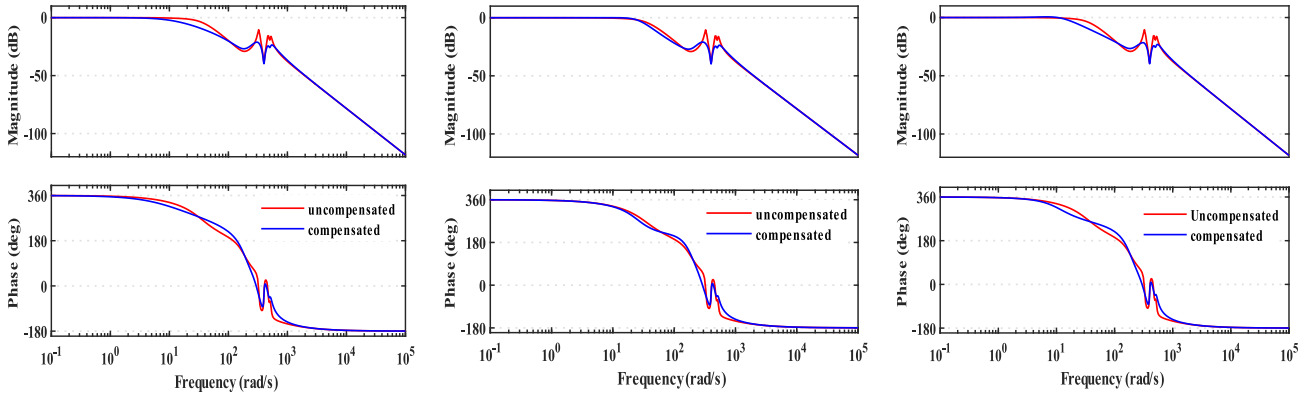


**FIGURE 11.** Frequency response of the closed-loop transfer function for PFC current tracking. (a) HPF outer loop; (b) DHPF outer loop; (c) inner loop compensator.

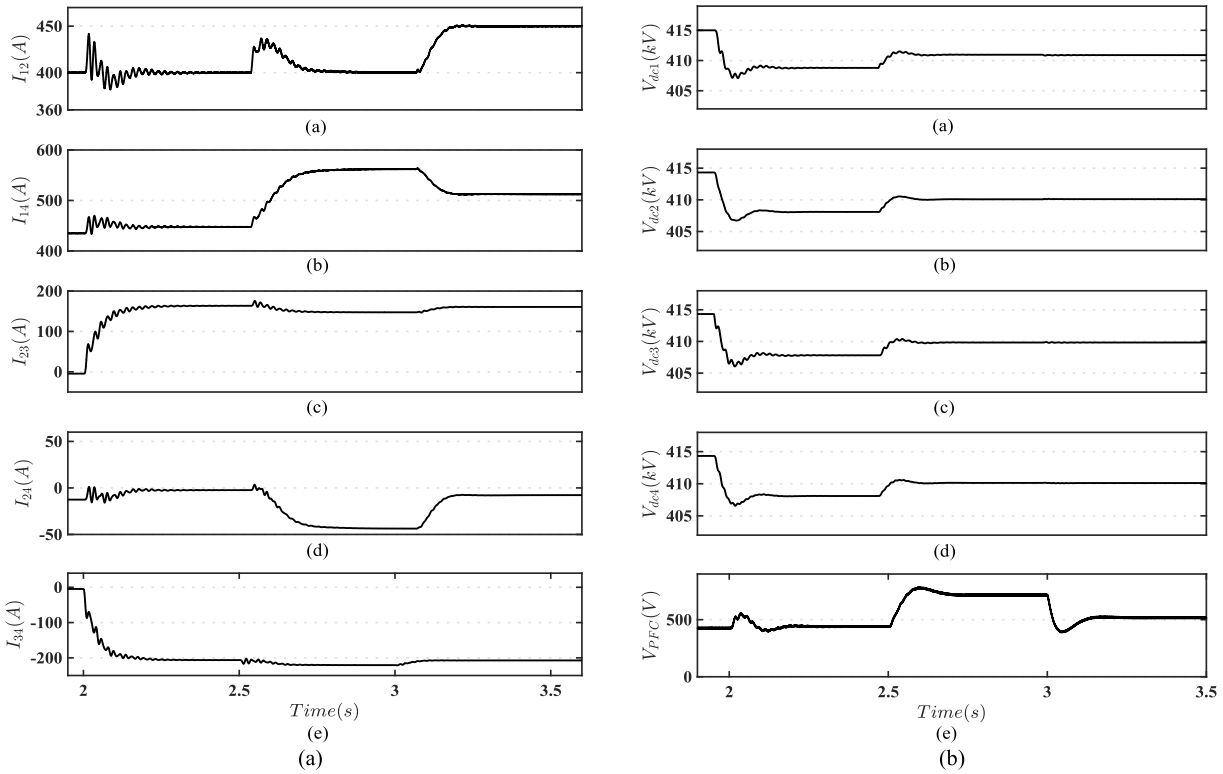


**FIGURE 12.** Response of the uncompensated MTDC grid. (a) Line currents response (b) Terminals and PFC voltage response.

PFC capacitor voltage under each of the proposed compensators. The dc-link voltage shows improved response due to the suppression of transmission lines' current oscillations. The damping loop appropriately modulates the PFC capacitor voltage during power disturbances to suppress line currents oscillations. Although the PFC voltage exhibits a transient overshoot, the voltage magnitude does not exceed the PFC capacitor nominal voltage.

### C. OPERATION UNDER FAULT CONDITION

In this sub-section, the impact of the DHPF outer loop-based compensator under single-line-to-ground fault at PCC3 is investigated. The fault, which results in a 50% sag of the ac voltage, occurred at $t = 2$ s and was cleared after 200 ms. As shown in Fig. 15, the uncompensated and compensated line current $I_{12}$ is subjected to double-fundamental frequency oscillations after the fault is applied. However, as depicted in Fig. 15(a), the uncompensated current has a higher peak and settling time after clearing the fault. Fig. 15(b) shows that the active compensator results in reduced oscillations and lower settling time than the uncompensated system due to increased damping.

## VII. CONCLUSION

This paper presented the oscillation damping functionality of the PFC to mitigate the current oscillations originating from dc-side resonance in an MTDC grid. Three active compensators integrated within the control loop of the PFC are

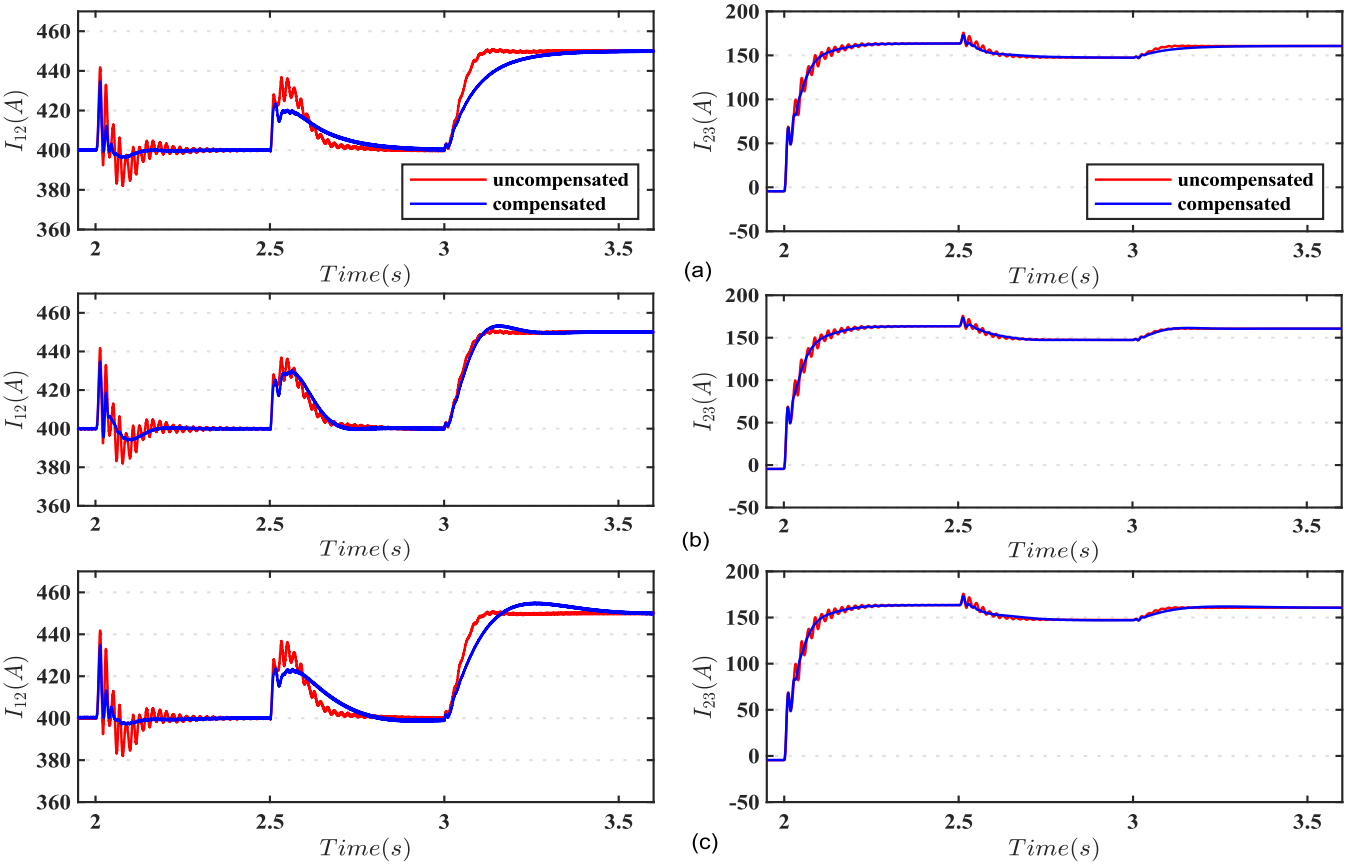


**FIGURE 13.** Response of compensated currents $I_{12}$ and $I_{23}$. (a) HPF outer loop; (b) DHPF outer loop; (c) inner loop compensator.

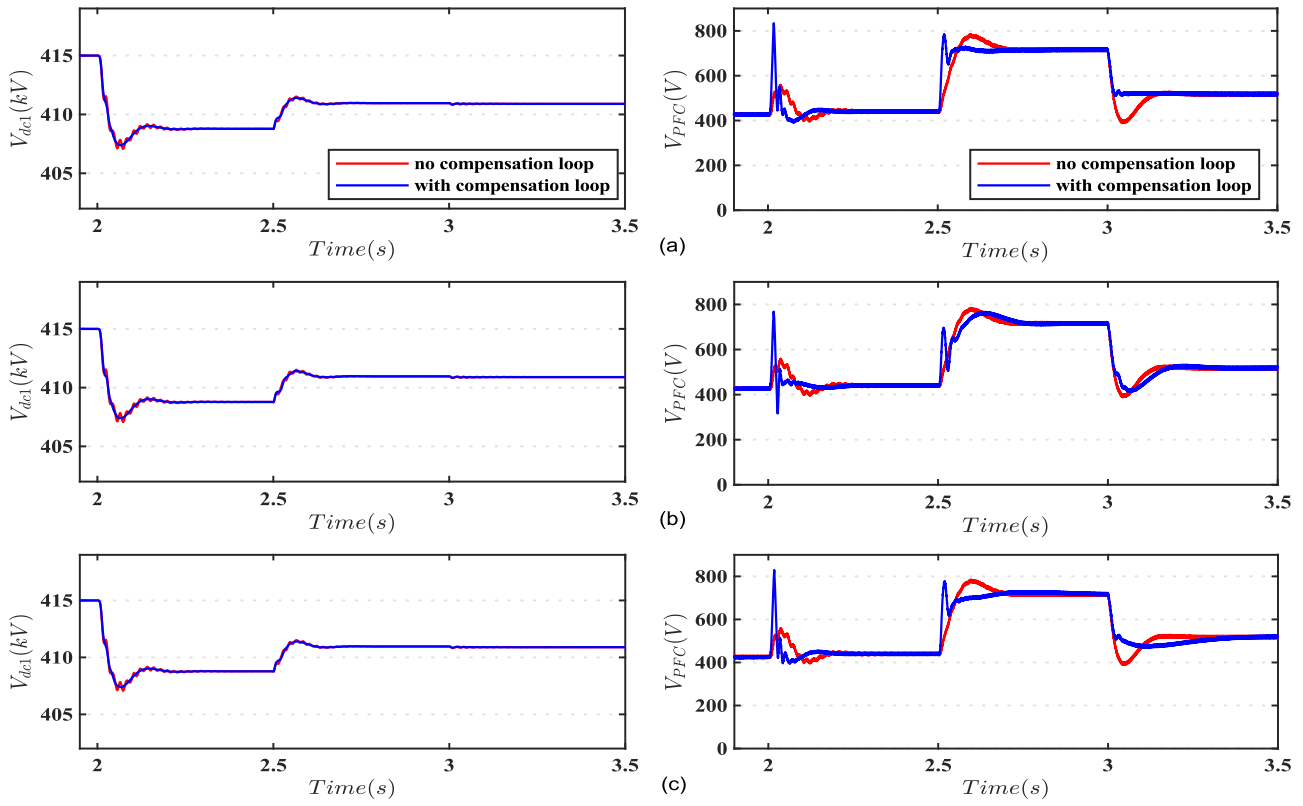


**FIGURE 14.** Response of $V_{dc1}$ and $V_{PFC}$ with active compensation. (a) HPF outer loop; (b) DHPF outer loop; (c) inner loop compensator.

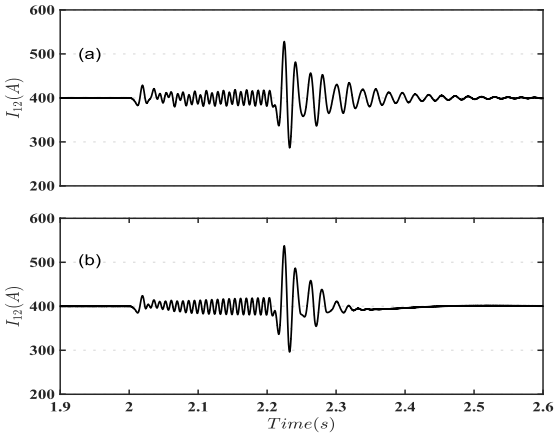


**FIGURE 15.** Response of current $I_{12}$ under single-line-to-ground fault: (a) Uncompensated system (b) Actively compensa.

proposed to improve the dynamic response of the MTDC grid. The proposed compensators inject a damping signal at the outer and inner control loop of the PFC. Eigenvalue and sensitivity analyses, based on the developed small-signal model, are conducted to assess the performance of the proposed compensators. The study indicated that the three compensators have a comparable damping capability, with the inner loop compensator providing the strongest damping. Furthermore, the sensitivity analysis showed that the DHPF outer loop compensator yields a highly decoupled performance with the current control loop of the PFC. In contrast, the HPF outer loop compensator showed a highly coupled response. Therefore, to achieve a highly damped and decoupled dynamic performance, the DHPF outer loop compensator can be implemented. The simulation results confirmed the theoretical analysis and the effectiveness of the proposed compensators in improving the dynamic response of the MTDC grid.

## APPENDIX

### A. SMALL-SIGNAL MODEL OF VSC1

#### 1) GRID-SIDE DYNAMICS FOR VSC1

$$\frac{d}{dt}\begin{bmatrix}\tilde{i}_{d1}\\ \tilde{i}_{q1}\end{bmatrix} = \underbrace{\begin{bmatrix}\frac{-R_{f1}}{L_{f1}} & w_o\\ -w_o & \frac{-R_{f1}}{L_{f1}}\end{bmatrix}}_{A11}\begin{bmatrix}\tilde{i}_{d1}\\ \tilde{i}_{q1}\end{bmatrix} + \underbrace{\begin{bmatrix}\frac{1}{L_{f1}} & 0\\ 0 & \frac{1}{L_{f1}}\end{bmatrix}}_{B11}\begin{bmatrix}\tilde{v}_{td1}\\ \tilde{v}_{tq1}\end{bmatrix} + \underbrace{\begin{bmatrix}\frac{-1}{L_{f1}} & 0\\ 0 & \frac{-1}{L_{f1}}\end{bmatrix}}_{C11}\begin{bmatrix}\tilde{v}_{sd1}\\ \tilde{v}_{sq1}\end{bmatrix} + \underbrace{\begin{bmatrix}i_{q1o}\\ -i_{d1o}\end{bmatrix}}_{D11}[\tilde{w}_1]$$

$$\frac{d}{dt}\begin{bmatrix}\tilde{i}_{gd1}\\ \tilde{i}_{gq1}\end{bmatrix} = \underbrace{\begin{bmatrix}\frac{-R_{g1}}{L_{g1}} & w_o\\ -w_o & \frac{-R_{g1}}{L_{g1}}\end{bmatrix}}_{A21}\begin{bmatrix}\tilde{i}_{gd1}\\ \tilde{i}_{gq1}\end{bmatrix} + \underbrace{\begin{bmatrix}\frac{1}{L_{g1}} & 0\\ 0 & \frac{1}{L_{g1}}\end{bmatrix}}_{B21}\begin{bmatrix}\tilde{v}_{sd1}\\ \tilde{v}_{sq1}\end{bmatrix} + \underbrace{\begin{bmatrix}\frac{-1}{L_{g1}} & 0\\ 0 & \frac{-1}{L_{g1}}\end{bmatrix}}_{C21}\begin{bmatrix}\tilde{v}_{gd1}\\ \tilde{v}_{gq1}\end{bmatrix} + \underbrace{\begin{bmatrix}i_{gq1o}\\ -i_{gd1o}\end{bmatrix}}_{D21}[\tilde{w}_1]$$

$$\frac{d}{dt}\begin{bmatrix}\tilde{v}_{sd1}\\ \tilde{v}_{sq1}\end{bmatrix} = \underbrace{\begin{bmatrix}0 & w_o\\ -w_o & 0\end{bmatrix}}_{A31}\begin{bmatrix}\tilde{v}_{sd1}\\ \tilde{v}_{sq1}\end{bmatrix} + \underbrace{\begin{bmatrix}\frac{1}{C_{f1}} & 0\\ 0 & \frac{1}{C_{f1}}\end{bmatrix}}_{B31}\begin{bmatrix}\tilde{i}_{d1}\\ \tilde{i}_{q1}\end{bmatrix} + \underbrace{\begin{bmatrix}\frac{-1}{C_{f1}} & 0\\ 0 & \frac{-1}{C_{f1}}\end{bmatrix}}_{C31}\begin{bmatrix}\tilde{i}_{gd1}\\ \tilde{i}_{gq1}\end{bmatrix} + \underbrace{\begin{bmatrix}v_{sq1o}\\ -v_{sd1o}\end{bmatrix}}_{D31}[\tilde{w}_1]$$

#### 2) PHASE-LOCKED LOOP MODEL

$$\frac{d}{dt}\begin{bmatrix}\tilde{\theta}_1\\ \tilde{x}_{pll1}\end{bmatrix} = \underbrace{\begin{bmatrix}0 & k_{i1}\\ 0 & 0\end{bmatrix}}_{A41}\begin{bmatrix}\tilde{\theta}\\ \tilde{x}_{pll1}\end{bmatrix} + \underbrace{\begin{bmatrix}0 & k_{p1}\\ 0 & 1\end{bmatrix}}_{B41}\begin{bmatrix}\tilde{v}^c_{sd1}\\ \tilde{v}^c_{sq1}\end{bmatrix}$$

$$\tilde{w}_1 = \underbrace{\begin{bmatrix}0 & k_{i1}\end{bmatrix}}_{A51}\begin{bmatrix}\tilde{\theta}_1\\ \tilde{x}_{pll1}\end{bmatrix} + \underbrace{\begin{bmatrix}0 & k_{p1}\end{bmatrix}}_{B51}\begin{bmatrix}\tilde{v}^c_{sd1}\\ \tilde{v}^c_{sq1}\end{bmatrix}$$

#### 3) CONVERTER AND AC SYSTEM REFERENCE FRAME TRANSFORMATION

$$\begin{bmatrix}\tilde{v}^c_{sd1}\\ \tilde{v}^c_{sq1}\end{bmatrix} = \begin{bmatrix}\tilde{v}_{sd1}\\ \tilde{v}_{sq1}\end{bmatrix} + \underbrace{\begin{bmatrix}v_{sqo1} & 0\\ -v_{sdo1} & 0\end{bmatrix}}_{T11}\begin{bmatrix}\tilde{\theta}_1\\ \tilde{x}_{pll1}\end{bmatrix}$$

$$\begin{bmatrix}\tilde{v}^c_{td1}\\ \tilde{v}^c_{tq1}\end{bmatrix} = \begin{bmatrix}\tilde{v}_{td1}\\ \tilde{v}_{tq1}\end{bmatrix} + \underbrace{\begin{bmatrix}v_{tqo1} & 0\\ -v_{tdo1} & 0\end{bmatrix}}_{T21}\begin{bmatrix}\tilde{\theta}_1\\ \tilde{x}_{pll1}\end{bmatrix}$$

$$\begin{bmatrix} \tilde{i}^c_{d1} \\ \tilde{i}^c_{q1} \end{bmatrix} = \begin{bmatrix} \tilde{i}_{d1} \\ \tilde{i}_{q1} \end{bmatrix} + \underbrace{\begin{bmatrix} i_{qo1} & 0 \\ -i_{do1} & 0 \end{bmatrix}}_{T31} \begin{bmatrix} \tilde{\theta}_1 \\ \tilde{x}_{pll1} \end{bmatrix}$$

#### 4) VSC CURRENT CONTROLLER DYNAMICS

$$\begin{bmatrix} \tilde{v}^c_{td1} \\ \tilde{v}^c_{tq1} \end{bmatrix} = \underbrace{\begin{bmatrix} -k_{p2} & -w_o L_{f1} \\ w_o L_{f1} & -k_{p2} \end{bmatrix}}_{A61} \begin{bmatrix} \tilde{i}^c_{d1} \\ \tilde{i}^c_{q1} \end{bmatrix} + \underbrace{\begin{bmatrix} k_{i2} & 0 \\ 0 & k_{i2} \end{bmatrix}}_{B61} \begin{bmatrix} \tilde{x}_1 \\ \tilde{x}_2 \end{bmatrix} + \underbrace{\begin{bmatrix} k_{p2} & 0 \\ 0 & k_{p2} \end{bmatrix}}_{C61} \begin{bmatrix} \tilde{i}^*_{d1} \\ \tilde{i}^*_{q1} \end{bmatrix} + \underbrace{\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}}_{D61} \begin{bmatrix} \tilde{v}^c_{sd1} \\ \tilde{v}^c_{sq1} \end{bmatrix}$$

$$\frac{d}{dt}\begin{bmatrix} \tilde{x}_1 \\ \tilde{x}_2 \end{bmatrix} = -\begin{bmatrix} \tilde{i}^c_{d1} \\ \tilde{i}^c_{q1} \end{bmatrix} + \begin{bmatrix} \tilde{i}^*_{d1} \\ \tilde{i}^*_{q1} \end{bmatrix}$$

#### 5) OUTER CONTROL LOOP DYNAMICS

$$\begin{bmatrix} \tilde{i}^*_{d1} \\ \tilde{i}^*_{q1} \end{bmatrix} = \underbrace{\begin{bmatrix} -1.5k_{p3}v_{sd1o} & -1.5k_{p3}v_{sq1o} \\ 0 & 0 \end{bmatrix}}_{A71} \begin{bmatrix} \tilde{i}^c_{d1} \\ \tilde{i}^c_{q1} \end{bmatrix} + \underbrace{\begin{bmatrix} -1.5k_{p3}i_{d1o} & -1.5k_{p3}i_{q1o} \\ \dfrac{k_{p4}}{1.5v_{sd1o}} & 0 \end{bmatrix}}_{B71} \begin{bmatrix} \tilde{v}^c_{sd1} \\ \tilde{v}^c_{sq1} \end{bmatrix} + \underbrace{\begin{bmatrix} k_{i3} & 0 \\ 0 & \dfrac{-k_{i4}}{1.5v_{sd1o}} \end{bmatrix}}_{C71} \begin{bmatrix} \tilde{x}_3 \\ \tilde{x}_4 \end{bmatrix} + \underbrace{\begin{bmatrix} k_{p3} & 0 \\ 0 & \dfrac{-k_{p4}}{1.5v_{sd1o}} \end{bmatrix}}_{D71} \begin{bmatrix} \tilde{P}^*_1 \\ \tilde{v}^*_{sd1} \end{bmatrix}$$

$$\frac{d}{dt}\begin{bmatrix} \tilde{x}_3 \\ \tilde{x}_4 \end{bmatrix} = \underbrace{\begin{bmatrix} -1.5v_{sd1o} & -1.5v_{sq1o} \\ 0 & 0 \end{bmatrix}}_{A81} \begin{bmatrix} \tilde{i}^c_{d1} \\ \tilde{i}^c_{q1} \end{bmatrix} + \underbrace{\begin{bmatrix} -1.5i_{d1o} & -1.5i_{q1o} \\ -1 & 0 \end{bmatrix}}_{B81} \begin{bmatrix} \tilde{v}^c_{sd1} \\ \tilde{v}^c_{sq1} \end{bmatrix} + \underbrace{\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}}_{C81} \begin{bmatrix} \tilde{P}^*_1 \\ \tilde{v}^*_{sd1} \end{bmatrix}$$

#### 6) DC-LINK VOLTAGE DYNAMICS OF VSC1

$$\frac{d}{dt}\left[\tilde{v}_{dc1}\right] = \underbrace{\begin{bmatrix} \dfrac{-1.5v_{td1o}}{C_{dc}v_{dc1o}} & \dfrac{-1.5v_{tq1o}}{C_{dc}v_{dc1o}} \end{bmatrix}}_{A91} \begin{bmatrix} \tilde{i}_{d1} \\ \tilde{i}_{q1} \end{bmatrix} + \underbrace{\begin{bmatrix} \dfrac{-i_{12o}-i_{14o}}{C_{dc}v_{dc1o}} \end{bmatrix}}_{B91} \left[\tilde{v}_{dc1}\right] + \underbrace{\begin{bmatrix} \dfrac{-1.5i_{d1o}}{C_{dc}v_{dc1o}} & \dfrac{-1.5i_{q1o}}{C_{dc}v_{dc1o}} \end{bmatrix}}_{C91} \begin{bmatrix} \tilde{v}_{td1} \\ \tilde{v}_{tq1} \end{bmatrix} + \underbrace{\begin{bmatrix} \dfrac{-1}{C_{dc}} & \dfrac{-1}{C_{dc}} & 0 & 0 & 0 \end{bmatrix}}_{D91} \begin{bmatrix} \tilde{i}_{12} \\ \tilde{i}_{14} \\ \tilde{i}_{23} \\ \tilde{i}_{24} \\ \tilde{i}_{34} \end{bmatrix}$$

Defining the following zero matrices:

$$Z_1 = 0_{2\times 2}, \quad Z_2 = 0_{2\times 1}, \; Z_3 = 0_{1\times 2}, \; Z_4 = 0_{2\times 37}$$

$$A_{VSC1} = \begin{bmatrix} a_{11} & Z_1 & a_{13} & B_{11}B_{61} & B_{11}C_{61}C_{71} & a_{16} & Z_2 & Z_4 & Z_5 & Z_6 \\ Z_1 & A_{21} & B_{21}+D_{21}B_{51} & Z_1 & Z_1 & D_{21}A_{51}+D_{21}B_{51}T_{11} & Z_2 & Z_4 & Z_5 & Z_6 \\ B_{31} & C_{31} & A_{31}+D_{31}B_{51} & Z_1 & Z_1 & D_{31}A_{51}+D_{31}B_{51}T_{11} & Z_2 & Z_4 & Z_5 & Z_6 \\ Z_1 & Z_1 & B_{41} & Z_1 & Z_1 & A_{41}+B_{41}T_{11} & Z_2 & Z_4 & Z_5 & Z_6 \\ A_{71}-I & Z_1 & B_{71} & Z_1 & C_{71} & a_{46} & Z_2 & Z_4 & Z_5 & Z_6 \\ A_{81} & Z_1 & B_{81} & Z_1 & Z_1 & A_{81}T_{31}+B_{81}T_{11} & Z_2 & Z_4 & Z_5 & Z_6 \\ a_{71} & Z_3 & C_{91}C_{61}B_{71}+C_{91}B_{61} & C_{91}B_{61} & C_{91}C_{61}C_{71} & C_{91}T_1 & B_{91} & Z_7 & D_{91} & Z_8 \end{bmatrix}$$

$$B_{VSC1} = \begin{bmatrix} B_{11}C_{61}D_{71} & Z_1 & Z_1 & D_{71} & C_{81} & Z_1 & C_{91}C_{61}D_{71} \\ Z_1 & R/C_{21} & Z_1 & Z_1 & Z_1 & Z_1 & Z_3 \\ Z_9 & Z_9 & Z_9 & Z_9 & Z_9 & Z_9 & Z_{10} \end{bmatrix}^T$$

$$A_{MTDC} = \begin{bmatrix} Z_1 & A_{10} & Z_1 & B_{10} & Z_1 & C_{10} & Z_1 & D_{10} & E_{10} & F_{10}+G_{10}A_{10} & G_{10}B_{20}A_{40} \\ Z_1 & Z_2 & Z_1 & Z_2 & Z_1 & Z_2 & Z_1 & Z_2 & A_{30} & B_{30}+C_{30}A_{20} & C_{30}B_{20}A_{40} \\ Z_1 & Z_2 & Z_1 & Z_2 & Z_1 & Z_2 & Z_1 & Z_2 & A_{50} & Z_3 & B_{50} \end{bmatrix}$$

$$B_{MTDC} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{13} & C_{50} \end{bmatrix}$$

$$Z_5 = 0_{2\times5}, \quad Z_6 = 0_{2\times4}, \; Z_7 = 0_{1\times37}, \; Z_8 = 0_{1\times4}$$
$$Z_9 = 0_{2\times13}, \quad Z_{10} = 0_{1\times13}$$

Substituting the value of $\tilde{v}^c_{td1}$, $\tilde{v}^c_{tq1}$ and $\tilde{w}_1$ in the grid-side dynamics model and writing down the system dynamics in the grid reference frame, the characteristic matrix $A_{VSC1}$ is obtained and presented at the bottom of the previous page. Similarly, the characteristic matrices for VSC2, VSC3, and VSC4 can obtained using the same procedure.

### B. SMALL-SIGNAL MODEL OF MTDC GRID

The linearized dynamics of the MTDC Grid (equipped with PFC) currents can be described as

$$\frac{d}{dt}\begin{bmatrix}\tilde{i}_{12}\\ \tilde{i}_{14}\\ \tilde{i}_{23}\\ \tilde{i}_{24}\\ \tilde{i}_{34}\end{bmatrix} = \underbrace{\begin{bmatrix}\frac{1}{L_{12}}\\ \frac{1}{L_{14}}\\ 0\\ 0\\ 0\end{bmatrix}}_{A10}\tilde{v}_{dc1} + \underbrace{\begin{bmatrix}\frac{-1}{L_{12}}\\ 0\\ \frac{1}{L_{23}}\\ \frac{1}{L_{24}}\\ 0\end{bmatrix}}_{B10}\tilde{v}_{dc2} + \underbrace{\begin{bmatrix}0\\ 0\\ \frac{-1}{L_{23}}\\ 0\\ \frac{1}{L_{34}}\end{bmatrix}}_{C10}\tilde{v}_{dc3} + \underbrace{\begin{bmatrix}0\\ \frac{-1}{L_{14}}\\ 0\\ \frac{-1}{L_{24}}\\ \frac{-1}{L_{34}}\end{bmatrix}}_{D10}\tilde{v}_{dc4} + \underbrace{\begin{bmatrix}\frac{-R_{12}}{L_{12}} & 0 & 0 & 0 & 0\\ 0 & \frac{-R_{14}}{L_{14}} & 0 & 0 & 0\\ 0 & 0 & \frac{-R_{23}}{L_{23}} & 0 & 0\\ 0 & 0 & 0 & \frac{-R_{24}}{L_{24}} & 0\\ 0 & 0 & 0 & 0 & \frac{-R_{34}}{L_{34}}\end{bmatrix}}_{E10}\times\begin{bmatrix}\tilde{i}_{12}\\ \tilde{i}_{14}\\ \tilde{i}_{23}\\ \tilde{i}_{24}\\ \tilde{i}_{34}\end{bmatrix} + \underbrace{\begin{bmatrix}\frac{D_o-1}{L_{12}}\\ \frac{D_o}{L_{14}}\\ 0\\ 0\\ 0\end{bmatrix}}_{F10}\tilde{v}_{pfc} + \underbrace{\begin{bmatrix}\frac{V_{pfco}}{L_{12}}\\ \frac{V_{pfco}}{L_{14}}\\ 0\\ 0\\ 0\end{bmatrix}}_{G10}\tilde{D}$$

#### 1) PFC VOLTAGE CONTROLLER

$$\tilde{D} = \underbrace{\begin{bmatrix}-k^{pfc}_{p,V} & k^{pfc}_{i,V}\end{bmatrix}}_{A20}\begin{bmatrix}\tilde{v}_{pfc}\\ \tilde{x}_{13}\end{bmatrix} + \underbrace{[k^{pfc}_{p,V}]}_{B20}\tilde{v}_{pfc}$$

The PFC voltage and voltage controller states can be written as

$$\frac{d}{dt}\begin{bmatrix}\tilde{v}_{pfc}\\ \tilde{x}_{13}\end{bmatrix} = \underbrace{\begin{bmatrix}\frac{1-D_o}{C_{pfc}} & \frac{-D_o}{C_{pfc}} & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0\end{bmatrix}}_{A30}\begin{bmatrix}\tilde{i}_{12}\\ \tilde{i}_{14}\\ \tilde{i}_{23}\\ \tilde{i}_{24}\\ \tilde{i}_{34}\end{bmatrix} + \underbrace{\begin{bmatrix}0 & 0\\ -1 & 0\end{bmatrix}}_{B30}\begin{bmatrix}\tilde{v}_{pfc}\\ \tilde{x}_{13}\end{bmatrix} + \underbrace{\begin{bmatrix}\frac{-I_{12o}-I_{14o}}{C_{pfc}}\\ 0\end{bmatrix}}_{C30}\tilde{D} + \underbrace{\begin{bmatrix}0\\ 1\end{bmatrix}}_{D30}\tilde{v}^*_{pfc}$$

#### 2) PFC CURRENT CONTROLLER

$$\tilde{v}^*_{pfc} = \underbrace{[k_{i10} \quad k_{p10} - \delta k_{i10}]}_{A40}\begin{bmatrix}\tilde{x}_{14}\\ \tilde{x}_{15}\end{bmatrix}$$

$$\frac{d}{dt}\begin{bmatrix}\tilde{x}_{14}\\ \tilde{x}_{15}\end{bmatrix} = \underbrace{\begin{bmatrix}-1 & 0 & 0 & 0 & 0\\ \frac{-1}{\delta} & 0 & 0 & 0 & 0\end{bmatrix}}_{A50}\begin{bmatrix}\tilde{i}_{12}\\ \tilde{i}_{14}\\ \tilde{i}_{23}\\ \tilde{i}_{24}\\ \tilde{i}_{34}\end{bmatrix} + \underbrace{\begin{bmatrix}0 & 0\\ 0 & \frac{-1}{\delta}\end{bmatrix}}_{B50}\begin{bmatrix}\tilde{x}_{14}\\ \tilde{x}_{15}\end{bmatrix} + \underbrace{\begin{bmatrix}1\\ \frac{1}{\delta}\end{bmatrix}}_{C50}\tilde{i}^*_{12} + \underbrace{\begin{bmatrix}\frac{-1}{C_{dc}} & \frac{-1}{C_{dc}} & 0 & 0 & 0\end{bmatrix}}_{D91}\times\begin{bmatrix}\tilde{i}_{12}\\ \tilde{i}_{14}\\ \tilde{i}_{23}\\ \tilde{i}_{24}\\ \tilde{i}_{34}\end{bmatrix}$$

**TABLE 3.** Parameters of the five-terminal DC Grid and PFC [33], [35].

| DC grid parameters | Value | Units |
|---|---|---|
| Line length $L12$, $L14$, $L23$, $L24$, $L34$ | 100, 175, 150, 100, 120 | km |
| Line resistance $R$ | 0.0114 | Ω/km |
| Line inductance $L$ | 0.9356 | mH/km |
| Line capacitance $C$ | 0.0123 | μF/km |
| DC link capacitance | 150 | μF |
| Reference voltage $V_{dc}$ | 400 | kV |
| PFC nominal voltage | 2 | kV |
| PFC capacitance $C_{pfc}$ | 10 | mF |
| PFC nominal voltage | 4 | kV |
| PFC switching frequency | 2 | kHz |

**TABLE 4.** Parameters of the VSC stations [36].

| AC side parameters | Value | Units |
|---|---|---|
| Rated power $P_1$, $P_2$, $P_3$, $P_4$ | 400, 350, 200, 350 | MW |
| Filter resistance $R_f$ | 1.09 | Ω |
| Filter inductance $L_f$ | 57.6 | mH |
| Filter capacitance $C_f$ | 4.15 | μF |
| Grid resistance $R_g$ | 1.08 | Ω |
| Grid inductance $L_g$ | 28.67 | mH |
| Grid voltage $V_{g,L-L}$ | 195 | kV |

**TABLE 5.** Control system parameters.

| Subsystem | Parameter | Value |
|---|---|---|
| VSC controllers | $G_c(s)$ | $\frac{23.04s + 436}{s}$ |
| | $G_P(s)$ | $\frac{1.4321e^{-6}s + 1.0624e^{-4}}{s}$ |
| | $G_{ac}(s)$ | $\frac{441849.32s}{s}$ |
| | $G_{pll}(s)$ | $\frac{0.057545s + 4.189}{s}$ |
| | $k_d$ | $12e^3$ |
| PFC controllers | $G_{c,pfc}(s)$ | $\left(\frac{7.23s + 80.13}{s}\right)\left(\frac{1}{0.02s + 1}\right)$ |
| | $G_{c,pfc}(s)$ | $\frac{0.00714s + 0.0905}{s}$ |

Defining the following zero matrices

$$Z_{11} = 0_{7\times16}, \quad Z_{12} = 0_{7\times1}, \; Z_{13} = 0_{2\times16}$$

Substituting the value of $\tilde{v}^*_{pfc}$ and $\tilde{D}$, the characteristic and control matrices off the MTDC grid equipped with PFC, $A_{MTDC}$ and $B_{MTDC}$, can be obtained as presented at the bottom of the previous page 11.

Then, the overall MTDC grid characteristic and control matrices can be written as

$$A = \begin{bmatrix} A_{VSC1} & A_{VSC2} & A_{VSC3} & A_{MTDC} \end{bmatrix}^T$$
$$B = \begin{bmatrix} B_{VSC1} & B_{VSC2} & B_{VSC3} & B_{MTDC} \end{bmatrix}^T$$

**TABLE 6.** Proposed compensators parameters.

| Compensator | Cut-off frequency (rad/s) | Gain |
|---|---|---|
| HPF-based outer loop | $\omega_c = 325$ | 15 |
| DHPF-based outer loop | $\omega_1 = 170, \omega_2 = 130$ | 12.5 |
| Inner loop | $\omega_c = 120$ | 16.5 |

### C. MTDC GRID AND CONTROL SYSTEM PARAMETERS

See Tables 3–6.

## REFERENCES

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