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A Wideband Multilevel Reconfigurable Class E/F_{23} Power Amplifier With a Band-Selecting Tracking Reactance Compensation Automatic Calibration Algorithm

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ABSTRACT This paper presents a wide-band multi-level switched mode class-E/F_{23} Power Amplifier (PA) with a reconfigurable power stage core transistor and a load with reconfigurable reactance compensation part. An Automatic Calibration Scheme (ACS) is proposed to perform the core and load reconfiguration based on a proposed algorithm. The PA is formed by a class-D driver amplifier, the switched mode cascaded reconfigurable power stage, the reconfigurable class-E/F23 load, the ACS and its algorithm, and the matching network at the end of the load before the antenna. The proposed PA is implemented using a 130 nm CMOS technology. The wideband PA operates in the frequency range from 470 MHz to 690 MHz for a TV White Space (TVWS) application with 220 MHz bandwidth. Even though reaching a high maximum Power Added Efficiency (PAEmax) for the design with low output powers is challenging a PAEmax of 32% for a 10 dBm output power level from a low supply voltage of 2.2 V. The proposed ACS provides an output power with a flatness around 0.6 dB which shows 57% improvement in compare with the structure without the ACS. The PA achieved a selectable multi-level output power from 10 dBm to 14 dBm over the 220 MHz bandwidth.

INDEX TERMS Class-E/F_{23}, CMOS power amplifier, TV white space (TVWS), wideband, switching amplifier, wireless communications, radio-frequency (RF) circuits.

I. INTRODUCTION

In the application of digital TVs, the spectrum of TV White Space (TVWS) that is from 470 MHz to 790 MHz, is significantly used. These spectrums can be utilized for new wireless applications, allowing for more spectrum exploitation [1]. Also, a significant portion of power consumption in modern communication systems is consumed in power amplifiers which is the critical concern for mobile applications. In order to achieve broadband performance, optimization of the fundamental and harmonic frequency impedances is essential. In switching amplifiers, the nonlinear shunt capacitance of the power transistor can affect the output impedance of it [2], [3]. Besides, it remains a challenge in broadband PA design to provide a desired output impedance in a wide frequency range.

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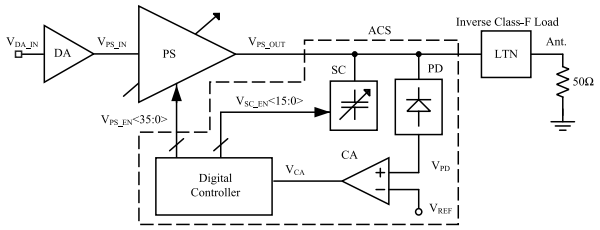

FIGURE 1. Simplified block diagram of PA with ACS.

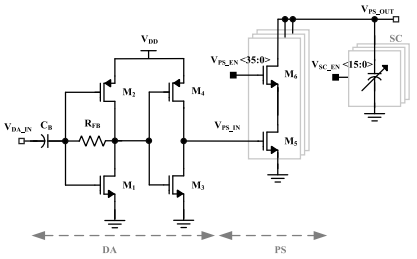

FIGURE 2. The proposed core for the reconfigurable PA.

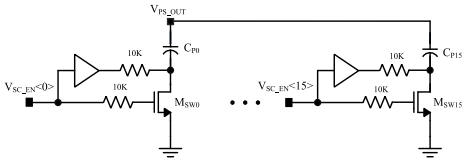

FIGURE 3. Schematic of the load switch-capacitor.

Various methods are developed, including transformer-based tuning, a varactor based tunable matching network [4]–[6], and using parallel input/output matching network [7]. However, these techniques use a large chip area and do not guarantee a constant power over a wide frequency range. Furthermore, high peak current and voltages in power amplifiers have a serious effect on the functionality of the circuits [7], [8]. High peak voltage have a damaging effect on the reliability of the circuit. To reduce the peak voltage factor and increasing the safe operating boundaries, stacked transistors [9] and inverse class-F load network [10], [11] are used.

In this paper an Automatic Calibration Scheme (ACS) is proposed and implemented to form an automatic calibration unit and providing a relatively less variation for the output power over the 220 MHz band. In addition to optimize the peak efficiency a class E/F_{23} is proposed that: 1) Causes the harmonic optimization to minimize I/V overlap and reducing the conduction loss for the peak operation and 2) facilitating squre switching waveform which results in a lower loss of high-frequency clock routing. The contribution of the proposed PA is its operation by the reconfigurable PA switching-core and the proposed reactance tracking load transfer network (LTN) through the ACS by the switch capacitor C_P, to provide the optimum operation for every selected band through the digital controller for the algorithm.

II. PROPOSED POWER AMPLIFIER

Fig. 1 shows the top block-diagram of the proposed PA which is formed by a class-D driver stage, a reconfigurable switching power amplifier core as the power stage which is controlled through the digital controller, a feedback path through the Peak Detector (PD) which tracks the amplitude of the output signal, an error amplifier to compare the output of the PD with a reference voltage (V_{REF}) that is also adjustable digitally, the digital controller which operates based on a proposed calibration algorithm which reconfigures both the power stage cores and the shunt switch capacitor part, and the LTN that is implemented to tune the fundamental and the harmonics. The calibration acts as an optimum power finder when the frequency of the channel changes or the uncertainty that happens due to process, voltage and temperature (PVT) variations. An ideal Class-E amplifier requires the load impedance Z_L at the fundamental frequency and an open circuit at harmonic frequencies which requires a large value load resistance for a low-power PA [12], [13].

Fig. 2 shows the proposed schematic for the driver stage and the reconfigurable power stage with the reconfigurable load capacitances. The driver stage is formed by a self-biased class-D inverter amplifier driving the power stage with a low power consumption and low loading effect on the stage before the PA.

The reconfigurable power stage core, is a switching power amplifier with a reconfigurable cascode transistor that is formed by 36 cores, controlled by the digital controller automatically based on the ACS's algorithm. Eventually, the reconfigurable load capacitance is placed at the shared drains of the cascode transistors of M6. The switch capacitor, shown in Fig. 3, is controlled by 16 control bit and with a fixed unit capacitor value.

III. AUTOMATIC CALIBRATION SCHEME

One of the issues of a wide-band operation is the large power variations that degrades the power flatness and introduces an inconsistent operation over the band. In this paper an ACS is proposed to sustain a flat output power over the band.

For implementing ACS, the algorithm is developed based on the relationship between output power (Pout) and peak amplitude of drain voltage. The ACS consists of a Peak Detector, comparator amplifier, and the proposed ACS algorithm which is implemented in digital controller. By selecting any particular frequency channel, PA Core, S_C, and V_{PD} parameters are initialized with their default values. Fig. 4, shows the proposed ACS control algorithm. V_{PD}, PA Core and SC are the parameters that are tuned by the control based on the ACS algorithm. The ACS, after an exhaustive iteration of parameters of the algorithm in three loops and finding optimized core and capacitor values, configures PA parameter values based on the maximum number of optimum events in each scenario. Therefore, the controller based on the

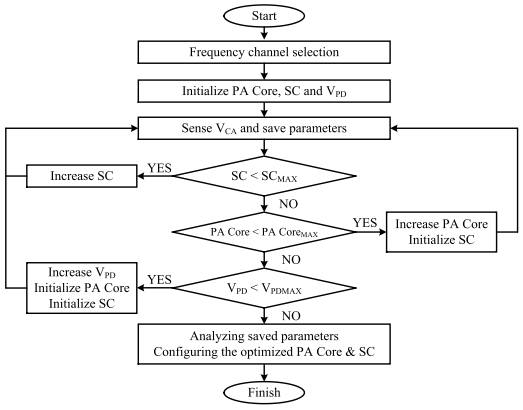

FIGURE 4. The proposed algorithm for the ACS.

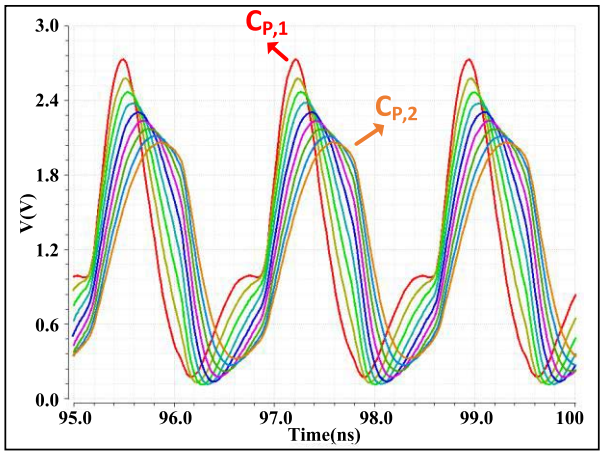

FIGURE 5. Voltage waveforms for tuning of peaking capacitor CP (CP,2 > CP,1).

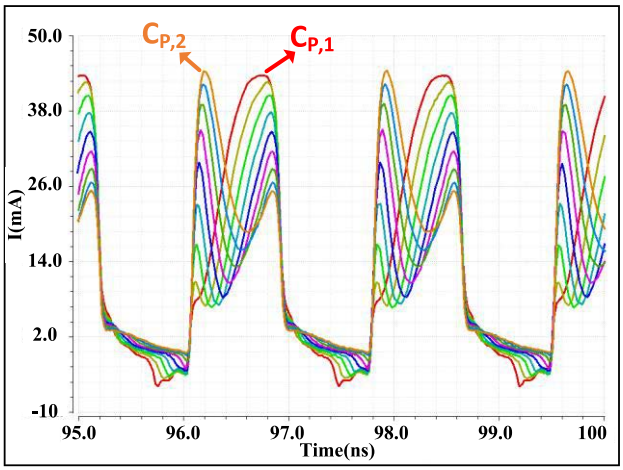

FIGURE 6. Current waveforms for tuning of peaking capacitor CP (CP,2 > CP,1).

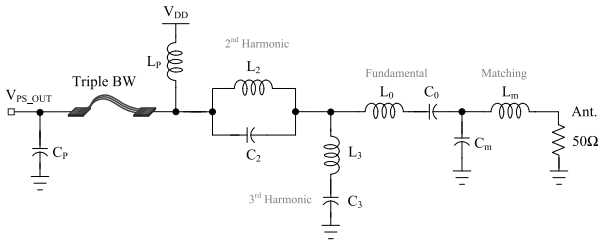

FIGURE 7. The proposed load transfer network for the PA.

proposed algorithm, performs the optimum power stage core reconfiguration and tracking the best reactance compensation for the load through the parallel capacitor.

Based on the proposed algorithm in Fig. 4, the operation starts by selecting the frequency channel. Therefore, in the rest of the power tunning process, the selected center frequency will be the target to provide the maximum power and efficiency. Then, the algorithm starts with an initial predefined core, SC C_P. Rest of the operation is performed by sensing the output power and changing the parameters. Fig. 5 and Fig. 6 show the current and voltage waveform samples when various values of C_P that by inverse Class-F tuning, the peak voltage and the RMS current of the PA reduces. It also improves the tolerance to drain capacitance that allows use of larger devices for reducing on-resistance. This tunning is performed based on the algorithm and the implemented feedback path from the output.

IV. LOAD TRANSFER NETWORK WITH CLASS-E/F23 IMPEDANCE TUNING

The proposed class-E/F_{23} load with the matching network is shown in Fig. 7. It is shown that a reactance compensation is formed by the load inductor, L_P, and the parallel capacitor, C_P as the shunt resonant circuit with L_2C_2 and L_0C_0 as the series resonant circuits. Based on the reactance compensation theory [14], the reactance of the resonant circuits changes when frequency changes, this change is with a positive slope at the resonant frequency (ω_0) for the series circuits and negative for the shunt circuits.

Therefore, by choosing the circuit elements, a constant load angle over a very wide frequency bandwidth, can be provided. Additionally, the capacitance value of the shunt resonant circuit, C_P, is reconfigurable by the ACS. This provides a uniq aspect to provide a wider bandwidth with an acceptable power flatness. The proposed transformer load with the parallel inductor and capacitor and fundamental and harmonic filters, an L type matching network, and bonding wire, gives a high inductive impedance and short circuit at second harmonic and third harmonic, respectively. C_P comprises of transistor intrinsic capacitance and S_C.

By controlling the parallel capacitor value, an inductive impedance at the fundamental and second harmonic with a short third harmonic is provided, satisfying Class-E/F_{23} operation [10], [15] for the desired frequency range. Therefore, the proposed load transfer network in combination with the reconfigurable power cores and the load capacitances optimizes an optimum operation to achieve a high efficiency while the output power and the power supply voltage are

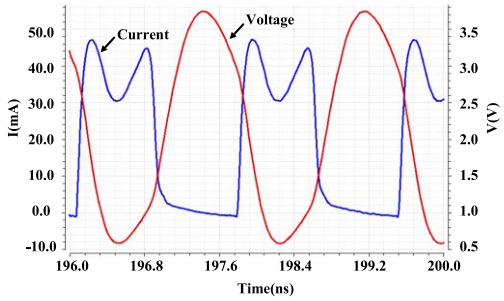

FIGURE 8. Voltage and current waveforms of PA.

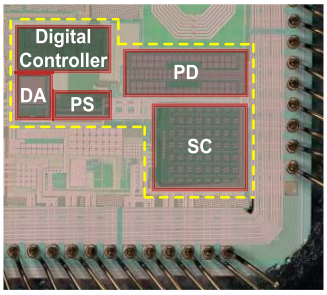

FIGURE 9. The chip-micrograph of the PA.

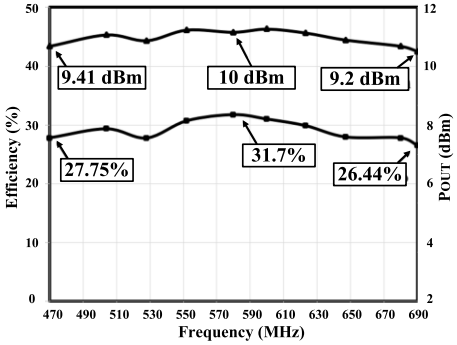

FIGURE 10. Output Power and PAE over the bandwidth.

limited that are restricting parameters in terms of achieving a higher efficiency.

By considering the power stage as an ideal switch and when switch is on for the first half-cycle, the voltage and current of C_P are as follow:

$$v(\omega t) = V_{DD} - v_{L_P}(\omega t) = 0$$
$$i_C(\omega t) = \omega C(dv(\omega t)/d(\omega t)V_{DD} - v_{L_P}(\omega t) = 0$$

therefore:

$$\begin{aligned} i(\omega t) &= i_{L_P}(\omega t) + i_{L_2}(\omega t) + i_{C_2}(\omega t) \\ &= \frac{V_{DD}}{\omega L_P}\omega t + \frac{V_{DD} - v_{L_P}(\omega t) - v_{L_3}(\omega t) - V_{C3}}{\omega L_2}\omega t \\ &\quad + C_2\frac{d(V_{DD} - v_{L_P}(\omega t) - v_{L_3}(\omega t) - V_{C3})}{dt} \end{aligned} \quad (1)$$

During the second half-cycle when the switch is off and $i(\omega t)$ is zero, for C_P capacitance current:

$$\begin{aligned} & i_{C_P}(\omega t) \\ &= i_{L_P}(\omega t) + i_{L_2}(\omega t) + i_{C_2}(\omega t) \\ & \omega C\frac{dv(\omega t)}{d(\omega t)} \\ &= \frac{1}{\omega L_P}\int_{\pi}^{\omega t}[V_{DD} - v(\omega t)]\,d(\omega t) \\ &\quad + \frac{1}{\omega L_2}\int_{\pi}^{\omega t}\begin{bmatrix} V_{DD} - v(\omega t) - v_{L_P}(\omega t) - v_{L_3}(\omega t) \\ -V_{C3} \end{bmatrix} d(\omega t) \\ &\quad + C_2\frac{d(V_{DD} - v(\omega t) - v_{L_P}(\omega t) - v_{L_3}(\omega t) - V_{C3})}{dt} \end{aligned} \quad (2)$$

Therefore, when the switch is off the current of the power core is zero and voltages reaches to its maximum level and when the switch is on the current reaches to its peak while voltage is zero. Like the idealized analysis, the real voltage and current of the power core follow this behavior which results in a higher efficiency even though the target output power level is not much high. Fig. 8 shows the voltage and current waveforms of the power core. The current wave is known as a deeply bifurcated current pulses which results in a higher efficiency while the power level is limited.

Finally, the proposed LTN with a fundamental matching and harmonics compensations provides an optimum load impedance before the matching network and the 50Ω antenna. The matching network transfers the optimum load impedance to the 50Ω antenna impedance.

V. EXPERIMENTAL RESULTS

Fig. 9 shows the chip micrograph of the proposed PA that is fabricated in a 130 nm CMOS technology. The area occupation of the PA is kept compact in a 0.4 mm^2. Experiments at the output of the PA shows an output reflection coefficient less than -10 dB over the desired frequency range.

The first measurement scenario is to do not use the automatic calibration mechanism. Therefore, for a fixed power stage by using a 2.2 V supply voltage, a 10 dBm output power is achieved as it is shown in Fig. 10. Also, the power variation over the bandwidth is less than 1 dB over the bandwidth. A maximum Power Added Efficiency (PAE_{max}) of 31.7% is achieved which is due to the switched mode operation of the power core as the performed analysis showed a class E voltage and current waveforms. Fig. 11, shows the spectrum of the PA at 472 MHz and 679 MHz, which illustrates the harmonics less than -30 dBm in terms of the linearity of the PA. By a 2.2 V supply voltage.

To perform a measurement using the proposed ACS, a target power must be defined through the digital controller which has implemented the algorithm. Therefore, by defining 12 dBm and 14 dBm target powers the measurement is performed as shown in Fig. 12. Consequently, the superiority of the proposed method is unveiled when by using the automatic calibration, the output power variations is reduced

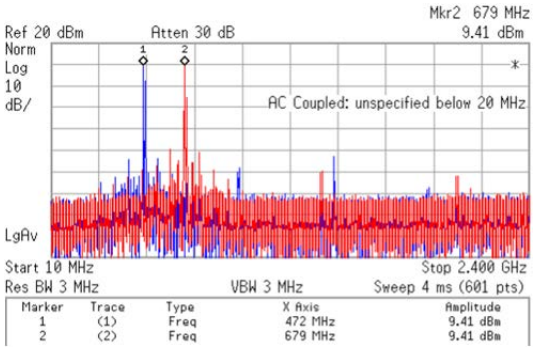

FIGURE 11. The output spectrum of the PA at 472 MHz and 679 MHz including the fundamentals and harmonics.

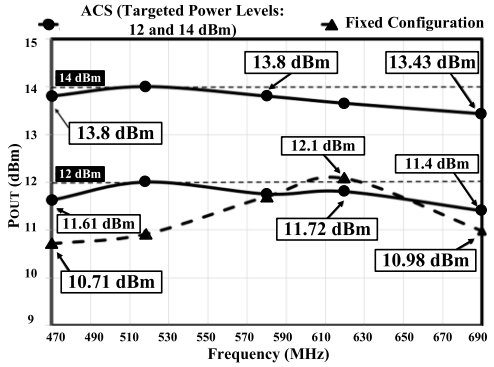

FIGURE 12. The measured output power for ACS output power targets.

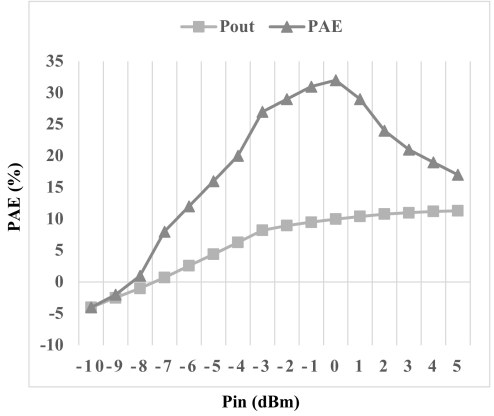

FIGURE 13. Output power and PAE versus input power when 10dBm is targeted by the ACS.

from 1.4 dB of the operation without ACS, to less than 0.6 dB by the ACS. In the ACS, by adjusting the cell size of the power stage and switch capacitor the power is kept close to the desired value. Fig. 13 illustrates the output power and PAE versus the input power for the targeted 10 dBm output power by the ACS.

Table 1 summarizes the performance of the proposed power amplifier and compares it with those of the reported works. For comparing the performance, the following figure-of-merit (FOM) is used [7]:

The comparison table reflects the superiority of the work in term of the compactness of the occupied area. Based on the mentioned merits in equations (3) and (4), the proposed

TABLE 1. Performance comparison table.

Parameters	[4]	[6]	[7]	This Work
Frequency (GHz)	0.7-1.2	2.4	1.8-2.74	0.47-0.69
CMOS Process	0.13 um	0.18 um	0.09 um	0.13 um
Class	F	F	E	E/F_{23}
Configuration	Fixed	Fixed	Fixed	ACS
Power (dBm)	24.6	19.2	28.7	10
Peak PAE (%)	48.3	26	48	31.7
Area (mm^2)	2.25	2.56	1.2	0.4
FOM_1	34.91	22.48	87.6	122
FOM_2	18.37	NA	36.26	46.6

design with its specs is reflecting a high performance. The proposed PA with a lower maximum power target and supplied by a lower supply voltage level has a lower PAE in compare with the similar works with a higher maximum target power. Despite of this comparison the achieved PAE for a 10 dB power target is provided by the proposed LTN and the switching core and is a high PAE by itself.

VI. CONCLUSION

A CMOS multi-level PA using drain impedance peaking was proposed for improving the efficiency and delivering a constant output power over wide frequency band for TVWS applications. The PA is implemented in a 130-nm CMOS technology process using an area of 0.4 mm^2. A peak PAE of 31.7% for the fixed configuration without ACS and a 10 dBm output with 1 dB variation with a supply voltage of 2.2 V, is measured. The operation of the PA by ACS provided a multi-level output power with a high flatness of the power-by-power core reconfiguration and tracking reactance compensation based on the proposed ACS algorithm. The proposed algorithm provides an automatic power level solution that adjust the loud reactance compensation and core of the power stage targeting a desired power level. Two experiments are done and the measurement results in both cases show that the output variations are improved from 1.4 dB of the operation without ACS to 0.6 dB when operation involves the ACS.

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REFERENCES

[1] R. A. Elliot, M. A. Enderwitz, K. Thompson, L. H. Crockett, S. Weiss, and R. W. Stewart, "Wideband TV white space transceiver design and implementation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 1, pp. 24–28, Jan. 2016, doi: 10.1109/TCSII.2015.2456272.

[2] H. Sekiya, N. Sagawa, and M. K. Kazimierczuk, "Analysis of class-DE amplifier with linear and nonlinear shunt capacitances at 25% duty ratio," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 9, pp. 2334–2342, Sep. 2010, doi: 10.1109/TCSI.2010.2043013.

[3] A. Sheikhi, M. Hayati, and A. Grebennikov, "A design methodology of class-E/F_3 power amplifier considering linear external and nonlinear drain–source capacitance," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 2, pp. 548–554, Feb. 2017, doi: 10.1109/TMTT.2016.2635658.

[4] K. K. Sessou and N. M. Neihart, "An integrated 700–1200-MHz class-F PA with tunable harmonic terminations in 0.13-μm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 4, pp. 1315–1323, Feb. 2015, doi: 10.1109/TMTT.2015.2403843.

[5] K. Ma, T. B. Kumar, and K. S. Yeo, "A reconfigurable K-/Ka-band power amplifier with high PAE in 0.18-μm SiGe BiCMOS for multi-band applications," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 4395–4405, Nov. 2015, doi: 10.1109/TMTT.2015.2495129.

[6] M. Gilasgar, A. Barlabe, and L. Pradell, "A 2.4 GHz CMOS class-F power amplifier with reconfigurable load-impedance matching," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 1, pp. 31–42, Jan. 2019, doi: 10.1109/TCSI.2018.2851608.

[7] M. D. Wei, D. Kalim, D. Erguvan, S. F. Chang, and R. Negra, "Investigation of wideband load transformation networks for class-e switching-mode power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, PART 2, pp. 1916–1927, Jun. 2012, doi: 10.1109/TMTT.2012.2191304.

[8] J. Liang and W.-H. Liao, "Steady-state simulation and optimization of Class-E power amplifiers with extended impedance method," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 6, pp. 1433–1445, Jun. 2011, doi: 10.1109/TCSI.2010.2097671.

[9] A. Mazzanti, L. Larcher, R. Brama, and F. Svelto, "Analysis of reliability and power efficiency in cascode class-E PAs," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1222–1229, May 2006, doi: 10.1109/JSSC.2006.872734.

[10] S. D. Kee, I. Aoki, A. Hajimiri, and D. Rutledge, "The class-E/F family of ZVS switching amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 6, pp. 1677–1690, Jun. 2003, doi: 10.1109/TMTT.2003.812564.

[11] F. You, S. Member, S. He, X. Tang, and X. Deng, "High-efficiency single-ended class-E/F_2 power," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 1, pp. 32–40, Nov. 2010.

[12] N. O. Sokal and A. D. Sokal, "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. SSC-10, no. 3, pp. 168–176, Jun. 1975, doi: 10.1109/JSSC.1975.1050582.

[13] F. Raab, "Idealized operation of the class E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. CS-24, no. 12, pp. 725–735, Dec. 1977, doi: 10.1109/TCS.1977.1084296.

[14] N. Kumar, C. Prakash, A. Grebennikov, and A. Mediano, "High-efficiency broadband parallel-circuit class E RF power amplifier with reactance-compensation technique," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 3, pp. 604–612, Mar. 2008, doi: 10.1109/TMTT.2008.916906.

[15] M. Babaie, F.-W. Kuo, H.-N.-R. Chen, L.-C. Cho, C.-P. Jou, F.-L. Hsueh, M. Shahmohammadi, and R. B. Staszewski, "A fully integrated Bluetooth low-energy transmitter in 28 nm CMOS with 36% system efficiency at 3 dBm," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1547–1565, Jul. 2016, doi: 10.1109/JSSC.2016.2551738.

[16] A. S. Porret, T. Melly, D. Python, C. C. Enz, and E. A. Vittoz, "An ultralow-power UHF transceiver integrated in a standard digital CMOS process: Architecture and receiver," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 452–466, Mar. 2001, doi: 10.1109/4.910484.

[17] M. Silva-Pereira and J. Caldinhas Vaz, "A single-ended modified class-E PA with HD2 rejection for low-power RF applications," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 1, pp. 22–25, Jan. 2018, doi: 10.1109/LSSC.2018.2803450.

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