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Modular Expandable Multiinput Multioutput (MIMO) High Step-Up Transformerless DC–DC Converter

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ABSTRACT In this paper, a Multi-Input Multi-Output (MIMO) high step-up transformerless DC-DC converter is proposed. The proposed converter can expand the number of ports from both input and output terminals. Also, it has a modular structure using voltage multiplier cells (a switch, two diodes, a capacitor, and an inductor). The proposed converter is useful for a wide range of applications and has the merit of interfacing multiple hybrid voltage sources with each other to supply different loads with various voltage levels. All the output voltages of the output ports can be regulated at the same time by tuning separate controlling parameters. Since digital control has the benefit of (1) enhancing efficiency, (2) higher flexibility than analog electronics, (3) ease of use, (4) improving reliability and stability in hybrid energy conversion applications, this method of controlling implementation is adopted. The key contributions of this article would be 1) expandable modular MIMO converter with high performance for all range of duty cycles; 2) integration of hybrid energy sources and delivering to multiple loads; 3) nonlinear digital controlling approach to achieve fast transient response under the variation of input voltage sources and output loads, and 4) high voltage gain with low normalized power stress on switches. To simplify the analysis, first, single-input, dual-output (SIDO) mother-module, dual-input, three-output (DITO) and three-input, four-output (TIFO) developed modules are carefully analyzed and then, the MIMO structure is explained. To verify the theoretical results, a prototype of SIDO operation of the proposed converter with a digital controlling scheme is implemented for 30V input voltage /150V, 250V output voltages with the total power of 450W. Furthermore, experimental results of DITO operation with 30V and 40V input voltages/150V, 250V, 405V output voltages with the total power of 800W are extracted.

INDEX TERMS Single-input/dual-output dc-dc converter, dual-input/three-output dc-dc converter, multi-input/multi-output dc-dc converter, high step-up, expandable structure, voltage multiplier cells.

I. INTRODUCTION

MULTIPORT DC-DC converters (MPCs) are applicable in versatile applications including photovoltaic (PV) energy systems [1], [2], microgrids with multiple sources and integrated energy storage [3], battery systems [4], data centers [5], and electric traction [6]. Fig. 1(a) shows the general application of a DC-DC multiport converter. MPCs with the capability of increasing the voltage levels to the standard levels of different output loads are widely required [7]. Also, MPCs increase the reliability of using these sources by interfacing multiple sources together since the renewable energy sources are affected by the environmental changes [8]–[10].

Although several single-input single-output (SISO) DC-DC boost converters can be used to interface each of the sources to the loads as shown in Fig. 1(b), in that case, the number of components, power loss, selected duty cycles for the switches and costs will be considerably high. It is noteworthy that the voltage gains of the conventional SISO DC-DC boost converters are directly related to the duty cycle of their switches and by adopting extreme duty cycles when there is a voltage drop in the voltage source, the active switches would experience severe voltage spikes [11]. One DC-DC MIMO converter can be utilized instead of using

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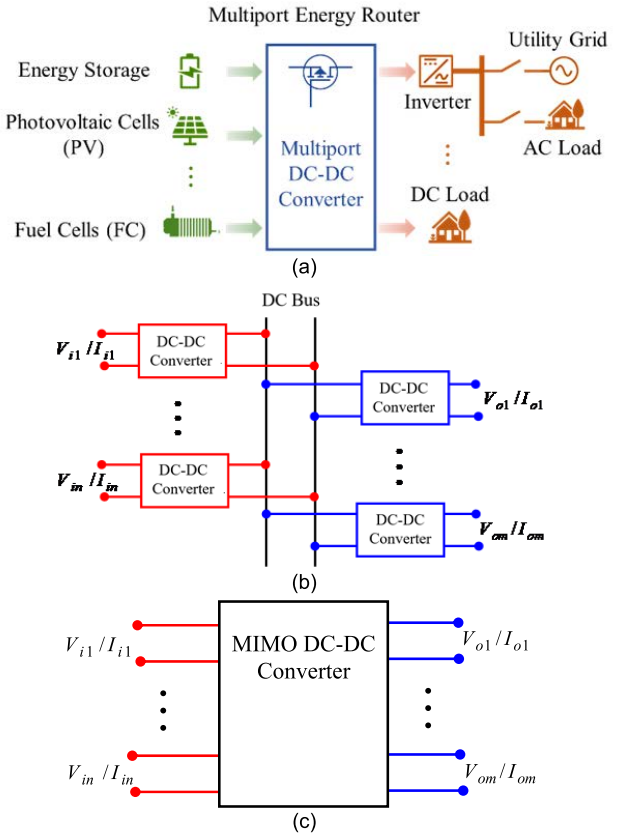

FIGURE 1. (a) General application of a DC-DC multiport converter; (b) Conventional schematic for integrating various input sources and output loads applying SISO DC-DC converters; (c) Proposed schematic for integrating various input sources and output loads applying MIMO DC-DC converter.

several SISO converters to integrate multiple sources and multiple output loads to optimize the performance of system as shown in Fig. 1(c). Consequently, by using MIMO converters, the components' number and power conversion stages can be decreased, also the power density can be increased.

Multiport DC-DC converters can be generally divided into two main groups transformer-based and transformerless boost MPCs. In [12]–[18], MPCs based on transformers and coupled inductors are presented. The conversion ratios of these converters are increased by adding the turn ratio of the secondary windings of their utilized transformers or coupled inductors. However, converters with transformers suffer from the high volume, high voltage spikes on elements, and as much as the operating powers of these converters increase, the size of their transformers increases. Also, converters with coupled inductors experience high input current ripples which affect the life span of the renewable energy sources and cause high leakage inductances and conduction losses.

To avoid the drawbacks of the coupled-inductor or transformer-based DC-DC boost MPCs, simpler structures are presented in [19]–[23]. The main drawback of these converters is that their conversion ratios are directly dependent on the duty cycles of their switches. By selecting high duty cycles, the switches may experience voltage spikes, especially in high power applications. To reduce the voltage spikes on switches in transformerless DC-DC boost MPCs, interleaved converters are presented such as in [24]. In these converters by shifting phases between the switches, the voltage stress on active switches can be reduced. However, these converters have the constraint of providing different conversion ratios for different ranges of duty cycles. To achieve high voltage gains in transformerless DC-DC boost MPCs, converters with voltage multiplier (VM) cells have been presented such as in [25] and [26]. However, in these converters there is no specific switch for each output port, as a result, there is not enough controlling criterion to control each of the output ports, separately. In [27], there has been a DC-DC MIMO converter utilizing a single inductor presented. This converter has low voltage gain. Also, in this converter, the voltage sources and output loads are non-common grounded. As a result, when one of the switches in one of the modules is failed, the power cannot be delivered to other modules.

In [28], to improve transient responses in dc-dc converters, the idea of proximate time-optimal digital control is applied as a hybrid digital adaptive (HDA) controller. By HDA controller, the currents of the inductor and capacitor are estimated by an adaptive adjustment and are sent to HAD. This method achieves optimal transient responses for a wide range of step changes of the load with fixed input voltage. Due to the development of microprocessor boards in recent years, the implementation of these controlling schemes has become easier. In [29], a digital control strategy has been employed on a bidirectional fly-back converter. The presented digital control scheme in [29] leads to high efficiency and fast charge/discharge speed [30]. Implemented digital control in [31] has been increased flexibility compared to analog feedback systems.

In this paper, a transformerless MPC is presented. The number of input and output terminals of the proposed converter can be increased which makes the converter suitable for a wide range of applications. The active and passive components of the proposed converter would not experience voltage stress caused by leakage inductances. Comparing the four-input developed module of the proposed converter with other conventional ones, the proposed converter has higher voltage gain for ports with the least power stress on switches. Moreover, the voltage gain of the converter is increased by the utilized VM cell for each output port, therefore, extreme duty cycles would not be applied to active switches to achieve higher powers or compensating the output voltages. There is a specific switch for each output port that can regulate the output voltage to the desired demanded level by the load. The voltage gain of each of the output ports is increased and controlled by its own cell and the ports can be operated independent from each other. Considering that the input voltage sources might be different from each other with different generated voltage and current ratings and if they are renewable energy sources such as photovoltaic cells (PVs), they might not be available all the time and they might experience a sudden drop in energy generation due to their dependency to

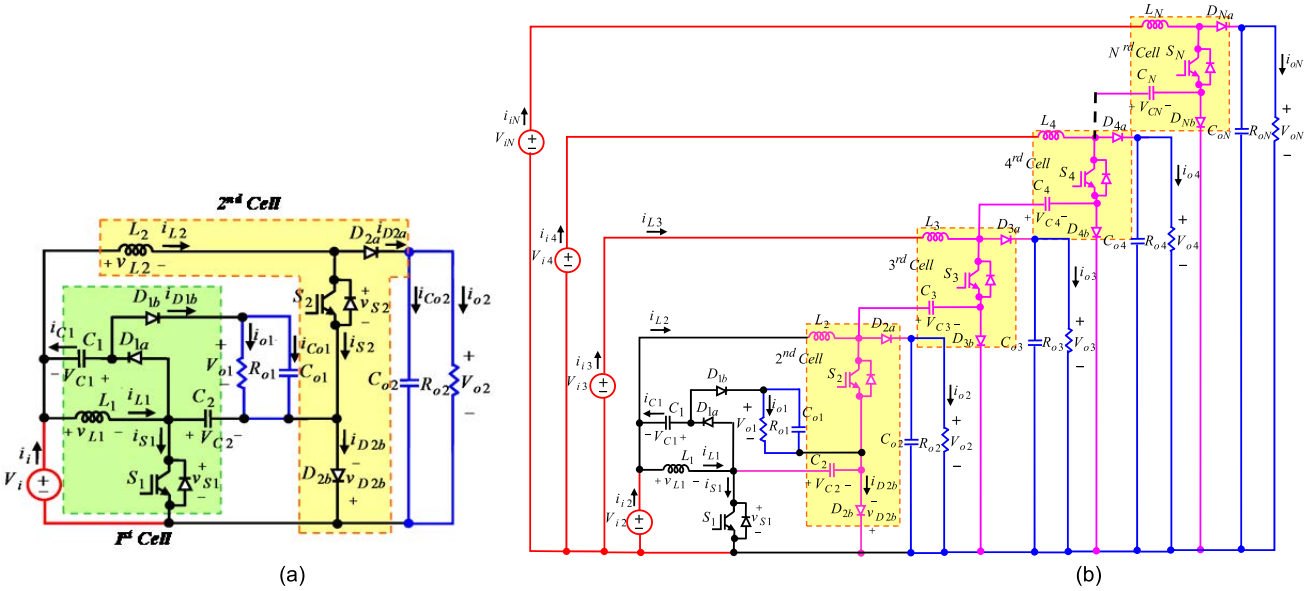

FIGURE 2. The proposed converter and its expanded structure; (a) SIDO converter; (b) MIMO converter.

the environmental conditions, a nonlinear-based control that can compensate for the transient drop or raise of power by these sources is adopted.

II. THE PROPOSED CONVERTER

The basic power circuit of the proposed single-input, two-output converter is shown in Fig. 2(a). The proposed converter has the components of the inductors L_1, L_2, capacitors C_1, C_2, diodes $D_{a1}, D_{b1}, D_{a2}, D_{b2}$. The capacitors are large enough to be considered the constant DC voltages across In the proposed converter, by using the duty cycles of D_1 and D_2, the first and second output voltages of V_{o1} and V_{o2}, respectively are regulated at the same time for any constant voltages under the input voltage or output loads variations. In this study, at first, the proposed SIDO mother-module is analyzed and then the results of the expanded form of the proposed converter to 2-input/3-output, 3-input/4-output, 4-input/5-output and also $(N-1)$-input/N-output are given. The power circuit of expanded multi-input, multi-output converter is illustrated in Fig. 2(b). As an example, in Fig. 3 the switching pattern of switches for $D_1 < D_2$ is shown.

Moreover, it includes two switches S_1 and S_2 with the operating duty cycles of D_1 and D_2, respectively.

A. ANALYSIS OF THE PROPOSED SINGLE-INPUT, DUAL-OUTPUT SIDO MOTHER-MODULE

The proposed converter can operate for two conditions of duty cycles as $D_1 < D_2$ and $D_1 > D_2$. As a result, it has different equations in these conditions which are explained in the following sections. The equivalent circuits of the proposed converter during a switching period for $D_1 < D_2$ and $D_1 > D_2$ are illustrated in Figs. 4 and 5, respectively.

1) ANALYSIS FOR $D_1 < D_2$

Considering Fig. 4, the proposed converter has three operating modes. Accordingly, the voltage across the inductor L_1 during a switching period would be:

$$v_{L1} = \begin{cases} V_i & during\ Mode\ 1\ (D_1 T_s) \\ V_i - V_{C2} & during\ Modes\ 2,3\ (1-D_1)\ T_s \end{cases} \quad (1)$$

As a result, in the steady state, the voltage balance law for the inductor L_1 can be written as follows:

$$\tilde{v}_{L1} = D_1 V_i + (1-D_1)(V_i - V_{C2}) = 0 \quad (2)$$

By simplifying the above equation, it is obtained as follows:

$$V_{C2} = [1/(1-D_1)]\, V_i \quad (3)$$

Considering Figs. 4(b) and 4(c), during modes 2 and 3, the switch S_1 is OFF and the diodes D_{1a} and D_{2b} are ON. As a result, it can be written as follows:

$$V_{C1} = V_{C2} - V_i = [D_1/(1-D_1)]\, V_i \quad (4)$$

Considering Fig. 4(a), during mode 1, the switch S_1 and diode D_{1a} are conducting. The conversion ratio of first output voltage over the input voltage for the first port $(G_1 = V_{o1}/V_i)$ is obtained as follows:

$$G_1 = V_{o1}/V_i = [(V_{C1} + V_{C2})/V_i + 1] = 2/(1-D_1) \quad (5)$$

Considering Fig. 4, the voltage across the inductor L_2 during a switching period is calculated as follows:

$$v_{L2} = \begin{cases} V_i + V_{C2} & during\ Mode\ 1\ (D_1 T_s) \\ V_i & during\ Mode\ 2\ [(D_2 - D_1) T_s] \\ V_i - V_{o2} & during\ Modes\ 3\ [(1-D_2)\ T_s] \end{cases} \quad (6)$$

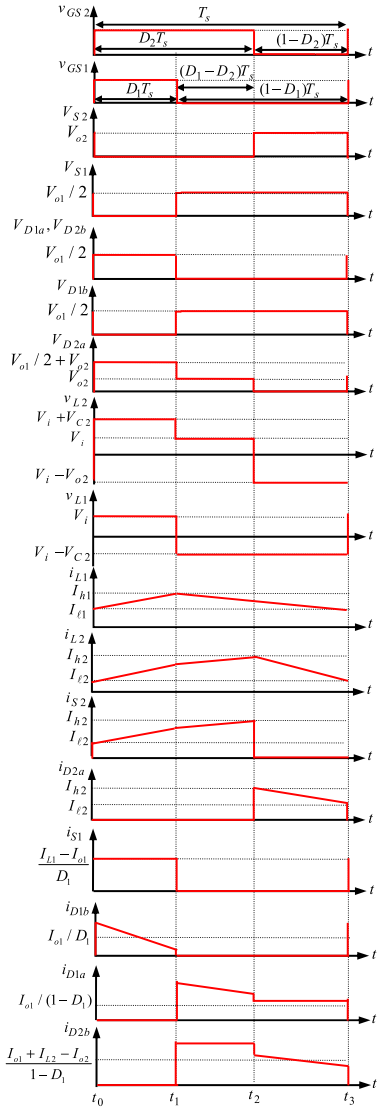

FIGURE 3. Theoretical waveforms of the proposed converter during a switching period for $D_2 > D_1$.

As a result, in the steady-state, it can be written that:

$$\tilde{v}_{L2} = (V_i + V_{C2})D_1 + V_i(D_2 - D_1) + (V_i - V_{o2})(1 - D_2) = 0 \quad (7)$$

Consequently, the conversion ratio of second output voltage over the input voltage ($G_2 = V_{o2}/V_i$) is obtained as follows:

$$G_2 = [D_1\, V_{C2}/V_i + 1]/(1 - D_2) = 1/[(1 - D_1)(1 - D_2)] \quad (8)$$

Considering Fig. 4, the voltage stresses on switches and diodes during the time interval that they are OFF is calculated as following equations:

$$V_{S1} = V_{C2} = V_{o1}/2 \quad during\ [(1 - D_1)\, T_s] \quad (9)$$

$$V_{D1b} = V_{o1} - V_{C2} = V_{o1}/2 \quad during\, (1 - D_1)\, T_s \quad (10)$$

$$V_{D1a} = V_{C2} = V_{o1}/2 \quad during\ D_1\, T_s \quad (11)$$

$$V_{S2} = V_{o2} \quad during\, Mode\, 3\ [(1 - D_2)\, T_s] \quad (12)$$

$$V_{D2b} = V_{C2} = V_{o1}/2 \quad during\, D_1\, T_s \quad (13)$$

$$V_{D2a} = \begin{cases} V_{C2} + V_{o2} = V_{o1}/2 + V_{o2} \\ \qquad during\, Mode\, 1\ (D_1\, T_s) \\ V_{o2} \\ \qquad Mode\, 2\ [(D_2 - D_1)\, T_s] \end{cases} \quad (14)$$

where considering Fig. 3, the interval time of $(1 - D_1)\, T_s$ is equal to the interval time of modes 2 and 3. $D_1\, T_s$ is equal to the time interval for mode 1. Considering Fig. 4, the average currents of switches and diodes during their conducting interval time are calculated as following equations:

$$I_{S1} = (I_{L1} - I_{o1})/D_1 \quad during\, D_1\, T_s \quad (15)$$

$$I_{D1b} = I_{o1}/D_1 \quad during\, D_1 T_s \quad (16)$$

$$I_{D1a} = I_{o1}/(1 - D_1 \quad during\ (1 - D_1)\, T_s \quad (17)$$

$$I_{S2} = I_{L2} = (I_{L2} - I_{o2})/D_2 \quad during\, D_2 T_s \quad (18)$$

$$I_{D2b} = (I_{o1} + I_{L2} - I_{o2})/(1 - D_1 \quad during\, (1 - D_1)\, T_s \quad (19)$$

$$I_{D2a} = I_{L2} = I_{o2}/(1 - D_2 \quad during\, (1 - D_2)\, T_s \quad (20)$$

It is obvious that the average input current of i_i would be equal to $I_{i1} = I_{L1} + I_{L2}$. Considering power balance law, the average current of I_{L1} would be obtained as follows:

$$I_{L1} = G_1 I_{o1} + G_2 I_{o2} - I_{L2} = \frac{D_1 I_{o1}}{(1 - D_1)(1 - D_2)} + \frac{2I_{o2}}{1 - D_1} \quad (21)$$

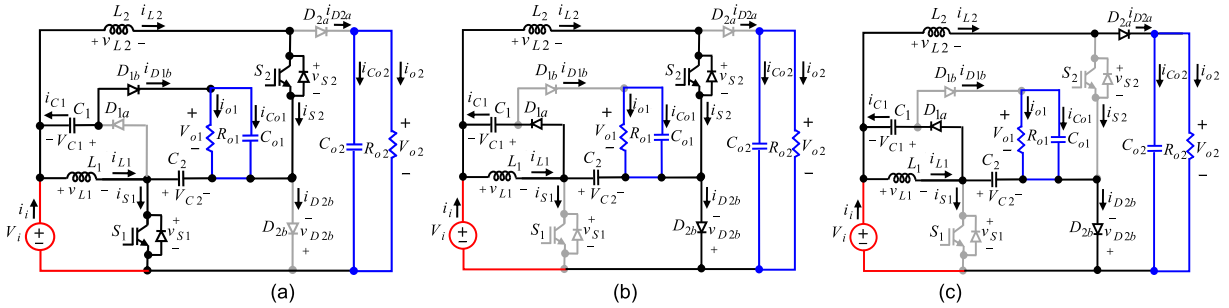

FIGURE 4. The equivalent power circuits of Modes 1, 2, 3 for $D_1 < D_2$; (a) Mode 1; (b) Mode 2; (c) Mode 3.

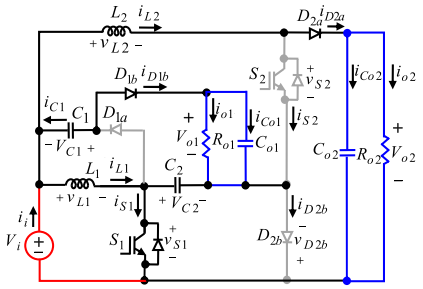

FIGURE 5. Mode 2 for $D_1 > D_2$.

2) ANALYSIS FOR $D_1 > D_2$

The equivalent circuits of the proposed converter during first and third modes for $D_1 > D_2$ are same as them for $D_1 < D_2$, which are illustrated in Fig. 4(a) and 4(c), respectively. The equivalent power circuit for second mode of $D_1 > D_2$ is shown in Fig. 5. Accordingly, the equations (1)-(5) are obtained in the operation of $D_1 > D_2$ same as $D_1 < D_2$. Considering Figs. 4(a), 4(c) and 4, the voltage across the inductor L_2 during a switching period is:

$$v_{L2} = \begin{cases} V_i + V_{C2} & during\ Modes\ 1, 2\ (D_2 T_s) \\ V_i - V_{o2} & during\ Modes\ 3\ [(1-D_2)\,T_s] \end{cases} \quad (22)$$

Consequently, applying the voltage balance law for the inductor L_2 results that the conversion ratio of second output voltage over the input voltage ($G_2 = V_{o2}/V_i$):

$$\begin{aligned} G_2 &= [D_2\, V_{C2}/V_i + 1]/(1-D_2) \\ &= [1 + D_2/(1-D_1)]/(1-D_2) \end{aligned} \quad (23)$$

The voltage stresses on switches and diodes during the time interval that they are OFF is calculated as follows:

$$V_{D2a} = V_{C2} + V_{o2} \quad during\ Mode\ 1\ \ (D_2 T_s) \quad (24)$$

$$V_{S2} = \begin{cases} V_{C2} + V_{o2} & during\ Mode\ 2\ [(D_1 - D_2)T_s] \\ V_{o2} & during\ Mode\ 3\ [(1-D_1)T_s] \end{cases} \quad (25)$$

Also, in this operation, same as the operation of $D_1 < D_2$, the equations (9)-(11) and (13) are obtained. Considering Figs. 4(a), 4(c) and 4, the average currents of switches and diodes during their conducting interval time are calculated as equations (15)-(20). Considering power balance law, the average current of I_{L1} would be obtained as follows:

$$I_{L1} = G_1 I_{o1} + G_2 I_{o2} - I_{L2} = \frac{D_2 I_{o1}}{(1-D_1)(1-D_2)} + \frac{2I_{o2}}{1-D_1} \quad (26)$$

3) DESIGN CONSIDERATIONS

In continuous conduction mode (CCM) operation of the proposed converter, the average values of the currents passing through the inductances L_1 and L_2 have to be higher than half of their current ripples [$I_L > (\Delta I_L/2)$]. Consequently, the following inequalities have to be verified;

$$L_1 > (V_i D_1)/(2 I_{L1} f_s) \quad (27)$$

$$L_2 > (V_i - V_{o2})(1-D_2)/(2 I_{L2} f_s) \quad (28)$$

The inductors' currents ripple is calculated as $\Delta i_{L1} = V_i D_1 T_s / L_1$ and $\Delta i_{L2} = (V_i - V_{o2})(1-D_2)\,T_s/L_2$.

Therefore, it can be written that:

$$i_{L1-\max} = I_{L1} \pm \Delta i_{L1}/2 \quad (29)$$

$$i_{L2-\max} = I_{L2} \pm \Delta i_{L2}/2 \quad (30)$$

For both conditions of $D_1 < D_2$ and $D_1 > D_2$, the average currents of the capacitors are calculated as follows;

$$I_{Co1} = \begin{cases} [(1-D_1)/D_1] I_{o1} & during\ (D_1 T_s) \\ -I_{o1} & during\ (1-D_1)\,T_s \end{cases} \quad (31)$$

$$I_{Co2} = \begin{cases} -I_{o2} \\ \qquad during\ (D_2 T_s) \\ I_{L2} - I_{o2} = [D_2/(1-D_2)] I_{o2} \\ \qquad during\ (1-D_2)\,T_s \end{cases} \quad (32)$$

$$I_{C1} = \begin{cases} I_{o1}/D_1 & during\ (D_1 T_s) \\ -I_{o1}/(1-D_1) & during\ (1-D_1)\,T_s \end{cases} \quad (33)$$

$$I_{C2} = \begin{cases} -[I_{L1} - I_{o2}/(1-D_1)](1-D_1)/D_1 \\ \qquad during\ D_1\,T_s \\ I_{L1} - I_{o2}/(1-D_1) \\ \qquad during\ (1-D_1)\,T_s \end{cases} \quad (34)$$

By considering the hold-up time required for step-load response, voltage ripple across each of the output capacitors (ΔV_{Co}) and voltage ripple caused by the Equivalent Series Resistance (ESR) of the output capacitors $\Delta V_{o1} = \Delta V_{Co1} + \Delta V_{Co-ESR} = \Delta V_{Co1} + r_{Co1}\Delta I_{Co1}$. As a result, the minimum values of the capacitors can be calculated as given in Table 1.

TABLE 1. Minimum values of capacitors.

$C_{1\_\min}$	$\frac{D_1 T_s (I_{o1}/D_1)}{\Delta V_{C1}} = \frac{D_1(-n_{s1})(-I_{H1})}{\{0.01 V_{C1} - r_{C1} I_{o1}/[D_1(1-D_1)]\} f_s}$
$C_{2\_\min}$	$\frac{[I_{L1} - I_{o2}/(1-D_1)](1-D_1)}{\{0.01 V_{C2} - r_C [I_{L1} - I_{o2}/(1-D_1)]/D_1\} f_s}$
$C_{o1-\min}$	$C_{o1\_ESR} = (1-D_1) I_{o1}/[(0.01 V_{Co1} - r_C I_{o1}/D_1) f_s]$ $C_{o1\_THT} = 1/[0.01\, R_{o1}(0.1 f_s)]$, $C_{o1-\min} = \max(C_{o1\_ESR}, C_{o1\_THT})$
$C_{o2-\min}$	$C_{o2\_ESR} = D_2 I_{o2}/[(0.01 V_{Co2} - r_C I_{L2}) f_s]$ $C_{o2-THT} = 1/[0.01\, R_{o2}(0.1 f_s)]$, $C_{o2-\min} = \max(C_{o2}\vert_{ESR}, C_{o2}\vert_{THT})$

4) SMALL SIGNAL ANALYSIS AND CONTROLLING SYSTEM OF PROPOSED SIDO MOTHER-MODULE

a: CONTINUES PI CONTROLLING SYSTEM

According to Fig. 4, it is assumed that the inductor currents i_{L1}, i_{L2}, capacitor voltages v_{C1}, v_{C2}, v_{Co1}, v_{Co2} are the state variables. The input voltage source v_i is defined by source vector u_{in}. The output voltages are v_{Co1}, v_{Co2} should be regulated. Accordingly, the state matrixes as follows:

$$sX = AX + B_0 \tilde{v}_i + B_1 \tilde{d}_1 + B_2 \tilde{d}_2 \quad (35)$$

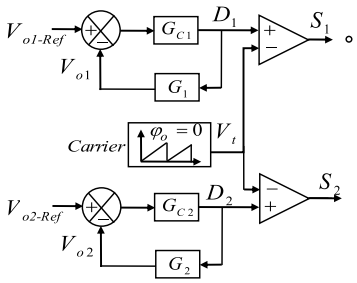

FIGURE 6. Closed loop controller of the output voltages for the proposed SIDO mother-module for $D_2 > D_1$.

The state matrix A and matrixes B_1, B_2 are obtained as (36) and (37), as shown at the bottom of the next page.

$$X = \begin{bmatrix} \tilde{i}_{L1} \\ \tilde{i}_{L2} \\ \tilde{v}_{C1} \\ \tilde{v}_{C2} \\ \tilde{v}_{Co1} \\ \tilde{v}_{Co2} \end{bmatrix}, \quad B_2 = \begin{bmatrix} 0 \\ \dfrac{V_{Co2}}{L_2} \\ 0 \\ 0 \\ 0 \\ \dfrac{-I_{L2}}{C_{o2}} \end{bmatrix},$$

$$B_1 = \begin{bmatrix} V_{C2}/L_1 \\ V_{C2}/L_2 \\ \dfrac{V_{Co1} - 2\,V_{C2} + r_C(I_{L2} - I_{L1})}{C_1} \\ \dfrac{V_{Co1} - 2(V_{C1} + V_i) - r_C(I_{L2} + I_{L1})}{C_2} \\ \dfrac{[V_{C1} + V_{C2} + V_i - V_{Co1} - r_C I_{L2}]}{2r_C C_{o1}} \\ 0 \end{bmatrix} \quad (36)$$

As a result, the transfer functions of the output voltages v_{Co1} and v_{Co2} are obtained as (38) and (39), as shown at the bottom of the next page, where

$$C_1 = [0\ \ 0\ \ 0\ \ 0\ \ 1\ \ 0] \quad (40)$$

$$C_2 = [0\ \ 0\ \ 0\ \ 0\ 0\ 1] \quad (41)$$

Therefore, by adjusting the PI parameters K_p and K_i of the voltage loop controllers, the closed-loop system of the proposed converter which is shown in Fig. 6, can achieve a better stability performance.

$$G_{c1} = K_{p1} + K_{i1}/s = 0.00001 + 0.24/s \quad (42)$$

$$G_{c2} = K_{p2} + K_{i2}/s = 0.0001 + 0.05/s \quad (43)$$

In order to generate the drive signals for S_1 and S_2 in Fig. 6 the PWM technique is used and D_1 and D_2 are respectively compared with the saw tooth wave V_t. When D_1 is higher than V_t, S_1 is in on-state. Moreover, S_2 is in on-state when D_2 is larger than V_t. The bode diagrams of the open-loop transfer functions with the PI voltage controllers in the step-up operating mode can be obtained as shown in Fig. 7. The amplitude margin and the phase margin are both greater

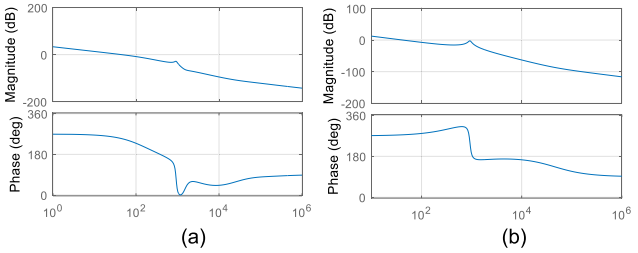

FIGURE 7. Bode plots of the small-signal open-loop transfer functions with PI voltage controller; (a) bode for ($G_{C1}(s) \times G_1(s)$); bode for ($G_{C2}(s) \times G_2(s)$).

than 0. Therefore, the closed-loop systems of the proposed converter, which adopts the PI voltage controllers, can operate stably. As mentioned before, the poles of transfer function are calculated before and were in the left half's plane.

b: DIGITAL NONLINEAR CONTROLLING SYSTEM DESIGN FOR THE PROPOSED SIDO MOTHER-MODULE

The proposed nonlinear control for the proposed converter is written as following form:

$$d_1 = \sqrt{k_{P1}(v_{Co1} - V_{Co1d}) + k_{I1} \int (v_{Co1} - V_{Co1d})\, dt} \quad (44)$$

$$d_2 = \sqrt{k_{P2}(v_{Co2} - V_{Co2d}) + k_{I2} \int (v_{Co2} - V_{Co2d})\, dt} \quad (45)$$

where, V_{Co1d} and V_{Co2d} are the final stable values of the capacitors voltages of v_{Co1} and v_{Co2}. d_1 and d_2 are controlling parameters for the two output voltages.

It is seen that the nonlinear control equations are the square root form of the linear PI controllers. where, d_1 and d_2 are always positive. The proposed control strategy in (44)-(45) leads to a stable closed-loop system. The output voltage's error will be close to zero under the variations of output load or input voltage. To demonstrate this capability, at first the average error closed-loop dynamics are obtained and then the stability analysis is resulted. Consequently, considering (36), the state error matrix would be written as follows;

$$\begin{bmatrix} e_1 \\ e_2 \\ e_3 \\ e_4 \\ e_5 \\ e_6 \end{bmatrix} = \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \\ v_{Co1} \\ v_{Co2} \end{bmatrix} - \begin{bmatrix} i_{L1d} \\ i_{L2d} \\ v_{C1d} \\ v_{C2d} \\ v_{Co1d} \\ v_{Co2d} \end{bmatrix} = x - x_d \quad (46)$$

Accordingly, by derivation from above equation, it can be resulted that $\dot{e} = \dot{x}$. Moreover, for simplifying the analysis of state Matrixes with nonlinear equations, two extra variables should be defined as follows;

$$z_1 = k_{I1} \int (v_{Co1} - V_{Co1d})\, dt = k_{I1} \int e_5\, dt \ or\ \dot{z_1} = k_{I1} e_5 \quad (47)$$

$$z_2 = k_{I2} \int (v_{Co2} - V_{Co2-r})\, dt = k_{I2} \int e_6\, dt \ or\ \dot{z_2} = k_{I2} e_6 \quad (48)$$

As a result, equations (44)-(45) are rewritten as follows:

$$d_1 = \sqrt{k_{P1}e_5 + k_{I1}\int e_5\,dt} = \sqrt{k_{P1}e_5 + z_1} \tag{49}$$

$$d_2 = \sqrt{k_{P2}e_6 + k_{I2}\int e_6\,dt} = \sqrt{k_{P2}e_6 + z_2} \tag{50}$$

Considering the equations (36)-(37), the state equations for time domain can be written as (51), as shown at the bottom of the next page. Consequently, the state equations for error dynamics can be concluded as equation (52), as shown at the bottom of the next page.

As a result, by replacing (49)-(50) into (52), it would be written as equation (53), as shown at the bottom of the next page. The equilibrium point of error Matrix in (53) is obtained by setting error matrix equal to 0 as follows;

$$\begin{bmatrix} \dot{e}_1 \\ \dot{e}_2 \\ \dot{e}_3 \\ \dot{e}_4 \\ \dot{e}_5 \\ \dot{e}_6 \\ \dot{z}_1 \\ \dot{z}_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad \text{results } e_{Equilibrium} = \begin{bmatrix} e_{1\infty} \\ e_{2\infty} \\ e_{3\infty} \\ e_{4\infty} \\ e_{5\infty} \\ e_{6\infty} \\ z_{1\infty} \\ z_{2\infty} \end{bmatrix} \tag{54}$$

Consequently, the linearization of the closed-loop system about $e_{Equilibrium}$ is obtained as follows;

$$\dot{\eta} = M\eta = M \begin{bmatrix} e_1 - e_{1\infty} \\ e_2 - e_{2\infty} \\ e_3 - e_{3\infty} \\ e_4 - e_{4\infty} \\ e_5 - e_{5\infty} \\ e_6 - e_{6\infty} \\ z_1 - z_{1\infty} \\ z_2 - z_{2\infty} \end{bmatrix}^T \tag{55}$$

Considering (53)-(55), the closed-loop system can be simplified as given in APENDIX, which will be asymptotically stable if all the eigenvalues lie in the left-half complex plane. The eigenvalues of the closed loop system are given by the characteristic equation of $|\lambda I - M| = 0$. Fig.8 shows schematic of the closed loop nonlinear digital controller for regulation of output voltages in the proposed SIDO mother-module for $D_2 > D_1$.

B. ANALYSIS OF THE PROPOSED DUAL-INPUT, THREE-OUTPUT DITO DEVELOPED MODULE

The power circuit of the proposed dual input, thee output converter is illustrated as Fig. 9. The proposed converter has six conditions of duty cycles for 2 input, 3 output topology as shown in the left column of Table 2. As a result, the calculated equations for the output voltage of V_{o3} in six conditions of duty cycle are illustrated in second column of Table 2.

According to the third row of Table 2, the output voltage of V_{o3}, is same for two conditions of $D_2 > D_1 > D_3$ and

$$B_0 = \begin{bmatrix} 1/L_1 \\ 1/L_2 \\ -1/(2r_C C_1) \\ (1-2D_1)/C_2 \\ D_1/(2r_C C_{o1}) \\ 0 \end{bmatrix},$$

$$A = \begin{bmatrix} 0 & 0 & 0 & -(1-D_1)/L_1 & 0 & 0 \\ 0 & 0 & 0 & D_1/L_2 & 0 & -(1-D_2)/L_2 \\ r_C(1-D_1)/C_1 & r_C D_1/C_1 & -1/(2r_C C_1) & (1-2D_1)/C_1 & D_1/C_1 & 0 \\ r_C(1-D_1)/C_2 & -r_C D_1/C_2 & (1-2D_1)/C_2 & -1/C_2 & D_1/C_2 & 0 \\ 0 & -D_1/(2C_{o1}) & D_1/(2r_C C_{o1}) & D_1/(2r_C C_{o1}) & -D_1/(2r_C C_{o1}) - 1/(R_{o1}C_{o1}) & 0 \\ 0 & (1-D_2)/C_{o2} & 0 & 0 & 0 & -1/(R_{o2}C_{o2}) \end{bmatrix} \tag{37}$$

$$G_1(s) = \frac{\tilde{v}_{Co1}}{\tilde{d}_1}\bigg|_{\tilde{d}_2=0,\tilde{v}_i=0} = \frac{G_{v_{Co1}-d1}(s)}{G_p(s)} = C_1B_1(sI - A)^{-1} \tag{38}$$

$$G_2(s) = \frac{\tilde{v}_{Co2}}{\tilde{d}_1}\bigg|_{\tilde{d}_1=0,\tilde{v}_i=0} = \frac{G_{v_{Co2}-d2}(s)}{G_p(s)} = C_2B_2(sI - A)^{-1} \tag{39}$$

$D_1 > D_2 > D_3$. In this part, as an example, the theoretical analysis of the two-input, three output converter with the duty cycle condition of $D_2 > D_1 > D_3$ is given. The equivalent power circuits of the proposed converter for the duty cycle condition of $D_2 > D_1 > D_3$, during a switching period is shown in Fig. 10.

Considering Fig. 10, the voltage stress on switch and diodes in the third stage of DITO converter, during the

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{i}_{L2} \\ \dot{v}_{C1} \\ \dot{v}_{C2} \\ \dot{v}_{Co1} \\ \dot{v}_{Co2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -(1-d_1)/L_1 & 0 & 0 \\ 0 & 0 & 0 & d_1/L_2 & 0 & -(1-d_2)/L_2 \\ r_C(1-d_1)/C_1 & r_C d_1/C_1 & -1/(2r_C C_1) & (1-2d_1)/C_1 & d_1/C_1 & 0 \\ r_C(1-d_1)/C_2 & -r_C d_1/C_2 & (1-2d_1)/C_2 & -1/C_2 & d_1/C_2 & 0 \\ 0 & -d_1/(2C_{o1}) & d_1/(2r_C C_{o1}) & d_1/(2r_C C_{o1}) & -d_1/(2r_C C_{o1}) - 1/(R_{o1}C_{o1}) & 0 \\ 0 & (1-d_2)/C_{o2} & 0 & 0 & 0 & -1/(R_{o2}C_{o2}) \end{bmatrix} \times \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \\ v_{Co1} \\ v_{Co2} \end{bmatrix} + \begin{bmatrix} 1/L_1 \\ 1/L_2 \\ -1/(2r_C C_1) \\ (1-2d_1)/C_2 \\ d_1/(2r_C C_{o1}) \\ 0 \end{bmatrix} V_i \tag{51}$$

$$\begin{bmatrix} \dot{e}_1 \\ \dot{e}_2 \\ \dot{e}_3 \\ \dot{e}_4 \\ \dot{e}_5 \\ \dot{e}_6 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -(1-d_1)/L_1 & 0 & 0 \\ 0 & 0 & 0 & d_1/L_2 & 0 & -(1-d_2)/L_2 \\ r_C(1-d_1)/C_1 & r_C d_1/C_1 & -1/(2r_C C_1) & (1-2d_1)/C_1 & d_1/C_1 & 0 \\ r_C(1-d_1)/C_2 & -r_C d_1/C_2 & (1-2d_1)/C_2 & -1/C_2 & d_1/C_2 & 0 \\ 0 & -d_1/(2C_{o1}) & d_1/(2r_C C_{o1}) & d_1/(2r_C C_{o1}) & -d_1/(2r_C C_{o1}) - 1/(R_{o1}C_{o1}) & 0 \\ 0 & (1-d_2)/C_{o2} & 0 & 0 & 0 & -1/(R_{o2}C_{o2}) \end{bmatrix} \times \left\{ \begin{bmatrix} e_1 \\ e_2 \\ e_3 \\ e_4 \\ e_5 \\ e_6 \end{bmatrix} + \begin{bmatrix} i_{L1d} \\ i_{L2d} \\ v_{C1d} \\ v_{C2d} \\ v_{Co1d} \\ v_{Co2d} \end{bmatrix} \right\} + \begin{bmatrix} 1/L_1 \\ 1/L_2 \\ -1/(2r_C C_1) \\ (1-2d_1)/C_2 \\ d_1/(2r_C C_{o1}) \\ 0 \end{bmatrix} V_i \tag{52}$$

$$\begin{bmatrix} \dot{e}_1 \\ \dot{e}_2 \\ \dot{e}_3 \\ \dot{e}_4 \\ \dot{e}_5 \\ \dot{e}_6 \\ \dot{z}_1 \\ \dot{z}_2 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -(1-\sqrt{k_{P1}e_5+z_1})/L_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \sqrt{k_{P1}e_5+z_1}/L_2 & 0 & -(1-\sqrt{k_{P2}e_6+z_2})/L_2 & 0 & 0 \\ r_C(1-\sqrt{k_{P1}e_5+z_1})/C_1 & r_C\sqrt{k_{P1}e_5+z_1}/C_1 & -1/(2r_C C_1) & (1-2\sqrt{k_{P1}e_5+z_1})/C_1 & \sqrt{k_{P1}e_5+z_1}/C_1 & 0 & 0 & 0 \\ r_C(1-\sqrt{k_{P1}e_5+z_1})/C_2 & -r_C\sqrt{k_{P1}e_5+z_1}/C_2 & (1-2\sqrt{k_{P1}e_5+z_1})/C_2 & -1/C_2 & \sqrt{k_{P1}e_5+z_1}/C_2 & 0 & 0 & 0 \\ 0 & -\frac{\sqrt{k_{P1}e_5+z_1}}{2C_{o1}} & \frac{\sqrt{k_{P1}e_5+z_1}}{2r_C C_{o1}} & \frac{\sqrt{k_{P1}e_5+z_1}}{2r_C C_{o1}} & -\frac{\sqrt{k_{P1}e_5+z_1}}{2r_C C_{o1}} - \frac{1}{R_{o1}C_{o1}} & 0 & 0 & 0 \\ 0 & (1-\sqrt{k_{P2}e_6+z_2})/C_{o2} & 0 & 0 & 0 & -\frac{1}{R_{o2}C_{o2}} & 0 & 0 \\ 0 & 0 & 0 & 0 & k_{I1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & k_{I2} & 0 & 0 \end{bmatrix} \times \begin{bmatrix} e_1 + i_{L1d} \\ e_2 + i_{L2d} \\ ce_3 + v_{C1d} \\ e_4 + v_{C2d} \\ e_5 + v_{Co1d} \\ e_6 + v_{Co2d} \\ z_1 \\ z_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ -k_{I1}v_{Co1d} \\ -k_{I2}v_{Co2d} \end{bmatrix} + \begin{bmatrix} 1/L_1 \\ 1/L_2 \\ -1/(2r_C C_1) \\ (1-2\sqrt{k_{P1}e_5+z_1})/C_2 \\ \sqrt{k_{P1}e_5+z_1}/(2r_C C_{o1}) \\ 0 \\ 0 \\ 0 \end{bmatrix} V_i \tag{53}$$

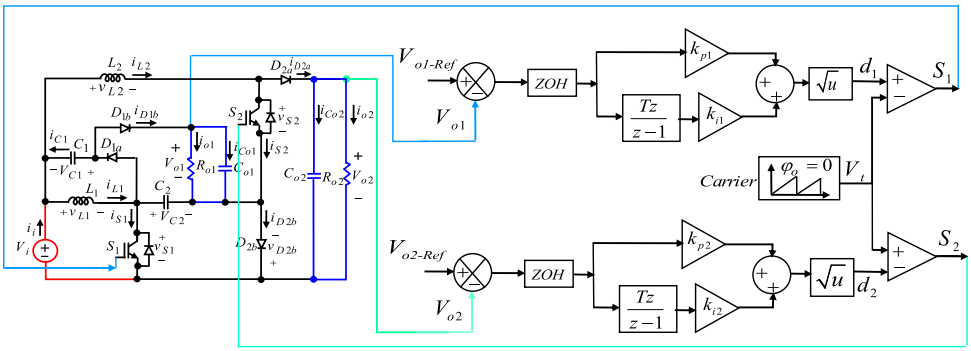

FIGURE 8. Closed loop nonlinear digital controller for regulation of output voltages in the proposed SIDO mother-module for $D_2 > D_1$.

TABLE 2. Output voltages of proposed converter for 2 input, 3 output topology.

Duty cycle conditions	The Output voltage of third load [V_{o3}]
$D_3 > D_2 > D_1$	$[V_{i3} + D_1V_{C2} + D_2V_{C3}]/(1-D_3)$ $= [V_{o2} + V_{i3} - V_i]/(1-D_3)$ $= 1/[(1-D_3)(1-D_2)(1-D_1)]$
$D_1 > D_2 > D_3$ $D_2 > D_1 > D_3$	$[V_{i3} + D_3(V_{C2} + V_{C3})]/(1-D_3)$ $= \{V_{i3} + [D_3/(1-D_1)]V_i + D_3V_{o2}\}/(1-D_3)$
$D_3 > D_1 > D_2$ $D_1 > D_3 > D_2$	$[V_{i3} + D_2(V_{C2} + V_{C3})]/(1-D_3)$ $= \{V_{i3} + [D_2/(1-D_1)]V_i + D_2V_{o2}\}/(1-D_3)$
$D_2 > D_3 > D_1$	$[V_{i3} + D_1V_{C2} + D_3V_{C3}]/(1-D_3)$ $= \{V_{i3} + [D_1/(1-D_1)]V_i + D_3V_{o2}\}/(1-D_3)$
$V_{C2} = V_i/(1-D_1)$ $\quad V_{C3} = V_{o2}$	

time interval that they are OFF is calculated as following equations:

$$V_{S3} = \begin{cases} V_{C2} + V_{C3} + V_{o3} = (V_{o1}/2) + V_{o2} + V_{o3} \\ \qquad (D_1 - D_3)T_s \\ V_{C3} + V_{o3} = V_{o2} + V_{o3} \\ \qquad (D_2 - D_1)T_s \\ V_{o3} \\ \qquad (1 - D_2)T_s \end{cases} \tag{56}$$

$$V_{D3b} = V_{D2a} = \begin{cases} V_{o1}/2 + V_{o2} & for\ D_1T_s \\ V_{o2} & for\ (D_2 - D_1)T_s \end{cases} \tag{57}$$

$$V_{D3a}\big|_{D_3T_s} = V_{C2} + V_{C3} + V_{o3} = (V_{o1}/2) + V_{o2} + V_{o3} \tag{58}$$

The voltage stress on switches and diodes in the first and second stages of the proposed DITO converter during their conducting interval time are calculated as (9)-(14) for SIDO converter.

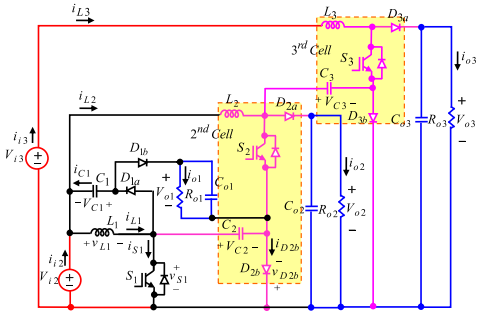

FIGURE 9. The proposed DITO converter.

Considering Fig. 10, the average currents of switch and diodes in the third stage of the proposed converter during their conducting interval time are calculated as following equations:

$$I_{S3} = (I_{L3} - I_{o3})/D_3 = I_{L3} \quad during\ D_3T_s \tag{59}$$

$$I_{D3a} = I_{o3}/(1 - D_3) = I_{L3} \quad during\ (1 - D_3)T_s \tag{60}$$

On the other hand, considering that the diodes D_{3b} and D_{2a} are turning ON in the same time interval. As a result, it can be written that:

$$I_{D3b} = \frac{I_{L3} - I_{o3}}{1 - D_2} = I_{L2} - \frac{I_{o2}}{1 - D_2} \quad during\ (1 - D_2)T_s \tag{61}$$

The average value of inductor current in the third stage is obtained as follows:

$$I_{L3} = I_{o3}/(1 - D_3) \tag{62}$$

By simplifying (61), it can be resulted that

$$I_{L2} = I_{o3}D_3/[(1 - D_3)(1 - D_2)] + [I_{o2}/(1 - D_2)] \tag{63}$$

It is obvious that the average input current of i_i would be equal to $I_{i1} = I_{L1} + I_{L2}$. Considering power balance law ($P_{oT} = P_{iT}$), results:

$$V_{o1}I_{o1} + V_{o2}I_{o2} + V_{o3}I_{o3} = V_{i2}(I_{L1} + I_{L2}) + V_{i3}I_{L3} \tag{64}$$

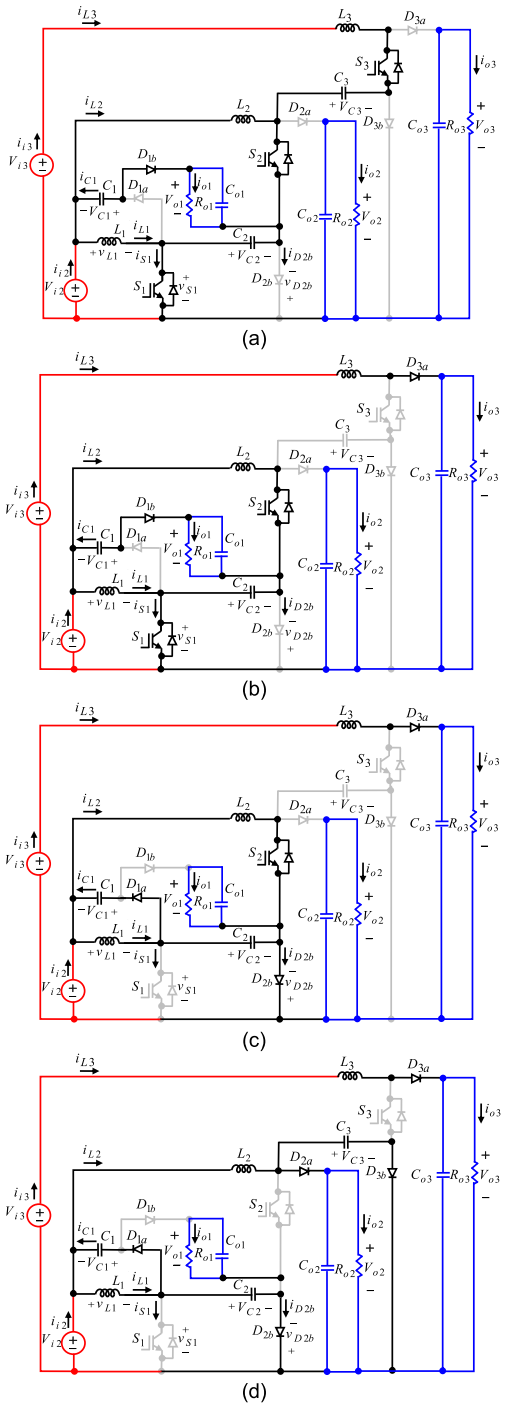

FIGURE 10. The equivalent circuits of proposed DITO converter during Modes 1, 2, 3, 4 for $D_2 > D_1 > D_3$; (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4.

$$\frac{2I_{o1}V_{i2}}{1-D_1}+\frac{I_{o2}V_{i2}}{(1-D_1)(1-D_2)}+(V_{i3}+\frac{D_3}{1-D_1}V_{i2}+D_3V_{o2})\frac{I_{o3}}{1-D_3}=V_{i2}I_{L1}+V_{i2}\left[\frac{D_3I_{o3}}{(1-D_3)(1-D_2)}+\frac{I_{o2}}{(1-D_2)}\right]+V_{i3}\frac{I_{o3}}{1-D_3} \quad (65)$$

TABLE 3. Output voltages of proposed converter for 3-input, 4-output topology.

Duty cycle conditions	The Output voltage of third load [V_{o4}]
$D_{1,2,4} > D_3 (D_3 = D_{\min})$ (6 states)	$[V_{i4}+D_3(V_{C2}+V_{C3}+V_{C4})]/(1-D_4)$ $=[V_{i4}+D_3(V_{C2}+V_{o2}+V_{o3})]/(1-D_4)$
$D_{1,2,3} > D_4 (D_4 = D_{\min})$ (6 states)	$[V_{i4}+D_4(V_{C2}+V_{C3}+V_{C4})]/(1-D_4)$ $=[V_{i4}+D_4(V_{C2}+V_{o2}+V_{o3})]/(1-D_4)$
$D_3 > D_2 > D_4 > D_1$ $D_2 > D_3 > D_4 > D_1$	$[V_{i4}+D_4(V_{C3}+V_{C4})+D_1V_{C2}]/(1-D_4)$ $=[V_{i4}+D_4(V_{o2}+V_{o3})+D_1V_{C2}]/(1-D_4)$
$D_3 > D_4 > D_2 > D_1$	$[V_{i4}+D_4V_{C4}+D_2V_{C3}+D_1V_{C2}]/(1-D_4)$ $=[V_{i4}+D_4V_{o3}+D_2V_{o2}+D_1V_{C2}]/(1-D_4)$
$D_4 > D_2 > D_3 > D_1$ $D_2 > D_4 > D_3 > D_1$	$[V_{i4}+D_3(V_{C3}+V_{C4})+D_1V_{C2}]/(1-D_4)$ $=[V_{i4}+D_3(V_{o2}+V_{o3})+D_1V_{C2}]/(1-D_4)$
$D_4 > D_3 > D_2 > D_1$	$[V_{i4}+D_3V_{C4}+D_2V_{C3}+D_1V_{C2}]/(1-D_4)$ $=[V_{i4}+D_3V_{o3}+D_2V_{o2}+D_1V_{C2}]/(1-D_4)$
$D_4 > D_1 > D_3 > D_2$ $D_4 > D_3 > D_1 > D_2$ $D_1 > D_4 > D_3 > D_2$	$[V_{i4}+D_3V_{C4}+D_2(V_{C3}+V_{C2})]/(1-D_4)$ $=[V_{i4}+D_3V_{o3}+D_2(V_{o2}+V_{C2})]/(1-D_4)$
$D_3 > D_1 > D_4 > D_2$ $D_1 > D_3 > D_4 > D_2$ $D_3 > D_4 > D_1 > D_2$	$[V_{i4}+D_4V_{C4}+D_2(V_{C3}+V_{C2})]/(1-D_4)$ $=[V_{i4}+D_4V_{o3}+D_2(V_{o2}+V_{C2})]/(1-D_4)$
$V_{C2}=V_i/(1-D_1)$, $V_{C3}=V_{o2}$, $V_{C4}=V_{o3}$	

Considering above equation, the average value of inductor current I_{L1}, would be obtained as follows:

$$I_{L1}=\frac{2I_{o1}}{1-D_1}+\frac{D_1I_{o2}}{(1-D_1)(1-D_2)}+\frac{D_3(1-D_2+D_1)I_{o3}}{(1-D_1)(1-D_2)(1-D_3)} \quad (66)$$

Consequently, the average currents of switches and diodes in the first and second stages of the proposed converter during their conducting interval time are calculated as (15)-(20) for SIDO converter.

C. ANALYSIS OF PROPOSED THREE-INPUT, FOUR-OUTPUT (TIFO) DEVELOPED MODULE

The proposed converter has twenty forth conditions of duty cycles for 3-input, 4-output topology as shown in the left column of Table 3. As a result, the calculated equations for the output voltages in each condition of duty cycles are illustrated in second column of Table 3.

D. ANALYSIS OF PROPOSED N – 1 INPUT, N OUTPUT CONVERTER

In the proposed converter, the number of input ports and output ports can be increased. As a result, considering Tables 2 and 3, the output voltages of the proposed $N-1$ input, N output converter in Fig. 2(b) for some duty cycle conditions can be calculated as the following equations.

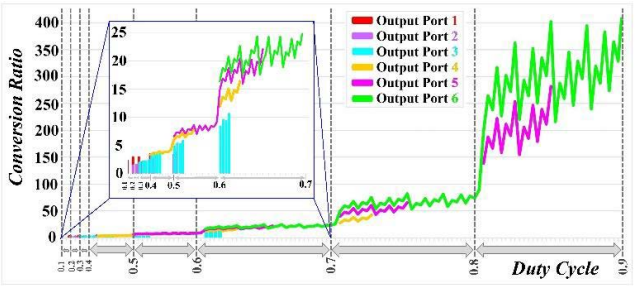

FIGURE 11. The possibility of output voltages conversion ratio considering the same input voltages and ascending duty cycles ($D_1 < D_2 < D_3 < \cdots < D_k$).

1) $D_1 < D_2 < D_3 < \cdots < D_k$

For this condition of duty cycles, kth output voltage (V_{ok}) is obtained as follows;

$$V_{ok} = \frac{1}{1 - D_k}[V_{ik} - V_{i(k-1)} + V_{o(k-1)}], \quad k = 3, 4, \ldots, N \tag{67}$$

where considering $V_{ik} = V_{i(k-1)} = V_i$, the above equation can be summarized as follows;

$$V_{ok} = \frac{V_{o(k-1)}}{1 - D_N} = \prod_{j=1}^{k} \frac{V_i}{1 - D_j} \quad for\ k = 3, 4, \ldots, N \tag{68}$$

2) $D_1 > D_2 > D_3 > \cdots > D_k$

For this condition of duty cycles, kth output voltage (V_{ok}) is obtained as follows;

$$V_{ok} = \frac{1}{1 - D_N}\left[V_{ik} + [D_k/(1 - D_1)]V_i + D_k \sum_{j=3}^{k-1} V_{o(j-1)}\right] \quad k = 3, 4, \ldots, N \tag{69}$$

3) $D_1, D_2, D_3, D_4, \ldots\ldots, D_{N-1} > D_N$ AND $D_1, D_2, D_3, D_4, \ldots\ldots, D_{N-2}, D_N > D_{N-1}$

In these conditions of duty cycles ($D_N = D_{\min}$) and ($D_{N-1} = D_{\min}$), N^{th} output voltage would be obtained as follows;

$$V_{oN} = \frac{1}{1 - D_N}[V_{iN} + [D_{\min}/(1 - D_1)]V_i + D_{\min} \sum_{j=4}^{N} V_{o(j-1)}] \tag{70}$$

In Fig. 11, the possibility of output voltages conversion ratio considering the same input voltages and ascending duty cycles ($D_1 < D_2 < D_3 < \cdots < D_k$) is shown. From Fig. 11, it can be obtained that the conversion ratio of the converter increases in the outer output ports. In contrast, for descending duty cycles ($D_1 > D_2 > D_3 > \cdots > D_k$), the inner output ports will have higher conversion ratios. This feature makes the proposed converter to be useful in versatile applications.

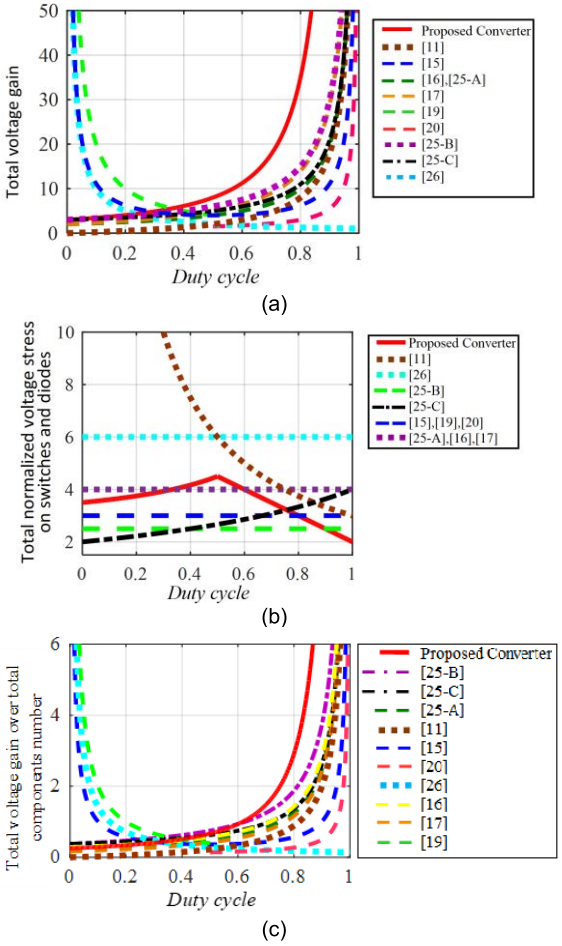

FIGURE 12. The comparison results of proposed SIDO mother-module with conventional SIDO converters versus duty cycle (D); (a) total voltage gain; (b) the total normalized voltage stress on switches and diodes; (c) total voltage gain over total components number.

III. COMPARATIVE RESULTS

The proposed converter with SIDO structure and the other conventional two-output converters are compared in Table 4 and their DC characteristics including voltage conversion ratio of first output port (G_{port-1}), second output port (G_{port-2}), total voltage gain (G_T), the total normalized maximum voltage stresses on the switches and diodes [$\Sigma(V_S + V_D)_{\max}/V_{o\_\max}$], number of switches ($N_S$), diodes ($N_D$), inductors ($N_I$), capacitors ($N_C$), coupled-inductors ($N_{CI}$) the total components number (N_T) are summarized in Table 4. The total voltage gain (G_T) versus duty cycle is shown in Fig. 12(a). The turn ratio of coupled inductors is considered as $n = 1$.

Considering Fig. 12(a) the proposed SIDO mother-module has higher voltage gain than the other conventional SIDO converters. G_T in the presented converters in Table 4 can be considered as $G_T = V_{o1}/V_i + V_{o2}/V_i$. Fig. 12(b) shows the ratio of $\Sigma(V_{S\_\max} + V_{D\_\max})/V_{o\_\max}$, which the proposed SIDO mother-module has the medium value comparing to other compared converters. The ratio of total voltage gain

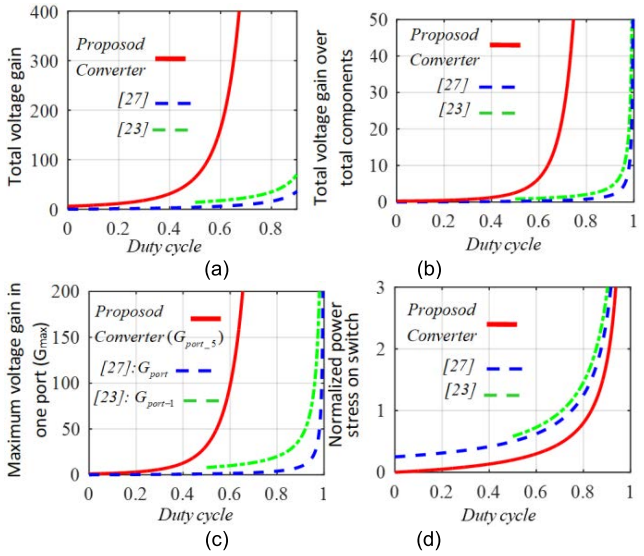

FIGURE 13. The comparison results proposed four-input converter with conventional four-input converters versus duty cycle (*D*); (a) total voltage gain; (b) total voltage gain over total components number; (c) the maximum voltage gain from one of output ports in the multi output converters; (d) the total normalized power (voltage × current) stress on switches.

over total components number (G_T/N_T) would be a fair factor to be compared as Fig. 12(c). Considering Fig. 12(c), the proposed SIDO mother-module has almost higher value of G_T/N_T than the other converters, which verifies the proposed SIDO mother-module has better performance comparing to other converters in Table 4.

The proposed converter with four input structure and the other conventional four input converters are compared in Table 5 and their DC characteristics including voltage conversion ratio of each output port (G_{port-1}, G_{port-2}, G_{port-2}, ...), total voltage gain (G_T), the normalized maximum voltage stress on switch [$V_{S\max}/V_{o\_\max}$], the average conducting current stress on the switch with maximum voltage stress $I_{S(Vs\max)}$, the normalized maximum power on switch, number of output ports (n_{out}), operating duty cycle range, number of switches (N_S), diodes (N_D), inductors (N_I), capacitors (N_C), the total components number (N_T) are summarized in Table 5. The total voltage gain (G_T) versus duty cycle is shown in Fig. 13 (a). Considering Fig. 13 (a) the proposed four-input converter has the highest voltage gain comparing to two other conventional four-input converters. G_T in the presented converters in Table 5 can be considered as $G_T = \sum_{j=1}^{j=n_{out}} V_{oj}/V_i$. By considering that, the voltage gain would be increased by using more components. As a result, the criteria of total voltage gain over total components number (G_T/N_T) would be a fair factor to be compared as Fig. 13 (b). Considering Fig. 13 (b), the proposed four-input converter has highest value of G_T/N_T which verifies the proposed converter has better performance comparing to two other converters. The presented converters in Table 5 have different voltage conversion ratios for the output ports (for the proposed four-input converter the voltage gain of five output ports are as G_{port_1}, G_{port_2}, G_{port_3}, G_{port_4}, G_{port_5}), in which, in one port the voltage gain is higher than that for other ports of the converter and it can be named as $G_{\max}$. Consequently, in Fig. 13(c), the maximum reachable voltage gain of the presented converters in Table 5 is compared. It is resulted that the proposed four-input converter has the highest value of $G_{\max}$ comparing to two other conventional four-input converters in Table 5. Fig. 13 (d) shows the normalized maximum power stress on switch, in which the proposed four-input converter has the minimum value comparing to other compared four-input converters in [22] and [28]. Consequently, the high cost related to selecting the switches with high power avoided for the proposed converter. Fig. 14 shows the two-input, three-output version of the proposed multiport DC-DC converter and its equivalent three single-input, single-output DC-DC converters. From Table 6, one can see that the proposed converter can provide much higher conversion ratio with the same voltage stress on switches in comparison with the usage of three SISO DC-DC converters with the same structures as the ones used in the proposed converter.

IV. EXPERIMENTAL RESULTS

The proposed converter is implemented in Laboratory and the experimental results which are shown in Figs. 15-17 and 21-22 verify the accuracy performance of the proposed converter and the calculated theoretical results for SIDO and DITO operations, respectively. The used experimental parameters are given in Table 7.

A. EXPERIMENTAL RESULTS OF THE PROPOSED SIDO MOTHER-MODULE

The input voltages and output voltages are considered as $V_i = 30\,V$ and $V_{o1}/V_{o2} = 150\,V/250\,V$, respectively. As a result, by considering the used parameters in Table 7, the currents and powers are calculated as $P_{o1} = 225\ W$ and $P_{o2} = 250\ W$, $I_{o1} = 1.5\ A$ and $I_{o2} = 1\ A$. The average currents of inductors are calculated as $I_{L1} = 5\,(I_{o1} + I_{o2}) = 12.5\,A$ and $I_{L2} = I_{o2}/0.3 = 3.33\,A$. Considering the input voltage as $V_i = 30\ V$, $D_1 = 0.6\ V$, $T_s = 20\ \mu$ sec, $I_{L1} = 12.5\ A$, the value of inductor L_1 should verify $L_1 > 14.4\ \mu H$. On the other hand, considering the $D_2 = 0.7\ V$, $I_{L2} = 3.33\ A$, the value of inductor L_2 should verify $L_2 > 198.2\ \mu H$. As a result, the values of inductances L_1 and L_2 can be selected as $L_1 = 100\ \mu H$ and $L_2 = 500\ \mu H$ for using in the implemented prototype. The theoretical values for the capacitors are calculated for the parameters of $D_1 = 0.6\ V$, $D_2 = 0.7\ V$, $r_C = 0.03\ \Omega$, $f_s = 50\ kHZ$ from Table 1 as $C_1 = 61.5\ \mu F$, $C_2 = 224\ \mu F$, $C_{o1-\min} = 200\ \mu F$, $C_{o2-\min} = 80\ \mu F$, therefore, the values of capacitors can be selected same as their values in Table 7.

The ripple of inductors' currents is obtained as $\Delta i_{L1} = 3.6\ A$ and $\Delta i_{L2} = 2.64\ A$. Therefore, the maximum and minimum value of inductor L_1 is calculated equal to $i_{L1-\max} = 14.3\ A$ and $i_{L1-\min} = 10.7\ A$. And also, the

TABLE 4. Comparison of high voltage gain single-input/dual-output converters.

DC-DC Converters	$G_{port\_1}=\frac{V_{o1}}{V_i}$	$G_{port\_2}=\frac{V_{o2}}{V_i}$	G_T	$\frac{\Sigma (V_S+V_D)_{\max}}{V_{o\_\max}}$	N_S	N_D	N_I	N_C	N_{CI}	N_T	Controllable output voltages at the same time with separate parameters of duty cycles	Expandable from input and output sides (Ninput, N output)
[11]	$D/(1-D)$	$\simeq D/(1-D)$	$2D/(1-D)$	$3/D$	2	1	3	3	-	9	Yes	No
[15]	$1/(1-D)$	$1/D$	$[1/(1-D)]+1/D$	3	3	-	2	4	2	11	No	Yes
[16]	$1/(1-D)$	$1/(1-D)$	$2/(1-D)$	4	2	2	-	2	1	7	Yes	No
[17]	$2N/(1-D)$	$D/(1-D)$	For N=1 $(2+D)/(1-D)$	4	4	3	-	3	2	12	No	No
[19]	$\simeq 1/D$ $0<D<0.5$	$1/D$ $0<D<0.5$	$2/D$ $0<D<0.5$	3	3	3	1	3	-	10	Yes	No
[20]	$1/(2-2D)$ $0.5<D<1$	$(1-D)/(2-2D)$ $0.5<D<1$	$(2-D)/(2-2D)$ $0.5<D<1$	3	4	2	2	3	-	11	Yes	No
[25-A]	$1/(1-D)$	$-1/(1-D)$	$2/(1-D)$	4	1	3	1	3	-	8	No	Yes up to four output
[25-B]	$1/(1-D)$	$2/(1-D)$	$3/(1-D)$	5/2	1	3	1	3	-	8	No	Yes up to four output
[25-C]	$1/(1-D)$	$(2-D)/(1-D)$	$(3-D)/(1-D)$	$4/(1-D)$	1	3	1	3	-	8	No	Yes up to four output
[26]	$\simeq 1/(2D)$	$\simeq 1/(2D)$	$\simeq 1/D$	6	2	2	1	2	-	7	No	Expandable only from output side (N output)
Proposed converter	$2/(1-D_1)$	$\frac{1}{(1-D_1)(1-D_2)}$ $0<D_1<D_2<1$	$\frac{1}{1-D_1}\left(\frac{1}{1-D_2}+2\right)$	For $0<D_2<0.5$: $2+\frac{3-D_2}{2(1-D_2)}$ For $0.5<D_2<1$: $7-5D_2$	2	4	2	4	-	12	Yes	Yes

TABLE 5. Comparison of high voltage gain four-input converters.

DC-DC Converters	$G_{port}=\frac{V_o}{V_i}$ $V_{i1}=V_{i2}=V_{i3}=V_{i4}$	$G_{\max}$	$I_{S(Vs\max)}$	$V_{S\max}$	$P_{S\_N}=\frac{V_{S\max}I_{S(Vs\max)}}{\sum_{j=1}^{n\_out}P_{oj}}$ $P_o=P_{o1}=P_{o2}=\ldots$	n_{out}	Operating duty cycle	N_S	N_D	N_I	N_C	N_T	Controllable output voltages at the same time	Expandable from input and output sides (N-input, N-output)
[23]	$G_{port\_1}=\frac{V_{o1}}{V_i}=\frac{2}{1-D_1}+\frac{1}{1-D_2}+\frac{1}{1-D_4}$ $G_{port\_2}=\frac{V_{o2}}{V_i}=\frac{1}{1-D_2}+\frac{1}{1-D_3}+\frac{1}{1-D_4}$ $G_T=\frac{7}{1-D}$	$G_{port\_1}=\frac{4}{1-D}$	$I_{S4}=\frac{I_{o1}+I_{o2}}{1-D_4}$	$V_{S4}=\frac{V_{o1}}{4}$	$\frac{\frac{V_{o1}}{4}\frac{I_{o1}+I_{o2}}{1-D_4}}{\Sigma P_o}=\frac{\frac{P_{o1}+(4/3)P_{o1}}{4(1-D_4)}}{2P_{o1}}=\frac{7/24}{1-D_4}$	2	$0.5<D_1, D_2, D_3, D_4<1$	4	7	4	5	20	Yes	Yes to N input and M output And M<N
[27]	$G_{port\_1}=\frac{V_{o1}}{V_i}=\frac{D_1}{1-D_1}$ $G_{port\_2}=\frac{V_{o2}}{V_i}=\frac{D_2}{1-D_2}$ $G_{port\_3}=\frac{V_{o3}}{V_i}=\frac{D_3}{1-D_3}$ $G_{port\_4}=\frac{D_4}{1-D_4}$ $G_T=\frac{4D}{1-D}$	$\frac{D}{1-D}$	$\frac{I_o}{1-D_4}$	V_{o1}	$\frac{\frac{I_o}{1-D_4}V_{o1}}{\Sigma P_o}=\frac{1}{4(1-D_4)}$	4	$0<D_1, D_2, D_3, D_4<1$	8	8	1	-	17	Yes	Yes to N input and N output
Proposed four input, converter	$G_{port\_1}=\frac{V_{o1}}{V_i}=\frac{2}{1-D_1}$ $G_{port\_2}=\frac{V_{o2}}{V_i}=\frac{1}{(1-D_1)(1-D_2)}$ $G_{port\_3}=\frac{V_{o3}}{V_i}=\frac{1}{(1-D_3)(1-D_2)(1-D_1)}$ $G_{port\_4}=\frac{1}{(1-D_4)(1-D_3)(1-D_2)(1-D_1)}$ $G_{port\_5}=\frac{1}{(1-D_5)(1-D_4)(1-D_3)(1-D_2)(1-D_1)}$ $G_T=G_{port\_1}+G_{port\_2}+G_{port\_3}+G_{port\_4}+G_{port\_5}$	$G_{port\_5}=\frac{1}{(1-D)^5}$	$I_{S5}=\frac{D_5 I_{o5}}{1-D_5}$	$V_{S5}=V_{o5}$	$\frac{D_5 I_{o5} V_{o5}}{(1-D_5)(\sum_{k=1}^{5}P_{ok})}=\frac{D_5}{5(1-D_5)}$	5	$0<D_1, D_2, D_3, D_4, D_5<1$	5	10	5	5	25	Yes	Yes to N-1 input and N output

TABLE 6. Comparison of proposed multiport dc-dc converter (for e.g. 2-input, 3-output version) with three single-input, single-output with the same application and the same derived structures.

DC-DC Converters	$G_{port}=\frac{V_o}{V_i}$ $V_{i1}=V_{i2}=V_{i3}=V_{i4}$	G_{max}	V_{Smax}	n_{in}	n_{out}	Operating duty cycle	N_S	N_D	N_I	N_C	N_T	Controllable output voltages at the same time
SISO CONVERTER1	$G_{port-1}=\frac{2}{1-D}$	$G_{port-1}=\frac{2}{1-D}$	$V_{S3}=V_{o3}$ $V_{S2}=V_{o2}$ $V_{S1}=V_{o1}$	2	3	$0>D_1>1$ $0>D_2>1$ $0>D_3>1$	1	3	1	3	16	Yes
SISO CONVERTER 2	$G_{port-2}=\frac{1}{1-D}$						1	1	1	1		
SISO CONVERTER 3	$G_{port-3}=\frac{1}{1-D}$						1	1	1	1		
three-input, three-output converter using three SISO converters	$G_T=G_{port-1}+G_{port-2}+G_{port-3}$						3	5	3	5		
Proposed two-input, three-output converter	$G_{port\_1}=\frac{V_{o1}}{V_i}=\frac{2}{1-D_1}$ $G_{port\_2}=\frac{V_{o2}}{V_i}=\frac{1}{(1-D_1)(1-D_2)}$ $G_{port\_3}=\frac{V_{o3}}{V_i}=\frac{1}{(1-D_3)(1-D_2)(1-D_1)}$ $G_T=G_{port-1}+G_{port-2}+G_{port-3}$	$G_{port-3}=\frac{1}{(1-D)^3}$	$V_{S3}=V_{o3}$ $V_{S2}=V_{o2}$ $V_{S1}=V_{o1}$	3	3	$0>D_3>D_2$ $>D_1>1$	3	6	3	6	18	Yes

maximum and minimum value of inductor L_2 is calculated as $i_{L2-\max} = 4.65\ A$ and $i_{L2-\min} = 2.01\ A$. According to Fig. 16, the experimental results of inductors currents can be verified. The voltage stresses on switches and diodes are;

$$V_{S1} = V_{D1b} = V_{o1}/2 = 75\ V|_{(1-D_1)T_s},$$
$$V_{S2} = V_{o2} = 250\ V|_{(1-D_2)T_s},.$$
$$V_{D1a} = V_{D2b} = V_{o1}/2 = 75\ V|_{D_1T_s},$$
$$V_{D2a} = \begin{cases} V_{o1}/2 + V_{o2} = 325\ V|_{D_1T_s} \\ V_{o2} = 250\ V|_{(D_2-D_1)T_s}. \end{cases}$$

The average currents of switches and diodes are;

$$I_{S1}|_{D_1T_s} = 18.33\,A, I_{D1b} = I_{o1}/D_1 = 2.5A|_{D_1T_s},.$$
$$I_{D1a} = I_{o1}/(1-D_1) = 3.75A|_{(1-D_1)T_s},.$$
$$I_{S2} = I_{L2} = 3.32A|_{D_2T_s},.$$
$$I_{D2b} = (I_{o1}+I_{L2}-I_{o2})/(1-D_1) = 9.55\,A|_{(1-D_1)T_s},.$$
$$I_{D2a} = I_{L2} = 3.33\,A|_{(1-D_2)T_s}.$$

A comparison between measured results in Figs. 15 and 16 and the theoretical results shows that they verify each other to a great extent. Both two output voltages can be controlled simultaneously as shown in Fig. 17. For controlling the output voltages, the microcontroller STM32F4DISCOVERY is used. The output voltage regulations of the proposed converter under variation of the input voltage, increasing suddenly from 30 V to 40 V and dropping to 20 V are extracted to demonstrate this capability of the circuit.

Fig.18 shows the output voltage regulations of the proposed SIDO mother-module by using the closed loop nonlinear digital controller under variation of the output powers. Where, from Fig. 18(a), the output power P_{o1} is decreasing suddenly at t = 0.3[sec], from 225W to 112W and increasing to 225W at t = 0.7[sec]. Moreover, based on Fig. 18(b), power P_{o2} is decreasing suddenly at t = 0.4[sec], from 250W to 125W and increasing to 250W at t = 0.8 [sec]. The values of used controlling parameters are as $k_{p1} = 0.0000000001$, $k_{i1} = 0.35$, $k_{p2} = 0.002$ and $k_{i2} = 0.3$. Considering Fig. 18, during variations of the output power of each of two output ports at different moments, the two output voltages are remained at the stable value.

Efficiency of the proposed SIDO mother-module depends on several parameters. conduction losses of switches

TABLE 7. Experimental parameters.

Input voltages/output voltages	$V_i\ /V_{o1}/V_{o2} = 30V\ /150V\ /250V$
Output Powers	$P_{o1}\ /\ P_{o2} = 225W\ /250W$
Duty cycles/Frequency	$D_1 = 0.6\ ,\ D_2 = 0.7\ ,\ f_s = 50\ kHz$
Capacitors	$C_{o1} = C_{o2} = C_2 = 220\mu F\ ,\ C_1 = 100\mu F$
Inductors	$L_1 = 100\mu H\ ,\ L_2 = 500\mu H\ ,$ Type: Toroid TDK PC40-T72
Switches/Diodes	S_1, S_2 : IPW60R017C7 Diodes $D_{1a}, D_{1b}, D_{2a}, D_{2b}$: DSEI 120
Loads	$R_{o1}\ /\ R_{o2} = 100\Omega\ /\ 250\Omega$ For $R_{o1}\ /\ R_{o2}\ /\ R_{o3} = 100\Omega\ /\ 250\Omega\ /\ 400\Omega$

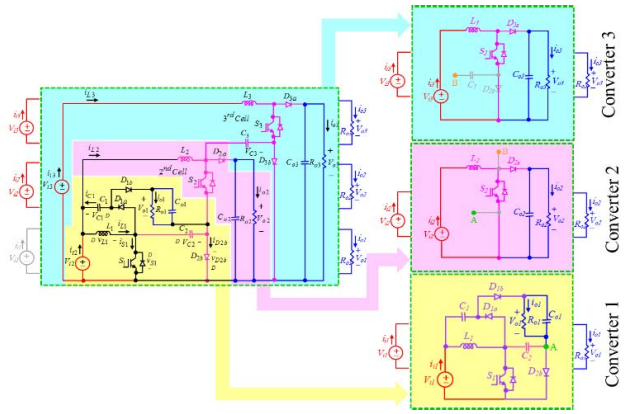

FIGURE 14. The combination of the two-input, three-output version of the proposed multiport DC-DC converter from three single-input, single-output DC-DC converters.

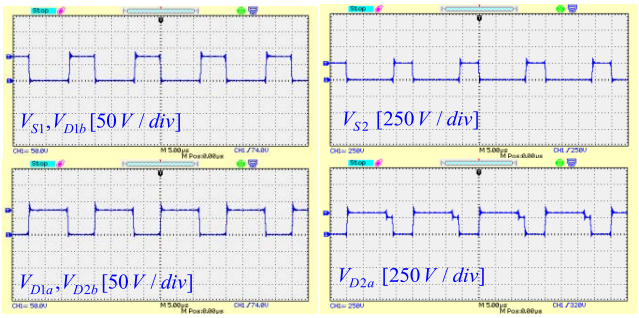

FIGURE 15. Voltages on switches and diodes.

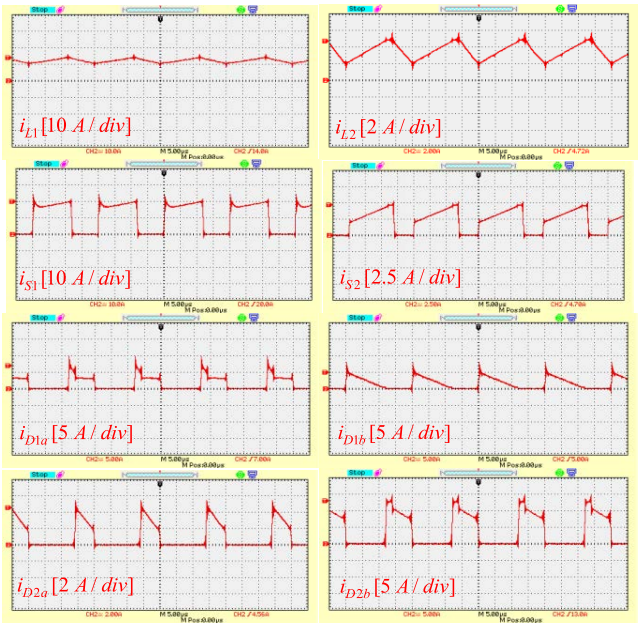

FIGURE 16. Currents of inductors, switches and diodes.

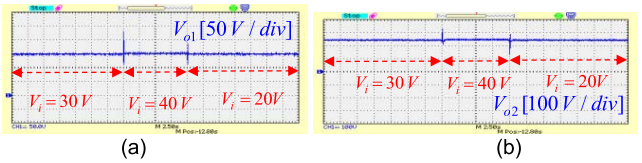

FIGURE 17. Output voltages regulation under the input voltage variation; (a) the output voltage V_{o1}; (b) the output voltage V_{o2}.

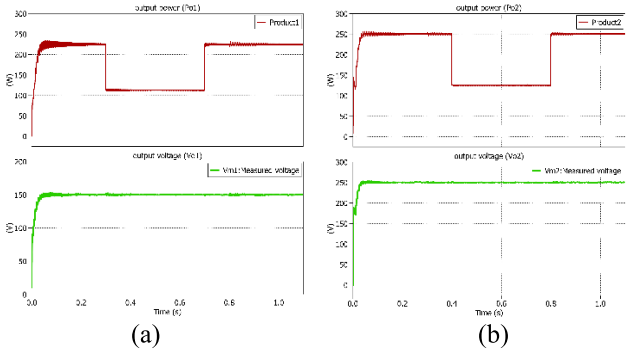

FIGURE 18. Closed loop nonlinear digital controller for regulation of output voltages in the proposed SIDO mother-module for $D_2 > D_1$. (a) the output voltage V_{o1} and power P_{o1}; (b) the output voltage V_{o2} and power P_{o2}.

($P_{Cond,S}$) and diodes ($P_{Cond,D}$), the switching losses for the switches ($P_{sw,S}$) and diodes ($P_{sw,D}$), conduction power loss of inductors ($P_{Cond,L1}$, $P_{Cond,L2}$), conduction power loss of capacitors ($P_{Cond,C}$), total power loss of switches ($P_{S,Tot}$), total power loss of diodes ($P_{D,Tot}$), total conduction loss of inductors ($P_{Cond,L}$), total conduction loss of capacitors ($P_{Cond,C}$) and total power loss of all components (P_{Loss}) are calculated as shown in Table 8. The efficiency of proposed converter is concluded as $Eff = P_{oT}/(P_{oT} + P_{Loss})$. where P_{oT} is output power that is written as $P_{oT} = P_{o1} + P_{o2}$. As a result, the internal resistors of diodes (r_D), switches (r_S), inductors (r_L), capacitors (r_C), forward drop voltage of diodes (V_{FD}), forward drop voltage of switches (V_{FS}), maximum instantaneous reverse current (I_R) and rise and full times of switches as (t_r and t_f) are considered for calculating power losses. At turning-off moment of diodes, the diode current reverses for a reverse recovery time (t_{rr}).

The theoretical calculated and experimental efficiency curves of proposed converter versus output power are plotted as illustrated in Fig. 19(a) where, in this figure the output powers ratio is as $P_{o1} = 0.9P_{o2}$. The total power is equal to ($0 < P_{oT} = P_{o2} + P_{o1} = 1.9P_{o2} < 500\ W$). The power loss calculation for the proposed converter is done for the output power equal to $P_{oT} = 445\ W$. where, $P_{o1} = 211\ W$ and $P_{o2} = 233\ W$. Therefore, the total power losses of switches, diodes, inductors, capacitors and total power loss are obtained as $P_{S,Tot} = 0.446\,P_{oT}$, $P_{D,Tot} = 0.215\,P_{oT}$, $P_{L,Tot} = 0.26\,P_{oT}$, $P_{C,Tot} = 0.075P_{oT}$, $P_{Loss} = 31.83\,W$, $P_{oT} = 444\,W$ respectively. As a result, the power loss distribution among the different components is shown in Fig. 19(b). The implemented prototype of the proposed converter in Laboratory is shown in Fig. 20.

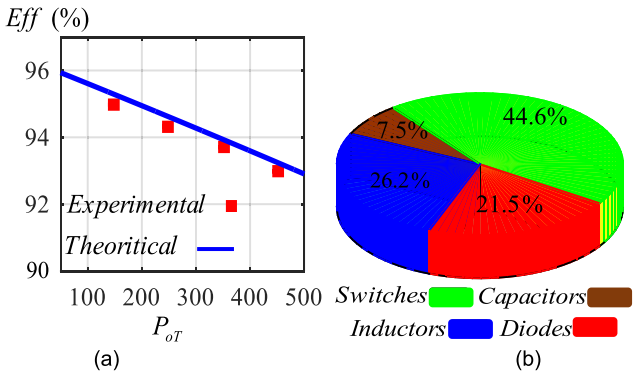

FIGURE 19. Efficiency of proposed converter versus output power and power loss distribution; (a) Experimental and theoretical efficiency; (b) Power loss distribution for $P_{oT} = 450\ W$.

FIGURE 20. Implemented prototype of the proposed converter.

B. EXPERIMENTAL RESULTS OF THE PROPOSED DITO DEVELOPED MODULE

The used experimental parameters are given in Table 9. The input voltages and output voltages are considered as $V_{i2}/V_{i3} = 30\ V/40\ V$ and $V_{o1}/V_{o2}/V_{o3} = 150\ V/250\ V/405\ V$, respectively. It is obvious that the output voltages V_{o1}, V_{o2}, output loads R_{o1}, R_{o2}, powers P_{o1}, P_{o2}, duty cycles D_1, D_2, inductors L_1, L_2 in first and second stage of DITO operation are same as SIDO operation. As a result, the voltages on switches, diodes, and capacitors in first and second stage of DITO operation are obtained same as SIDO operation. The voltage waveforms of third stage in DITO operation, are shown in Figs 21 and 22. As a result, by considering the used parameters in Table 9, the output currents and powers are calculated as $P_{o1} = 225\ W$, $P_{o2} = 250\ W$, $P_{o3} = 410\ W$, $I_{o1} = 1.5\ A I_{o2} = 1\ A$ and $I_{o3} = 0.98\ A$. The average currents of inductors are calculated as $I_{L1} = 20\,A$ and $I_{L2} = 6.71\,A$, $I_{L3} = 2I_{o3} = 2.02\,A$.

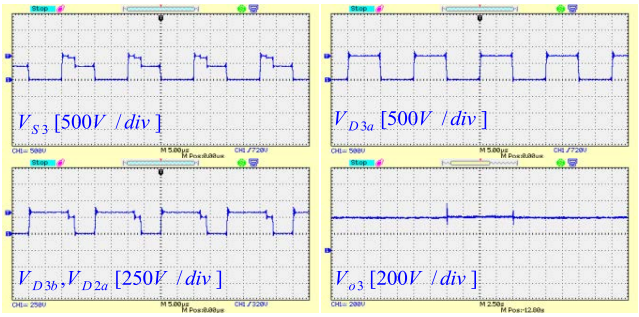

FIGURE 21. Voltages on switches and diodes.

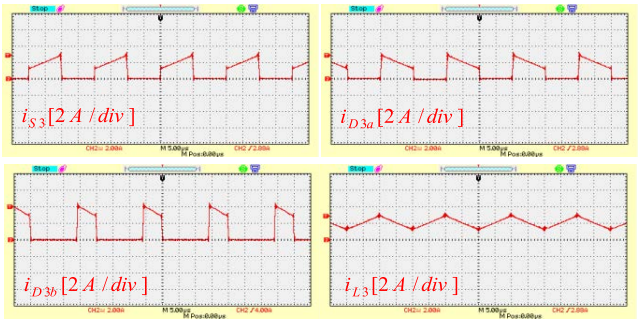

FIGURE 22. Currents of inductors, switches and diodes.

The voltage stresses on switch and diodes in the third stage;

$$V_{S1}\big|_{(1-D_1)T_s} = V_{D1b}\big|_{(1-D_1)T_s} = V_{o1}/2 = 75\,V,$$

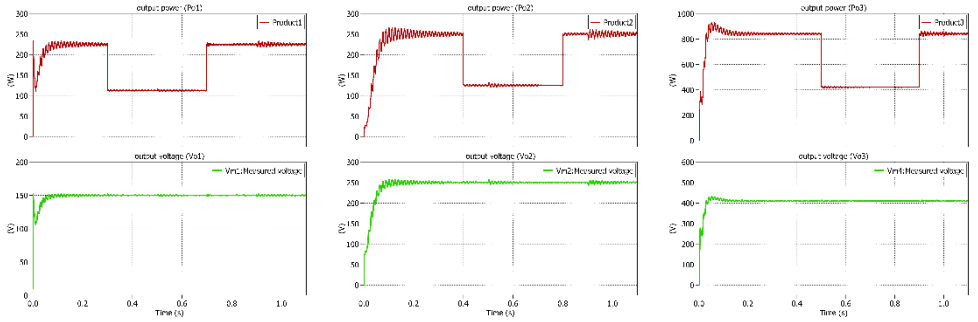

FIGURE 23. Three output voltages regulation under the output powers variation; (a) the output voltage V_{o1} and power P_{o1}; (b) the output voltage V_{o2} and power P_{o2}; (c) the output voltage V_{o3} and power P_{o3}.

TABLE 8. Power loss calculation for all components of the proposed converter.

Conduction loss	$P_{Cond,S1}=\frac{1}{T_s}\int_0^{D_1T_s}(V_{FS1}i_{S1}+r_S{i_{S1}}^2)dt=[V_{FS1}+r_S\frac{I_{S1}}{D_1}]I_{S1}$ $P_{Cond,S2}=[V_{FS2}+r_SI_{S2}/D_2]I_{S2}$, $P_{Cond,D1b}=(V_{FD1b}+r_DI_{D1b}/D_1)I_{D1b}$ $P_{Cond,D1a}=[V_{FD1a}+r_DI_{D1a}/(1-D_1)]I_{D1a}$ $P_{Cond,D2b}=[V_{FD2b}+r_DI_{D2b}/(1-D_1)]I_{D2b}$ $P_{Cond,D2a}=(V_{FD2a}+r_DI_{D2a}/(1-D_2))I_{D2a}$
Switching loss	$P_{sw,S1}=\frac{1}{T_s}\left(\int_0^{ton}v_{S1}i_{S1}dt+\int_0^{toff}v_{S1}i_{S1}dt\right)=f_SV_{S1}\frac{I_{S1}}{D_1}\frac{t_r+t_f}{6}$. $P_{sw,S2}=f_SV_{S2}(I_{S2}/D_2)(t_r+t_f)/6$ $P_{sw,D1b}=\frac{1}{T_s}\int_0^{t_{rr}}P_D(t)dt=\frac{f_SV_{D1b}I_Rt_{rr}}{6}$, $P_{sw,D1a}=\frac{f_SV_{D1a}I_Rt_{rr}}{6}$ $P_{sw,D2b}=f_SV_{D2b}I_Rt_{rr}/6$, $P_{sw,D2a}=f_SV_{D2a}I_Rt_{rr}/6$
Total switches loss	$P_{S,Tot}=P_{Cond,S1}+P_{Cond,S2}+P_{sw,S1}+P_{sw,S2}$
Total diodes loss	$P_{D,Tot}=P_{Cond,D1b}+P_{Cond,D1a}+P_{Cond,D2b}+P_{Cond,D2a}$ $+P_{sw,D1b}+P_{sw,D1a}+P_{sw,D2b}+P_{sw,D2a}$
Total losses of the inductors	$P_{Cond,L1}=r_L{I_{L1}}^2$, $P_{Cond,L2}=r_L{I_{L2}}^2$, $P_{L,tot}=P_{Cond,L1}+P_{Cond,L2}$
Total capacitors loss	$P_{Cond,C}=\frac{1}{T_s}\int_0^{T_s}r_C{i_C}^2dt$ $P_{Cond,C1}=r_C(I_{o1}/D_1)^2D_1+r_C[I_{o1}/(1-D_1)]^2(1-D_1)$ $P_{Cond,C2}=r_C\{[I_{L1}-I_{o2}/(1-D_1)](1-D_1)/D_1\}^2D_1+$ $r_C[I_{L1}-I_{o2}/(1-D_1)]^2(1-D_1)$ $P_{Cond,Co1}=r_C\{[(1-D_1)/D_1]I_{o1}\}^2D_1+r_C{I_{o1}}^2(1-D_1)$ $P_{Cond,Co2}=r_C{I_{o2}}^2D_2+r_C[I_{o2}D_2/(1-D_2)]^2(1-D_2)$ $P_{C,Tot}=P_{Cond,C1}+P_{Cond,C2}+P_{Cond,Co1}+P_{Cond,Co2}$
Total power loss	$P_{Loss}=P_{S,Tot}+P_{D,Tot}+P_{C,Tot}+P_{L,Tot}$

$$V_{S2}|_{(1-D_2)T_s}=V_{o2}=250\,V,$$
$$V_{D1a}\,|_{D_1T_s}=V_{D2b}\,|_{D_1T_s}=V_{o1}/2=75\ V|,$$
$$V_{D3b}=V_{D2a}=\begin{cases}V_{o1}/2+V_{o2}=325V: & for\ D_1T_s\\ V_{o2}=250\,V: & for\ (D_2-D_1)T_s,\end{cases}$$
$$V_{D3a}\,|_{D_3T_s}=V_{C2}+V_{C3}+V_{o3}=730\,V$$
$$V_{S3}=\begin{cases}V_{C2}+V_{C3}+V_{o3}=730\,V & (D_1-D_3)T_s\\ V_{C3}+V_{o3}=655\,V & (D_2-D_1)T_s\\ V_{o3}=405\,V & (1-D_2)T_s\end{cases}$$

The average currents of switches and diodes are;

$$I_{S1}|_{D_1T_s}=30.83\,A,$$
$$I_{D1b}|_{D_1T_s}=I_{o1}/D_1=2.5A,$$
$$I_{D1a}|_{(1-D_1)T_s}=I_{o1}/(1-D_1)=3.75A,\ I_{S2}|_{D_2T_s}=8.15\,A,$$
$$I_{D2b}\,|_{(1-D_1)T_s}=(I_{o1}+I_{L2}-I_{o2})/(1-D_1)=18.05\,A,.$$

TABLE 9. Simulation parameters.

Input voltages/output voltages	$V_{i2}/V_{i3}/V_{o1}/V_{o2}/V_{o3}=30V\ /40V\ /150V\ /250V\ /405V$
Output Powers	$P_{o1}/P_{o2}/P_{o3}=225W\ /250W\ /410W$
Duty cycles/Frequency	$D_1=0.6$, $D_2=0.7$, $D_3=0.5$, $f_s=50\,kHz$
Capacitors	$C_{o1}=C_{o2}=C_2=C_{o3}=220\mu F$, $C_1=100\mu F$
Inductors	$L_1=100\mu H$, $L_2=500\mu H$, $L_3=2mH$
Loads	For $R_{o1}/R_{o2}/R_{o3}=100\Omega/250\Omega/400\Omega$

$$I_{D2a}\,|_{(1-D_2)T_s}=I_{o2}/(1-D_2)=3.33A,$$
$$I_{S3}|_{D_3T_s}=I_{L3}=2A$$
$$I_{D3a}|_{(1-D_3)T_s}=I_{L3}=2A$$
$$I_{D3b}|_{D_3T_s}=D_3I_{L3}/(1-D_2)=3.33A$$

A comparison between measured results in Figs. 21 and 22 and the theoretical results shows that they verify each other to a great extent.

Fig. 23 shows the output voltage regulations of the proposed DITO converter by using the closed loop nonlinear digital controller under variation of the output powers. From Fig. 23(a), the output power P_{o1} decreasing suddenly at t = 0.3[sec], from 225W to 112W and increasing to 225W at t = 0.7[sec]. Moreover, in Fig. 23(b), power P_{o2} decreasing suddenly at t = 0.4[sec], from 250W to 125W and increasing to 250W at t = 0.8 [sec]. Furthermore, power P_{o3} is decreasing suddenly at t = 0.5[sec], from 820W to 410W and increasing to 820 W at t = 0.9[sec] according to Fig. 23(c). The values of used controlling parameters are as k_{p1} = 0.002, k_{i1} = 0.3, k_{p2} = 0.00000002 and k_{i2} = 0.08, k_{p3} = 0.001 and k_{i3} = 0.08. Considering Fig. (21), it can be seen that even by changing the out put load of each of three output ports at different moments, the three output voltages are remained at the stable value and the variations of output voltages under the variation of three output loads are negligible.

V. CONCLUSION

In this paper, a transformerless multiport converter is presented. The number of input and output ports of the proposed converter can be increased which makes the converter suitable for a wide range of applications. The proposed converter has higher voltage gain for ports with the low power stress on switches. Moreover, high duty cycles would not be applied to the switches to obtain higher powers or stabilizing the output voltages. The voltage gain of each of the output ports is increased and controlled by its own cell and the ports can be operated independent from each other. Also, a nonlinear-based control that can compensate for the transient drop or raise of power by these sources is adopted.

APPENDIX

Equation (A.1), as shown at the top of the next page.

$$
M = \begin{bmatrix}
\frac{\partial \dot{e_1}}{\partial e_1} = 0 & \frac{\partial \dot{e_1}}{\partial e_2} = 0 & \frac{\partial \dot{e_1}}{\partial e_3} = 0 & \frac{\partial \dot{e_1}}{\partial e_4} = \frac{-(1-\sqrt{k_{P1}e_5+z_1})}{L_1} \\
\frac{\partial \dot{e_2}}{\partial e_1} = 0 & \frac{\partial \dot{e_2}}{\partial e_2} = 0 & \frac{\partial \dot{e_2}}{\partial e_3} = 0 & \frac{\partial \dot{e_2}}{\partial e_4} = \sqrt{k_{P1}e_5+z_1/L_2} \\
\frac{\partial \dot{e_3}}{\partial e_1} = r_C\left(1-\sqrt{k_{P1}e_5+z_1}\right)/C_1 & \frac{\partial \dot{e_3}}{\partial e_2} = r_C\sqrt{k_{P1}e_5+z_1}/C_1 & \frac{\partial \dot{e_3}}{\partial e_3} = -1/\left(2r_C C_1\right) & \frac{\partial \dot{e_3}}{\partial e_4} = \left(1-2\sqrt{k_{p1}e_4+z_1}\right)/C_2 \\
\frac{\partial \dot{e_4}}{\partial e_1} = r_C\left(1-\sqrt{k_{p1}e_5+z_1}\right)/C_2 & \frac{\partial \dot{e_4}}{\partial e_2} = -r_C\sqrt{k_{p1}e_5+z_1}/C_2 & \frac{\partial \dot{e_4}}{\partial e_3} = \left(1-2\sqrt{k_{p1}e_4+z_1}\right)/C_2 & \frac{\partial \dot{e_4}}{\partial e_4} = -1/C_2 \\
0 & -\frac{\sqrt{k_{P1}e_5+z_1}}{2C_{ol}} & \frac{\sqrt{kr_1e_5+z_1}}{2r_C C_{a1}} & \frac{\sqrt{kr_1e_s+z_1}}{2r_C C_{ol}} \\
0 & \left(1-\sqrt{k_{P2}e_6+z_2}\right)/C'_{\sigma 2} & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0
\end{bmatrix}
$$

$$
\frac{\partial \dot{e_1}}{\partial e_5} = \frac{(e_4+v_{C2d})k_{P1}}{2L_1\sqrt{k_{P1}e_5+z_1}} \quad \frac{\partial \dot{e_2}}{\partial e_5} = \frac{(e_4+v_{C2d})k_{P1}}{2L_1\sqrt{k_{P1}e_5+z_1}}
$$

$$
\frac{\partial \dot{e_3}}{\partial e_1} = \left(1-2\sqrt{k_{P1}e_5+z_1}\right)/C_1
$$

$$
\frac{\partial \hat{\dot{e}_3}}{\partial e_5} = \frac{-\left(e_4+v_{C2\,d}\right)k_{P1}}{C_1\sqrt{k_{p1}e_5+z_1}} + \frac{k_{p2}\left(e_5+v_{Co1\,d}\right)}{2C_1\sqrt{k_{pl}e_5+z_1}} + \frac{\sqrt{k_{P1}e_5+z_1}}{C_1}
$$

$$
\times \quad \frac{\partial \dot{e_4}}{\partial e_5} = \frac{k_{P1}\left(e_5+v_{Cold}\right)}{2\sqrt{k_{p1}e_5+z_1}C_2} + \sqrt{k_{p1}e_5+z_1}/C_2 + \frac{-k_{P1}\left(e_3+v_{C1\delta}\right)}{\sqrt{k_{p1}e_5+z_1}/C_2} + -\frac{r_C k_{P1}\left(e_2+i_{L2\delta}\right)}{2\sqrt{k_{p1}e_5+z_1}C_2} - \frac{r_C k_{P1}\left(e_1+i_{L1\,d}\right)}{2C_2\sqrt{k_{p1}e_5+z_1}}
$$

$$
\left[-\frac{\sqrt{k_{p1}e_5+z_1}}{2r_C C_{o1}} - \frac{1}{R_{o1}C_{o1}}\right] + \frac{-k_{p1}\left(e_5+v_{\text{cold}}\right)}{4r_C C_{o1}\sqrt{k_{p1}e_5+z_1}} + \frac{k_{p1}\left(e_4+v_{C2\,d}\right)}{4r_C C_{o1}\sqrt{k_{p1}e_5+z_1}} + \frac{k_{p1}\left(e_3+v_{C1\,d}\right)}{4r_C C_{o1}\sqrt{k_{p1}e_5+z_1}} - \frac{k_{p1}\left(e_2+i_{T2\,d}\right)}{4C_{o1}\sqrt{k_{p1}e_5+z_1}}
$$

$$
\begin{matrix} 0 \\ k_\Omega \\ 0 \end{matrix}
$$

$$
\times \begin{bmatrix}
\frac{\hat{\partial}\dot{e}_1}{\partial e_6} = 0 & \frac{\partial e_1}{\partial z_1} = \frac{(e_4+v_{C2\,d})}{2L_1\sqrt{k_{p_1}e_{\leq}+z_1}} & \frac{\partial e_1}{\partial z_2} = 0 \\
\frac{\hat{\partial}e_2}{\partial e_6} = -\frac{1-\sqrt{k_{P2}e_6+z_2}}{I_{L_2}} + \frac{k_{P_2}\left(e_6\right.}{2L_2\sqrt{k_3}} & \frac{\hat{\partial}e_2}{\partial z_1} = \frac{(e_4+v_{c2\,d})}{2L_2\sqrt{k_{p_1}e_5+z_1}} & \frac{\partial \hat{e}_2}{\partial z_2} = \frac{(e_6+v_{Co2\,d})}{2L_2\sqrt{k_{222}e_6+z_2}} \\
\frac{\partial \dot{e}_3}{\partial e_6} = 0 & \frac{\partial \dot{e}_3}{\partial z_1} = r_C\frac{-1\left(e_1+i_{21d}\right)}{2C_1\sqrt{k_{P1}e_5+z_1}} + r_C\frac{\left(e_2+i_{L2\,d}\right)}{2C_1\sqrt{k_{P1}e_5+z_1}} + \frac{-\left(e_4+v_{C2\,d}\right)}{C_1\sqrt{k_{P1}e_5+z_1}} + \frac{e_5+v_{Cold}}{2C_1\sqrt{k_{P1}e_5+z_1}} & \frac{\partial \dot{e}_3}{\partial z_2} = 0 \\
\frac{\partial e_4}{\partial e_6} = 0 & \frac{\partial \dot{e}_1}{\partial z_1} = r_C\frac{-1\left(e_1+i_{L2\,d}\right)}{2C_2\sqrt{k_{p1}e_5+z_1}} + r_c\frac{-\left(e_2+i_{L2\,dl}\right)}{2C_1\sqrt{k_{p_1}e_5+z_1}} + \frac{-\left(e_3+v_{C1\,d}\right)}{C_2\sqrt{k_{pl}e_5+z_1}} + \frac{e_5+v_{COld}}{2C_2\sqrt{k_{r1}e_5+z_1}} & \frac{\partial \dot{e}_1}{\partial z_2} = 0 \\
0 & \frac{\partial e_5}{\partial z_1} = \frac{-\left(e_5+v_{Co1\,d}\right)}{4r_C C_{o1}\sqrt{k_{P_1}e_5+z_1}} + \frac{\left(e_4+v_{C2\,d}\right)}{4r_C C_{o1}\sqrt{k_{p_1}e_5+z_1}} + \frac{\left(e_3+v_{C1\,d}\right)}{4r_C C_{u1}\sqrt{k_{p_1}e_5+z_1}} - \frac{\left(e_2+i_{L2\,d}\right)}{4C_{o1}\sqrt{k_{p1}e_5+z_1}} & \frac{\partial e_4}{\partial z_2} = 0 \\
-\frac{1}{R_{o2}C_{o2}} - \frac{k_{P2}\left(e_2+i_{L2\,d}\right)}{2\sqrt{k_{P2}e_6+z_2)}}C_{o2} & 0 & \frac{-\left(e_2+i_{L2\,d}\right)}{2\sqrt{k_{p2}e_6+z_2)}C_{o2}} \\
0 & 0 & 0 \\
k_{I2} & 0 & 0
\end{bmatrix} \tag{A.1}
$$

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