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A Single-Ended Transmitter With Low Switching Noise Injection and Quadrature Clock Correction Schemes for DRAM Interface

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ABSTRACT This paper presents a transmitter with a phase controller for low switching noise injection and a quadrature clock corrector (QCC) for correcting both phase error and duty cycle distortion of the divided quadrature clocks. The phase errors and the duty cycle distortions of the quadrature clocks determine the quality of the output DQS. The proposed QCC simultaneously runs phase correction and the duty adjustment of quadrature clocks for fast correction time. In order to reduce power switching noise induced by output drivers, the proposed transmitter transfers the data at different timings using the phase controller which generates the interpolated quadrature clocks for even and odd channels. Since the even channel is synchronized with the reference quadrature clocks and the odd channel is synchronized with the interpolated quadrature clocks, the peak switching currents consumed by output drivers are spread. The proposed circuit has been designed in 180-nm CMOS process using VDD of 1.8-V and VDDQ of 0.6-V and the target data rate is 3.2 Gbps. The corrected quadrature clocks have the duty cycle distortion of 0.2% and the phase error of 1.18° with input clock distortion. The output DQS of the transmitter shows the peak-to-peak jitter of 30.55-ps in the low switching noise injection mode with the phase offset of 122°, which is improved by 28.8% as compared to the normal mode.

INDEX TERMS DRAM, transmitter (TX), double data rate (DDR), clock correction, switching noise.

I. INTRODUCTION

The developments of the Internet, mobile devices, Internet-of-Things (IoT) technologies and the processing of big data give rise to the high performance computing system. With the development of computing technologies, the performance requirements of dynamic random access memory (DRAM) have also increased. So various advanced technologies are adopted in DRAM interface such as write and read trainings, periodic ZQ calibration, and low voltage swing terminated logic (LVSTL) with separate low supply [1], [2].

In the DRAM interface, the parallel communication is more effective than the serial communication since a large amount of data should be transferred at the high speed. When the same amount of data is transferred between a memory controller and a DRAM, the parallel communication can reduce the frequency by the number of data pin. Therefore, in the high frequency operation, the parallel communication has an advantage in relaxing design conditions. However, the parallel output drivers simultaneously operate to transmit internal data to off-chip and so instantaneously consume a lot of output current. The large output current induces supply voltage drop that causes the power switching noise and the electromagnetic interference (EMI) problem. In order to reduce the switching noise and EMI, a conventional slew-rate control scheme is commonly used in DRAM, which increases the rising and falling times of output signals [3]. But the slew-rate control reduces the eye opening of the data so it should be carefully applied in high speed interfaces such as DDR4, LPDDR4, DDR5, and LPDDR5. Therefore, an alternative solution is required to decrease the maximum level of switching currents without any reduction in the eye opening.

In the high-speed DRAM interfaces, the internal quadrature clock architecture can be used to mitigate the internal bandwidth limitation of a DRAM process. But the phase

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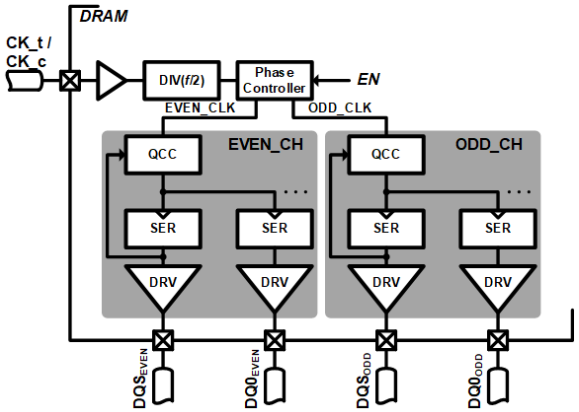

FIGURE 1. Block diagram of the proposed transmitter.

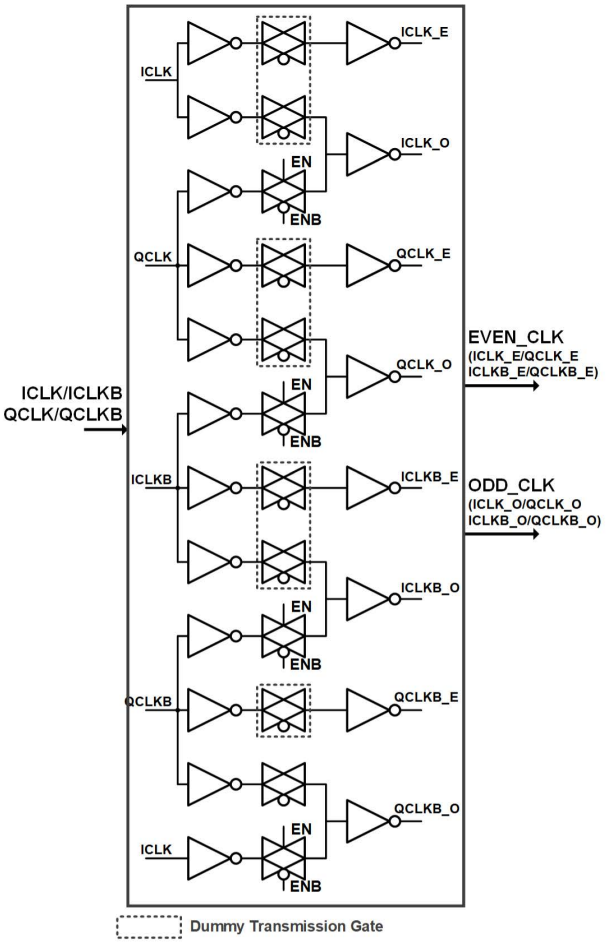

FIGURE 2. Block diagram of the phase controller.

difference among quadrature clocks should be preserved in the quadrature clock architecture because the phase difference determines the data width and the duty cycle of strobe signal. There are many non-ideal factors resulted in phase error and duty cycle distortion of quadrature clocks, such as input clock distortion, input offset voltage, and process variations. Therefore, a duty cycle corrector and a clock phase corrector are required in the clock path to minimize the phase error and the duty cycle distortion which degrade write/read timing margins between a memory controller and DRAMs [4]–[10].

This paper presents a transmitter (TX) with a phase controller for low switching noise injection and a quadrature clock corrector (QCC) for correcting the quadrature clocks. The paper is organized as follows. Section II describes the overview of the proposed transmitter. Section III explains the operation of the phase controller. The QCC for the divided clocks is explained in Section IV. The measurement results of the proposed circuit are shown in Section V. Section VI summarizes this paper.

II. OVERVIEW OF TRANSMITTER

The block diagram of the proposed transmitter is shown in Fig. 1. The proposed transmitter consists of a CK buffer, a divider (DIV), a phase controller, quadrature clock correctors (QCCs), serializers (SERs), and output drivers (DRVs). The transmitter of DRAM interface has four channels and each channel consists of 8 data paths and 1 data strobe path [11]. The output driver of each data path consumes a large amount of current because it transmits the data through a back-plane channel which causes a loss of signal power. In a conventional transmitter for DRAM interface, since each output driver is synchronized with the single clock that comes from the memory controller, the output drivers simultaneously switch output nodes, which causes the switching noise injection and EMI problem. In the proposed transmitter, to solve this problem, each output driver is synchronized with different clocks that are generated by the phase controller. The phase controller generates two 4-phase clock groups (EVEN_CLK and ODD_CLK). Reference phases of two groups are different from each other. For example, if the reference phase of EVEN_CLK is 0°, the reference phase of ODD_CLK becomes $0 + \Phi°$. As a result, the even channel and odd channel drivers switch output nodes at different timings, which reduces the switching noise injection. Even if there is a timing skew between even and odd channels, the data sampling margin is ensured in the receiver because the DRAM interface employs a source synchronous signaling so the data and the DQS are synchronized and aligned in the same channel.

III. PHASE CONTROLLER

The detailed circuit of the phase controller is shown in Fig. 2. Transmission gates (TG) are added to a conventional phase interpolator for on/off control using the external signal (EN). Dummy transmission gates are also added to reduce the delay mismatch of clock paths. Fig. 3 shows the operation of the phase controller according to the EN. The EN controls the phase of ODD_CLK (ICLK_O, QCLK_O, ICLKB_O and QCLKB_O) If the EN is high, each clock of ODD_CLK has the interpolated phase by two adjacent phases of EVEN_CLK clocks so phases of ODD_CLK clocks and EVEN_CLK

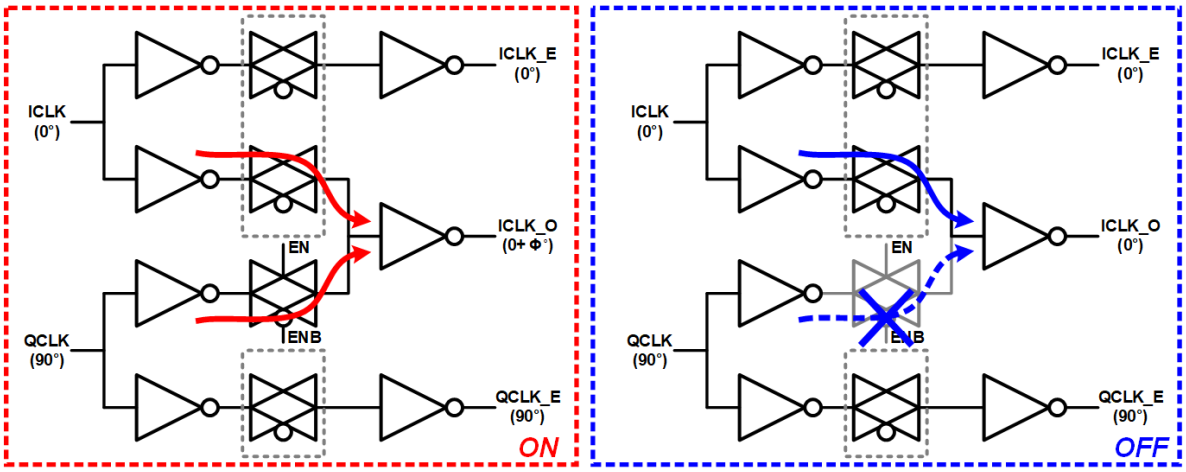

FIGURE 3. Operation of the phase controller according to EN.

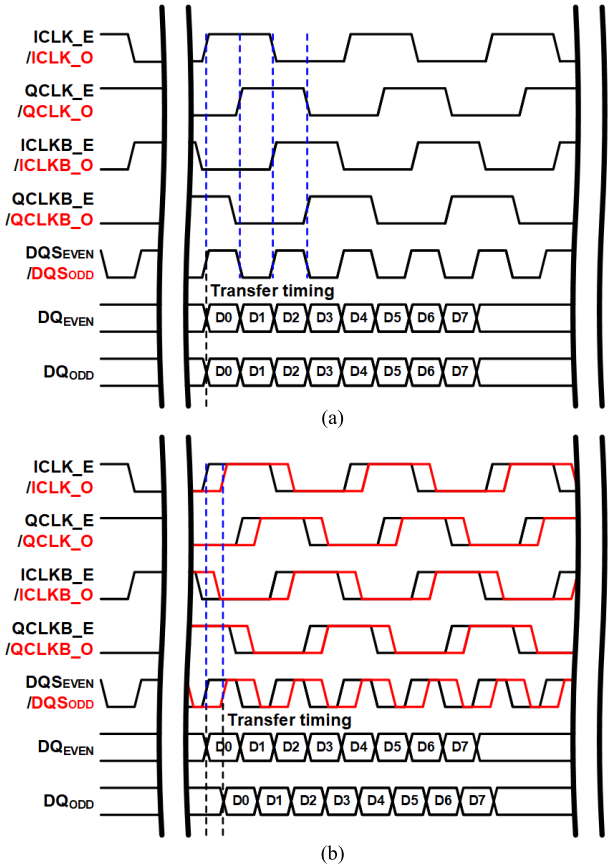

FIGURE 4. Timing diagram of output DQ and DQS for (a) the normal mode and (b) the low switching noise injection mode according to EN.

clocks are different from each other. If the EN is low, transmission gates are opened and one input path to ODD_CLK is cut off so clock phases of ODD_CLK and EVEN_CLK are the same like a conventional scheme. Fig. 4 shows the timing diagram of the output DQ and DQS signals.

$DQS_{EVEN/ODD}$ signals are generated by serializers with quadrature clocks. If the proposed circuit are used as the conventional transmitter or the EN is low, output timings of DQ_{EVEN}/DQS_{EVEN} and DQ_{ODD}/DQS_{ODD} are the same. If the EN is high, the output timings of even and odd channels are different since switching timings of EVEN_CLK and ODD_CLK are different. Thus, switching currents of output drivers are dispersed and the maximum current peak value of the output drivers is reduced. The maximum peak current reduction using the phase controller does not degrade rising and falling times of output signals, whereas the conventional slew-rate control scheme increases the rising and falling times of output signals, which reduces the eye opening of the data. However, in a low speed mode, the slew-rate control scheme is effective from a power consumption point of view. Thus, the phase controller can be turned off to reduce the power consumption. The phase difference between EVEN_CLK and ODD_CLK is changed by size ratio of inverters in the phase controller. The simulated interpolated phase (Φ) variation according to process and temperature variation and the maximum current consumption of VDDQ (0.6 V) according to Φ are shown in Fig. 5. The VDDQ is the specified VDD that supplied only output drivers for reducing power consumption in [1]. According to simulation results with PVT variations, if inverter ratio is 1:1, the Φ varies from 34 to 52 degrees with PVT variations. In this range, the effect of reducing maximum current consumption is at least 42.3% compared to the OFF mode. A control block can be added to set the optimal Φ but it is not effective since the power and area consumptions increase. The Φ is obviously changed by PVT variations if the fixed inverter ratio is used. However, the peak current reduction by changing the data switching timing is effective.

Applying this ratio, the total maximum current consumption of the 4-channel TX including the proposed clocking circuits, data serialization circuits and the output drivers which are supplied by the VDD and VDDQ is reduce by 23% in low

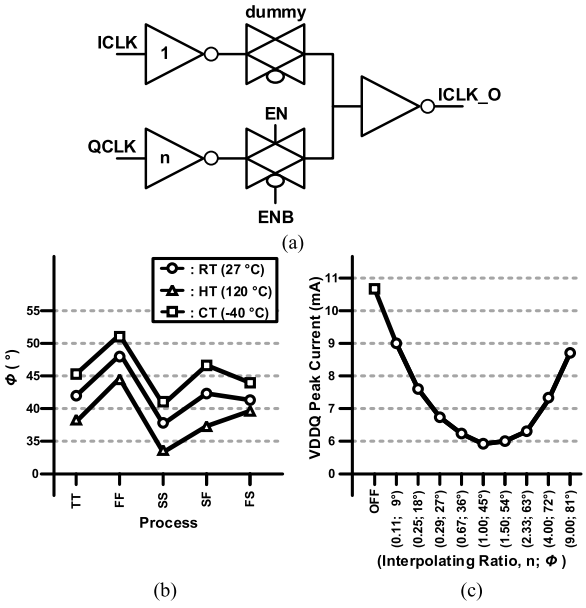

FIGURE 5. (a) Schematic of the phase interpolator, (b) the interpolated phase variation according to PT variations with 1:1 ratio, and (b) the peak current of VDDQ according to the interpolating ratios.

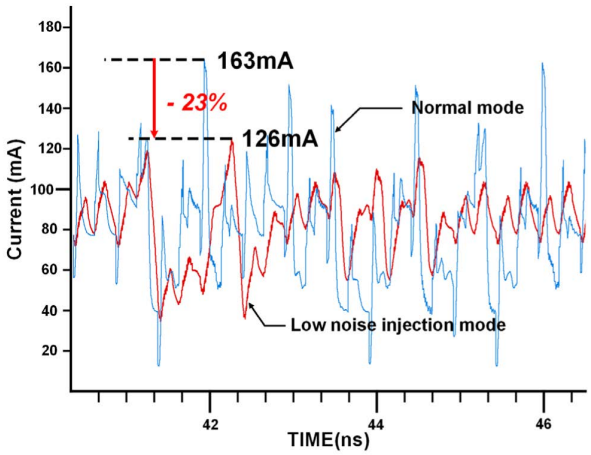

FIGURE 6. Total current profile of the proposed transmitter.

noise injection mode as compared with the normal mode as shown in Fig. 6.

IV. QUADRATURE CLOCK CORRECTOR

The block diagram of the QCC is shown in Fig. 7. The quadrature clock corrector consists of four duty cycle adjusters (DCA), two duty cycle detectors (DCD), a phase error detector (PED) and cross-coupled latches. The DCA corrects the duty cycle and phase of clocks. The duty cycle adjuster in the proposed QCC is possible to correct phase error and duty cycle distortion at the same time. The output DQS is distorted by both phase errors and the duty cycle distortions of quadrature clocks. Therefore, the DCD uses the quadrature clocks to generate a control voltage V_{CTRL} for the duty cycle correction of 4-phase clock and the PED uses the output DQS

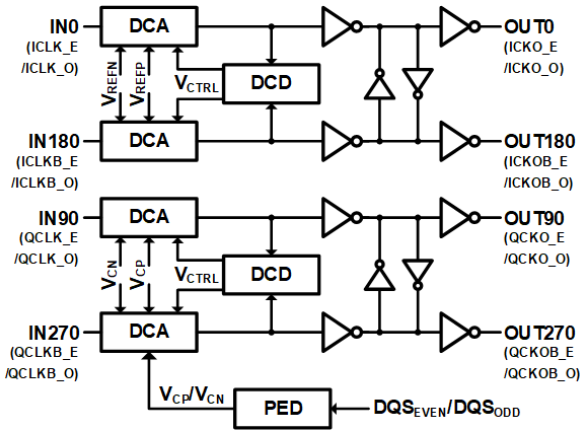

FIGURE 7. Block diagram of the quadrature clock corrector (QCC).

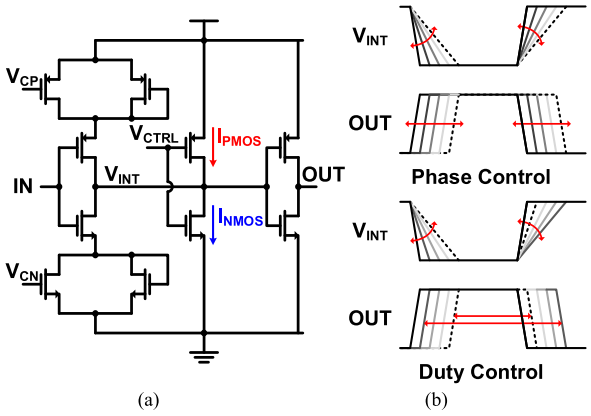

FIGURE 8. (a) Unit cell and (b) the waveform of the DCA according to phase control signal and duty cycle control signal.

signal to generate control voltages V_{CP} and V_{CN} for the phase error reduction. For the IN0 and IN180 clocks, especially the constant phase control signals V_{REFP} and V_{REFN} are applied to provide reference phases so these clocks are not affected by the phase control loop.

A. DUTY CYCLE ADJUSTER

The unit cell of the DCA is shown in Fig. 8 (a). The duty cycle adjuster consists of 8-unit cells. In the unit cell, the transistors are added to the conventional structure to correct the duty cycle of input clock [6]. The waveform of unit cell of duty cycle adjuster is shown in Fig. 8 (b). As shown in Fig. 8 (b), according to the phase control signals V_{CP} and V_{CN}, rising and falling times of the signal at the internal node V_{INT} is differently controlled to correct the duty cycle of the clock according to the duty cycle control signal V_{CTRL} applied to both pull-up and pull-down transistors. For example, if the V_{CTRL} is high, the NMOS current I_{NMOS} is larger than the PMOS current I_{PMOS} so the rising time of V_{INT} is increased and the falling time is decreased. As a result, the duty cycle of output signal OUT is increased and wider than the input signal IN. If the V_{CTRL} is low, I_{NMOS} is smaller than I_{PMOS} so

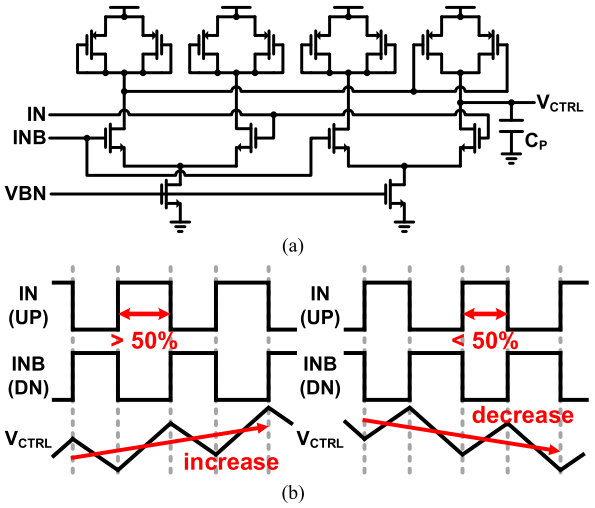

FIGURE 9. (a) Schematic of the DCD and (b) the output voltage according to the input duty distortion.

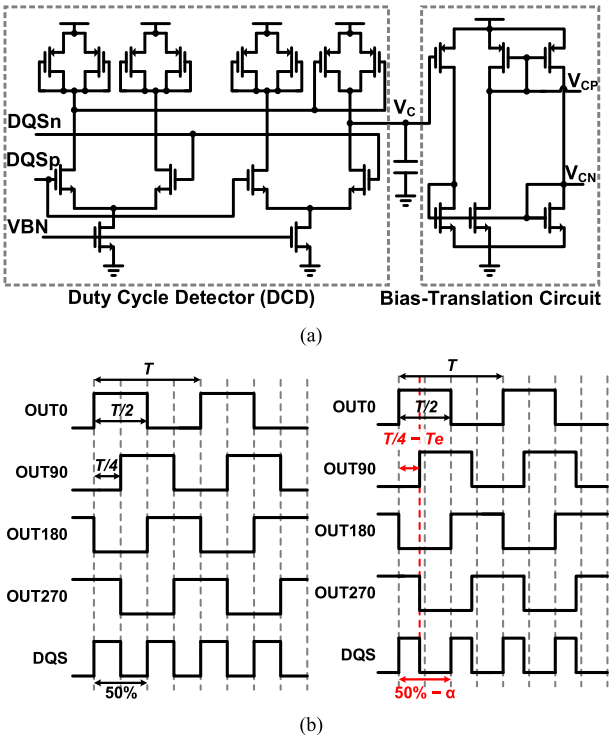

FIGURE 10. (a) Schematic of the PED and (b) a timing diagram of the quadrature clocks and the output DQS.

the rising time is decreased and the falling time is increased. As a result, the duty cycle of the output signal OUT is decreased more than the input signal IN.

B. DUTY CYCLE DETECTOR AND PHASE ERROR DETECTOR

Fig. 9 shows the schematic of the DCD and the output voltage when the input duty is distorted. The DCD uses a charge pump structure and consists of two charge pumps [12]. The DCD receives clock signals passing through the DCA as inputs and generates the V_{CTRL} according to the duty of

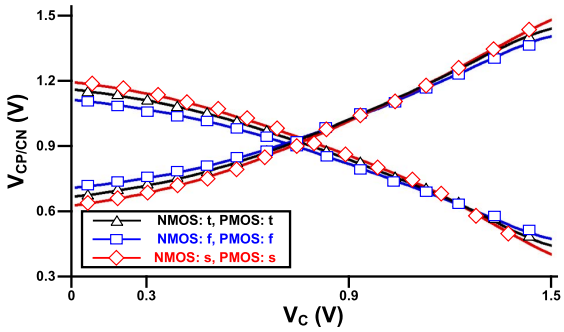

FIGURE 11. Simulated voltage profiles of the V_{CP} and V_{CN} in various process corners.

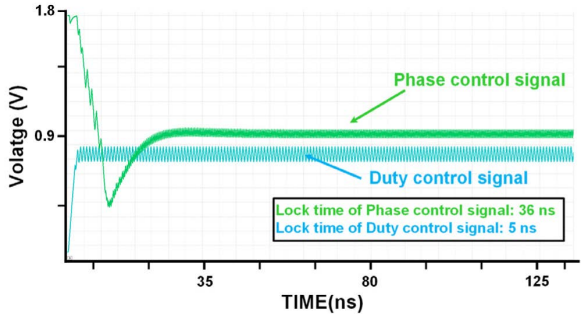

FIGURE 12. Simulated waveforms of clock control signals.

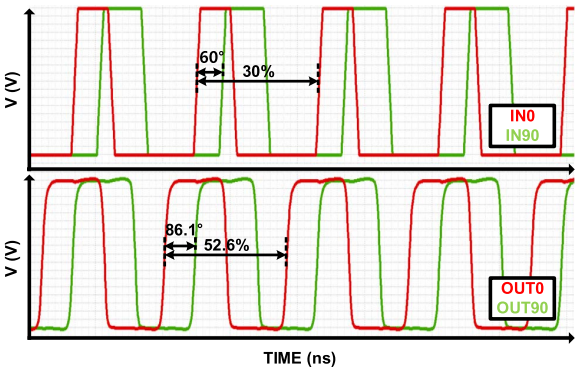

FIGURE 13. Simulated maximum duty and phase error of corrected clocks.

input signals. If duty cycle of the input clock, IN is greater than 50%, the V_{CTRL} is increased. Whereas, if duty cycle of the IN is less than 50%, the V_{CTRL} is decreased as shown in Fig. 9 (b). The generated V_{CTRL} is applied to DCA for correcting the duty cycle of the quadrature clocks.

Fig. 10 show a schematic of the PED and a timing diagram of the quadrature clocks and the output DQS. The PED consists of the DCD structure and a bias-translation circuit. The PED corrects phase errors between the quadrature clocks using output DQS signals (DQSp, DQSn). The output DQS signal is distorted if the quadrature clocks have a phase error as shown in Fig. 10 (b). In the PED, the DCD generates phase control voltage V_C according to the duty of the output DQS and then the bias-translation circuit generates V_{CP}

TABLE 1. Performance summary.

	[6]	[7]	[8]	[9]	[10]	This work
Process	130nm	55nm	130nm	65nm	90nm	**180nm**
Supply Voltage	1.2V	1.2V	1.2V	1.2V	1.0V	**1.8V**
Frequency	0.1-2 GHz	1-3 GHz	0.4-0.8GHz	0.9-1.1GHz	0.1-2.7GHz	**1.6 GHz**
Duty Cycle Distortion	3.2% @1GHz	0.8% @3GHz	0.97% @0.8GHz	1% @1GHz	1.9% @2.7GHz	**0.2%**
Phase Error	3.68 ps @2GHz	1.03 ps @3GHz	6.25 ps @0.8GHz	5 ps @1GHz	3.71 ps @2.7GHz	**3.75 ps**
P-P Jitter	N/A	19.75 ps @3GHz	20.0 ps @0.8GHz	2.98 ps @1GHz	N/A	**30.55 ps**
RMS Jitter	N/A	2.14 ps @3GHz	2.3 ps @0.8GHz	19.38 ps @1GHz	N/A	**8.95 ps**
Lock Time	N/A	<275 cycles	<75-374 cycles	<56 cycles	N/A	**<58 cycles***
Area	0.01 mm^2	0.003mm^2	0.025mm^2	0.086mm^2	0.089mm^2	**0.071 mm^2**

* Simulation result

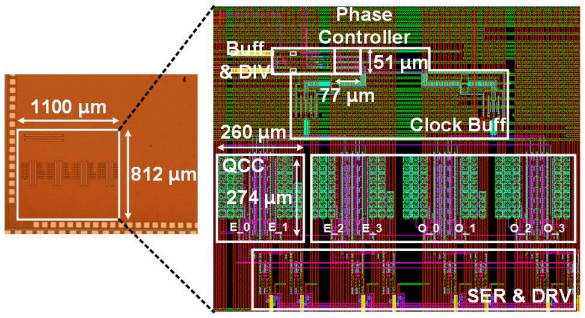

FIGURE 14. Die micrograph of the proposed TX.

and V_{CN} for the PMOS and NMOS controls, respectively. Fig. 11 shows the simulated voltage profiles of the V_{CP} and V_{CN} in various process corners. The V_C is translated to an appropriate control voltage insensitive to process variation by the bias-translation circuit.

The simulated waveforms of duty cycle and phase control signals are shown in Fig. 12. The duty cycle control signal is locked at 5-ns and the phase control signal is locked at 36 ns. So the maximum locking time is 58 cycles which is 4.74 times faster as compared to the conventional QCC.

According to the simulation results, when the duty cycle distortion of ±20% and phase error ±30° are applied to the input quadrature clocks of the QCC, the maximum duty cycle error of the corrected clocks is 2.6%, and the maximum phase error between the OUT0 and the OUT90 is 3.9° as shown in Fig. 13.

V. MEASUREMENT RESULTS

The proposed transmitter circuit has been implemented in 180-nm CMOS technology. The die micrograph with the magnified layout is shown in Fig. 14. The prototype chip consists of a clock input buffer, a clock divider, a phase controller and 4 channels (2-EVEN channels and 2-ODD channels). The output drivers have been designed using LVSTL with 0.6-V supply voltage and the other circuits have been implemented with a 1.8-V supply voltage. The whole circuit consumes 0.893-mm^2 including the modeled clock distribution network

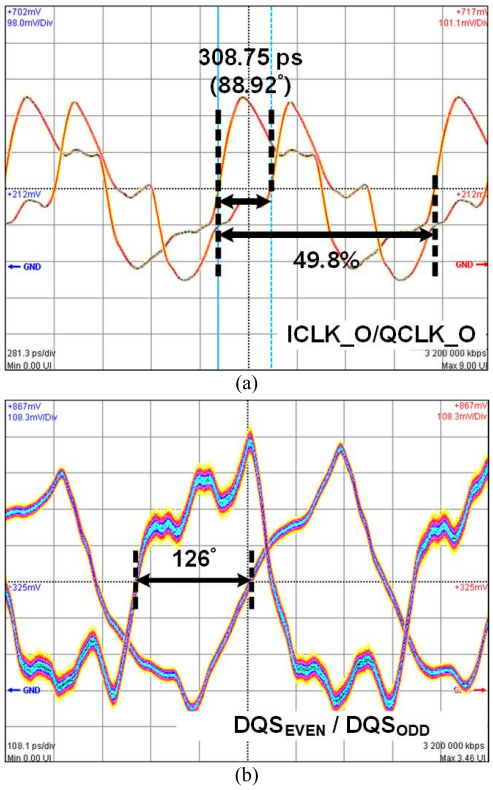

FIGURE 15. Measured waveforms of (a) corrected clock signals and (b) DQS_{EVEN} and DQS_{ODD}.

but the phase controller and the QCC occupy 0.004-mm^2 and 0.071 mm^2, respectively.

Fig. 15 (a) shows the measured waveform of quadrature clocks corrected by QCC. When the input clock with the duty distortion of 10% is applied, the output quadrature clocks show the maximum duty cycle distortion of 5.82% and the maximum phase error of 9.8 degrees without QCC. But when the QCC is enabled, the duty cycle distortion and the phase error are reduced to 0.2% and 1.18°, respectively.

The measured waveform of the $DQS_{EVEN/ODD}$ is shown in Fig. 15 (b). The output DQS signals are distorted by the reflection caused by the impedance mismatch of the pull-up

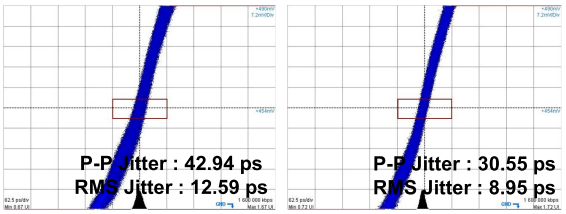

FIGURE 16. Measured jitters of DQS_{EVEN} and DQS_{ODD} for (a) the normal mode and (b) the low switching noise mode.

NMOS transistor with 0.6-V supply for the LVSTL driver. In the low switching noise mode, the phase controller generates EVEN_CLK and ODD_CLK with different quadrature phases. When the phases of EVEN_CLK are 0°, 90°, 180°, and 270° and the interpolated phases of ODD_CLK are 63°, 153°, 243°, and 333°, the phase difference of DQS_{EVEN} and DQS_{ODD} becomes 126°.

The measured jitters of $DQS_{EVEN/ODD}$ are shown in Fig. 16. In the low switching noise injection mode, jitter characteristics are improved by 28.8 % as compared to the normal mode. The peak-to-peak jitter and the RMS jitter of $DQS_{EVEN/ODD}$ are 30.55-ps and 8.95-ps, respectively. The comparison results between conventional QCC and the proposed QCC is shown in Table 1.

VI. CONCLUSION

In this paper, a single-ended transmitter has been proposed to minimize the switching noise injection. The transmitter uses the phase controller to generate two groups of quadrature clocks with different reference phases. In order to spread the peak switching currents of parallel output drivers, the even channel is synchronized with the reference quadrature clocks and the odd channel is synchronized with the interpolated quadrature clocks. Since pulse widths of output DQ and DQS are determined by the quality of quadrature clocks, the QCC has been implemented in the proposed circuit. The proposed QCC uses a dual loop structure to achieve fast correction time, which simultaneously adjust both phase error and duty cycle distortion. The proposed circuit has been fabricated with 180-nm CMOS technology. According to the experimental results, the quadrature clock shows the duty cycle distortion of 0.2% and the phase error of 1.18° with the QCC. In the low switching noise injection mode, the peak-to-peak jitter and the RMS jitter of $DQS_{EVEN/ODD}$ are improved by 28.8% as compared to the normal mode.

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