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New FOM-Based Performance Evaluation of 600/650 V SiC and GaN Semiconductors for Next-Generation EV Drives

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ABSTRACT The drive inverter represents a central component of an electric vehicle (EV) drive train, being responsible for the DC/AC power conversion between the battery and the electrical machine. In this context, novel converter topologies adopting modern 600/650 V wide bandgap (WBG) semiconductor devices will play a crucial role in improving the performance of next-generation drive inverters. In fact, WBG devices theoretically allow to achieve both higher inverter power density and higher conversion efficiency with respect to conventional silicon (Si) IGBT based solutions. Even though silicon carbide (SiC) devices are already well established in the automotive industry, high-voltage gallium nitride (GaN) devices are rapidly entering the market, promising higher theoretical performance but featuring a lower degree of maturity. As a consequence, it is currently not clear which semiconductor technology is most suited for future EV drive inverters. Therefore, this paper aims to address this gap providing a comparative performance evaluation of state-of-the-art SiC and GaN 600/650 V active switches. In particular, a novel figure-of-merit (FOM) representing the minimum theoretical semiconductor losses under hard-switching operation is introduced. Remarkably, this FOM enables a fair and accurate performance comparison among semiconductor devices, allowing to clearly determine the best performing technology for a given set of application-specific conditions. The results of the comparative assessment show that currently available SiC and GaN active switch technologies can outperform each other depending on the semiconductor operating temperature and the converter switching frequency.

INDEX TERMS Wide bandgap (WBG) devices, silicon carbide (SiC), gallium nitride (GaN), high electron mobility transistors (HEMTs), figure-of-merit (FOM), hard-switching, electric vehicles (EVs).

I. INTRODUCTION

As a result of both government policies and consumer demand, the electrification of the transportation sector is rapidly gaining momentum. The automotive industry is increasingly pushing for cheaper, lighter and more efficient electric vehicle (EV) powertrains, leading to considerable technological development challenges.

The drive inverter is a crucial component of an EV traction line, since it performs the AC/DC power conversion between the battery and the electrical machine (cf. Fig. 1). As a consequence, this power electronic converter is subject to great pressure for improvement [1], [2] and

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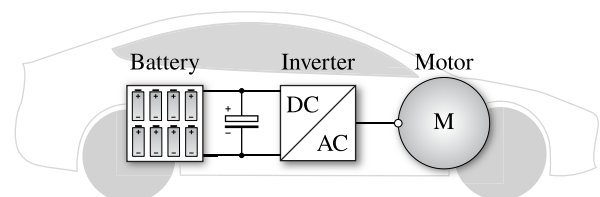


FIGURE 1. Simplified schematic overview of an electric vehicle (EV) drive train, including the battery, the drive inverter and the electric motor.

simultaneously requires high power density (both volumetric and gravimetric), high efficiency over a wide load range (especially at light load [3]), high temperature operation capability, and high switching frequency. In particular, this last requirement is necessary to provide sufficient control margin and limit PWM-induced losses in low-inductance,

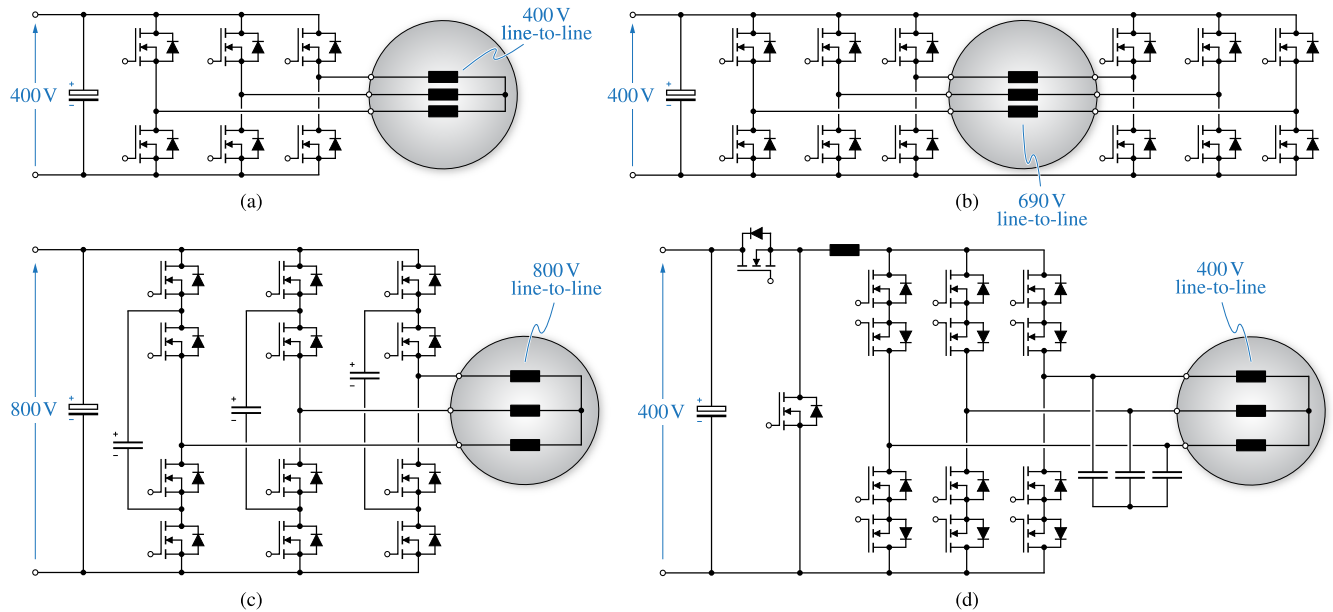


FIGURE 2. Equivalent circuit schematic of various promising converter topologies for next-generation electric vehicle drives exploiting 600/650 V semiconductor devices [9], [10]: (a) two-level inverter (2LI), (b) double bridge inverter (DBI), (c) three-level flying capacitor inverter (3LFCI), (d) current source inverter (CSI).

high-speed machines with several pole pairs typically adopted in automotive [3]–[7]. High switching frequencies also enable the size reduction of the inverter energy storage components (e.g., the DC-link capacitor in voltage-source inverters, the DC-link inductor in current-source inverters) [1] and potentially allow for the addition of a full-sinewave filter between the inverter and the electrical machine (i.e., eliminating the machine losses and wearing induced by PWM and high dv/dt values) [8]–[10].

In the near future, two key enabling technologies will play a significant role in addressing these challenging requirements: novel drive inverter topologies (i.e., different from the conventional two-level voltage-source inverter) [10]–[13] and modern wide bandgap (WBG) semiconductor devices [14]–[18]. Fig. 2 shows some of the most promising candidate inverter topologies for next-generation EV drives [11], [12], either based on a 400 V battery architecture in (a), (b) and (d), or designed for a 800 V battery supply in (c). In this work, all considered drive inverter topologies only adopt semiconductor devices rated at 600/650 V. Both the multi-level approach in (b), (c) and the current-source approach in (d) allow to significantly reduce the high-frequency voltage/current stress on the supplied machine [10]–[13], thus limiting the PWM-induced losses [7]. To best exploit these new inverter architectures, modern 600/650 V silicon carbide (SiC) and gallium nitride (GaN) semiconductor devices are excellent candidates, as they significantly outperform traditional silicon (Si) devices of the same voltage class [14]–[18]. Even though WBG devices currently pose many practical challenges, including PCB layout, gate driving, increased EMI, cable reflections, machine bearing currents and motor insulation stress [3], they feature outstanding properties such as low specific on-state

resistance, fast switching and high-temperature operation capability, which unlock unprecedented performance at the converter level [3]. As a consequence, advanced topologies and WBG devices enable a significant increase of the drive inverter switching frequency, which may reach ≈ 20 –200 kHz and above [19]–[23], depending on the power level, the adopted semiconductor devices and the characteristics of the driven electrical machine.

At present, 650 V SiC devices are well established in the automotive industry, being already employed in EV drive inverters, battery chargers and DC/DC converters. Meanwhile, 600/650 V GaN devices are rapidly entering the market, promising higher theoretical performance that are yet to be proven. Therefore, determining the most suitable semiconductor technology for next-generation EV drive inverters is currently a central research topic for both industry and academia.

In this context, this paper aims to comparatively assess the characteristics and performance of state-of-the-art 600/650 V SiC and GaN semiconductor devices for future EV drives. To this end, a novel and straightforward tool to compare the device-level performance of different semiconductor technologies in hard-switching applications is proposed, featuring simple use and wide applicability (e.g., drive inverters and battery chargers for electrified transportation, grid-connected converters for renewable energy generation, datacenter power supplies, etc.). The main contributions of this work can be summarized in:

- a comprehensive review of the most significant device-level figures-of-merit (FOMs) for benchmarking semiconductor technologies;
- the proposal of a novel device-level semiconductor FOM representing the minimum theoretical

losses of a hard-switching bridge-leg, including the reverse-recovery loss (when present);

- a comparative performance assessment among commercially available 600/650 V SiC and GaN active power switches, highlighting the prominent effects of switching frequency and operating temperature on the semiconductor performance.

This paper is structured as follows. In Section II the material properties of WBG materials are recalled, highlighting their promising performance with respect to Si, and the most established SiC and GaN active switch technologies are described. In Section III a detailed review of existing device-level semiconductor FOMs is performed and a novel hard-switching FOM is proposed. Therefore, a comparative performance evaluation among existing SiC and GaN devices is carried out and the results are discussed. Finally, Section IV summarizes and concludes this work.

II. SiC AND GaN SEMICONDUCTOR TECHNOLOGIES

During the last decades, the development of Si semiconductor technology for power electronic applications has been rapidly approaching the theoretical performance limits of the material itself [14]–[18]. To overcome these limits, new wide-bandgap (WBG) semiconductor materials have been developed and are rapidly replacing Si in several applications, due to their superior performance in terms of blocking voltage, conduction characteristics, switching speed, operating temperature and overall footprint per conducted current [14]–[18]. At present, the most developed and established WBG materials in power electronics are silicon carbide (SiC) and gallium nitride (GaN).

This section aims to provide a background on state-of-the-art WBG technologies, highlighting their main positive and/or negative features and providing an insight on their different level of maturity. In Section II-A the key WBG material properties enabling their superior performance with respect to Si are described. Moreover, a detailed overview of the currently available SiC and GaN active power switch technologies is provided in Section II-B.

A. MATERIAL PROPERTIES

To better understand the reasons behind the superior performance of WBG power devices, a comparison of the key material properties of Si, SiC and GaN is reported in Table 1 and is graphically illustrated in Fig. 3. In particular 4H-SiC is considered herein, as it represents the only SiC polytype practically adopted by manufacturers due to its isotropic structure, as opposed to 6H-SiC [24].

The first key property of a semiconductor material is its energy gap (also referred to as band gap), expressed in eV. WBG materials have a ≈ 3 times larger energy gap with respect to Si, which leads to a higher breakdown electric field and consequently higher device-level breakdown voltages. In particular, the high breakdown field allows to significantly increase the semiconductor doping levels, thus enabling thinner drift regions (i.e., lower on-state resistance and faster

TABLE 1. Key material properties of Si, 4H-SiC and GaN at 25°C and atmospheric pressure [18], [24], [25].

Parameter	Description	Si	SiC	GaN
E_g (eV)	Energy Gap – Band Gap	1.12	3.26	3.39
μ_n (cm ² /Vs)	Electron Mobility	1430	900	2000
v_n (Mcm/s)	Electron Saturation Velocity	10	20	25
E_b (MV/cm)	Breakdown Electric Field	0.3	3.0	3.3
λ_{th} (W/cmK)	Thermal Conductivity	1.5	3.7	1.3
T_m (°C)	Melting Point	1414	2730	2500

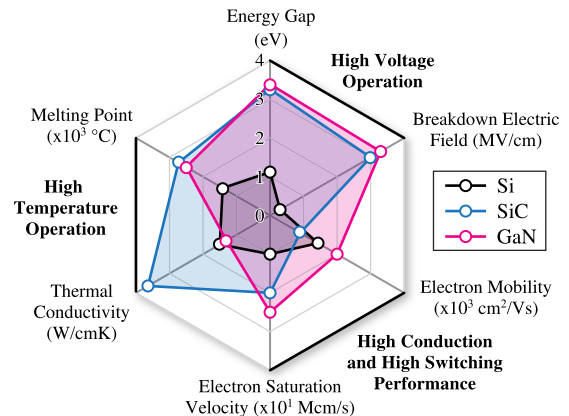


FIGURE 3. Radar chart of the key material properties of Si, 4H-SiC and GaN at 25°C and atmospheric pressure [18], [24], [25].

switching speed) for a constant breakdown voltage target. The large band gap also allows for higher temperature operation, as the thermal energy required for the electrons to jump from the valence band to the conduction band increases. The higher operating temperature primarily unlocks increased device-level current and power densities for a given cooling system performance. While GaN has a slightly lower thermal conductivity with respect to Si, the conductivity of SiC is ≈ 2.5 times higher than Si, allowing for a better heat transfer from the semiconductor device junction to its case and thus enabling even higher current/power densities. Furthermore, the high values of electron saturation velocity and electron mobility of WBG materials lead to faster switching and improved conduction properties, for both unipolar devices (e.g., MOSFETs) and bipolar devices (e.g., diodes). For instance, a higher value of electron saturation velocity directly translates into a faster removal of the charge stored in the depletion region of a diode, thus reducing the reverse-recovery charge and the related losses.

Therefore, it is clear that the material properties of SiC and GaN inherently provide the foundation for semiconductor devices characterized by far superior performance than Si. In particular, this preliminary material-level analysis highlights that GaN features the best properties, theoretically promising best-in-class breakdown voltage, specific on-state resistance and switching speed. Nevertheless, SiC appears a better candidate for high-current density, high-temperature applications.

B. SEMICONDUCTOR POWER SWITCHES

Even though GaN features superior theoretical performance with respect to SiC, both WBG technologies are currently competing in the high-voltage 600/650 V class, due to the lower maturity level of GaN devices and processes [15], [17]. In fact, while GaN is already the undisputed leader in low-voltage applications (i.e., up to ≈ 200 V) [26], and SiC dominates the high-voltage market (i.e., ≥ 1200 V) due to the lack of available GaN devices, at present no clear winner has been identified in the 600/650 V class, where most-recent GaN semiconductors are increasingly challenging SiC devices. In this section, a detailed overview of the currently available 600/650 V WBG semiconductor power switches and their manufacturers is provided.

C. SILICON CARBIDE (SiC) [27]–[30]

The latest achievements in both SiC material growth and processing have led to SiC wafers with larger size and higher quality, enabling a simultaneous cost reduction and production increase of SiC power devices. The following SiC active power switch technologies are commercially available at the time of writing:

- *MOSFET* (normally-off) [31]–[34]; it is the most common SiC semiconductor structure, as it simultaneously provides a normally-off switch with an integrated free-wheeling body-diode. The gate voltage is typically driven between -4 V/ $+15$ V or -5 V/ $+18$ V, depending on the device generation, and the gate threshold voltage lies around $\approx 2 \dots 4$ V. The intrinsic pn body-diode shows a relatively high $\approx 2 \dots 3$ V voltage drop, nevertheless it features lower reverse-recovery charge and losses with respect to Si. Furthermore, 650 V SiC MOSFETs are characterized by a very limited temperature dependence of both on-state resistance and reverse-recovery charge, making them suitable for high-temperature operation. At present, the main manufacturers of 650 V SiC MOSFETs include Wolfspeed [35], Infineon [36], STMicroelectronics [37], ROHM Semiconductor [38] and ON Semiconductor [39]. The MOSFET symbol is reported in Fig. 4(a).
- *JFET* (normally-on) [40]; it is the first SiC device that has been developed and commercialized, due to the simplicity of its structure, the low value of specific on-state resistance and the absence of a gate oxide. SiC JFETs also feature high switching speed and high operating temperature capability, requiring a typical unipolar driving voltage between -18 V/ 0 V (i.e., the gate threshold voltage is ≈ -12 V). Unfortunately, SiC JFETs are normally-on switches (i.e., depletion-mode JFETs) and do not feature an intrinsic reverse-conduction mechanism when turned off, therefore they are unsuited for direct use in power electronic applications. At present, the only manufacturer of 650 V SiC JFETs is UnitedSiC [41]. The JFET symbol is reported in Fig. 4(b).

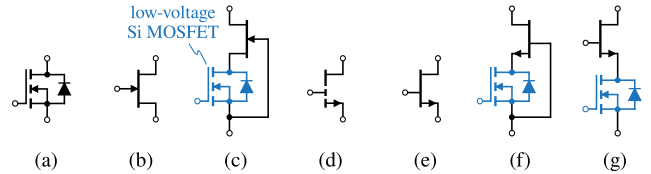


FIGURE 4. Equivalent circuit schematic symbols of (a) SiC MOSFET (normally-off), (b) SiC JFET (normally-on), (c) SiC cascode JFET (normally-off), (d) GaN e-mode HEMT (normally-off), (e) GaN d-mode HEMT (normally-on), (f) GaN cascode d-mode HEMT (normally-off), (g) GaN direct-drive d-mode HEMT.

- *Cascode JFET* (normally-off) [42]; this structure features a depletion-mode SiC JFET in cascode configuration with a low-voltage (i.e., ≈ 30 V) Si MOSFET. This approach allows to leverage the superior performance of the SiC JFET by turning it into a normally-off device with free-wheeling capability by means of a simple Si MOSFET. The combined switch features low on-state resistance, low reverse-recovery charge, low body-diode threshold voltage (i.e., < 1 V) and limited footprint. When the Si MOSFET is turned on, the gate and source of the JFET are shorted and the device conducts. Instead, when the Si MOSFET is turned off, the JFET source voltage rises to the point where its gate threshold voltage is exceeded, turning off the JFET itself. Since the Si MOSFET controls the switching process, the gate of a cascode JFET is typically supplied with a unipolar driving voltage between 0 V/ $+15$ V, being the gate threshold voltage around ≈ 5 V. The main drawbacks of this device include the physical cascode connection of the two semiconductor chips inside the same package, leading to higher stray inductance, and the quasi-uncontrolled switching of the JFET (i.e., due to the indirect control of its gate-source voltage), typically requiring external RC snubbers in hard-switching applications. At present, the only manufacturer of 650 V SiC cascode JFETs is UnitedSiC [41]. The symbol of the cascode JFET is reported in Fig. 4(c).

D. GALLIUM NITRIDE (GaN) [43]–[49]

Even though less mature than SiC, GaN semiconductor technology is progressing rapidly and several high-voltage 600/650 V semiconductor devices have already been commercialized. Notably, most manufacturers still exploit established large-size Si substrates for the GaN epitaxial layer growth, to leverage the existing knowledge/facilities and reduce production costs [44]. This practice however forces GaN semiconductor manufacturers to realize power devices with lateral structure, known as high electron mobility transistors (HEMTs), preventing the realization of vertical power devices with superior theoretical performance. In particular, HEMTs consist of an AlGaN/GaN heterojunction featuring a layer of high-mobility electrons, referred to as two-dimensional electron gas (2DEG), which operates as a current conduction channel between the drain and source terminals of the device modulated by the applied gate voltage

(i.e., electric field). Unfortunately, due to the natural presence of the 2DEG, the simplest HEMT structure operates in depletion-mode and is thus normally-on. At the time of writing, the following GaN active power switch technologies are commercially available:

- *E-mode HEMT* (normally-off) [50]–[56]; although the 2DEG makes the basic HEMT natively depletion-mode (d-mode), the gate structure can be modified to shift the threshold voltage positively and thus realize an enhancement-mode (e-mode) device. The overall behavior is similar to the one of a MOSFET, however the gate voltage is typically driven in a narrower range $\approx 0\text{ V}/+6\text{ V}$ (with a gate threshold voltage of $\approx 1 \dots 2\text{ V}$) and the reverse conduction mechanism is of different nature. In particular, the device structure does not include an intrinsic body-diode, however HEMTs feature a self-commutated reverse conduction (SCRC) mechanism that resembles the operation of a free-wheeling diode. In fact, because of the structural gate-source/gate-drain symmetry, HEMTs are inherently bidirectional, starting to conduct as soon as one between the gate-source and gate-drain voltages exceeds the gate threshold voltage. Therefore, in order for the HEMT to conduct in the reverse direction when driven in the off-state, the negative voltage across the device needs to exceed the sum of the gate threshold voltage and the negative gate bias voltage (if any), yielding a diode-like reverse conduction characteristic with a relatively large voltage drop. Overall, the main advantages of this device are its simple architecture and packaging, due to its normally-off nature, and the zero reverse-recovery charge, due to the absence of a physical (i.e., bipolar) body-diode. Conversely, the main drawbacks of e-mode HEMTs are the large voltage drop in off-state reverse conduction (i.e., during dead-times), the low gate threshold voltage, making the device operation susceptible to ringing, and the limited maximum gate voltage of $\approx 7\text{ V}$, which may require to reduce the driving dynamics in order to avoid the device failure. It is worth noting that the e-mode HEMT category also includes the gate injection transistor (GIT) [57], which trades superior conduction/switching performance (i.e., it is not affected by the well known HEMT dynamic on-state resistance issue [58]) for an increased driving complexity [59]. At present, the main manufacturers of 600/650 V GaN e-mode HEMTs include Panasonic [60], Infineon [36], GaN Systems [61] and Navitas [62]. The symbol of the e-mode HEMT is reported in Fig. 4(d).
- *D-mode HEMT* (normally-on) [63]–[66]; it represents the basic depletion-mode HEMT device, featuring the lowest specific on-state resistance values due to the simplicity of its structure. The gate is typically driven between 0 V, with the device fully in the on-state, and -15 V for complete turn-off, being the gate threshold voltage around $\approx -6 \dots -8\text{ V}$. Same as the e-mode HEMT, this device features intrinsic bidirectional capabilities (i.e., SCRC) and no reverse-recovery charge. At present no manufacturer produces purely d-mode GaN HEMTs, because of their normally-on nature. Nevertheless these devices are utilized in other configurations. The symbol of the d-mode HEMT is reported in Fig. 4(e).
- *Cascode d-mode HEMT* (normally-off) [67]–[69]; the cascode configuration allows to turn a d-mode HEMT into a normally-off device with the simple addition of a low voltage Si MOSFET, connected in the same way as in the cascode SiC JFET structure. This approach allows to combine the superior conduction/switching performance of the d-mode HEMT with the driving simplicity and robustness of a Si MOSFET (i.e., $0\text{ V}/+15\text{ V}$). Moreover, the reverse-conduction mechanism is provided by the MOSFET body-diode, which turns on the HEMT gate as soon as it gets reverse biased, thus leading to a lower off-state reverse voltage drop (i.e., $< 1\text{ V}$) during dead times. Nevertheless, the cascode configuration leads to higher packaging complexity, additional stray inductance in the power loop, non-zero reverse-recovery charge (i.e., due to the Si MOSFET body-diode) and quasi-uncontrolled switching transitions, due to the indirect control of the HEMT gate. At present, the main manufacturers of 600/650 V GaN cascode d-mode HEMTs include Transphorm [70] and Nexperia [71]. The symbol of the cascode d-mode HEMT is reported in Fig. 4(f).
- *Direct-drive d-mode HEMT* [45], [46]; it represents a modification of the cascode structure, aimed at addressing its main drawbacks. In particular, in the direct-drive configuration the source of the low-voltage Si MOSFET is not connected to the gate of the d-mode HEMT. In fact, the Si MOSFET is only exploited as protection device to avoid power-up shoot-through (i.e., requiring an enable gate signal after the converter start-up), while the d-mode HEMT is directly driven at the switching frequency with a negative unipolar voltage (i.e., $-15\text{ V}/0\text{ V}$). If the converter is turned-off and/or the auxiliary supply is missing, the Si MOSFET is automatically turned-off and the complete device behaves similarly to a cascode, turning off safely. The main advantage of this approach resides in the direct exploitation of the switching properties of the d-mode HEMT, avoiding the uncontrolled commutation and the reverse-recovery charge of the conventional cascode implementation. Nevertheless, the series connection of two semiconductor devices still leads to higher device-level parasitic inductance with respect to e-mode HEMTs and, differently from the cascode structure, the off-state reverse voltage drop is determined by the d-mode HEMT (i.e., $\approx 6 \dots 8\text{ V}$). At present, the main manufacturers of 600/650 V GaN direct-drive d-mode HEMTs include Texas Instruments [72] and VisiC Technologies [73]. The symbol of the direct-drive d-mode HEMT is reported in Fig. 4(g).

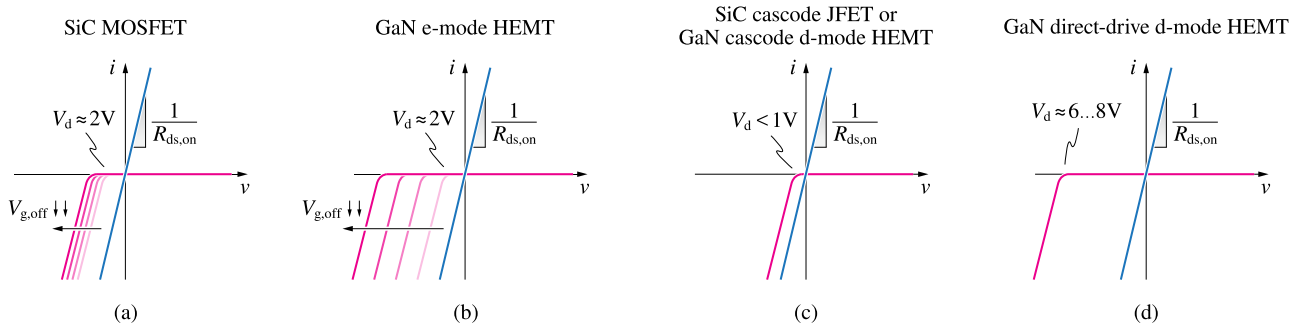


FIGURE 5. Qualitative overview of the conduction characteristics of (a) SiC MOSFET, (b) GaN e-mode HEMT, (c) SiC cascode JFET or GaN cascode d-mode HEMT, (d) GaN direct-drive d-mode HEMT. The blue lines represent the on-state conduction characteristics, while the pink lines represent the off-state conduction characteristics. $R_{ds,on}$ is the on-state resistance, V_d is the diode voltage threshold, $V_{g,off}$ is the turn-off gate voltage (i.e., ≤ 0).

A qualitative overview of the on-state and off-state conduction characteristics of the SiC MOSFET, the SiC cascode JFET, the GaN e-mode HEMT, the GaN cascode e-mode HEMT and the GaN direct-drive d-mode HEMT is provided in Fig. 5.

As a final remark, it is worth highlighting that all currently available GaN devices are characterized by a relatively low maximum junction temperature of 150 °C and feature a large temperature dependence of the on-state resistance (i.e., $\approx 2.5x$ increase between 25 °C and 150 °C), as opposed to SiC devices. These aspects may favor the adoption of SiC in high-temperature environments and/or in applications trading lower conversion efficiency for higher power density, as shown in Section III.

III. FOM-BASED PERFORMANCE EVALUATION

The goal of this section is to propose a novel performance metric to compare different semiconductor devices and technologies under hard-switching operation. In particular, the semiconductor loss mechanisms in a generic two-level bridge-leg are described and expressed analytically in Section III-A, highlighting the most relevant loss contributions in high-voltage fast-switching devices. In Section III-B, a review of existing semiconductor device figures-of-merit (FOMs) is carried out, identifying their major limits and leading to the proposal of a novel hard-switching figure-of-merit (HSFOM) for fast-switching devices in Section III-C (i.e., formally derived in Appendix A). Therefore, a comparative performance evaluation among the currently available 600/650 V SiC and GaN active power switch technologies is performed in Section III-D. For the first time, the semiconductor operating temperature and the converter switching frequency are considered in the analysis, substantially affecting the results of the comparison. Remarkably, the presented comparative performance assessment has broad applicability, since it can be extended to all hard-switching power converter topologies employing identical transistors, as shown in Fig. 6.

A. HALF-BRIDGE HARD-SWITCHING LOSS

The total semiconductor losses P_{semi} generated by the hard-switching two-level bridge-leg illustrated in Fig. 6(a) can

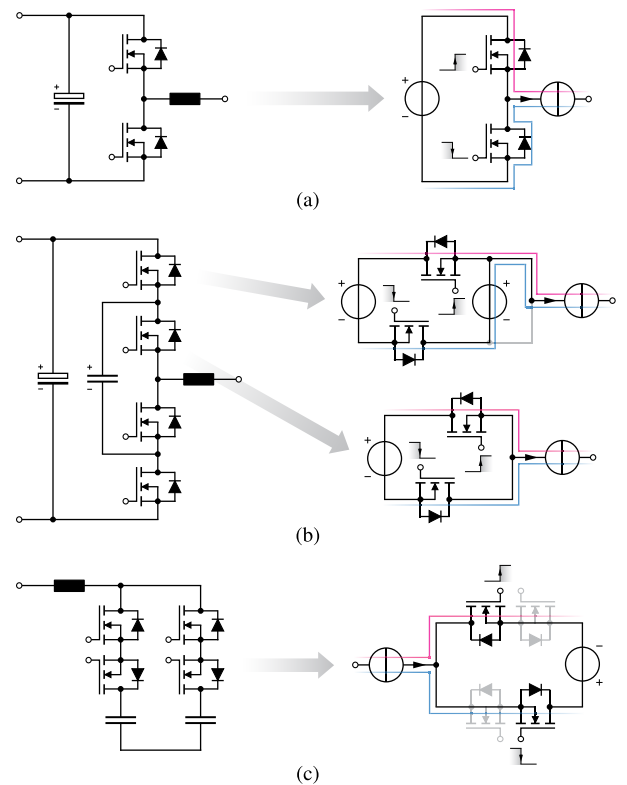


FIGURE 6. Simplified graphical representation of the hard-switching commutations taking place in (a) two-level inverter (2LI) and double bridge inverter (DBI), (b) three-level flying capacitor inverter (3LFCI), (c) current-source inverter (CSI). The blue and pink lines indicate the current path before and after the switching event, respectively. It is observed that the switching events in (b) and (c) can be reconducted to the commutation of the conventional two-level bridge-leg in (a).

be divided into a conduction loss contribution P_{cond} and a switching loss contribution P_{sw} , as

$$P_{semi} = P_{cond} + P_{sw}. \tag{1}$$

1) CONDUCTION LOSS

Due to the resistive nature of both FETs and HEMTs, the bridge-leg conduction losses can be expressed as

$$P_{cond} = R_{ds,on} I_{RMS}^2, \tag{2}$$

where $R_{ds,on}$ is the on-state resistance of the employed transistor and I_{RMS} is the RMS value of the total current flowing through the bridge-leg.

2) SWITCHING LOSS

For reasons of convenience, all those loss mechanisms that are proportional to the switching frequency f_{sw} are here included within the switching loss contribution, namely

$$P_{sw} = P_g + P_{dt} + P_{oss} + P_{rr} + P_{vi}, \quad (3)$$

where P_g is the gate driving loss, P_{dt} is the dead-time reverse conduction loss, P_{oss} is the transistor output capacitance charge/discharge loss, P_{rr} is the reverse-recovery loss and P_{vi} is the loss generated by the overlap of voltage and current (i.e., V - I overlap) during the switching transition.

The gate driving loss can be expressed as

$$P_g = f_{sw} |V_{g,on} - V_{g,off}| Q_g, \quad (4)$$

where $V_{g,on}$ and $V_{g,off}$ are the turn-on and turn-off driving voltages, respectively, and Q_g is the total gate charge. In high-voltage hard-switching applications P_g is typically negligible with respect to the other switching loss components and can thus be neglected (i.e., $P_g \approx 0$).

The dead-time loss arises from the body-diode conduction (or SCRC for HEMTs) during the interval between the turn-off of one device and the successive turn-on of the complementary device. This loss is proportional to the diode voltage drop V_d and the difference between the dead-time t_{dt} and the time to achieve complete zero-voltage switching (ZVS) t_{zvs} [74], as

$$P_{dt} = f_{sw} I_{sw} V_d [t_{dt} - t_{zvs}(I_{sw})], \quad (5)$$

where I_{sw} is the switched current. Being t_{zvs} dependent on the switched current, an adaptive dead-time control strategy can be typically implemented, with the goal of minimizing/eliminating the dead-time loss [75]–[77]. Therefore $P_{dt} \approx 0$ will be considered here.

One major loss mechanism in hard-switching applications is the charging/discharging of the output capacitance C_{oss} of the transistors. The total loss arising from this process can be quantified as [78]

$$P_{oss} = f_{sw} V_{sw} Q_{oss}(V_{sw}), \quad (6)$$

where V_{sw} is the switched voltage (e.g., the DC-link voltage in a two-level inverter) and Q_{oss} is the charge stored in C_{oss} at V_{sw} .

A similar charge-related loss mechanism is the reverse-recovery loss, arising from the dynamics of the stored charge in bipolar diodes. Notably, this mechanism only affects SiC MOSFETs, cascode SiC JFETs and cascode GaN d-mode HEMTs, which all feature intrinsic pn diodes. The reverse-recovery loss can be expressed as a function of the current-dependent reverse-recovery charge Q_{rr} :

$$P_{rr} = f_{sw} V_{sw} Q_{rr}(I_{sw}). \quad (7)$$

Finally, the V - I overlap loss is generated by the simultaneous presence of high voltage and high current across the device channel during the turn-on transition (i.e., the turn-off transition is assumed to be soft/lossless for unipolar

devices) [79]. In particular, the V - I overlap produces two loss contributions inversely proportional to the time derivatives of voltage and current (i.e., dv/dt and di/dt , respectively) as

$$P_{vi} = f_{sw} \left(\frac{1}{2} \frac{V_{sw}^2}{dv/dt} I_{sw} + \frac{1}{2} \frac{I_{sw}^2}{di/dt} V_{sw} \right). \quad (8)$$

Since the aim of this section is to identify a useful performance index to compare different semiconductor devices and technologies, the minimum theoretical switching loss (i.e., unaffected by driving, packaging or parasitic parameters) is of interest here. As the overlap losses progressively decrease with increasing switching speeds, the hypothesis of infinitely fast switching transitions (i.e., $dv/dt \approx \infty$, $di/dt \approx \infty$) allows to identify the lowest theoretical limit of P_{sw} , completely defined by the charge-related loss contributions (i.e., $P_{vi} \approx 0$). Interestingly, this hypothesis also allows to express the diode reverse-recovery charge as a linear function of the switched current, since the condition $di/dt \approx \infty$ forces the complete diode forward-bias injected charge to be swept away as Q_{rr} , as there is no time for the charge recombination process to take place [80]:

$$Q_{rr} \approx \tau_{rr} I_{sw}, \quad (9)$$

where τ_{rr} represents the charge carrier recombination lifetime.

Overall, the minimum theoretical hard-switching loss of a two-level bridge-leg can be expressed as [81]

$$P_{sw} \approx f_{sw} V_{sw} [Q_{oss}(V_{sw}) + Q_{rr}(I_{sw})], \quad (10)$$

which is linear with respect to the switched current.

B. REVIEW OF EXISTING FOMs

Figures-of-merit (FOMs) are defined and exploited to evaluate the properties of materials and technologies, providing common performance indices to carry out comparative assessments. Several FOMs have been defined in the power electronics field over the years, in order to best express the performance of semiconductor technologies at the material-level [82]–[85], device-level [85]–[94] and converter-level [94]. In particular, various device-level FOMs have been introduced to compare the performance of power transistors under hard-switching operation, namely:

- *Baliga high-frequency figure-of-merit* (BHFFOM) [86]; considering the resistive conduction characteristic of FETs and assuming that hard-switching losses are dominated by the charging/discharging of the transistor gate input capacitance C_{iss} , the following FOM is defined:

$$\text{BHFFOM} = \frac{1}{R_{ds,on} C_{iss}}. \quad (11)$$

Notably, (11) is obtained inverting the performance factor introduced in [95]. Since the switching loss assumption is only valid for low-voltage devices (i.e., where $C_{iss} V_g^2 \gg C_{oss} V_{ds}^2$), the BHFFOM loses significance in the present case [96].

- *New high-frequency figure-of-merit* (NHFFOM) [87]; this FOM is defined under the assumption that hard-switching losses are dominated by the charging/discharging of the transistor output capacitance C_{oss} :

$$\text{NHFFOM} = \frac{1}{R_{ds,on} C_{oss}}. \quad (12)$$

This assumption corresponds to $C_{oss} V_{ds}^2 \gg C_{iss} V_g^2$, particularly valid in high-voltage applications [96]. Nevertheless, C_{oss} is defined in [87] as the high-voltage differential value of the non-linear output capacitance, which does not represent the semiconductor capacitive losses [74].

- *Huang device figure-of-merit* (HDFOM) [85]; a different hard-switching loss model with respect to [86] and [87] is considered, assuming that the V - I overlap contribution (i.e., neglected in the previous two FOMs) dominates the total switching losses. In particular, since the gate charge supplied during the Miller-plateau time interval is directly proportional to the voltage transition time (i.e., under the assumption of fixed driving voltage and gate resistance), the following FOM is defined:

$$\text{HDFOM} = \sqrt{R_{ds,on} Q_{gd}}, \quad (13)$$

where Q_{gd} is the gate-drain charge (i.e., stored in C_{gd} or C_{rss} during the voltage transition period). The main deficiency of this FOM is that it neglects the current transition time in the estimation of the hard-switching losses [96].

- *Switching figure-of-merit* (SFOM) [47], [88]; to improve the definition in (13), the current transition time is taken into account by adding another gate charge component to the FOM:

$$\text{SFOM} = R_{ds,on} (Q_{gd} + Q_{gs,i}), \quad (14)$$

where $Q_{gs,i}$ is the charge stored in C_{iss} during the current transition period. However, the direct addition of Q_{gd} and $Q_{gs,i}$ no longer represents the V - I overlap time, as the gate current during the current transition is higher than during the voltage (Miller) transition [90].

- *New switching figure-of-merit* (NSFOM) [90]; this FOM addresses the main drawback of (14), by considering a charge term effectively proportional to the V - I overlap time:

$$\text{NSFOM} = R_{ds,on} (Q_{gd} + k_{gs,i} Q_{gs,i}), \quad (15)$$

where $k_{gs,i}$ is a coefficient dependent on the gate driving voltage, gate resistance, FET transconductance and load current defined in [90]. This is the most complete FOM that expresses the V - I overlap loss, nevertheless $k_{gs,i}$ introduces a large amount of complexity in the FOM definition, since detailed information on both the device and its operating conditions is required. Furthermore, like all FOMs that focus on the V - I overlap, the NSFOM does not represent the minimum theoretical loss limit

of fast-switching devices, as explained in Section III-A. In fact, this FOM considers finite (and loss-dominant) voltage/current derivatives, under the assumption of fixed gate driving conditions (i.e., gate voltage and gate resistance). It is worth noting that no specific name is given to (15) in [90]: the expression NSFOM is proposed here as extension of the SFOM in (14).

- *Device figure-of-merit* (DFOM) [94]; this FOM includes the correct capacitive loss contribution in hard-switching bridge-legs, leveraging the charge-equivalent output capacitance $C_{oss,Q}$ defined in [74], as opposed to the energy-equivalent one used in [91]–[93]:

$$\text{DFOM} = \frac{1}{\sqrt{R_{ds,on} C_{oss,Q}}}. \quad (16)$$

As demonstrated in [94], one major benefit of the DFOM is that it is inversely proportional to the minimum theoretical hard-switching losses in a two-level bridge-leg, therefore it allows a quantitative performance comparison among semiconductor technologies. However, this FOM only holds significance for those semiconductor devices featuring no reverse-recovery charge (e.g., GaN d-mode and e-mode HEMTs), as the Q_{rr} term present in (10) is not taken into account in (16).

It is worth noting that, even though all presented FOMs can be easily evaluated with available datasheet information, their values are chip size (A_{semi}) independent, as the on-state resistance of the device is $\propto 1/A_{semi}$ and all charge/capacitance terms are $\propto A_{semi}$, leaving their product unaffected by the typically unknown semiconductor chip area. Therefore, all FOMs uniquely depend on the chip area specific properties, which are directly related to the considered semiconductor technology.

Interestingly, the most widespread performance index exploited to compare GaN devices with more conventional Si and SiC power switches is the product $R_{ds,on} Q_g$ [16], [17], [43], [48], which resembles the definition of the SFOM in (14) and is practically easier to evaluate from available datasheet information. However, this performance index is ill-defined, since it does not provide a direct relation with the semiconductor hard-switching losses [97], [98], therefore it should not be used to comparatively assess high-voltage fast-switching power devices. The product $R_{ds,on} Q_g$ is in fact better suited for low-voltage and/or soft-switching applications [99], where the switching losses are mostly defined by the gate charge contribution, as for the BHFFOM in (11). Even in this case, however, the gate voltage information should be included to achieve a fair comparative index among different semiconductor technologies (e.g., $R_{ds,on} Q_g |V_{g,on} - V_{g,off}|$).

C. NEW HARD-SWITCHING FOM

Sharing the same goal of the DFOM in (16) of providing a device-level performance index related to the minimum theoretical hard-switching losses in a two-level bridge-leg, a novel comprehensive hard-switching figure-of-merit

(HSFOM) is proposed here:

$$\text{HSFOM} = \frac{1}{\sqrt{R_{\text{ds,on}} Q_{\text{oss}} + k_i \sqrt{f_{\text{sw}} V_{\text{sw}}} \tau_{\text{rr}}}}. \quad (17)$$

This FOM is derived in Appendix A and takes into account both capacitive and reverse-recovery losses, addressing the main limitation of (16). It can be observed that when $k_i \sqrt{f_{\text{sw}} V_{\text{sw}}} \tau_{\text{rr}} \ll \sqrt{R_{\text{ds,on}} Q_{\text{oss}}}$ (e.g., for low values of f_{sw} or when GaN HEMTs with $\tau_{\text{rr}} = 0$ are adopted), the proposed HSFOM reduces to the DFOM in (16) (i.e., where the charge-equivalent capacitance is used instead of Q_{oss}). Remarkably, being the HSFOM inversely proportional to the minimum theoretical amount of hard-switching semiconductor losses (i.e., unaffected by driving, packaging or parasitic parameters), as demonstrated in (22)–(23), it can be exploited to quantitatively and comparatively assess the performance of different semiconductor technologies. Although the HSFOM expression does not account for the unavoidable V - I overlap switching loss component (8), it becomes an increasingly accurate indicator of the total semiconductor losses of a two-level bridge-leg for faster switching transitions (i.e., WBG devices, improved gate driving conditions, reduced parasitics, etc.) and/or for lighter load levels (i.e., high-efficiency applications, such as EV drive inverters).

For a given switched voltage V_{sw} defined by the application, the HSFOM value is mainly influenced by two operating conditions, namely the switching frequency f_{sw} and the semiconductor junction temperature T_j , being $R_{\text{ds,on}}(T_j)$ and $\tau_{\text{rr}}(T_j)$. In particular, higher f_{sw} values negatively affect the HSFOM of those devices characterized by $\tau_{\text{rr}} \neq 0$ (i.e., SiC MOSFETs, SiC cascode JFETs, GaN cascode d-mode HEMTs), inevitably favoring semiconductor technologies featuring zero Q_{rr} in high-frequency applications. Moreover, T_j strongly affects both the semiconductor on-state resistance and the diode reverse-recovery charge (if any). Interestingly, the T_j dependence is rarely considered when comparing FOMs of different semiconductor technologies, even though different operating values of T_j can lead to very different comparative outcomes.

D. SEMICONDUCTOR PERFORMANCE EVALUATION

In this section, a comparative performance assessment among the commercially available SiC and GaN active power switch technologies is carried out. The $R_{\text{ds,on}} Q_{\text{oss}}$ product is firstly considered as comparative index, as it provides a preliminary insight on the achievable conduction and switching performance of high-voltage semiconductor switches, similarly to the DFOM in (16). For a given switched voltage V_{sw} set by the application, the $R_{\text{ds,on}} Q_{\text{oss}}$ product allows to rapidly compare several different technologies, as its value only depends on the operating temperature T_j . Nevertheless, the $R_{\text{ds,on}} Q_{\text{oss}}$ product does not fully represent the semiconductor performance in hard-switching applications, especially for those active power switch technologies featuring non-zero reverse-recovery charge. Therefore, the HSFOM is exploited to address this gap and provide a more

accurate comparative analysis, taking into account both the semiconductor operating temperature T_j and the converter switching frequency f_{sw} . Due to the higher complexity of the HSFOM, two SiC and GaN semiconductor technologies are selected for comparison purposes, highlighting the benefits of using such FOM in a one-to-one comparative assessment.

1) $R_{\text{ds,on}} Q_{\text{oss}}$ COMPARISON

To provide a broad overview of the commercially available 600/650 V SiC and GaN active power switch technologies, all major semiconductor manufacturers are considered herein. In this section, a first performance assessment is carried out by evaluating the chip-size independent $R_{\text{ds,on}} Q_{\text{oss}}$ product, which holds the same meaning as the DFOM in (16) but avoids the introduction of the less-known charge-equivalent output capacitance $C_{\text{oss,Q}}$.

While the $R_{\text{ds,on}}$ value is always provided in the manufacturer's datasheet (i.e., typically for several values of T_j), the Q_{oss} value is normally not given. Nevertheless, Q_{oss} can be obtained by integrating the available non-linear output capacitance C_{oss} as

$$Q_{\text{oss}} = \int_0^{V_{\text{sw}}} C_{\text{oss}}(v) dv, \quad (18)$$

where v is the transistor drain-source voltage and $V_{\text{sw}} = 400$ V is the considered switched voltage. Once the values of $R_{\text{ds,on}}$ and Q_{oss} are available for all semiconductor devices belonging to the same manufacturer, the $R_{\text{ds,on}} Q_{\text{oss}}$ product is averaged among all devices, yielding a performance index uniquely related to the manufacturer's technology. The results of this process are graphically illustrated in Fig. 7 and Fig. 8 for $T_j = 25$ °C and $T_j = 150$ °C, respectively. Furthermore, the same results are numerically reported in Table 2 and Table 3 for SiC and GaN, respectively.

Since a lower $R_{\text{ds,on}} Q_{\text{oss}}$ value corresponds to better semiconductor conduction and switching performance, it is observed from Fig. 7 that SiC devices are outperformed by most GaN devices at 25 °C. In particular, the best semiconductor switches appear to be GaN e-mode HEMTs, among which GaN GITs from Infineon and Panasonic have the lowest $R_{\text{ds,on}} Q_{\text{oss}}$. On the contrary, cascode devices (i.e., SiC cascode JFETs and GaN cascode d-mode HEMTs) show the worst overall performance, even without considering the reverse-recovery charge contribution. Interestingly, GaN direct-drive d-mode HEMTs from VisIC achieve similar performance to GaN e-mode HEMTs, strongly outperforming cascode devices. Fig. 7 shows the comparative results assuming $T_j = 150$ °C. Notably, in this case SiC MOSFETs appear to outperform the majority of GaN devices, highlighting the fundamental need to consider T_j when comparing different semiconductor technologies. In fact, as pointed out in Section II, GaN HEMTs feature a much larger temperature dependence of the on-state resistance with respect to SiC devices. This is best highlighted in Fig. 9, where the $R_{\text{ds,on}} Q_{\text{oss}}$ values for Wolfspeed SiC MOSFETs

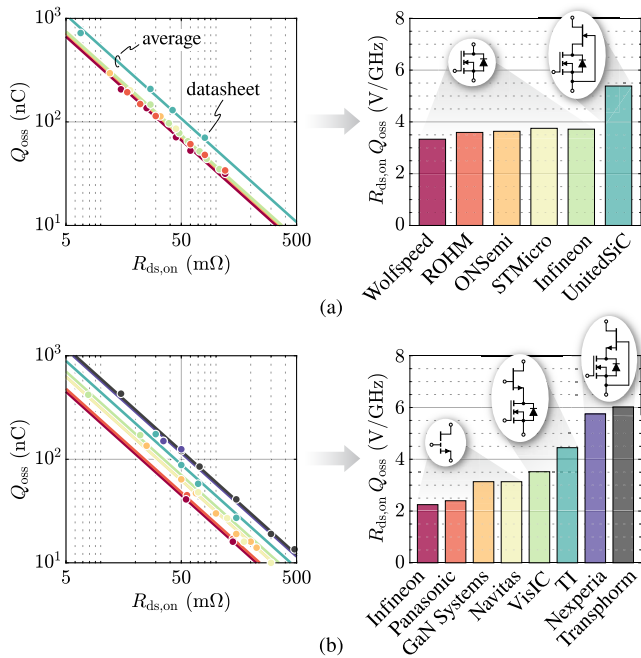


FIGURE 7. Comparative performance evaluation of 600/650 V (a) SiC and (b) GaN semiconductor technologies, based on the $R_{ds,on}Q_{oss}$ product at $V_{sw} = 400$ V and $T_j = 25^\circ\text{C}$. On the left, the dots represent single semiconductor devices and the lines are the $R_{ds,on}Q_{oss} = \text{const}$ curves representing the average performance of each semiconductor technology. Lower lines correspond to lower $R_{ds,on}Q_{oss}$ products and thus better performance.

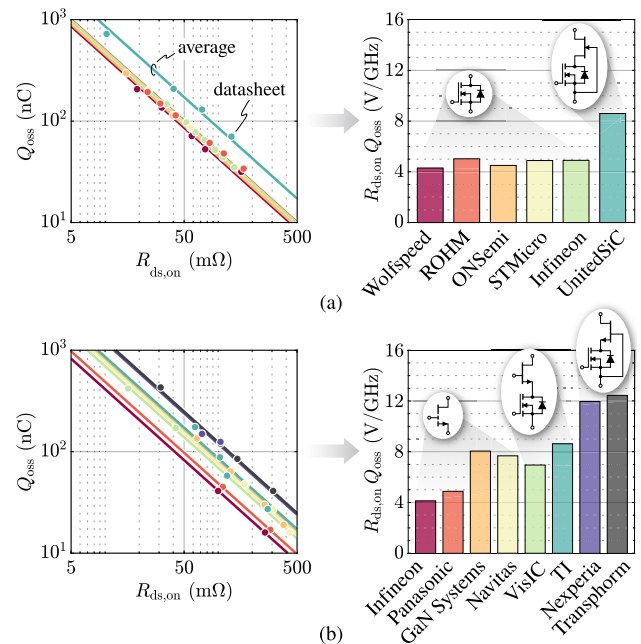


FIGURE 8. Comparative performance evaluation of 600/650 V (a) SiC and (b) GaN semiconductor technologies, based on the $R_{ds,on}Q_{oss}$ product at $V_{sw} = 400$ V and $T_j = 150^\circ\text{C}$. On the left, the dots represent single semiconductor devices and the lines are the $R_{ds,on}Q_{oss} = \text{const}$ curves representing the average performance of each semiconductor technology. Lower lines correspond to lower $R_{ds,on}Q_{oss}$ products and thus better performance.

and GaN Systems GaN HEMTs are shown as functions of the operating temperature.

Even though $R_{ds,on}Q_{oss}$ does not fully characterize the semiconductor performance in hard-switching applications, this preliminary analysis suggests that the operating conditions can substantially affect the performance of a semiconductor device, possibly leading to very different outcomes when different technologies are compared. As a consequence, typical FOM-based semiconductor device comparisons performed at ambient temperature have very limited validity and are thus worth reconsidering (i.e., for different temperature values).

2) HSFOM COMPARISON

A technology performance comparison with broader applicability and higher accuracy can be carried out leveraging the newly introduced HSFOM. To reduce and simplify the analysis, one manufacturer of SiC devices and one manufacturer of GaN devices are selected, performing a one-to-one comparative assessment. In particular, Wolfspeed SiC MOSFETs and GaN Systems GaN HEMTs are the considered semiconductor technologies, strictly because of their higher data availability. For instance, Wolfspeed is the only SiC device manufacturer providing accurate reverse-recovery charge Q_{rr} information at 25°C – 175°C and very high values of di/dt (i.e., ≈ 5000 A/ μs). In fact, other manufacturers typically provide Q_{rr} data only at ambient temperature (i.e., preventing temperature-dependent evaluations) and/or for relatively low values of di/dt (i.e., ≈ 1000 A/ μs), which poorly reflect the assumption made in (9).

To evaluate the charge carrier recombination lifetime τ_{rr} , the real value of $Q_{rr}(I_{sw})$ must be obtained by subtracting Q_{oss} to the Q_{rr} value given in the manufacturer’s datasheet, since the capacitive charge component is typically included in the total reverse-recovery charge. Once $Q_{rr}(I_{sw})$ is available, τ_{rr} is calculated by inverting (9) as $\tau_{rr} = Q_{rr}/I_{sw}$. Same as for the $R_{ds,on}Q_{oss}$ product, the τ_{rr} values of all devices belonging to the same manufacturer are averaged, obtaining a performance index uniquely related to the manufacturer’s technology. The results are reported in Table 2 and Table 3 for SiC and GaN devices, respectively. It is worth noting that, while SiC MOSFETs feature a positive temperature dependence of τ_{rr} , as attested by Wolfspeed devices, SiC cascode JFETs from UnitedSiC are characterized by an opposite behavior.

Once the technology-related values of $R_{ds,on}Q_{oss}$ and τ_{rr} are extracted, the HSFOM can be calculated according to (17) for given values of f_{sw} and T_j . In particular, since $R_{ds,on}Q_{oss}$ and τ_{rr} are available for a limited number of temperature values, linear interpolation is performed for different values of T_j . Therefore, assuming sinusoidal AC operation (i.e., $k_i = \sqrt{2}/\pi$, cf. Appendix A) and constant switched voltage $V_{sw} = 400$ V, the HSFOM is evaluated for both Wolfspeed SiC MOSFETs and GaN Systems GaN HEMTs as function of f_{sw} and T_j . The results are shown in Fig. 10 from two different perspectives.

In Fig. 10(a), the HSFOM values are reported as function of the switching frequency and they are compared at different temperature levels. It is observed that only the HSFOM

TABLE 2. Performance comparison among commercially available 650 V SiC active power switch technologies, considering $V_{sw} = 400$ V and $T_j = 25^\circ\text{C}$, 150°C . The reported results are obtained by averaging the $R_{ds,on}Q_{oss}$ and τ_{rr} values of all devices belonging to the same manufacturer, exploiting the information provided in the respective datasheets. The abbreviation ‘n.a.’ refers to ‘not available.’

Manufacturer	Semiconductor Technology	$R_{ds,on}Q_{oss}$		$\tau_{rr} = Q_{rr}/I_{sw}$	
		$T_j = 25^\circ\text{C}$	$T_j = 150^\circ\text{C}$	$T_j = 25^\circ\text{C}$	$T_j = 150^\circ\text{C}$
Wolfspeed	SiC MOSFET	3.33 V/GHz	4.30 V/GHz	5.95 ns	9.10 ns
ROHM Semiconductor	SiC MOSFET	3.59 V/GHz	5.03 V/GHz	0.83 ns	n.a.
ON Semiconductor	SiC MOSFET	3.64 V/GHz	4.51 V/GHz	≈ 0 ns	n.a.
STMicroelectronics	SiC MOSFET	3.75 V/GHz	4.89 V/GHz	1.06 ns	n.a.
Infineon	SiC MOSFET	3.72 V/GHz	4.91 V/GHz	2.93 ns	n.a.
UnitedSiC	SiC cascode JFET	5.39 V/GHz	8.60 V/GHz	2.16 ns	0.87 ns

TABLE 3. Performance comparison among commercially available 600/650 V GaN active power switch technologies, considering $V_{sw} = 400$ V and $T_j = 25^\circ\text{C}$, 150°C . The reported results are obtained by averaging the $R_{ds,on}Q_{oss}$ and τ_{rr} values of all devices belonging to the same manufacturer, exploiting the information provided in the respective datasheets. The abbreviation ‘n.a.’ refers to ‘not available.’

Manufacturer	Semiconductor Technology	$R_{ds,on}Q_{oss}$		$\tau_{rr} = Q_{rr}/I_{sw}$	
		$T_j = 25^\circ\text{C}$	$T_j = 150^\circ\text{C}$	$T_j = 25^\circ\text{C}$	$T_j = 150^\circ\text{C}$
Infineon	GaN e-mode HEMT (GIT)	2.25 V/GHz	4.13 V/GHz	–	–
Panasonic	GaN e-mode HEMT (GIT)	2.40 V/GHz	4.88 V/GHz	–	–
GaN Systems	GaN e-mode HEMT	3.13 V/GHz	8.05 V/GHz	–	–
Navitas	GaN e-mode HEMT	3.13 V/GHz	7.68 V/GHz	–	–
VisiC Technologies	GaN direct-drive d-mode HEMT	3.52 V/GHz	6.95 V/GHz	–	–
Texas Instruments	GaN direct-drive d-mode HEMT	4.45 V/GHz	8.63 V/GHz	–	–
Nexperia	GaN cascode d-mode HEMT	5.75 V/GHz	11.96 V/GHz	≈ 0 ns	n.a.
Transphorm	GaN cascode d-mode HEMT	6.02 V/GHz	12.44 V/GHz	≈ 0 ns	n.a.

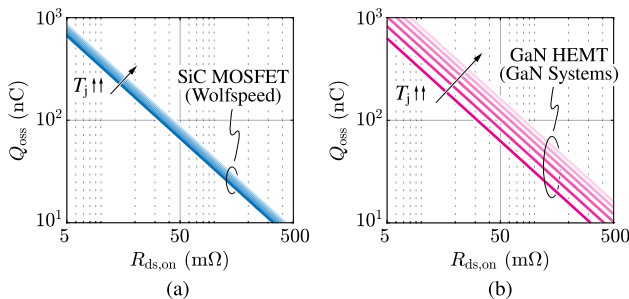


FIGURE 9. Semiconductor junction temperature T_j dependence of the $R_{ds,on}Q_{oss} = \text{const}$ curves for (a) 650 V SiC MOSFETs from Wolfspeed and (b) 650 V GaN e-mode HEMTs from GaN Systems, considering $V_{sw} = 400$ V and $T_j = 25, 50, \dots, 150^\circ\text{C}$.

of SiC MOSFETs is affected by f_{sw} , as GaN HEMTs are characterized by $\tau_{rr} = 0$. Furthermore, the fast performance drop of GaN HEMTs with increasing temperature is clearly seen. Due to these different features, an intersection between the SiC and GaN HSFOM curves is obtained for several temperature values. When this is the case, there exists a boundary switching frequency that separates a low-frequency region where SiC MOSFETs outperform GaN HEMTs from a high-frequency region where the opposite takes place, as highlighted in Fig. 10(a). In the case at hand

this region-delimiting frequency varies within 0...100 kHz, depending on the value of T_j .

Similar considerations can be made by analyzing Fig. 10(b), where the HSFOM values are reported as function of the junction temperature and are compared at different switching frequency levels. It is immediately observed that an intersection point between the HSFOM characteristics of the two semiconductor technologies exists up to a certain f_{sw} value, above which SiC MOSFETs always perform worse than GaN HEMTs. When present, the intersection point between the HSFOM curves defines a boundary temperature that separates a low-temperature region where GaN HEMTs outperform SiC MOSFETs from a high-temperature region where the opposite takes place.

To better highlight the region-delimiting boundary, the HSFOM value of the best performing technology is reported in Fig. 11 as function of both f_{sw} and T_j . The contour plot clearly shows the two separate regions where Wolfspeed SiC MOSFETs outperform GaN Systems GaN HEMTs and viceversa. While GaN HEMTs appear to perform best in low-temperature high-frequency applications, where they can fully leverage their superior switching performance, SiC MOSFETs still prove to be unmatched for lower frequency high-temperature operation, due to their limited $R_{ds,on}(T_j)$ dependence.

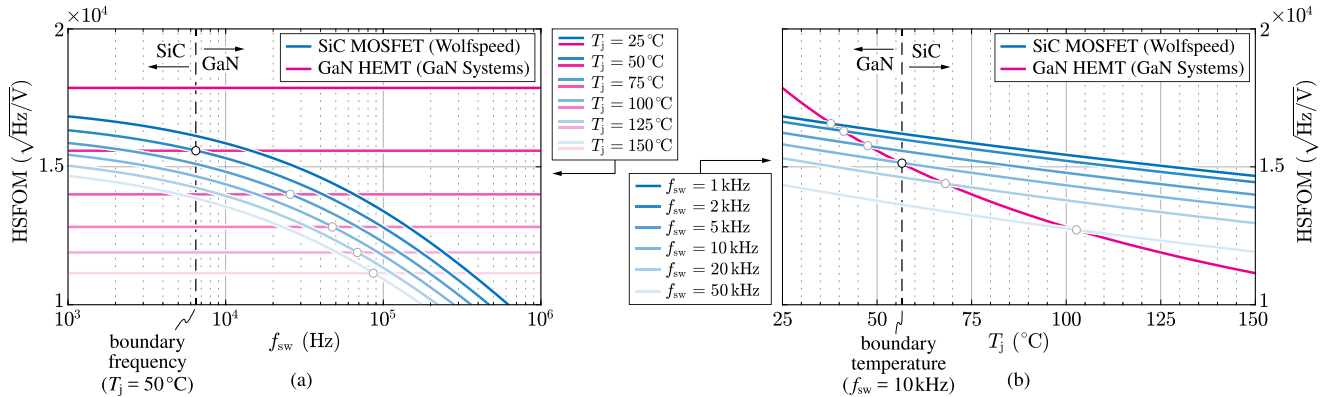


FIGURE 10. Comparative HSFOM-based performance evaluation between Wolfspeed 650 V SiC MOSFETs and GaN Systems 650 V GaN e-mode HEMTs considering $V_{sw} = 400$ V: (a) HSFOM as function of the switching frequency (f_{sw}) for different junction temperature (T_j) values, (b) HSFOM as function of T_j for different f_{sw} values. In (a), the boundary frequency above which GaN devices outperform SiC devices is indicated for $T_j = 50^\circ\text{C}$. In (b), the boundary frequency above which SiC devices outperform GaN devices is indicated for $f_{sw} = 10$ kHz.

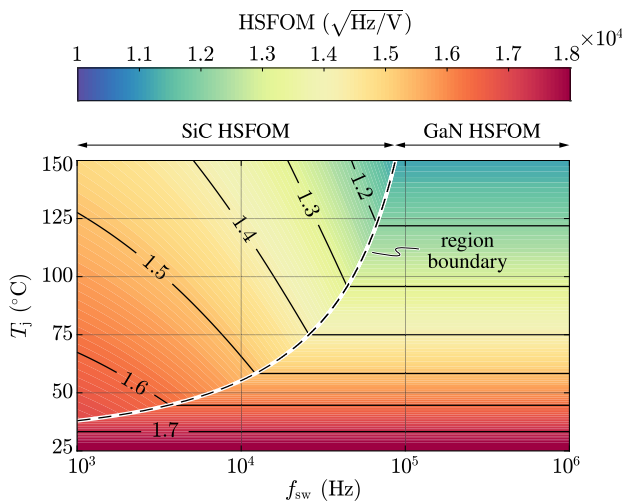


FIGURE 11. HSFOM contour plot of the best performing semiconductor devices between Wolfspeed 650 V SiC MOSFETs and GaN Systems 650 V GaN e-mode HEMTs considering $V_{sw} = 400$ V, $1 \text{ kHz} \leq f_{sw} \leq 1 \text{ MHz}$ and $25^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$. The region-delimiting boundary, indicating the intersection between the two HSFOM surfaces, is highlighted.

IV. CONCLUSION

This paper has presented a comparative performance evaluation of state-of-the-art 600/650 V SiC and GaN semiconductor devices in hard-switching applications, mainly targeting next-generation electric vehicle (EV) drives.

The material properties of wide bandgap (WBG) semiconductor devices, enabling their superior performance with respect to Si, have been recalled and a survey of the most established silicon carbide (SiC) and gallium nitride (GaN) active switch technologies has been presented in detail. In order to derive a performance metric to quantitatively compare such technologies, the semiconductor loss mechanisms in a generic hard-switching two-level bridge-leg have been described. Moreover, a review of existing device-level figures-of-merit (FOMs) has been performed, highlighting their inability to fully represent the performance of high-voltage semiconductor devices under hard-switching operation. Therefore, a novel hard-switching FOM (HSFOM) directly related (i.e., inversely proportional) to the minimum

theoretical loss of semiconductor devices in a bridge-leg configuration has been proposed.

Finally, a comparative assessment of commercially available 600/650 V SiC and GaN active power switch technologies has been carried out. A conventional performance index (i.e., the $R_{ds,on}Q_{oss}$ product) has been first exploited to provide a simplified preliminary overview of the performance of each semiconductor technology. To achieve more accurate results, the newly defined HSFOM has been then employed, assessing the performance of two selected SiC MOSFET and GaN HEMT technologies. For the first time, the semiconductor operating temperature and the converter switching frequency have been considered in the analysis. In particular, it has been demonstrated that these factors strongly affect the results of the comparison, showing that different technologies may outperform each other depending on their operating conditions (i.e., their application).

Remarkably, the newly proposed FOM is widely applicable (e.g., drive inverters and battery chargers for electrified transportation, grid-connected converters for renewable energy generation, datacenter power supplies, etc.) and allows to clearly determine the best performing technology for a given set of application-specific conditions, providing a straightforward tool to assess SiC and GaN active power switches of arbitrary voltage levels (e.g., 100 V, 200 V, 600/650 V, 1200 V, etc.). Furthermore, the results have suggested that 600/650 V GaN HEMTs are currently more suited for low-temperature high-frequency applications, where they can fully leverage their superior switching performance, while 650 V SiC MOSFETs still prove to be unmatched for lower frequency high-temperature operation, due to their limited on-state resistance increase with temperature.

**APPENDIX A
HSFOM DERIVATION**

The proposed FOM is derived from the semiconductor loss expression of a two-level hard-switching bridge-leg, similarly to [94], substituting (2) and (10) into (1):

$$P_{semi} = \frac{r_{ds,on}}{A_{semi}} I_{RMS}^2 + f_{sw} V_{sw} (q_{oss} A_{semi} + \tau_{rr} I_{avg}), \quad (19)$$

where $r_{ds,on} = R_{ds,on} A_{semi}$ and $q_{oss} = Q_{oss}/A_{semi}$ are the semiconductor specific on-state resistance and output capacitance charge, respectively, A_{semi} is the semiconductor chip area of a single transistor and I_{avg} is the average bridge-leg current over a fundamental cycle. It is worth noting that, to properly extend the analysis to the CSI bridge-leg illustrated in Fig. 6(c), an equivalent switch must be considered, featuring two times the on-state resistance, two times the semiconductor chip area and same output capacitance charge as the single transistor.

The optimal semiconductor chip size that minimizes the total bridge-leg losses is found by solving $dP_{semi}/dA_{semi} = 0$, obtaining

$$A_{semi}^* = \frac{I_{RMS}}{\sqrt{f_{sw} V_{sw}}} \sqrt{\frac{r_{ds,on}}{q_{oss}}}, \quad (20)$$

which shows that the reverse-recovery loss, being chip-size independent, does not play a role in defining the optimal semiconductor chip area. Therefore, by substituting (20) into (19), the minimum semiconductor loss expression is derived:

$$P_{semi}^* = 2 I_{RMS} \sqrt{f_{sw} V_{sw} r_{ds,on} q_{oss}} + f_{sw} V_{sw} I_{avg} \tau_{rr}. \quad (21)$$

This expression highlights that the minimum bridge-leg loss depends on both the semiconductor device technology (i.e., $r_{ds,on}$, q_{oss} , τ_{rr}) and the bridge-leg operating conditions (i.e., f_{sw} , V_{sw} , I_{RMS} , I_{avg}).

In order to derive a performance index directly related to the semiconductor hard-switching loss, (21) is rearranged by expressing I_{RMS} and I_{avg} as functions of the bridge-leg peak current I , obtaining:

$$P_{semi}^* \propto \sqrt{r_{ds,on} q_{oss}} + k_i \sqrt{f_{sw} V_{sw}} \tau_{rr} \quad (22)$$

where k_i is a coefficient taking into account the bridge-leg current waveform, namely $k_i = 1/2$ for DC (e.g., buck converter, boost converter, CSI) and $k_i = \sqrt{2}/\pi$ for sinusoidal AC (e.g., VSI topologies). Therefore, a hard-switching figure-of-merit (HSFOM) taking into account both semiconductor technology (i.e., $r_{ds,on}$, q_{oss} , τ_{rr}) and application (i.e., f_{sw} , V_{sw}) can be defined as

$$HSFOM = \frac{1}{\sqrt{r_{ds,on} q_{oss}} + k_i \sqrt{f_{sw} V_{sw}} \tau_{rr}}. \quad (23)$$

It is worth noting that q_{oss} is a non-linear function of V_{sw} and thus depends on the constant DC-link capacitor voltage in VSI topologies and on the variable AC-side capacitor voltage in the CSI. Therefore, to obtain a unique HSFOM value for the CSI, the V_{sw} -dependent terms in (23) (i.e., $\sqrt{q_{oss}}$, $\sqrt{V_{sw}}$) must be averaged within a fundamental AC period, assuming V_{sw} as the rectified line-to-line output voltage. Notably, the averaging of $\sqrt{q_{oss}}$ can be only performed numerically.

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