Printed Circuit Board Implementation of N-Way Power Combiner With Isolated Input Ports

POURIA TOOFANZADEH, SAYYED-HOSSEIN JAVID-HOSSEINI, AND VAHID NAYYERI, (Senior Member, IEEE)

School of Advanced Technologies, Iran University of Science and Technology, Tehran 1684613114, Iran

Corresponding author: Vahid Nayyeri (nayyeri@iust.ac.ir)

ABSTRACT A planar implementation of N-way radial power combiners with isolated input ports is presented. While keeping the design simple, the presented combiner can be manufactured solely using printed circuit board technology, and as a result, has a low weight and manufacturing cost. As proof of concept, two power combiners are designed and built. First, a 6-way combiner working at the center frequency of 3.1 GHz with a fractional bandwidth of around 30% was designed. Our measurements of the fabricated combiner showed an input and output return loss of better than 10 dB in a frequency band of 2.65-3.55 GHz where an isolation of higher than 23 dB, amplitude balance of ± 0.1 dB, and phase balance of ± 1 degree between the input ports were obtained. Then, a simple approach was implemented to widen the frequency band, achieving a fractional bandwidth of 80%. According to our measurements, the wideband combiner has an operating frequency band of 1.35-3.15 GHz, in which an input and output return loss of better than 10 dB with an isolation of higher than 21 dB, amplitude balance of ± 0.15 dB, and phase balance of ± 1 degree were achieved.

I. INTRODUCTION

One of the most diverse devices used in communication systems are power combiners [1]. They can be categorized based on power combining method, combining medium, number of ports, power handling, size, combining stages, isolation, etc. In literature, power combiners are usually first divided into two groups based on the combing method and then into subcategories based on combining medium, etc. [2], [3]. These two main groups are single- and multi-stage combiners. Single-stage combiners inevitably need to be N-way to be capable of combining any given number (to some extend) of ports in a single stage. On the other hand, multi-stage power combiners have a limitation when it comes to the number of ports. Combining a large number of inputs in these combiners requires multiple stages and, as a result, a larger combining network, usually meaning not only more weight, a larger size, and higher costs but also higher loss. From this aspect, single-stage power combiners have a significant advantage over multi-stage combiners since a higher number of ports has little effect on their size, weight, cost, and losses.

The associate editor coordinating the review of this manuscript and approving it for publication was Wenjie Feng.

A weakness of most single-stage N-way combiners (let say N-way combiners for simplicity) is the low isolation between input ports. The low isolation is such a magnificent factor in decision making that system designers usually prefer the higher loss, cost, and size of multi-stage power combiners over the low isolation of N-way combining. As such, an N-way power combiner having isolated inputs would be of much value in system design. Considerable effort has been done to achieve this goal [4]–[13]. It is also notable that, generally speaking, increasing the input ports would increase the isolation [14]; however, depending on geometry, not all ports would have the same isolation from each other, and in case of a failure, some will be affected worse than others.

One of the best-known types of power combiners, which also has good isolation, is the Wilkinson power combiner [15]. Although the two-input port variant of this combiner is the one that is most used and well known, it was originally introduced as an N-way combiner. The reason that the two-input variant is by far more popular than the higher-input variants is the way the isolation resistors are mounted. While the two-way variant of the Wilkinson topology can be implemented in a planar structure, with a higher number of input ports, mounting the resistors on the signal plane is no longer possible.
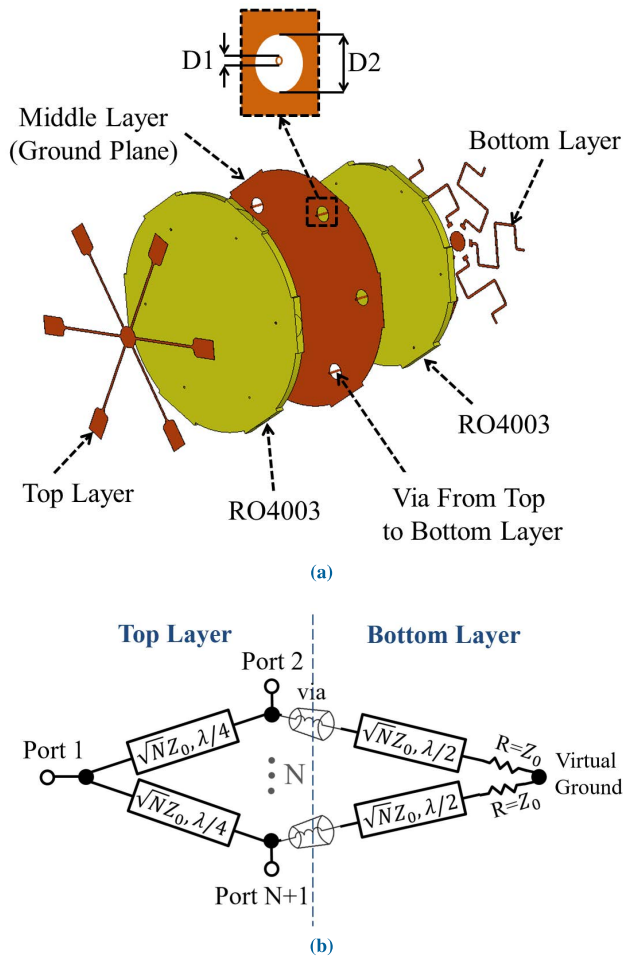
FIGURE 1. Proposed narrowband power combiner: (a) exploded view and (b) schematic. The combiner is implemented on a three-layer PCB (two dielectric substrates and three layers of metalization).

The significance of a planar structure lies in manufacturing. A planar structure can be realized using standard printed circuit board (PCB) technology. PCB will significantly reduce the cost and weight of the design [16]–[19]. In addition, implementing isolation resistors in a PCB is much easier than other media such as waveguides.

In this paper, we present a planar implementation of N-way power combiners. Our proposed designs are based on the Wilkinson topology and so provide high isolation between the inputs. Meantime, using a three-layer PCB and implementing the isolation resistors on the third layer of metalization, the realization of a planar combiner using a multilayer PBC technology becomes possible. As a proof of concept, two combiners were designed and fabricated. The first one is a 6-way narrowband combiner. After explaining the design approach and exploring the results, some tweaks were applied to increase the bandwidth of the combiner for broadband scenarios. The wideband design was validated by manufacturing a 5-way combiner. To close this section, the advancement of this work is to bring the following features for an N-way power combiner together. First, the input ports are highly isolated from each other. Second, owing to the planar structure of the design, it can be realized using
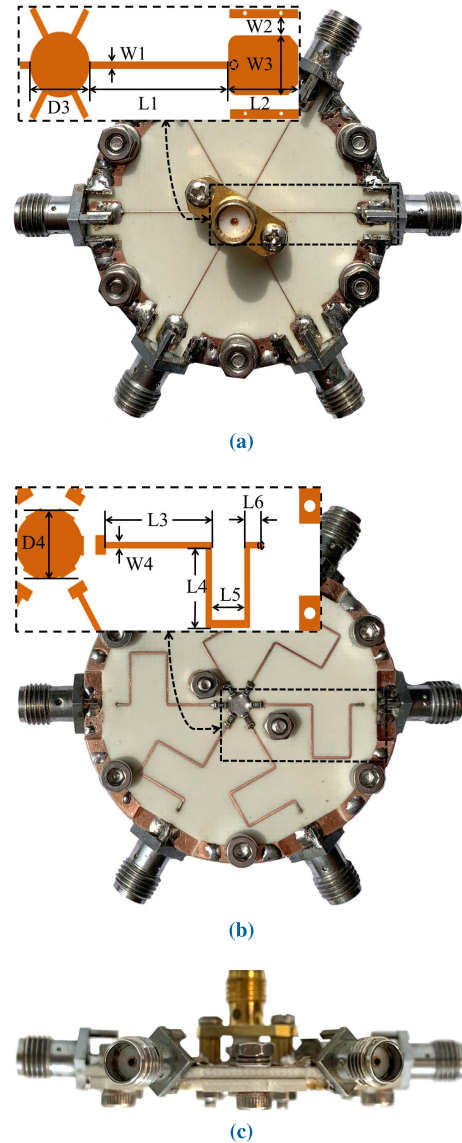

FIGURE 2. Fabricated combiner: (a) top and (b) bottom and (c) side view.

TABLE 1. Value of design parameters indicated in FIGURE 1a and FIGURE 2 (all in mm).

Parameter	Value	Parameter	Value
D1	2.88	W4	0.4
D2	0.4	L1	15.3
D3	4	L2	5
D4	3.66	L3	6.1
W1	0.23	L4	6.8
W2	2	L5	4.68
W3	3.4	L6	1.48

the standard PCB technology. Third, the design method is straightforward with very low complexity. And fourth, the proposed designs provide competitive performance with the state-of-the-art.
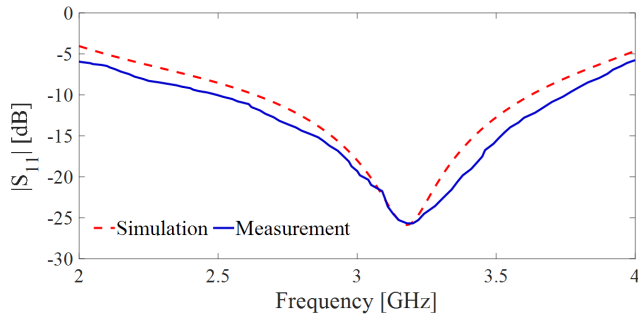
FIGURE 3. Magnitude of measured and simulated reflection coefficient of port 1 (main port).
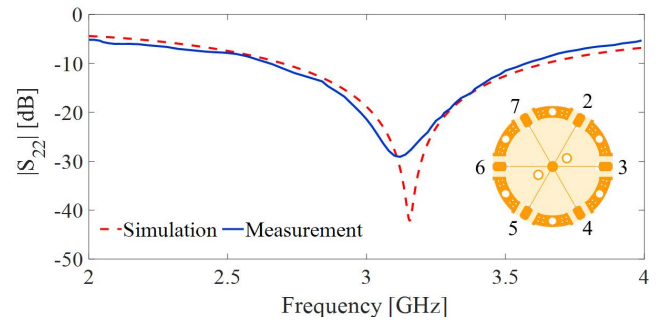

FIGURE 4. Magnitude of measured and simulated reflection coefficient of port 2 (one of the peripheral ports).

II. NARROWBAND DESIGN

A. STRUCTURE AND DESIGN

This combiner is designed on a three-layer PCB, with signal strips on the first (top) and third (bottom) layer of metalization. The second (middle) layer is mostly dedicated to the ground. An exploded view of the combiner is shown in FIGURE 1a. Also, a schematic view of this design can be seen in FIGURE 1b.

1) SIGNAL CIRCUIT

The main signal path of the combiner, from input ports to the output port, is on the top layer of the PCB and is shown in FIGURE 2a. On the periphery of the combiner, input SMA connectors are placed on 50 Ω microstrip transmission lines. These short lines have no role other than providing enough space for soldering the connector. At the end of the 50 Ω line, a quarter-wavelength transmission line moves toward the center of the combiner. At the center, this $\lambda/4$ joins with others from other ports to form the circular pad that, in radial combiners, is sometimes referred to as launcher. The output connector is mounted on this pad.

The characteristic impedance of the quarter-wavelength transformer (QWT) is the geometric mean of the impedance of the input port (i.e., 50 Ω) and the impedance that should appear at the end of the QWT to keep the output port at 50 Ω (i.e., $50 \times N$ Ω), i.e.,

$$Z_q = Z_0 \times \sqrt{N} \tag{1}$$

where N is the number of ways and $Z_0 = 50$ Ω is the reference impedance at the input and output ports. In our case, since $N = 6$, then $Z_q = 122.5$ Ω.

In the side view picture of the fabricated combiner in FIGURE 2c, the means by which the output connector is mounted to the combiner can be seen. The inner conductor of the connector is soldered to the launcher, while two brass spacers connect the outer conductor to the ground (middle) layer. The spacers (having 4 mm length) sit on screw pads connected to the ground plane.

2) ISOLATION CIRCUIT

On the top layer of metalization, at the connection point of the $Z = 122.5$ Ω $\lambda/4$ and 50 Ω lines, there is a via between the top and bottom layer of metalization, passing through the middle layer (the ground plain) without touching it. In case

of unbalanced working conditions, part of the input signal will pass through this via to the bottom layer. On this layer, which can be seen in FIGURE 2b, a microstrip transmission line with a characteristic impedance similar to that of the $\lambda/4$ line but with a length of $\lambda/2$ connects the via to an isolation resistor which is placed at the center of the combiner on the bottom layer. The other end of the resistor is connected to a circular pad, which in the Wilkinson power combiner is known as virtual ground. The resistors have the same impedance as Z_0, which in our case is 50 Ω.

In the original Wilkinson power combiner, the resistors are assumed to be ideal, meaning they are assumed to have an electrical length of zero. However, at higher frequencies, this assumption is inaccurate. On the other hand, resistors should all connect to the virtual ground at the input ports of the combiner, which is the main problem with Wilkinsons of more than two ways. In this work, we remedied both of these issues by adding a $\lambda/2$ line. It allows us to move the resistors to the center of the bottom layer and easily connect them to the virtual ground. By ever so slightly tuning the length of the $\lambda/2$ line, we can absorb the electrical length of the resistor, i.e., the length of the resistor and the line together equals $\lambda/2$.

3) COMPUTER SIMULATION

After the initial design, which included calculating line impedances and lengths of transmission lines for a central frequency of 3.15 GHz and a 60 mil RO4003c substrate, the combiner was modeled and simulated in CST Microwave Studio. While the straightforwardness of the design put the results very close to the desired ones, there were a few objects which needed to be sorted out with optimization. These were the absorption of the length of resistors and the effect of the output connector. The height of the output connector's spacers showed an effect on the result, which was accounted for by slightly varying the impedance of the $\lambda/4$ line by about 10 percent. Absorption of the length of isolation resistors into the $\lambda/2$ line was readily done as well.

Another parameter calculated using computer simulations was the distance of the ground plane from the vias ($(D2 - D1)/2$ in FIGURE 1a). The final dimensions are given in TABLE 1.

B. RESULTS

The combiner was built using standard PCB manufacturing technology and tested using a network analyzer. The mea-
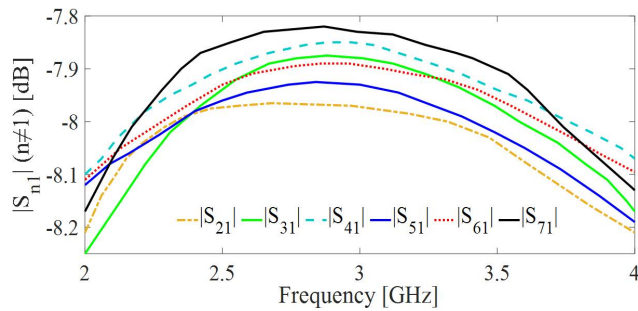
FIGURE 5. Measured magnitude of transmission coefficient of peripheral ports when port 1 (main port) is excited.
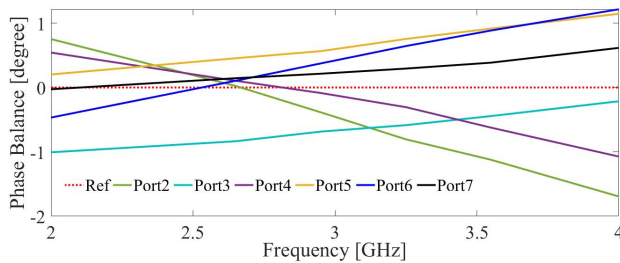

FIGURE 6. Measured phase balance of the combiner. The average of the phase of S(n,1) for all peripheral ports was calculated and set as the reference. The Phase balance of peripheral ports is reported with regard to this reference.

FIGURE 7. Measured isolation of peripheral ports with each other. Notice that due to symmetry, two port pairs have similar isolation where one is omitted from the figure for better clarity.

sured and simulated magnitude of the reflection coefficient of the combine port (port-1) and one of the split (peripheral) ports (port-2) is shown in FIGURE 3 and FIGURE 4, respectively. The inset of FIGURE 4 indicates the ports numbering (the combine port, port-1, is not shown). Good agreement between simulation and measurements is evident in both cases. From these figures, considering -10 dB to be the criteria for an acceptable matching, the achieved operational bandwidth is from 2.65 to 3.55 GHz with a central frequency of 3.1 GHz.

Two important figures of merit of a combiner are its amplitude and phase balances. In FIGURE 5, the magnitude of the measured transmission coefficient of all six peripheral ports when port-1 is excited is plotted. It shows an amplitude balance of less than $\pm$ 0.08 dB. Considering that in an ideal 6-way combiner, the transmission coefficient (theoretical loss) of every peripheral port is -7.78 dB, FIGURE 5 shows that the additional transmission loss of the combiner -caused by mismatch and attenuation- is less than 0.3 dB within the operating bandwidth. The measured phase balance of the combiner is presented in FIGURE 6. The measured phases of all the transmission coefficients $(S(n,1)|n \neq 1)$ were averaged, and the average value was taken as the reference. The difference between the phase of every peripheral port and this reference is reported in FIGURE 6. It is seen that anywhere in the operating bandwidth, the phase balance is better than $\pm$ 1 degree.

The measured isolation between the peripheral ports is presented in FIGURE 7. The transmission coefficient between port-2 and all other peripheral ports was measured. During these measurements, any ports not involved in the
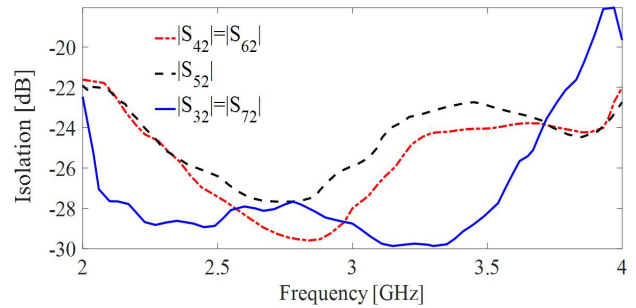
measurement were terminated in a matched load. Due to symmetry, some of the measurements were almost identical and were omitted from the figure for better clarity. It is observed that in the entire bandwidth, isolation was measured to be better than -23 dB.

Finally, a comparison between the presented combiner and state-of-the-art planar N-way power combiners manufactured using PCB technology, albeit those with some degree of isolation, is presented in TABLE 2. From this table, it can be concluded that our design, with low complexity, provides excellent isolation and phase and amplitude balances between the input ports. However, the bandwidth of our design is not competitive with some other works.

III. WIDEBAND DESIGN
The 29 percent of fractional bandwidth achieved in the previous design may not be enough for some applications. Analyzing the results of the narrowband combiner (FIGURE 3, FIGURE 4, and FIGURE 7) shows that the limiting factor of the bandwidth of the first combiner is not its isolation, but the input and output return loss. What affects the bandwidth of the input and output matching is the impedance transformation of the QWT. Generally speaking, a single-section QWT can transform two arbitrary real impedances; however, the impedance transformation has a narrow bandwidth when the two impedances are far away. A classic way of extending the bandwidth is employing multisection transformers allowing gradual change of impedance. This is the tweak we applied to achieve a wideband combiner, as described in the following.

A. STRUCTURE AND DESIGN
FIGURE 8a shows the exploded view of a wideband 5-way combiner. Similar to the previous design, this one is also built on a three-layer PCB with signal strips on the top (first) and bottom (third) layers of metalization, and the middle (second) layer is the ground plane. However, while in the narrowband combiner, the main signal paths (from the input to the output) are entirely in the top layer of metalization, in the proposed wideband design, the signals enter from the input (peripheral) ports on the bottom layer and exit from the output port on the top layer. The isolation resistors are also mounted on the bottom layer as in the previous design.

TABLE 2. Comparison between planar N-way power combiners. Operating bandwidth (BW) is calculated based on input and output return losses of better than 10 dB and insertion loss of lower than 1 dB.

Ref.	BW (fractional) [GHz] (%)	No. of ways	Phase Balance [degree]	Amplitude Balance [dB]	Isolation [dB]	No. of layers	Diameter $[\lambda_0]$[a]	Design Complexity
[6]	3 - 3.5 (15)	14	9.96	0.74	12	2	0.57	Simple
[9]	0.75 - 1.275 (51)[b,c]	4	Not Reported	Not Reported	15[b]	2	0.28	Complex
[10]	2.48 - 2.49 (1)[b,c]	3	0.5[b]	0.1[b]	21[b]	3	0.37	Medium
[11]	0.87 - 1.17 (29)[b,c]	8	Not Reported	Not Reported	21[b]	2	0.4	Simple
[12]	0.7 - 1.26 (57)[b,c]	4	Not Reported	Not Reported	22[b]	3	0.24	Medium
[13]	0.75 - 1.25 (50)	4	6	0.6	15	2	0.9	Simple
[20]	3.5 - 4.5 (25)	16	2	0.4	22[b]	3	1.52	Complex
[21]	5.8 - 8.5 (37)[b]	8	Greater than 15[b]	1.1[b]	16[b]	3	0.95	Complex
Proposed narrowband	2.65 - 3.55 (29)	6	2	0.16	23	3	0.44	Simple
Proposed wideband	1.35 - 3.25 (83)	5	2	0.3	21	3	0.35	Simple

[a] λ_0 is the free-space wavelength at the center of the bandwidth.

[b] The numbers were extracted from the available plots because either they were not directly reported or the criteria applied to extract them were not the same as those in our work.

[c] The combiners exhibit more than 1 dB insertion loss (in addition to the theoretical splitting loss).

1) CIRCUIT

A schematic of this design can be seen in FIGURE 8b. The top and bottom layers of PCB are also shown in FIGURE 9a and FIGURE 9b, respectively. On the bottom layer, at the periphery of the board, each input SMA connector is connected to a short 50 Ohm line. A quarter-wavelength transmission line section, having a characteristic impedance of Z_{q2} in the schematic of FIGURE 8b, connects to this 50 Ohm line and moves toward the center, stopping some distance from it, where it ends at a via connecting the bottom and top layers. One pad of the 100 Ohm isolation resistor is also connected to this via. The other end of the isolation resistor is connected to the virtual ground located in the center of the third layer. It is notable that since the quarter-wavelength transmission lines help to move the resistors to the center of the combiner, the half-wavelength lines are omitted from this design.

At the end of the via, on the other side of the combiner on the top layer, another quarter-wavelength transmission line section, having a characteristic impedance of Z_{q1} in the schematic of FIGURE 8b, starts to move from the via toward the periphery of the combiner, but at about half its length, turns back toward the center, where it joins the other lines from other ports to form the launcher circle. The inner conductor of the output connector is connected to the center of the launcher, and just like the first combiner, the outer connector of the output connector is connected both physically and electrically to the board using brass spacers. The spacers used were 2.5 mm long.

While the length of both QWT sections (on the top and bottom layers) is calculated for the center frequency of design, a decision must be made regarding their characteristic impedances and the value of isolation resistors. The function of these two $\lambda/4$ sections is to bring a 50 Ω impedance at each input port to $N \times 50 = 250\Omega$ at the end of each branch at the output launcher so that we have a 50 Ω impedance at the output port. When designing a multisection impedance transformer, there is a degree of freedom in choosing the characteristic impedances; however, this choice directly impacts the matching response. Theoretically, the multisection Chebyshev matching transformer provides maximum bandwidth at the expense of passband ripple.

Designing a two-section Chebyshev matching transformer converting a 50 Ω to 250 Ω with a maximum allowable reflection coefficient magnitude of 0.15 results in $Z_{q1} = 155$ Ω and $Z_{q2} = 80$ Ω (where Z_{q1} and Z_{q2} are shown in FIGURE 8b) [1]. Alternatively, a schematic model of the combiner (as shown in FIGURE 8b) was created in Keysight ADS and the characteristic impedance of the quarter-wavelength transmission lines (Z_{q1} and Z_{q2}), along with the value of the isolation resistors (R), were optimized for best achievable performance, which resulted in $Z_{q1} = 143$ Ω, $Z_{q2} = 74$ Ω, and $R = 100$ Ω. A good agreement between the results of the Chebyshev matching transformer design and the circuit optimization in ADS is observed. Considering that the ADS simulation is more comprehensive than Chebyshev transformer analysis with regards to the effects of the whole combiner circuit, the small drift of impedances is acceptable.

2) COMPUTER SIMULATION

With the three mentioned parameters at hand, the length and width of the lines were calculated for a 32 mil RO4003c substrate. The 3D computer model was created in CST Microwave Studio, and full-wave simulations were performed. Naturally, due to the parasitic effects of the
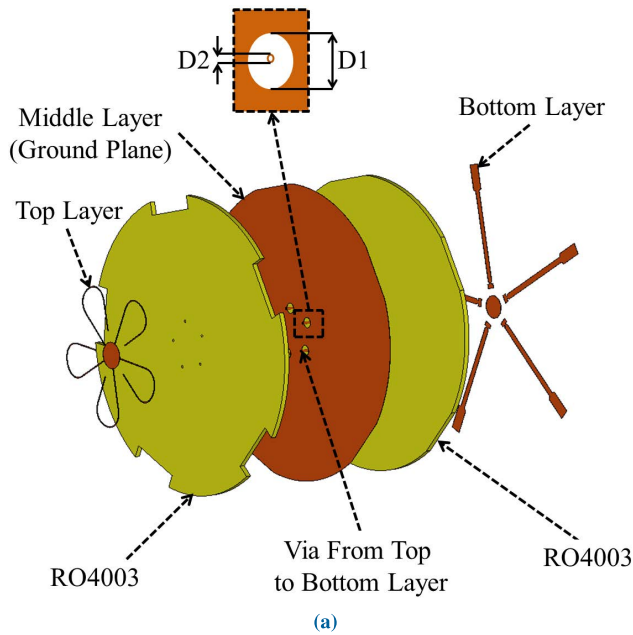
FIGURE 8. Proposed wideband power combiner: (a) exploded view and (b) schematic. The combiner is implemented on a three-layer PCB.

FIGURE 9. Fabricated wideband combiner: (a) top and (b) bottom view.

TABLE 3. Value of design parameters indicated in FIGURE 8, FIGURE 9a and FIGURE 9b (all in mm).

Parameter	Value	Parameter	Value
D1	1.6	W3	1.81
D2	0.41	L1	8.2
D3	4	L2	9.8
D4	3.52	L3	4.4
W1	0.15	L4	14.81
W2	0.88	L5	4.1

vias and output connector and electrical length of the resistors, the initial results needed some tuning. However, after some iterations, the results were satisfactory. The final parameter values of the combiner are reported in TABLE 3. To summarize, the wideband combiner is designed in the following steps. First, we choose the number of ports; second, we calculate the length of quarter wavelength transmission lines based on the substrate and center frequency. In the third step, the characteristic impedance of both quarter wavelength transmission lines and resistance of the isolation resistors are calculated/optimized for the desired bandwidth.

It is worth mentioning that a few factors limit the maximum number of ways in both designs. As the number of ways increases, the impedance of the quarter wavelength transmission lines increases with it. However, in practice,
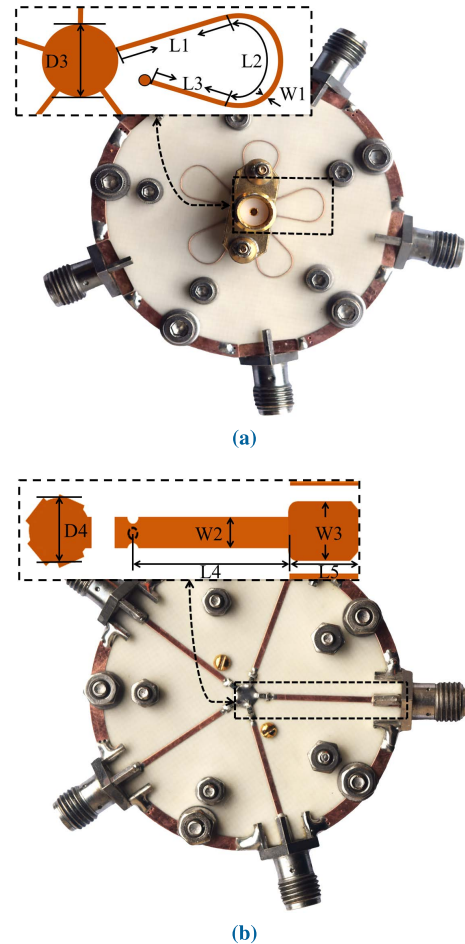
there is a limitation on how high the impedance of a transmission line can be to be fabricable. Regarding the wideband design, fitting the desired shape on the PCB is also a limiting factor due to the curved lines. The legs of the central SMA connector might get in the way of the transmission lines, and there is a certain limit on how much they can be evaded by meandering the line. Of course, the designer can always play with the material a little to find working solutions to these limitations to a certain degree. All things considered, in the low GHz regime, a maximum of around ten ways seems to be the limit of our proposed designs.
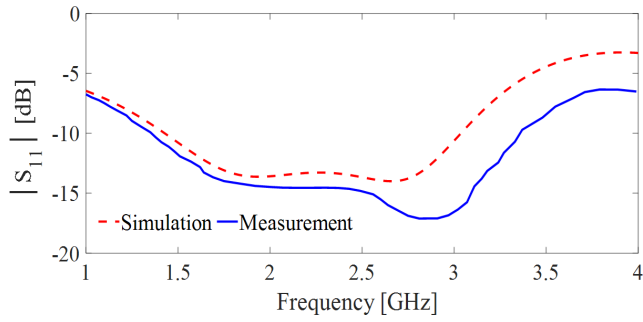
FIGURE 10. Magnitude of measured and simulated reflection coefficient of port 1 (main port).
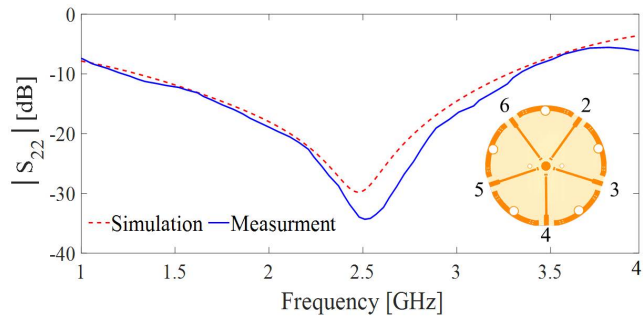

FIGURE 11. Magnitude of measured and simulated reflection coefficient of one of peripheral ports (port 2).

FIGURE 12. Measured magnitude of transmission coefficient of peripheral ports when port 1 (main port) is excited.

FIGURE 13. Measured phase balance of the combiner. The average of the phase of S(n,1) for all peripheral ports was calculated and set as the reference. The Phase balance of peripheral ports is reported with regard to this reference.

FIGURE 14. Measured isolation of peripheral ports with each other. Due to symmetry, the isolation between some port pairs is similar where only one is shown for better clarity of the figure.

B. RESULTS

The wideband combiner was tested using a vector network analyzer. The magnitude of the reflection coefficient of the main port (port-1) while all other ports were terminated in 50 Ω loads is shown in FIGURE 10. The magnitude of the reflection coefficient of one of the peripheral ports (port-2) can be seen in FIGURE 11, where the inset of the figure indicates the port numbering. Both the measured results compare well with the full-wave simulations. The increased bandwidth of both measurements is evident compared to FIGURE 3 and FIGURE 4. Assuming an input/output reflection coefficient of -10 dB to be acceptable, the operating frequency band of the combiner would be from 1.35 GHz to 3.35 GHz, corresponding to about 85% fractional bandwidth.

The amplitude of the transmission coefficients of the combiner when port-1 is excited is shown in FIGURE 12. It can be seen that within the -10 dB reflection bandwidth (i.e., from 1.35 GHz to 3.35 GHz), every $|S_{n1}|$ (transmission coefficient between port-1 and a peripheral port) stays above -8.5 dB. It is worth mentioning that for an ideal 5-way combiner, the theoretical transmission loss is 7 dB. However, this 1.5 additional transmission loss might be unacceptable in some applications. If we consider 0.7 dB (or 1 dB) of additional transmission loss to be acceptable, then the operating bandwidth of the combiner becomes from 1.35 GHz to 3.15 GHz (or 3.25 GHz), i.e., 80% (or 83%) of fractional bandwidth. Within this bandwidth (1.35 GHz to 3.25 GHz), the amplitude balance between $|S_{n1}|$ is better than ±0.15 dB, as shown in FIGURE 12.
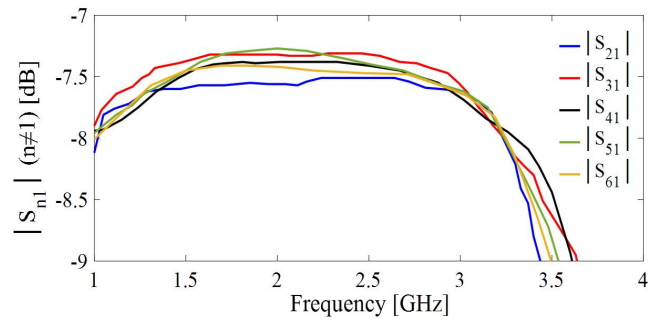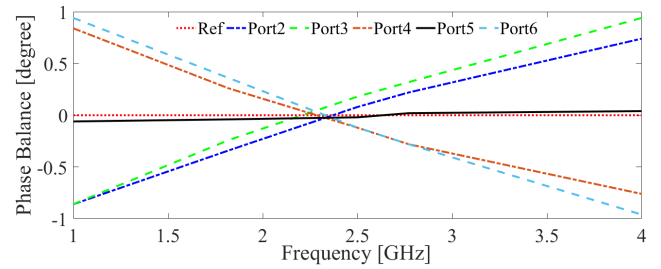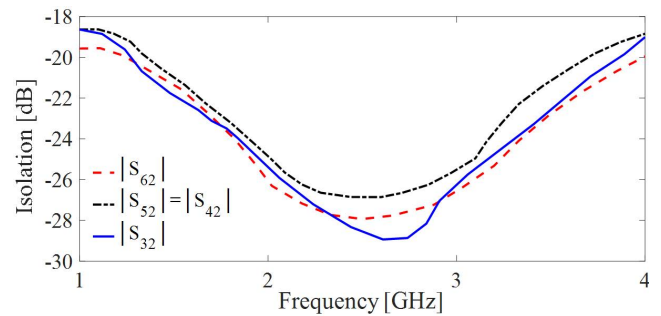
In FIGURE 13, the phase balance of the combiner is presented. Just like the first design, the figure shows the difference between the measured phase of every transmission coefficient $(S(n, 1)|n \neq 1)$ and a reference which is their average. It can be seen that the phase balance varies between ±0.8 degrees.

In FIGURE 14, the measured isolation between port-2 and other peripheral ports is shown. It can be observed that at worst case, the isolation is better than 21 dB.

Finally, from TABLE 2 which provides a comparison between state-of-the-art planar N-way combiners, it can be seen that the presented wideband combiner not only provides the widest bandwidth among all the works listed in the table but also keeps the great features of the narrowband combiner presented in the previous section, such as the simplicity of the design and excellent phase and amplitude balances and isolation between the input ports.

IV. CONCLUSION

A straightforward approach based on Wilkinson topology for designing N-way radial power combiners having high isolation between their input ports was presented. The proposed designs are planar and fully implemented using standard PCB manufacturing technology, which results in inexpensive, light and small combiners compared to waveguide products requiring machine work.

Two combiners were designed and fabricated, a narrow-band and wideband. The narrowband combiner showed an operational bandwidth of 2.65-3.55 GHz, minimum input and output return loss of 10 dB, amplitude balance of ± 0.1 dB, phase balance of ± 1 degrees, isolation of better than 23 dB, and additional transmission loss of less than 0.3 dB. The wideband combiner exhibited an input and output return loss of better than 10 dB, amplitude balance of ± 0.15 dB, phase balance of ± 1 degrees, isolation of higher than 21 dB, and additional transmission loss of less than 0.7 dB, in a fractional bandwidth of 80%, from 1.35 GHz to 3.15 GHz.

ACKNOWLEDGMENT

REFERENCES

[1] D. M. Pozar, "Power dividers and directional couplers," in *Microwave Engineering* 4th ed. Hoboken, NJ, USA: Wiley, 2011.

[2] K. J. Russell, "Microwave power combining techniques," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-27, no. 5, pp. 472–478, May 1979.

[3] J. Schellenberg, "The evolution of power combining techniques: From the 60s to today," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2015, pp. 1–4.

[4] A. E. Fathy, S.-W. Lee, and D. Kalokitis, "A simplified design approach for radial power combiners," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 1, pp. 247–255, Jan. 2006.

[5] Q. X. Chu, D. Y. Mo, and Q. S. Wu, "An isolated radial power divider via circular waveguide TE_{01} mode transducer," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 3988–3996, Dec. 2015.

[6] Y. J. Chen and R. B. Wu, "A wide-band multiport planar power-divider design using matched sectorial components in radial arrangement," *IEEE Trans. Microw. Theory Techn.*, vol. 46, no. 8, pp. 1072–1078, Aug. 1998.

[7] S.-Y. Yin, J.-L. Li, and S.-S. Gao, "Compact dual-band five-way Wilkinson power divider," *Electron. Lett.*, vol. 53, no. 13, pp. 866–868, Jun. 2017.

[8] Y. J. Chen, Y. H. Pang, and R. B. Ruey-Beei, "The use of symmetry to simplify the mixed-potential integral-equation method with application to N-way radial power dividers/combiners with isolation resistors," *IEEE Trans. Microw. Theory Techn.*, vol. 47, no. 9, pp. 1609–1616, Sep. 1999.

[9] T. Yu, J.-H. Tsai, and Y. Chang, "A radial four-way power divider with the proposed isolation network," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 3, pp. 194–196, Mar. 2018.

[10] S. Chen, W.-C. Lee, and T.-L. Wu, "A resistor-free N-way power divider with simultaneous output matching and isolation," *IEEE Microw. Wireless Compon. Lett.*, vol. 29, no. 8, pp. 523–525, Aug. 2019.

[11] T. Yu, B.-S. Lin, and Y. Chang, "Eight-way radial power splitter including ring-shape isolation network," *Electron. Lett.*, vol. 53, no. 24, pp. 1587–1589, Nov. 2017.

[12] C.-W. Tang and Z.-H. Huang, "Analytical design of the radial power divider with wide isolation bandwidths," in *Proc. 49th Eur. Microw. Conf. (EuMC)*, Oct. 2019, pp. 117–120.

[13] Y. Liu, S. Sun, and L. Zhu, "Design of N-way wideband filtering power dividers with good port–port isolation," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 7, pp. 3298–3306, Jul. 2021.

[14] H. Kagan, "N-way power divider (correspondence)," *IRE Trans. Microw. Theory Techn.*, vol. 9, no. 2, pp. 198–199, Mar. 1961.

[15] E. J. Wilkinson, "An N-way hybrid power divider," *IRE Trans. Microw. Theory Techn.*, vol. 8, no. 1, pp. 116–118, Jan. 1960.

[16] K. J. Abouzahra and K. C. Gupta, "Multiple-port power divider/combiner circuits using circular microstrip disk configurations," *IEEE Trans. Microw. Theory Techn.*, vol. 35, no. 12, pp. 1269–1302, Dec. 1987.

[17] M. D. Abouzahra and K. C. Gupta, "Multiport power divider-combiner circuits using circular-sector-shaped planar components," *IEEE Trans. Microw. Theory Techn.*, vol. 36, no. 12, pp. 1747–1751, Dec. 1988.

[18] S.-H. Javid-Hosseini and V. Nayyeri, "Printed circuit board implementation of wideband radial power combiner," *IEEE Access*, vol. 7, pp. 83536–83542, 2019.

[19] B. Zhang, K. Song, X. Wang, Y. Yan, Y. Zhou, and Y. Fan, "Compact quasi-planar four-way power divider with wide isolation bandwidth," *IEEE Access*, vol. 7, pp. 77915–77922, 2019.

[20] H. J. D. Toit and D. I. L. de Villiers, "A fully isolated N-way radial power combiner," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 2531–2538, Jul. 2020.

[21] K. Song, Y. Chen, T. Kong, and Y. Fan, "Broadband eight-way substrate integrated waveguide radial power divider/combiner with high-isolation," *IEEE Access*, vol. 8, pp. 69268–69272, 2020.

POURIA TOOFANZADEH was born in Ahwaz, Iran. He received the B.Sc. degree in electrical engineering from Shiraz University, Shiraz, Iran, in 2016, and the M.Sc. degree in satellite engineering from the Iran University of Science and Technology (IUST), Tehran, Iran, in 2021.

His research interests include microwave circuits and antennas.

SAYYED-HOSSEIN JAVID-HOSSEINI was born in Tehran, Iran. He received the B.Sc. degree in electrical engineering from the K. N. Toosi University of Technology, Tehran, in 2014, and the M.Sc. degree in satellite engineering from the Iran University of Science and Technology (IUST), Tehran, in 2018, where he is currently pursuing the Ph.D. degree in satellite engineering.

Since 2015, he has been an antenna and RF-circuit designer with ACECR-Nasir Branch, Tehran. His research interests include antennas and microwave circuits both passive and active.

VAHID NAYYERI (Senior Member, IEEE) was born in Tehran, Iran, in 1983. He received the B.Sc. degree from the Iran University of Science and Technology (IUST), Tehran, in 2006, the M.Sc. degree from the University of Tehran, Tehran, in 2008, and the Ph.D. degree from IUST in 2013, all in electrical engineering.

From 2007 to 2013, he was a Research Assistant at IUST and a Visiting Scholar at the University of Waterloo, ON, Canada. In 2013, he joined at the Faculty of IUST, where he is currently an Associate Professor, the Head of the Department of Satellite Engineering, and the Co-Director of the Antenna and Microwave Research Laboratory. In 2019, he was a Visiting Professor at the University of Waterloo. He has authored and coauthored one book (in Persian) and over 90 technical papers. His research interests include applied and computational electromagnetics and microwave circuits.

Dr. Nayyeri received the Best Ph.D. Thesis Award from the IEEE Iran Section, in 2014. He was the General Co-Chair of the "1st National Conference on Space Technology and Its Applications" Tehran, in 2019. He was the Co-Guest Editor of *Sensors*, the Special Issues on Metamaterials for Near-Field Microwaves Sensing, in 2019, and State-of-the-Art Technologies in Microwave Sensors, in 2020. Currently, he is serving as an Associate Editor for the IEEE TRANSACTIONS ON MICROWAVES THEORY TECHNIQUES and the *IET Microwaves, Antennas and Propagation* and as a Co-Guest Editor of the *Sensors*, the Special Issue on State-of-the-Art Technologies in Microwave Sensors. He is the Chair of the Membership Development Committee, IEEE Iran Section, and a Steering Committee Member of the Electromagnetics and Photonics Chapter.

• • •