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Active-Matrix Pixelated-LED Control System for Automotive Headlamps

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ABSTRACT This paper presents a driving circuitry system for high-resolution, pixelated-LED automotive headlamps. The system consists of an array of pixel drivers, and a row/column driver suitable for an active-matrix array configuration with the individual dimming control capabilities on each pixelated-LED. An asynchronous serial communication protocol is introduced to minimize the number of data transmission interface signals between the row/column driver and pixel drivers. The proposed pixel driver is designed to drive each pixelated-LED with constant current and pulse width modulation (PWM). It contains a memory cell for dimming data, and a sample-and-hold driver stage to minimize the static power consumption of the pixel driver. The proposed system has been fabricated by using a 0.18-μm CMOS process. The test chip includes a 2 $\times$ 16 pixel array with an embedded row/column driver. The functional operation has been verified with an 8 $\times$ 16 LED array system prototype.

INDEX TERMS Active-matrix, pixelated-LED control, automotive headlamps, advanced driver assistance system (ADAS), high-resolution, pulse width modulation (PWM).

I. INTRODUCTION

The latest passenger vehicles have adopted advanced driver assistance systems (ADAS). Automotive headlamp modules are needed to support drivers with various new functions such as light distribution control or symbol projection based on road and traffic conditions [1]–[4]. With light distribution control, the automotive headlamp system controls a specific area of the headlight to reduce glare for oncoming vehicles or pedestrians on the road. The light of the headlamp is also used as a projector in order to show text messages or safety signs to driver or pedestrians. To meet these new trends, an automotive headlamp system must support higher resolutions along with individually controllable light source.

LED-based headlamps are widely adopted thanks to their better efficiency, longer lifetime, and flexible form factor [5]. At the same time, the number of LEDs composing a headlamp increases continuously to achieve better resolution. In order to drive the LEDs of the headlamp, a dc-dc converter has been commonly used as a constant current source. Also, the architecture based on a string of LEDs with multiple channels is often used as shown in Fig. 1(a) [6]–[10].

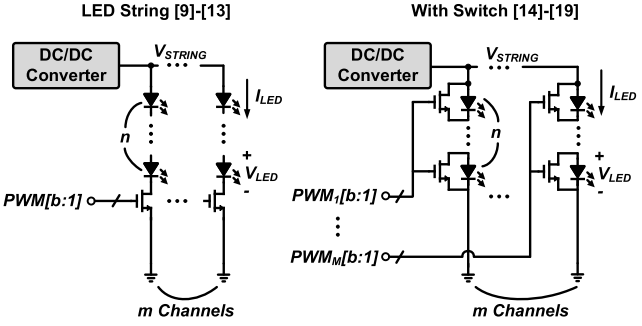

FIGURE 1. Previous LED-based headlamps; (a) LED string and (b) with switch.

However, a string-based LED driving solution has some limitations: First, the number of LEDs in a string is limited. As shown in Fig. 1(a), V_{STRING} would be equal to $n \times V_{\mathrm{LED}}$ where V_{STRING} is the output voltage of the dc-dc converter, n is the number of LEDs used in a string, and V_{LED} is the

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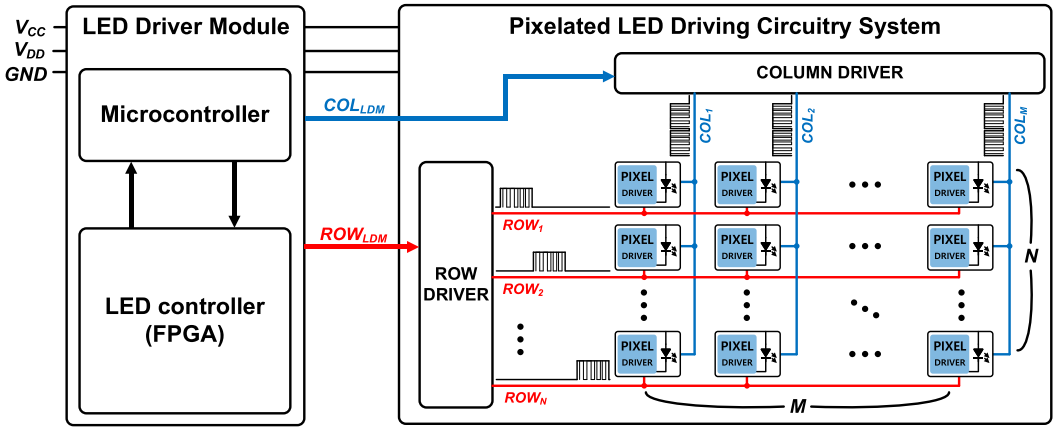

FIGURE 2. Proposed active-matrix pixelated-LED control system.

forward voltage of the LED. For a higher number of n, the dc-dc converter would have to provide an excessively high output voltage for V_{STRING}. Second, this scheme controls the LEDs only by the group of LEDs in each string. In a commercial product [8], a dc-dc converter drives 4 channels with V_{STRING} of 30 V for 16 LEDs in one channel. To solve the problem, a switch or a controller should be added across each LED to individually control the LEDs in a string, as shown in Fig. 1(b) [11]–[16]. In a commercial product [16], it controls 12 LEDs individually with V_{STRING} of 60 V. As the number of channels increases in order to achieve a higher resolution, an external switch must be added for each LED which requires many interface lines. Also, it is not possible to control different light intensity for each LED. In summary, the existing architecture with a dc-dc converter is not suitable for achieving higher resolutions.

In this paper, a pixelated-LED control system is presented. It is based on an active-matrix array configuration[17]–[25]. It achieves individual dimming control on each pixelated-LED while meeting demand for ever-increasing resolution of automotive headlamp modules. The system also supports a Pulse Width Modulation (PWM) driving scheme for each pixelated-LED with a constant current source. For an active-matrix array configuration, the pixel driver is designed with the proposed function blocks. An asynchronous serial communication protocol between the pixel driver and the associated row/column driver is introduced to minimize the number of interface signal lines within the system.

This paper is organized as follows: Section II presents an overview and design considerations for the proposed active-matrix and pixelated-LED control system architecture. The implementation of the proposed pixel driver circuit is discussed in Section III. The system prototype and measurement results are presented in Section IV and the conclusion in Section V.

II. PROPOSED ACTIVE-MATRIX PIXELATED-LED CONTROL SYSTEM

The proposed active-matrix control system consists of two main blocks as shown in Fig. 2: an LED driver module (LDM) and a pixelated-LED driving circuitry (PLDC) system. LDM provides control signals to the PLDC through ROW_{LDM} and COL_{LDM} signals. It consists of microcontroller and field programmable gate array (FPGA) to generate control signals. The PLDC contains an active-matrix array of $N \times M$ pixel drivers with pixelated-LEDs and an associated row/column driver. The pixel driver contains a memory cell, combinational logic circuitry, a fixed current source, and an LED driver stage circuit. The dimming data of the pixel driver is programmed through the row/column driver.

The row/column driver takes ROW_{LDM} and COL_{LDM} signals from LDM and provide the output signals: ROW_1 – $ROW_N$and COL_1 – COL_M. The output signals control the pixel driver for each location. The operation of the control signals and its timing diagram are shown in Fig. 3. The ROW/COL signals of the control system have several fields based on the proposed asynchronous serial communication protocol. Each field is distinguished with the operation of the pixel driver. There are three fields in the ROW signal. The first is the pixel selection field, which specifies the address of the pixel position during the Reset mode. The second is the memory clock field for the memory cell during the Data-store mode. The last is the PWM pulse field for the LED driver stage during the PWM-drive mode. The COL signal has two fields. The first is the pixel selection field associated with ROW signal for the pixel position. The other is the memory dimming data field for the Data-store mode.

In order to program each pixel driver in the array, LDM generates the ROW_{LDM} signal for ROW_1 to ROW_N sequentially, while feeding the COL_1 – COL_M signals simultaneously to each selected row. The pixel driver is programmed by four operation modes during 1 frame time: Power-ON, Reset, Data-store, and PWM-Drive. At first, all the pixel drivers remain in Power-ON mode before the PLDC starts operation. Then, the programming operation of the first frame in the array starts when the pixel drivers at the first row enter the Reset mode. During this mode, the pixel drivers at the first row are reset. During the Data-store mode, COL_1 – COL_M feeds the dimming data to the pixels in the first row to store the data into the memory cell of each pixel

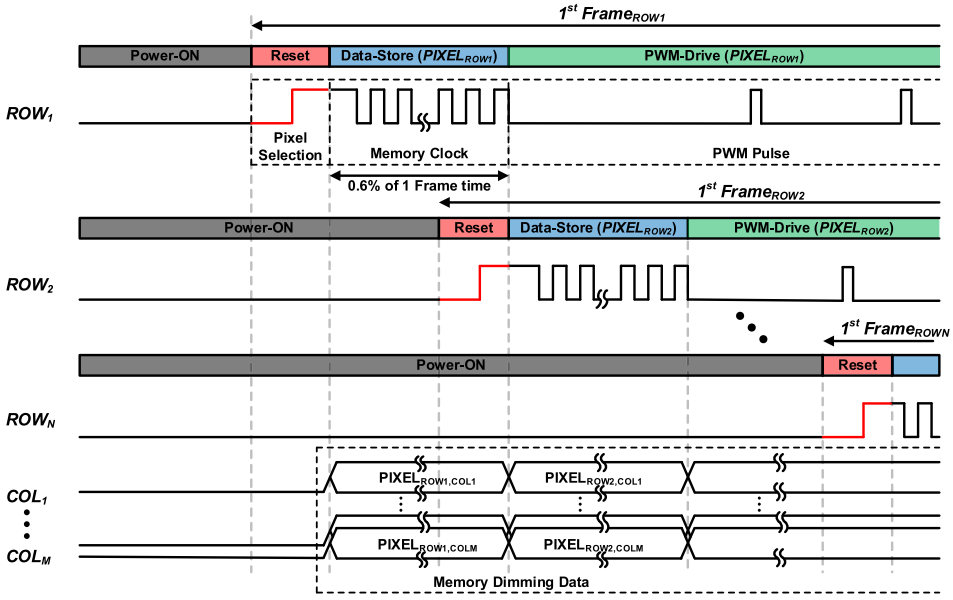

FIGURE 3. Timing diagram of the proposed control system.

driver. This mode only occupies about 0.6% of 1 frame time. At the end of the Data-store mode of the first row, the pixel drivers in the second row enter the Reset mode. After that, the pixel drivers in the first row drive the LEDs with the PWM signal. At the same time, the pixel drivers in the second row store the dimming data from the COL_1 – COL_M. The control system proceeds this sequence up to the pixel driver in the N^{th} row. When the PWM driving operation of the first frame is done, the operation of the second frame proceeds immediately.

In order to design higher resolution, the pixel driver should operate normally even with high number of N and M in PLDC. Depending on the N and M, the ROW/COL signals have a delay due to the load components affecting the control of the pixel driver. Fig. 4(a) shows a simplified block diagram of the $N \times M$ array PLDC and the delay effect of the ROW_N/COL_M signals that control the pixel driver at the (N, M) location. This location is most affected by the delay as it passes through all the row/column metal routing and pixel drivers. Therefore, the delay in this location should be shorter than the margin in the operation of the control signals. In particular, since the ROW signal is connected to all D-FFs as a clock source, it is more affected by the load of the pixel driver than the COL signal. Therefore, the load resistor and capacitors that affect the delay of the ROW signal in this location are shown in Fig. 4(b). Depending on the number of matrices, $t_{pd,ROWN}$, $t_{pd,COLM}$ at the location are defined as the Elmore delay as follows:

$$t_{pd,ROWN} = \frac{M\,(M+1)}{2} * 3R_N C_N * \ln\left(\frac{V_X}{0.82}\right) \quad (1)$$

$$t_{pd,COLM} = \frac{N\,(N+1)}{2} * 3R_M C_M * \ln\left(\frac{V_X}{0.82}\right) \quad (2)$$

where R_{metal} is resistance of the metal routing between pixels, R_N is the sum of R_{metal} in the N^{th} row, C_{metal} is the

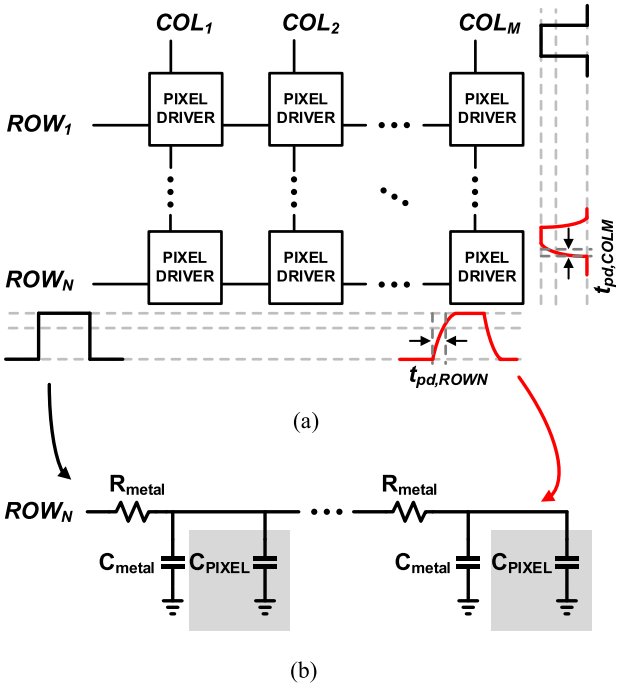

FIGURE 4. (a) Simplified block diagram of the PLDC and (b) equivalent circuit of the ROW_N signal.

load capacitance of the metal routing, C_{PIXEL} is the load capacitance of the pixel driver, C_N is the sum of C_{metal} and C_{PIXEL} in the N^{th} row, and V_X is the 1.8-V V_{DD}. Therefore, the maximum number of N and M are determined according to the $t_{pd,ROWN}$ and $t_{pd,COLM}$ shorter than the operation margin.

III. PIXEL DRIVER CIRCUIT IMPLEMENTATION

The block diagram of the pixel driver is shown in Fig. 5. It contains various function blocks: a Level shifter (LS), a memory cell, a reset, and an LED driver stage. The LED

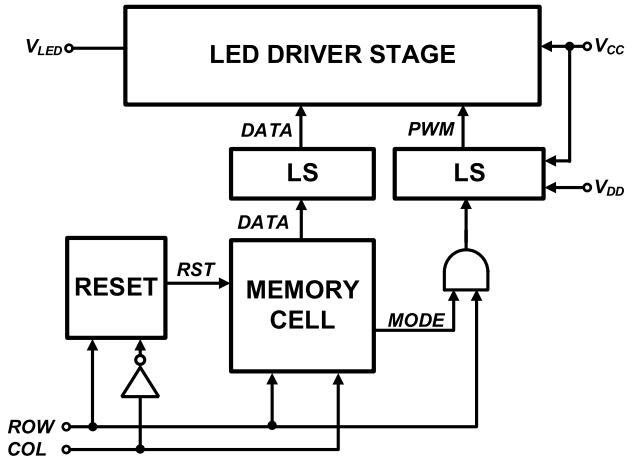

FIGURE 5. Block diagram of the proposed pixel driver.

driver stage is operated at 5-V V_{CC} while other three blocks are operated at 1.8-V V_{DD}. The LS block is used to interface the power domain between 1.8 V and 5 V. The operation of the pixel driver is as follows: It resets the existing dimming data in the memory cell before the pixel driver stores new dimming data with the ROW signal and inverted COL signal. The memory cell uses the ROW signal as the clock source and the COL signal as data to update the dimming data. Based on the dimming data of the memory cell and the PWM pulse through the ROW signal, the LED driver stage block drives an LED.

A. RESET & MEMORY CELL

The simplified circuit diagram and its timing diagram of the reset and memory cell are shown in Fig. 6. After Power-ON mode, the RST signal is generated with a combination of the ROW signal at the rising edge of the COL signal. When this RST signal is in the logic low, the D-FF in the memory cell resets the dimming data. As shown in the timing diagram, the RST signal always maintains the logic high after Reset mode. In other words, the ROW signal is always logic high of the rising edge of the COL signal. Therefore, the D-FF of the memory cell is not affected by the RST signal except during Reset mode. In the Data-store mode, the ROW signal operates as a clock source with a duty cycle of 50% and a period of 8 μs. The COL signal operates as serial dimming data through two different pulse widths with a period of 8 μs. When the COL signal represents '1' data, it delays the ROW signal. Therefore, the logic high of COL signal is stored at the falling edge of the ROW signals. At this time, the interval between the falling edge of the ROW signal and the falling edge of the COL signal is 0.8 μs. When the COL signal represents '0' data, the pulse width of the COL signal is only 2.4 μs. Thus, the logic low of the COL signal is stored at the falling edge of the ROW signal. The interval from the falling edge of the ROW signal to the falling edge of the COL signal is also 0.8 μs.

The circuit implementation of the memory cell is shown in Fig. 7. It consists of multiple D-FFs in series determined by the scale of the dimming level, a D-FF for a flag, and

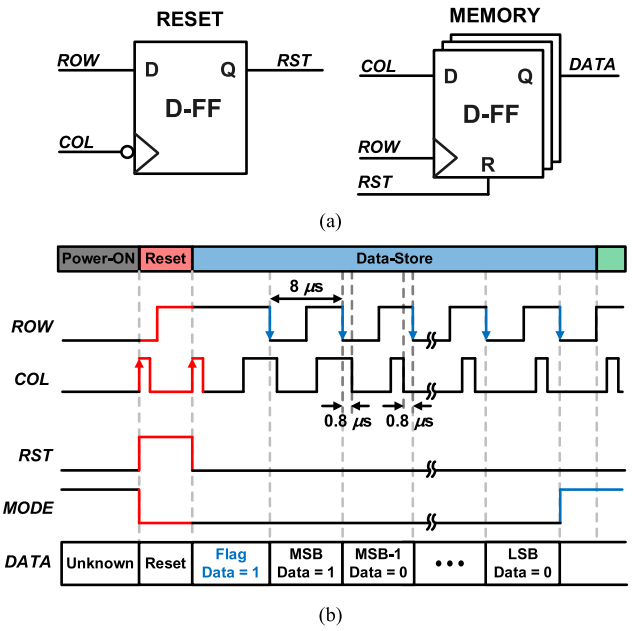

FIGURE 6. (a) Simplified circuit diagram of the reset and memory cell and (b) its operational timing diagram.

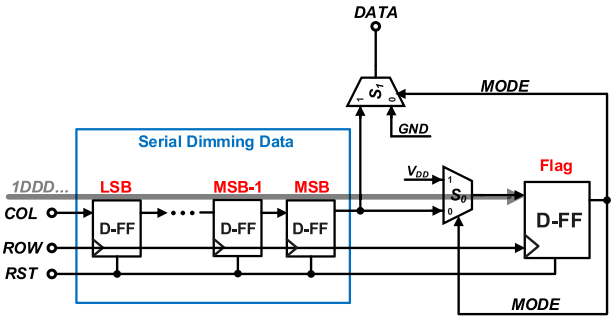

FIGURE 7. Circuit implementation of the memory cell.

multiplex switches that control the operation mode through the MODE signal. As shown in Fig. 6 (b), the COL signal always starts with '1' data for the MODE signal and proceeds sequentially from the most significant bit (MSB) to the least significant bit (LSB) for serial data. At first, the MODE signal is set to logic low by the RST signal during Reset mode. When the first '1' data of the COL signal arrives at the D-FF for a flag, the MODE signal becomes logic high. Then, S_0 keeps the MODE signal logic high by switching V_{DD} into the D-FF for a flag. It also prevents the transfer of MSB to the D-FF for a flag. During PWM drive mode, S_1 transfers the stored dimming data to the LED driver stage in order from MSB.

B. LED DRIVER STAGE

The circuit implementation and operation of the proposed LED driver stage is shown in Fig. 8. This circuit is designed with a cascoded structure to provide a self-biasing current source. M_{M1} and M_{D1} of the driving stage are 1.8-V devices, while M_{M0} and M_{D0} of the cascoded stage are 5-V devices. M_{D0} is for protecting M_{D1} when the LED turns off, because a voltage higher than 1.8 V can be applied to $V_{DS,D1}$. In order to

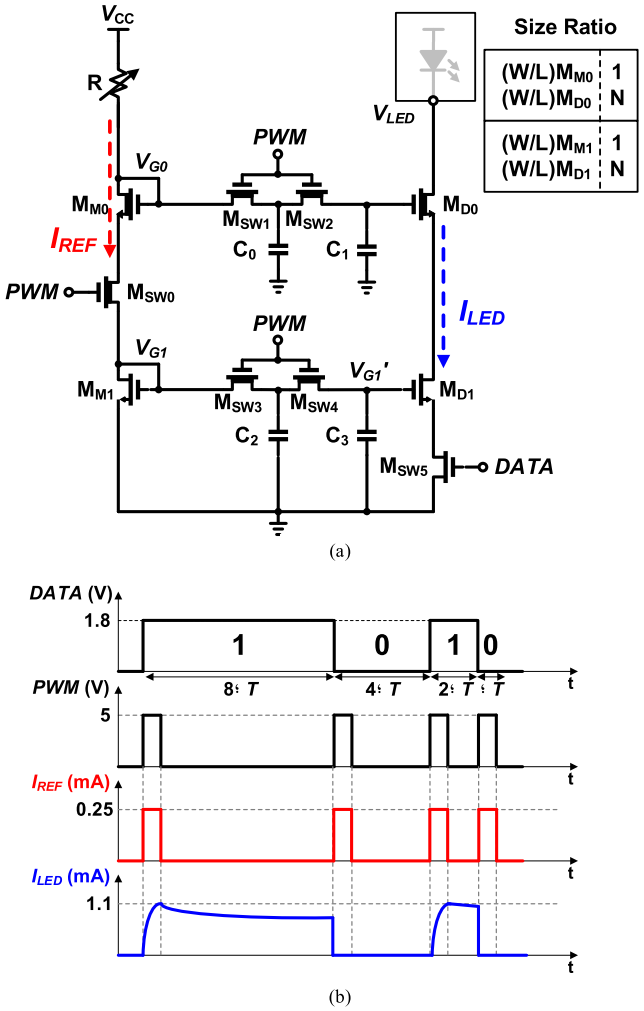

FIGURE 8. **(a) Circuit implementation of the LED driver stage and (b) its operation with timing diagram.**

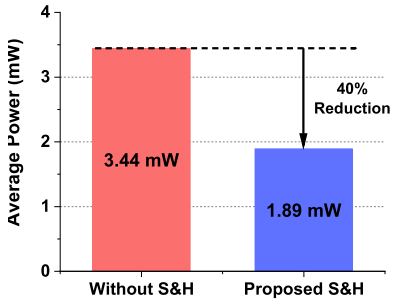

FIGURE 9. **Simulated average power consumption at 1 frame time of the LED driver stage w/o sample-and-hold (S/H).**

generate constant driving current, I_{LED}, during PWM-Drive, a sample-and-hold scheme for I_{REF} is adopted to minimize the static power consumption.

Fig. 8(b) shows the operation example when the DATA signal is '1010'. While the PWM signal is logic high, $\mathrm{M_{SW0}}-\mathrm{M_{SW4}}$ turn on and I_{REF} on the left side flows to charge $\mathrm{C_1}$ and $\mathrm{C_3}$. At the same time, the flow of I_{LED} on the right side is controlled by the logic state of the DATA signal. When the DATA signal is logic high, I_{LED} flows by the charged state of $\mathrm{C_1}$ and $\mathrm{C_3}$ even if the switch is off due to the logic low of the PWM signal. However, when the DATA signal is logic low, the I_{LED} cuts off regardless of the logic state of the PWM signal. Thus, I_{REF} flows only when the PWM signal is logic high, resulting in static power consumption of the LED driver. Since the operation occupies about 99% of one frame time, it dominates the power dissipation of the pixel driver. Fig. 9 shows the simulated average power consumption of the LED driver over one frame time. It calculates the average of simulating the current through the LED driver power for one frame time. Without the sample-and-hold scheme, I_{REF} always flows during one frame time, consuming about 2.95 mW of static power. With the sample-and-hold scheme, only 1.8 mW is consumed, which corresponds to a power savings of 40%.

In Fig. 8(a), I_{REF} and I_{LED} can be expressed by the MOSFET drain current equation.

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{M1}(V_{G1} - V_{th})^2 \tag{3}$$

$$I_{LED} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{D1}(V'_{G1} - V_{th})^2 \tag{4}$$

From (3) and (4), I_{LED} is multiplied by the size ratio to I_{REF} when $V_{G1} = V'_{G1}$. However, by adding a switch for the sample-and-hold scheme, V'_{G1} is decreased by the V_{DS} of the switches and is as follows:

$$V'_{G1} = V_{G1} - V_{DS,SW3} - V_{DS,SW4} \tag{5}$$

From (5), the size ratio of $\mathrm{M_{D1}}$ and $\mathrm{M_{M1}}$ should be determined to achieve the target I_{LED} value.

When the switch is turned off, the leakage current of the switch transistor discharges $\mathrm{C_3}$ during the LED driving time, which then deteriorates the constant LED current level. The relationship between the subthreshold current and the threshold voltage can be expressed as follows:

$$I_{OFF} \propto \frac{W}{L}\cdot 10^{-\left(\frac{V_{th}}{S}\right)} \tag{6}$$

where the V_{th} is the threshold voltage of the MOSFET, and S is the subthreshold swing. When using the short channel length MOSFET, the threshold voltage is decreased by a process called $\mathrm{V_{th}}$ roll-off [26]. The equation of $\mathrm{V_{th}}$ roll-off can be expressed as follows:

$$V_{th} = V_{th0} - V_{DS}\cdot e^{-\frac{L}{l_d}} \tag{7}$$

where V_{th0} is the threshold voltage when the length is sufficient, L is the length of the MOSFET, and l_d is the length of the drain-induced barrier lowering (DIBL) characteristic. The T-switch model minimizes V_{DS} which helps reducing the subthreshold current [27], [28]. In this scheme, $V_{DS}$of the switches is divided and then the discharging speed of $\mathrm{C_1}$ and $\mathrm{C_3}$ are decreased until $\mathrm{C_0}$ and $\mathrm{C_2}$ are fully discharged, respectively.

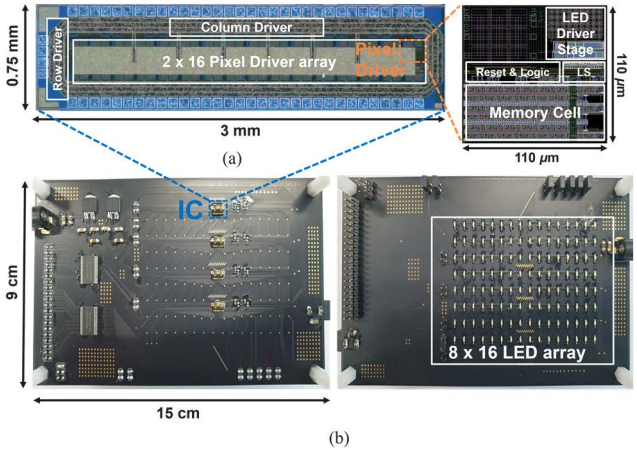

FIGURE 10. (a) Chip micrograph of the proposed IC and (b) demo board.

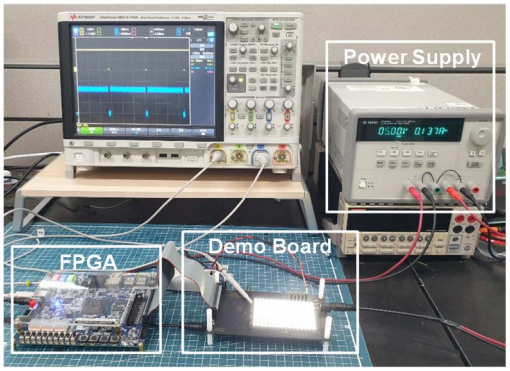

FIGURE 11. Test set-up environment for the demo board.

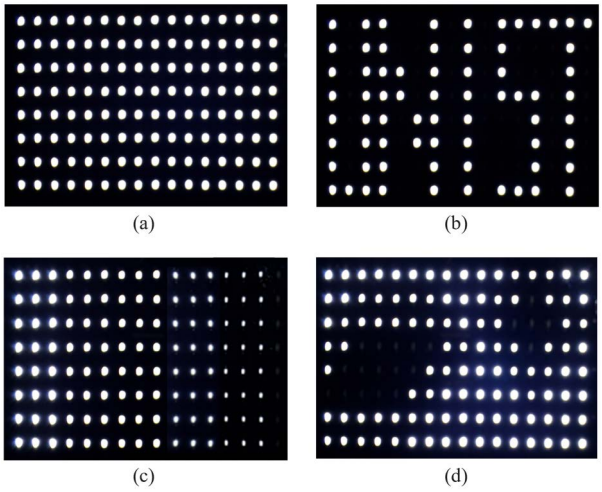

FIGURE 12. Measured various display patterns on LED of the system prototype (a) all LEDs turn on, (b) 'UNIST' projection, (c) brightness control with gradation, and (d) control the specific area.

IV. SYSTEM PROTOTYPE AND MEASUREMENT RESULTS

The prototype IC has been fabricated using a 0.18-μm CMOS process. Fig. 10(a) shows a chip micrograph with a total chip area of 3.00 mm $\times$ 0.75 mm including I/O pads. The area of the pixel driver block is only 110 μm $\times$ 110 μm. It contains a 2 $\times$ 16 pixel array with an embedded row/column driver. Fig. 10(b) shows the demo board to demonstrate the proposed

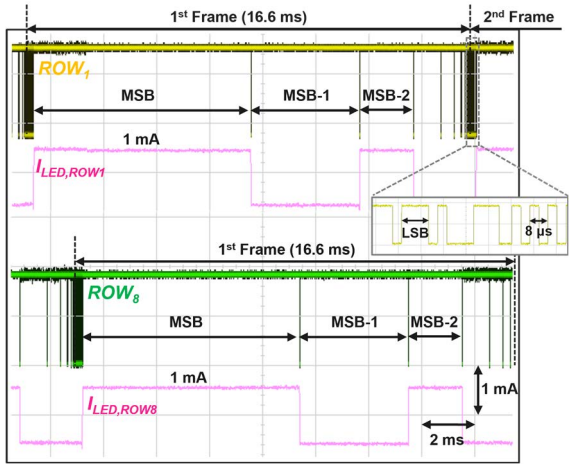

FIGURE 13. Measured LED current with ROW signal when the binary dimming data is 10100000000_2.

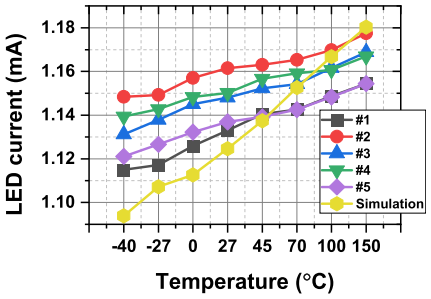

FIGURE 14. Measured LED current.

driving circuitry system. The front side of the demo board contains four ICs. On the back side, the 8 $\times$ 16 commercial white LED array is connected to the ICs. Fig. 11 shows the test set-up environment of the demo board. The demo board is connected to an FPGA board in order to provide the $\mathrm{ROW_{LDM}/COL_{LDM}}$ signal [29].

The individual control capability of the pixelated-LED with various display patterns is demonstrated as shown in Fig. 12: (a), all LEDs turned on with the brightest level. (b) shows a 'UNIST' text pattern. (c) shows the gradation pattern with different brightness level by a group of 3 vertical lines. Binary dimming data from the left represent 1111111111_2, 0100000000_2, 0010000000_2, 0001000000_2, and 0000100000_2. Finally, (d) shows a zone control pattern to demonstrate a glare-free pattern.

Fig. 13 shows the measured LED current with the $\mathrm{ROW_1}$ and $\mathrm{ROW_8}$ signals when the binary dimming data is 10100000000_2. Each I_{LED} is set to 1 mA current during MSB and MSB-2 by the stored dimming data. Even if $\mathrm{ROW_8}$ starts the Data-store mode, the driving level of $I_{\mathrm{LED,ROW1}}$ is maintained. Thus, the significant characteristics of maintaining I_{LED} during one frame time of an active-matrix control system can be demonstrated.

Fig. 14 shows measured I_{LED} at different samples over the temperature variation from -40°C to 150°C comparing to the simulation result. In Fig. 8(a), V_{G1} can be expressed as

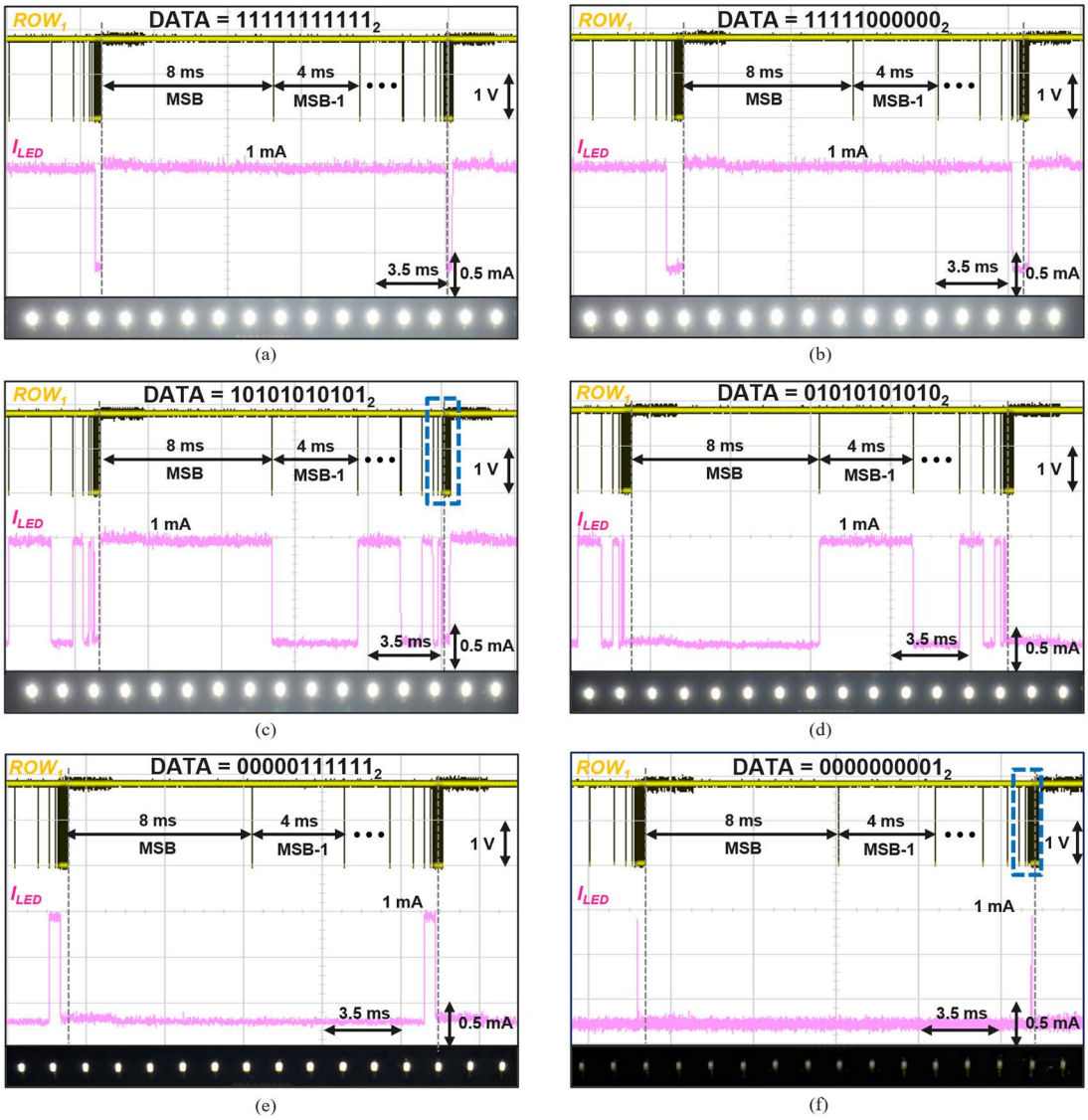

FIGURE 15. Measured LED current at the one frame (16 ms) with respect to binary dimming data (a) 11111111111_2, (b) 11111000000_2, (c) 10101010101_2, (d) 01010101010_2, (e) 00000111111_2, and (f) 00000000001_2.

TABLE 1. Comparison table to previous led drivers.

	ICIT '19 [7]	TPE '21 [13]	TI TPS92663 [14]	ISAL'15 [15]	J-EDS '19 [19]	TCAS II '18 [25]	**This work**
Technology	N/A	N/A	N/A	N/A	0.11-μm CMOS	0.18-μm CMOS	**0.18-μm BCD**
Architecture	DC-DC Converter	DC-DC Converter	DC-DC Converter	Active-Matrix	Active-Matrix	Active-Matrix	**Active-Matrix**
Applications	Automotive Headlamp	Automotive Headlamp	Automotive Headlamp	Automotive Headlamp	Display	Display	**Automotive Headlamp**
LED Control	String	Individual	Individual	Individual	Individual	Individual	**Individual**
Resolution (Number of LEDs)	2~5	12	12	1,024	4,410	768	**Demo : 128 Target : Max 204 × 107**
Power Supply	13.5 V	12 V	5 V	12 V	4 V	6 V	**5 V**
LED Current	1 A	550 mA	800 mA	15 mA	0.19 nA (Blue)	12 μA	**1 mA**
LED Forward Voltage	3.3 V	3 V	5 V	N/A	N/A	N/A	**~3 V**
Frame Rate	N/A	120 Hz	120 Hz	N/A	120 Hz	N/A	**60/120 Hz**
Light Intensity Control	PAM	PWM	PWM	8-bit PWM	PAM	8-bit PWM	**11-bit PWM**
Pixel Area (μm^2)	N/A	N/A	N/A	115 × 115	5.8 × 1.9	N/A	**110 × 110**

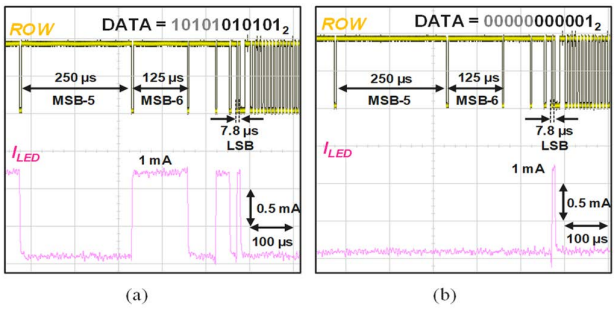

FIGURE 16. Measured LED current of magnified views of blue boxes in Fig. 14(c) and (f), respectively.

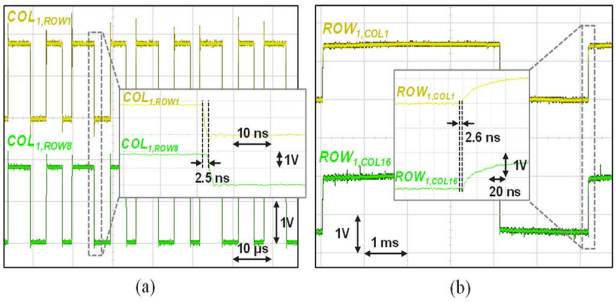

FIGURE 17. Measured delay of the (a) ROW signal and (b) COL signal.

follows:

$$V_{G1} = V_{CC} - RI_{REF} - V_{DS,M0} - V_{DS,SW0} \tag{8}$$

Combining (5) and (8), the LED current equation from (3) is obtained as follows:

$$I_{LED} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{D1}\left(V_{CC} - RI_{REF} - V_{DS,Total} - V_{th}\right)^2 \tag{9}$$

where $V_{\mathrm{DS,Total}}$ is the sum of $V_{\mathrm{DS,M0}}$, $V_{\mathrm{DS,SW0}}$, $V_{\mathrm{DS,SW3}}$, and $V_{\mathrm{DS,SW4}}$. In equation (9), the dominant factor of the temperature variation is the resistor as shown in Fig. 8(a). The temperature coefficient of resistance (TCR) used in this circuit has a negative value. Thus, as the temperature increases, the I_{LED} also increases. An approximately 5% difference in I_{LED} is observed between −40°C and 150°C. Changes in brightness due to differences in I_{LED} are difficult to distinguish with the naked eye. Also, a difference between the highest and lowest I_{LED}at 27°C is about 2% among the samples.

Fig. 15(a)-(f) shows different level of LED brightness with the measured LED current and the ROW_1 signal at one frame time depending on the dimming data. The I_{LED} is driven with PWM pulses according to the dimming data expressed in binary format. Fig. 15(a) shows the brightest level with the dimming data of 11111111111_2, while Fig. 15(f) shows the lowest brightness level with the dimming data of 00000000001_2. Fig. 16(a) and (b) show the measured LED current in magnified views of the blue boxes from Fig. 15(c) and (f), respectively.

Fig. 17 shows the delay of the $\mathrm{ROW}_1/\mathrm{COL}_1$ signal measured with the demo board of the 16 × 8 pixel array. Fig. 17(a) shows the delay of the COL_1 signal between the pixel drivers located in ROW_1 and ROW_8. Fig. 17(b) shows the delay of the ROW_1 signal between the pixel drivers located in COL_1 and COL_{16}. From (1) and (2) with measurement results, the maximum value of $N \times M$ would be 204 × 107.

The comparison table of the state-of-the-art LED driver is shown in Table 1. The proposed work establishes an active-matrix configuration for an automotive headlamp with an 11-bit PWM driving of 1-mA LED current.

V. CONCLUSION

This paper introduces driving circuitry system which allows an individual controllability at higher resolution for pixelated-LED headlamp module. Individual dimming function on each pixelated-LED is controlled by a combination of PWM pulses based on dimming data along with a constant current source. Row/column driver communicates with the pixel driver array by an asynchronous serial communication protocol in order to minimize the interface routing signals on a system board. The proposed pixel driver circuit supports a multi-bit dimming scale with a constant current source of 1 mA. The LED driver stage using sample-and-hold scheme demonstrate about 40% static power saving on each pixel which would be great saving at higher resolution. The proposed system has been fabricated in a 0.18-μm CMOS process. The functionality of the system is demonstrated with a prototype IC with an 8 × 16 pixel array of the active-matrix array configuration.

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