Three-Level T-Type Quasi-Z Source PV Grid-Tied Inverter With Active Power Filter Functionality Under Distorted Grid Voltage

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ABSTRACT Distributed energy resources (DER) such as solar photovoltaic (PV) interfaces with the utility grid by high-efficiency power electronic converters. This equipment is sometimes underutilized in terms of its power capacity; thus, the remaining capacity can be used to provide support to the distribution system. In this sense, this work assesses the performance of the three-level T-type quasi-impedance source inverter (3L-T-type qZSI) injecting not only active power to the grid, but also providing support to it by injecting reactive power and acting as an active power filter (APF) simultaneously. The global control strategy of the grid-connected inverter is derived from the instantaneous i_d-i_q power theory. The combination of an improved deadbeat current controller and a level-shifted carrier-based pulse-width-modulation (PWM) technique, using both the upper shoot-through (UST) and the lower shoot-through (LST) alternating states, allows a successful tracking of the current references. Both the dc-link voltage control and the neutral-point balancing are properly achieved by taking the advantage of the shoot-through (ST) states and the redundant states simultaneously. These control actions are implemented by simple proportional-integral (PI) controllers. The simulation and experimental results demonstrate the above-mentioned functionalities and verify the stability and good dynamic response of the grid-connected 3L-T-type qZSI.

INDEX TERMS Active power filter, dead-beat current controller, distributed energy resources, grid-connected inverter, multilevel inverter, 3L-T-type qZS inverter.

I. INTRODUCTION

Power electronic inverters used for integrating solar photovoltaic (PV) dc power into ac grid are underutilized in terms of its current capacity during low irradiation period. In that time, the unused inverter capacity can support the grid through reactive power and harmonic current compensation at the point of common coupling (PCC) [1]–[4]. In other words, it would integrate the PV to the grid as well as operates as an active power filter (APF) simultaneously. The need of such compensation comes from the fact that most converters

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behave as non-linear loads, demanding distorted and unbalanced currents from the ac grid. These currents will cause distortion in grid voltages.

Among the power topologies used for inverters, the impedance-source (Z-source) topology, and its evolution, the quasi-Z-source topology proposed in [5], allow overcoming a typical limitation associated to the conventional voltage-source inverter (VSI): it has buck and boost capabilities which avoids the need for an extra dc/dc converter and/or step-up transformer and, additionally, it is suitable for drawing a continuous input current from the power source. These features are required when it comes to install an inverter in PV generation systems.

On the other hand, multilevel inverters, and more specifically the three-level inverters, show lower switching losses and lower harmonic contents in the output voltage than the two-level inverters [6]. The neutral-point-clamped (NPC) inverter is a well-known topology of this family; in reference [7], this circuitry is used for a dual purpose of shunt active power filtering and solar PV power integration to a distribution grid. Another three-level topology is the T-type, which in comparison with NPC presents additional improvements, as reduced switching losses at lower switching frequencies [8]. The combination of a three level T-type inverter with of a quasi-Z network, therefore adding the boost capability, was studied in [9], [10], but they do not implement interaction with the grid. There are not many works that deal with the grid-interactive inverters based on Z-source/quasi-Z-source topologies. References [11], [12] treat the Z-source-T-type and quasi-Z-source-T-type topologies, respectively, including grid control, but do not perform compensating actions. Authors in [13] introduced a grid control strategy with compensating action; however, it has not been shown to work well under distorted grid voltages. Besides no experimental tests have been reported. Reference [14] discusses the operation under a distorted grid voltage, but for a single-phase quasi-Z topology, and it does not include APF functions. Moving a step further, this paper contributes with the implementation in the one-stage three-phase quasi-Z three-level T-type topology of a control strategy which achieves its operation as a dual-purpose inverter. It regulates the active power injected into the grid (extracting the maximum or a reference power from PV panels), and also it operates as a shunt APF simultaneously, injecting or demanding reactive power and compensating unbalanced and harmonic current components from non-linear loads connected at the PCC. The two functionalities show a successful performance under distorted and unbalanced grid voltage. To accomplish this, a set of inverter output reference currents is generated by the control strategy based on the instantaneous i_d-i_q power theory. The actual inverter output currents are produced by commutation of the converter's electronic switches, following these references using an appropriate current controller. At the same time, the dc-link voltage is regulated in the presence of PV voltage variations, taking advantage of the buck/boost capability of this type of converter.

Concerning the current controller, in the dead-beat implementation originally presented in [15], a discrete-time model is used to predict the current trajectory one or more sampling periods in advance, to determine the plant input (i.e., the duty cycle) that makes the reference tracking error equal to zero at the same number of periods. The controller is characterized by a relatively low complexity and, at the same time, by a very good dynamic performance. It is regarded as one of the best choices for obtaining a good tracking of the reference currents at converter output [16]–[19]. Nevertheless, its application to a quasi-Z T-type inverter has not been proved so far. In this paper, an improved and robust dead-beat controller is applied to that topology, which simultaneously tracks the reference

converter output currents and achieves a neutral-point balancing of the internal dc capacitors' voltage. For this family of converter, the neutral-point balance has been addressed in several works [10], [20]–[22]. For example, a sinusoidal PWM based technique with a PI regulator has been selected for the 3L-T-type Z-source inverter [20]. At the same time, advanced SVPWM methods are employed with similar purpose [10], [21]. A SVPWM technique for the neutral-point balancing in a 3L inverter with Z-source network demonstrated an effective elimination of the neutral-point voltage imbalance [21]. This approach was improved by integrating the reduction of the common-mode voltage with the voltage imbalance elimination [10], [22].

Regarding the modulation technique in the quasi-Z source inverters, the insertion of dc-link short circuits in the switching sequence, the so-called shoot-through (ST) states, enables the desired voltage boost capability. Besides the full shoot-through (FST) state, two additional switching states are also possible for three-level inverters: the upper shoot-through (UST) and the lower shoot-through (LST). These states were defined in [23]; the idea was applied to a 3L-NPC Z-source inverter [24], to a 3L-NPC-quasi-Z-source inverter [25], and to a 3L-T-type Z-source inverter [26]. In this work, a PWM carrier-based technique using UST/LST states is applied to a three-phase three-level T-type quasi-Z-source inverter (3L-T-type qZS inverter). It achieves better performance, less electromagnetic interference (EMI), and lower harmonic content of the output voltage signal compared to the modulation that uses only the FST state [27]. It also permits the use of electronic devices with less blocking voltage capability, thus improving converter reliability, size and cost. Besides, using carrier-based approach it is easier to be practically implemented in comparison with space vector modulation (SVM) approaches.

Summarizing, the main contribution of this paper are as follows:

- Implementation of a control strategy for the first time in a 3L-T-type qZS inverter which simultaneously boosts and adjusts the dc-link voltage to the variable PV voltage. Besides, it controls the active power fed into the grid and functions as a shunt active power filter, thus mitigating, during non-peak PV power periods, reactive power, unbalanced and harmonic current components of non-linear loads connected at the PCC. All these functionalities are experimentally tested, under distorted and unbalanced grid voltage, demonstrating a satisfactory performance.
- The combination of an improved deadbeat current controller and a level-shifted carrier-based pulse-width-modulation (PWM) technique, using both the UST and the LST alternating states instead of the classical FST states. Simultaneously, by means of a simple controller, the switching signal generation achieves a neutral-point balancing of the internal dc capacitors' voltage.

The paper is organized as follows. The general operation principle and control scheme are described in Section II.

The control scheme is composed by the reference current waveforms calculation at the output of the converter and its current controller to track these references. The dc voltage control loop is also explained there. Then, Section III presents the simulation results for different operation modes, which are experimentally verified in Section IV. Finally, conclusions are drawn in Section V.

II. SISTEM DESCRIPTION

Figure 1 shows the power circuit of the 3L-T-type qZS inverter. This converter simultaneously adjusts the variable PV voltage, controls the active power fed into the grid, both in maximum power point (MPP) or in reference power point (RPP) tracking mode, and functions as an APF. It can be seen in the different blocks the following subsystems: the dc voltage source which represents the renewable energy source, the quasi-Z network, the T-type three-level inverter and the output filter. The voltage and current from the PV panels are U_{PV} and I_{PV}, respectively. The inverter output currents are denoted as i_a, i_b, i_c. A simple representation of the unbalanced and non-linear load is included as well, connected at the PCC. The currents demanded by this load are i_{La}, i_{Lb}, i_{Lc} and the total currents injected into the grid (inverter current minus load currents) are i_{ga}, i_{gb}, i_{gc}. Grid voltages, which are supposed to be distorted and unbalanced, are u_a, u_b, u_c.
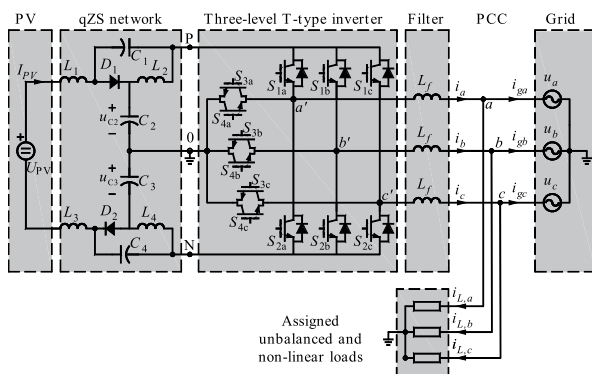

FIGURE 1. Grid-connected three-phase 3L-T-type qZS inverter topology and the unbalanced and non-linear load.

Using switching combinations, the inverter outputs (a', b', c') are connected to the terminals P, 0 or N; thus, three-phase voltage waveforms with three voltage values $(-U_{PN}/2, 0$ and $U_{PN}/2)$ are possible. The conventional switching combinations correspond to the non-shoot-through (NST) states. When P and N points are joined by closing both the upper (S_1) and lower (S_2) switches of any phase, a zero-voltage value is obtained at the corresponding output. The state is the so-called full shoot-through (FST) state. Besides this state, used in most Z-source topologies, two new switching states named UST and LST states are possible [23], as stated above. The UST state corresponds to the simultaneous activation of switches S_1 and S_3 in any phase leg. It produces a short circuit in the upper half dc-link, connecting terminals P and 0. On the other hand, the LST state takes place when switches

S_4 and S_2 in any phase branch are simultaneously turned on. This produces a short-circuit in the lower half dc-link, connecting the terminals 0 and N. Application of these new states reduces the harmonic distortion of the output line-to-line voltages compared to the FST strategy [26], [27]. Table 1 summarizes the states for the case of phase-a.

TABLE 1. Switches turned on and phase-leg voltage.

State	ON switches (phase a)	OFF switches (phase a)	$u_{a'0}$
P	S_{1a}, S_{4a}	S_{3a}, S_{2a}	$U_{PN}/2$
0	S_{3a}, S_{4a}	S_{1a}, S_{2a}	0
N	S_{2a}, S_{3a}	S_{4a}, S_{1a}	$-U_{PN}/2$
FST	$S_{1a}, S_{2a}, S_{3a}, S_{4a}$	-	0
UST	S_{1a}, S_{3a}	S_{2a}, S_{4a}	0
LST	S_{2a}, S_{4a}	S_{1a}, S_{3a}	0

Note: For P, 0 and N states (NST states), S_1 and S_3 are complementary; and S_2 and S_4 are also complementary.

Adjusting the ST duty cycle, a voltage gain similar to that of the boost dc–dc converter is achieved. This boost capability is derived in [25] as following outlined. To ensure symmetric operation, the duration of UST or LST states are set to be equally to T_0. The ST duty ratio is $D_0 = T_0/T_S$, where T_S is the switching period. Assuming that the quasi-Z-source network is symmetric (i.e. $L_1 = L_3$, $L_2 = L_4$ and $C_1 = C_4$, $C_2 = C_3$), the voltages through the passive components are $u_{L1} = u_{L3}$, $u_{L2} = u_{L4}$ and $u_{C1} = u_{C4}$, $u_{C2} = u_{C3}$. It is also assumed that the converter operates in the continuous conduction mode. Then, since the average voltage across inductors over one switching period should be zero in steady state, the boost factor is obtained and given by.:

$$B = \frac{\hat{U}_{PN}}{U_{PV}} = \frac{1}{1 - 2D_0} \quad (1)$$

The utilization of the UST/LST states results in a discontinuous dc-link voltage (U_{PN}), which is switching between $\hat{U}_{PN}/2$ and a peak value of $\hat{U}_{PN}$. It is worth noting that $\hat{U}_{PN}$ is the dc-link peak voltage value present during NST states. Then, under any modulation scheme, the inverter is modulated in order to have three-phase output voltages, whose fundamental peak phase value is accordingly given by

$$\hat{U}_{an,1} = m \frac{1}{1 - 2D_0} \frac{U_{PV}}{2}, \quad (2)$$

with m representing the modulating signal. UST/LST states are inserted within the zero intervals into the modulation period using the method described later in the modulation technique subsection.

A. CONTROL STRATEGY

Figure 2 shows the block diagram of the 3L-T-type qZS inverter control system. The reference inverter output currents represented by the vector $\mathbf{i}^* = \left(i_a^* \ i_b^* \ i_c^* \right)^T$, are calculated by means of the control strategy, aiming that the active power and reactive power setpoints (P^* and Q_1^* respectively) are fulfilled. Besides, if the inverter rated power is not exceeded,
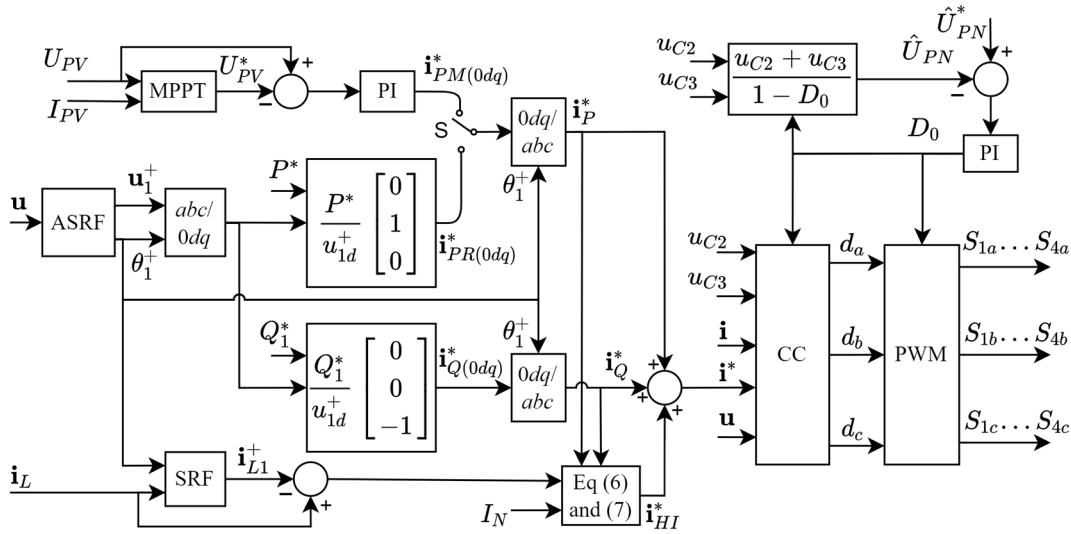
FIGURE 2. Block diagram of the inverter control system.

harmonics and unbalanced currents demanded by the non-linear load $\mathbf{i_L} = (i_{La}\ i_{Lb}\ i_{Lc})^T$ are completely or partially compensated at the PCC. Thus, $\mathbf{i}^*$ is composed by three terms, explained in detail in the next subsections: active power $\mathbf{i}_P^* = \left(i_{Pa}^*\ i_{Pb}^*\ i_{Pc}^*\right)^T$, fundamental reactive power $\mathbf{i}_Q^* = \left(i_{Qa}^*\ i_{Qb}^*\ i_{Qc}^*\right)^T$ and harmonic and imbalance load current $\mathbf{i}_{HI}^* = \left(i_{HI\,a}^*\ i_{HI\,b}^*\ i_{HI\,c}^*\right)^T$. The calculation of these reference currents is based on the instantaneous power theory, using the power-invariant Park transformation, expressing the three-phase magnitudes in the synchronous reference frame $0dq$.

1) ACTIVE POWER CONTROL (P MODE)

If this mode is activated exclusively, the inverter would operate with unity power factor, providing output sinusoidal currents, balanced and in phase with the positive-sequence fundamental grid voltages. Into this P mode, in turn, two operation sub-modes are possible (selected by the switch 'S' in Figure 2):

1. Maximum power point tracking mode (MPPT mode). In this mode, the reference current vector in the $0dq$ frame is $\mathbf{i}_{PM(0dq)}^* = \left(0\ i_{PM\,d}^*\ 0\right)^T$. The d component i_{PMd}^* is calculated to extract the maximum available power from PV panels, measuring PV voltage (U_{PV}) and current (I_{PV}), and using a MPPT algorithm, such as the classical perturb and observe. This mode is not further explored for simplicity reasons.

2. Reference power point tracking (RPPT mode). An active power setpoint P^* must be tracked in the RPPT mode. This setpoint is sent from the energy management system (EMS), which coordinates the operation of several inverters into a facility according to criteria that depends on a variety of different goals, which are out of the scope of this paper. As an

example, if an inverter is associated with an energy storage system, it might happen that the power from PV panels would have to be limited if the batteries are fully charged and the solar irradiation is too high [28]. To carry out this mode of operation, a sinusoidal current (SC) control strategy is derived from the perfect harmonic cancelation (PHC) strategy [29]. Hence, when the RPPT mode is activated, the reference currents in the $0dq$ power-invariant reference frame ($\mathbf{i}_{PR(0dq)}^*$) are calculated from the active power setpoint P^* and grid voltages as follows:

$$\mathbf{i}_{PR(0dq)}^* = \frac{P^*}{u_{1,d}^+} \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix}, \tag{3}$$

where $u_{1,d}^+$ is the d-axis component of the positive-sequence fundamental grid voltage vector $\mathbf{u}_1^+ = (u_{1,a}^+\ u_{1,b}^+\ u_{1,c}^+)^T$. From the grid voltage $\mathbf{u}$, an auto-adjustable synchronous reference frame (ASRF) phase locked-loop [30] extracts the positive-sequence fundamental vector, $\mathbf{u}_1^+$ and its phase angle θ_1^+. Afterwards, the block $abc/0dq$ applies the Park transformation to obtain $\mathbf{u}_{1(0dq)}^+ = (0\ u_{1,d}^+\ u_{1,q}^+)^T$.

Finally, whatever mode (MPPT or RPPT) is selected, the reference current vector $\mathbf{i}_P^*$ is obtained by means of the inverse transformation $0dq/abc$.

2) REACTIVE POWER CONTROL (Q MODE)

Concurrently and, according to economic reasons, based on tariff incentives, reactive power management or PCC voltage support can be provided by several inverters installed in a specific facility, controlled in a collaborative way under a central EMS. Thus, a fundamental three-phase reactive power

setpoint ($Q_1^* > 0$ to be injected or $Q_1^* < 0$ to be absorbed) would be sent to an individual inverter.

To accomplish with the reactive power setpoint, a quadrature SC (QSC) control strategy is used in this case, which is also derived from the PHC strategy [29]. This approach causes the currents injected into the grid are sinusoidal, balanced, and in quadrature with the positive-sequence fundamental grid voltages (lagging 90° for $Q_1^* > 0$ or leading 90° for $Q_1^* < 0$). Thus, in Q mode, currents in the 0dq power-invariant reference frame are calculated from the fundamental reactive power setpoint Q_1^* and grid voltages by the following current vector:

$$\mathbf{i}_{Q(0dq)}^* = \frac{Q_1^*}{u_{1,d}^+} \begin{bmatrix} 0 \\ 0 \\ -1 \end{bmatrix}. \quad (4)$$

Likewise, the reference current vector in the *abc* frame $\mathbf{i}_Q^*$ is obtained by means of the inverse transformation 0dq/*abc*.

3) LOAD CURRENT HARMONICS AND IMBALANCE MITIGATION (HI MODE)

The objective of this mode is to compensate the harmonic and unbalanced currents demanded by the loads connected at the PCC, so that the inverter behaves as an APF.

The load current can be decomposed into the following terms: $\mathbf{i}_L = \mathbf{i}_{L1}^+ + \mathbf{i}_{L1}^- + \mathbf{i}_{L1}^0 + \mathbf{i}_{Lh}$, where $\mathbf{i}_{L1}^+$, $\mathbf{i}_{L1}^-$ and $\mathbf{i}_{L1}^0$ are the positive-sequence, negative-sequence and zero-sequence fundamental components, respectively, and $\mathbf{i}_{Lh}$ the harmonic component. A total harmonic and imbalance compensation (THIC) control strategy is proposed aiming that the inverter current is equal to the harmonic and fundamental unbalanced components of $\mathbf{i}_L$, that is:

$$\mathbf{i}_{HI}^* = \mathbf{i}_L - \mathbf{i}_{L1}^+. \quad (5)$$

The synchronous reference frame (SRF) block is in charge to extract $\mathbf{i}_{L1}^+$ from the load current vector $\mathbf{i}_L$, by using the positive-sequence fundamental phase angle provided by the ASRF block; thus obtaining $\mathbf{i}_{L1}^+$ angle with respect to $\mathbf{u}_1^+$ angle.

The reference current in (5) must be saturated to ensure the 3L-T-type qZS inverter does not exceed its nominal current I_N. Therefore, the maximum RMS value of the reference current for the *HI* mode is obtained as

$$I_{HI,\max} = \sqrt{I_N^2 - I_P^2 - I_Q^2}, \quad (6)$$

where I_P and I_Q are the RMS values for $\mathbf{i}_P^*$ and $\mathbf{i}_Q^*$, respectively. Finally, the reference current vector is obtained from the equations below.

$$\mathbf{i}_{HI}^* = \mathbf{i}_L - \mathbf{i}_{L1}^+ \quad \text{if } I_{HI} \leq I_{HI,\max}$$
$$\mathbf{i}_{HI}^* = \mathbf{i}_L - \mathbf{i}_{L1}^+ \frac{I_{HI,\max}}{I_{HI}} \quad \text{if } I_{HI} > I_{HI,\max}, \quad (7)$$

where I_{HI} is the highest RMS value of the components of $\mathbf{i}_{HI}^*$.

B. CURRENT CONTROLLER

Once the reference currents are calculated, a current controller (block called CC in Figure 2) is used to ensure that the inverter output currents will track such references. A dead-beat control technique is used for this purpose. This is a well-known discrete control technique based on the idea of reducing to zero the error in the controlled variable at the end of the control period. The operation principle applied in this paper is explained below for the phase *a*, with the help of Figures 1 and 3.
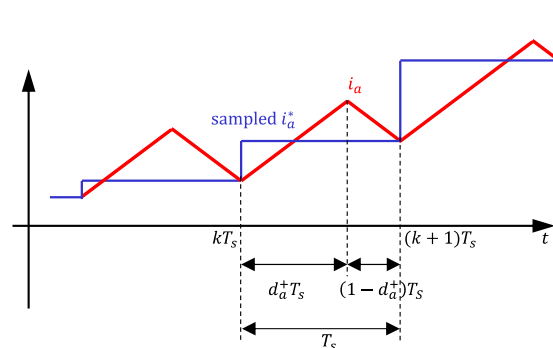

FIGURE 3. Dead-beat control technique operation to follow a reference current.

Since the inverter voltage u_a' and the grid voltage u_a are connected via a L-type filter, the following continuous-time dynamic relationship for the output i_a current can be obtained:

$$u_{Lf} = u_{a'} - u_a = L_f \frac{di_a}{dt}. \quad (8)$$

Voltage u_a' is the output voltage of the inverter, consisting of three voltage levels (U_{P0}, 0 and U_{N0}) depending on the switching state applied in a specific period. On the other hand, since the switching period T_s (1/10000 s) is significantly shorter than the grid voltage period (1/50 s), voltage u_a can be considered constant during one switching period. Therefore, for the positive current half-cycle, voltage $U_{P0} - R_f i_a - u_a$ is applied to inductance L_f terminals during the S_{1a} on-state (P state) and $0 - R_f i_a - u_a$ during the S_{1a} off-state (0 state). Note that the filter resistance (R_f) is included for a more realistic approach. Hence, the current i_a is approximately a positive ramp in the first case and a negative ramp in the second case. Then, to generate a current waveform i_a that follow the reference i_a^*, at the beginning of one switching period i_a is measured and compared with a sample of i_a^*. Calling T_{S1a} the time duration of the positive ramp, i.e., the time interval while switch S_{1a} is in the on-state (the operation of S_{3a} is complementary to S_{1a}), the signal representing the duty cycle for S_{1a} ($d_a^+ = T_{S1a}/T_s$) necessary to achieve i_a to be equal to i_a^* at the end of that period, can be calculated from the fact that the following equality must be satisfied:

$$i_a^* - i_a = \frac{\hat{U}_{PO} - R_f i_a - u_a}{L_f} d_a^+$$
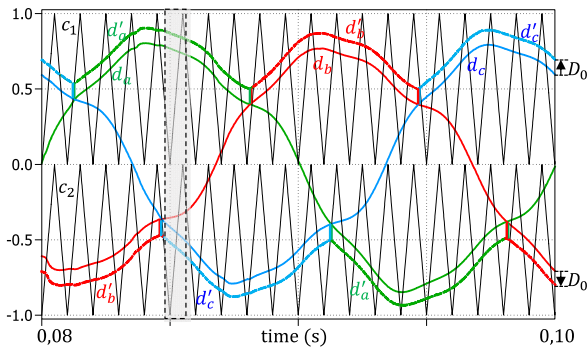$$\times T_s + \frac{0 - R_f i_a - u_a}{L_f}(1 - d_a^+)T_s. \quad (9)$$

FIGURE 4. Modulating and carrier signals for one fundamental cycle, $D_0 = 0.1$ and $m_f = 20$.

Then, the duty cycle d_a^+ for the a-leg is obtained from the equation below.

$$d_a^+ = \frac{\left(i_a^* - i_a\right)\frac{L_f}{T_s} + R_f i_a + u_a}{\hat{U}_{PO}} \tag{10}$$

On the other hand, for the negative half-cycle of the reference current, the explanation is analogous, obtaining the duty cycle for S_{2a} (the operation of S_{4a} is complementary to S_{2a}):

$$d_a^- = \frac{\left(i_a^* - i_a\right)\frac{L_f}{T_s} + R_f i_a + u_a}{-\hat{U}_{NO}}. \tag{11}$$

Signals from (10) and (11) are almost equal because $\hat{U}_{P0} \simeq -\hat{U}_{N0} \simeq \hat{U}_{PN}/2$. Nonetheless, the use of different calculation for positive and negative half cycle gives more accuracy as it considers the inequality in the voltages u_{C2} and u_{C3}. Signals d_a^+ and d_a^- can be combined in a unique signal d_a. Finally, the three output signals from the CC block will be d_a, d_b, d_c, as indicated in Fig. 2.

C. NEW CARRIED-BASED MODULATION METHOD
A carrier-based level shifted PWM (LS-PWM) in phase disposition with a variant of the maximum constant boost control (MCBC) is applied. This technique, discussed in [27] for an inverter supplying a passive load; is improved and adapted to the specific conditions of this paper. Details of this novel application of the modulation technique are discussed below.

The three modulating signals d_a, d_b, d_c are the inputs for the PWM block. They are used as in the traditional PWM scheme. Another three modulating signals d_a', d_b', d_c' are generated by shifting d_a, d_b, d_c by the ST duty cycle (D_0) up for the positive half-cycle and down for the negative half-cycle and using only the portion where the correspondent signal is maximum or minimum. The arrangement of reference and carrier signals is depicted in Figure 4, for the case of $D_0 = 0.1$. A switching frequency value of 1000 Hz (i.e., a frequency modulation index $m_f = 20$) is used for better visualization. Then, the switching signals (including the ST states) are generated by comparing the two sets of modulation signals with the two vertically disposed in-phase carrier signals c_1 and c_2.

Under these six reference signals, the converter is modulated as follows: for any phase-leg x, S_{1x} is turned on when d_x' is larger than c_1; and S_{3x} is turned on when d_x is smaller than c_1; while S_{2x} is turned on when d_x' is smaller than c_2 and S_{4x} is turned on when d_x is larger than c_2.

Generation of the gate signals is demonstrated in Figure 5 for one switching cycle T_s in the region shaded in Figure 4. S_{3x} and S_{2x} would have complementary states to S_{1x} and S_{4x}, respectively, if there were no ST states. The insertion of UST states can be observed on the overlapping of the on-states of S_{1a} and S_{3a}; and the insertion of LST states on the overlapping of the on-states of S_{2c} and S_{4c}.
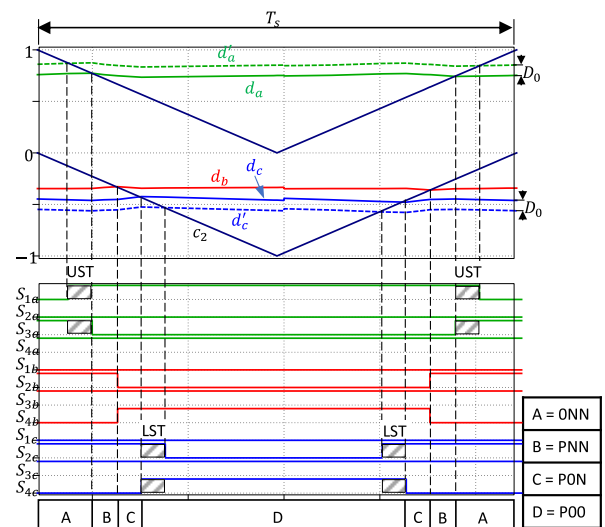

FIGURE 5. Reference, carrier, and gate signals of the proposed modulation scheme for one switching cycle T_S in the region shaded in Figure 4.

D. NEUTRAL-POINT IMBALANCE CONTROL
Symmetric operation of the 3L-T-type qZS inverter implies that $u_{C1} = u_{C4}$ and $u_{C2} = u_{C3}$. The neutral-point imbalance refers to the inequality condition of these capacitor voltages. It can be produced by incorrect control pulse generation, unbalanced loading conditions, and/or nonideal capacitance values. Neutral-point voltage imbalance increases output voltage harmonics, may drift the output voltage to unacceptable level, and may damage the switching devices and filter capacitors. In this paper, the neutral-point imbalance control method from [20] is modified and applied. The core idea is explained below.

Figure 6 is the representation for the 27 possible switching combinations of NST states for a three-level converter, commonly used in the space-vector-modulation context. As can be seen, the combinations indicated on the vertices of the inner hexagon come in pairs (e.g., P0P and 0N0), which means that both combinations generate the same output inverter voltage and are called redundant states.

Figures 7(a) and (b) present the equivalent circuits of a pair of redundant states (0NN and P00). The pairs of redundant
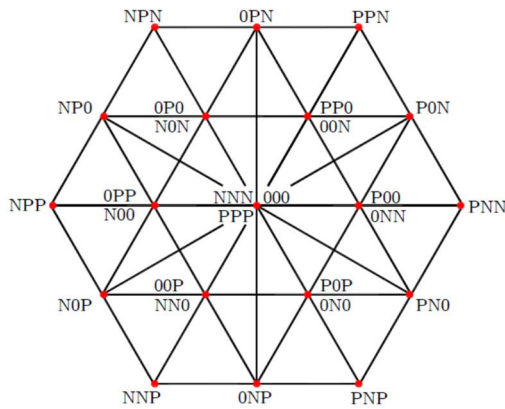
FIGURE 6. Representation for the 27 possible NST switching combinations for a 3-level inverter.
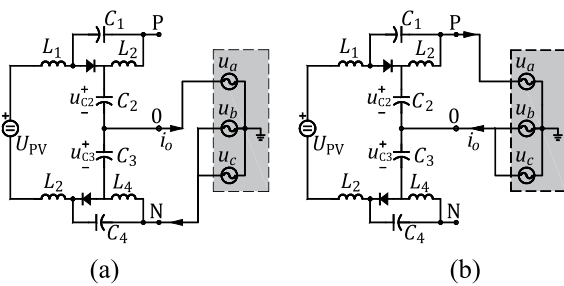

FIGURE 7. Pair of redundant states. (a) 0NN. (b) P00.

states connect a phase to the neutral-point, changing the sign of the current flowing in that direction. Therefore, 0NN discharges C_3, while P00 discharges C_2. The task of the proposed neutral-point voltage balance control is to modulate the relative duration of the redundant states within each switching cycle to maintain the balance of the neutral-point. This is achieved by adding a common shift to the carriers. Indeed, Fiure 8 shows a specific switching period, where c_1 and c_2 are the original carriers and c'_1 and c'_2 the shifted ones. As can be seen, the relative duration of states 0NN and
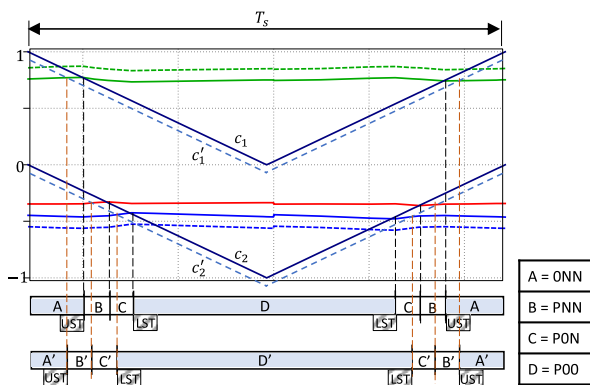

FIGURE 8. Detail of the same switching period as in Figure 5, illustrating the action of the neutral-point imbalance control.

P00 is changed while the non-redundant sates maintain the same duration. The UST and LST states are displaced but its duration remains. The figure presents the case in which u_{C2} is higher than u_{C3}, then, carriers are shifted down, reducing the time duration of 0NN and increasing the time duration of P00 in the same amount; and, consequently, u_{C2} will decrease and u_{C3} will increase. A proportional-integral (PI) controller is employed to generate this common shift, with the input signal being the difference $u_{C2} - u_{C3}$.

Considering a positive imbalance ($u_{C2} - u_{C3} > 0$) and denoting the common shift to the carriers as (γ), the control block diagram for the neutral-point imbalance regulation is displayed in Fig. 9(a). $C(s)$ and $G(s)$ indicate the continuous transfer functions of the PI controller and plant, respectively. By solving the circuit in Fig. 7(b), then the closed-loop transfer function $G_{cl}(s)$ is derived as

$$G_{cl}(s) = \frac{\left(K_p + K_i/s\right) K'}{1 + K'K_p + (K_iK')/s}, \tag{12}$$

with K_p and K_i as the proportional and integral constants of the PI controller. K' corresponds to a static gain representing $G(s)$ as follows:

$$G(s) = K' = \frac{1}{C_2} i_o. \tag{13}$$

The selection of both K_p and K_i were analysed in simulation and experimentally to be a trade-off solution between imbalance reduction and the output current quality. With the selected values of K_p and K_i, and the rated parameters i_o and C_2 the stability of the system is assured. Both the zeros and poles of $G_{cl}(s)$ are located on the left-hand side of the complex plane (Fig. 9 (b) and (c)). The action represented by the diagram of Fig. 9(a) is included into the CC block of Fig. 2

E. DC BUS VOLTAGE REGULATION

The control of the dc-link voltage (the peak voltage $\hat{U}_{PN}$ present during NST states) is realized by adjusting D_0 according to Equation (1) from the variable value of the PV voltage U_{PV}, which changes according to the solar irradiance. Because dc-link voltage is a pulsed voltage waveform, it is not appropriate as feedback signal, thus, an indirect approach is used. From capacitors C_2 and C_3 voltages, already measured for the neutral-point imbalance control, the actual magnitude of peak dc-link voltage is calculated from the following relation: $u_{C2} + u_{C3} = (1 - D_0) \hat{U}_{PN}$. In Figure 2 (top right), the calculated magnitude $\hat{U}_{PN}$ is compared with the reference magnitude $\hat{U}^*_{PN}$; then, the error signal is processed by a PI controller, generating the ST duty-cycle value D_0. The small-signal model of the single qZS network was considered for a proper selection of the PI controller [31], [32]. These parameters were selected aiming for a slower dynamic response in the dc-side than in the ac-side of the 3L-T-type qZS inverter. This duty-cycle, together with the output of the current controller, are the inputs for the PWM stage.
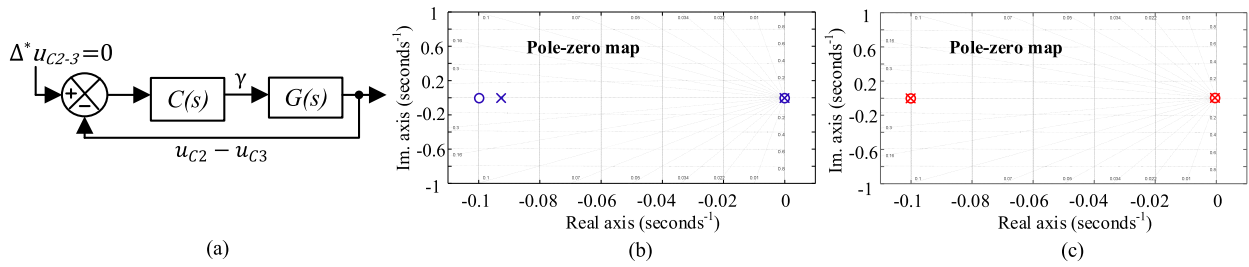
FIGURE 9. Considerations of the neutral-point voltage control approach. (a) Block diagram. (b) Pole-zero map for the simulation study case. (c) Pole-zero map for the experimental case.

III. SIMULATION RESULTS

A simulation model for the inverter system, as shown in Figures 1 and 2, has been developed in PLECS (from Plexim GmbH) simulation tool using the parameters in Table 2. These parameters have been chosen considering a possible practical application as PV inverter in the power range of around 50 kW, which is suited for commercial and industrial applications and for PV power plants. Passive element parameter values are calculated based on the guidelines given in references [33], [34].

TABLE 2. Main system parameter values.

Parameter	Simulation values		Experimental values	
Inductors $L_1 \ldots L_4$	0.5 mH		2 mH	
Capacitors $C_1 \ldots C_4$	9.9 mF		3.3 mF	
Output Filter L_f	1 mH		15.2 mH	
PV voltage U_{PV}	$600 - 900$ V		200-300 V	
dc-link peak voltage reference $\widehat{U}_{PN}^*$	900 V		292 V	
Rated Grid voltage (phase-to-neutral)	230 V		230/3 V	
Grid frequency	50 Hz		50 Hz	
Switching frequency	10 kHz		10 kHz	
Sampling frequency	10 kHz		10 kHz	
Rated output power P_{out}	50 kW		1.2 kW	
Rated output current	72.5 A		5.2 A	
Unbalanced and non-linear load rated current (3-Phase diode bridge rectifier)	30 A		3 A	
K_p and K_i of neutral-point controller	0.008	0.0008	0.08	0.008
K_p and K_i of dc-link controller	0.0005	0.05	0.001	0.1

The performance evaluation as an APF is tested by means of the inclusion of an unbalanced and no-linear load. According to [35], in commercial buildings and industrial plants, harmonic analysis and the corresponding correction measures are required when many non-linear loads (typically greater than 25% to 30% of the total load) are present or anticipated to be added. Hence, in this work, as a very demanding situation, a diode bridge rectifier load in parallel with a resistive unbalanced load is considered, with total power about 40% of the PV rated power (30 A over 72.5A). Besides, to make the grid voltage more realistic, the grid was supposed to be distorted

and unbalanced according to the limits indicated in [36], [37]. Individual distortion percentage for third harmonic is selected at its limit (5%), while for fifth and seventh harmonics the percentages (4.5% and 4%, respectively) are calculated for having a total harmonic distortion (THD) below the 8% limit. The inverse- and zero- to positive-sequence component ratios are set over the limits ($U^-/U^+ = U^0/U^+ = 3.77\%$). These values are summarized in Table 3.

TABLE 3. Grid voltages characteristics.

Harmonic Distortion (%)			Voltage THD (%)	U^-/U^+ (%)	U^0/U^+ (%)
HD3	HD5	HD7			
5	4.5	4	7.83	3.77	3.77

U^+, U^-, U^0: positive-, negative- and zero-sequence fundamental components.

As aforementioned, only the RPPT mode is tested. In this mode, the simulation starts at $t = 0$, with the following operation sequence:

1. $t = 0.02$ s. Connect PV panel. The PV voltage is set to $U_{PV} = 900$ V and $D_0 = 0$.
2. $t = 0.04$ s. Connect the inverter to the grid.
3. $t = 0.06$ s. Activate inverter operation with setpoints $P^* = 30$ kW and $Q_1^* = 10$ kVAr.
4. $t = 0.5$ s. U_{PV} changes from 900 V to 720 V. D_0 changes from 0 to 0.1 according to the PI response.
5. $t = 0.6$ s. Activate HI function.
6. $t = 0.7$ s. Setpoints change: $P^* = 45$ kW and $Q_1^* = -22$ kVAr.

From the full simulation span, the most representative cases and signals were selected. Figure 10 illustrates the buck/boost function, showing from top to bottom grid voltages (u_a, u_b, u_c) and grid currents (i_{ga}, i_{gb}, i_{gc}); inverter output currents (i_a, i_b, i_c) and their references (i_a^*, i_b^*, i_c^*); PV voltage (U_{PV}) and dc-link voltage (U_{PN}); and phase-to-phase inverter output voltage before filtering ($u_{a'b'}, u_{b'c'}, u_{c'b'}$). PV voltage is set initially to $U_{PV} = 900$V. Setpoints for active and reactive power are $P^* = 30$ kW and $Q_1^* = 10$ kVAr. In this case $U_{PV} = \widehat{U}_{PN}^*$, i.e., no boost operation is required, and the ST states are not activated, then $D_0 = 0$. At $t = 0.5$ s, U_{PV} decreases to 720 V and, consequently, according to equation (1), D_0 changes to 0.1, achieving $\widehat{U}_{PN}$ about the desired
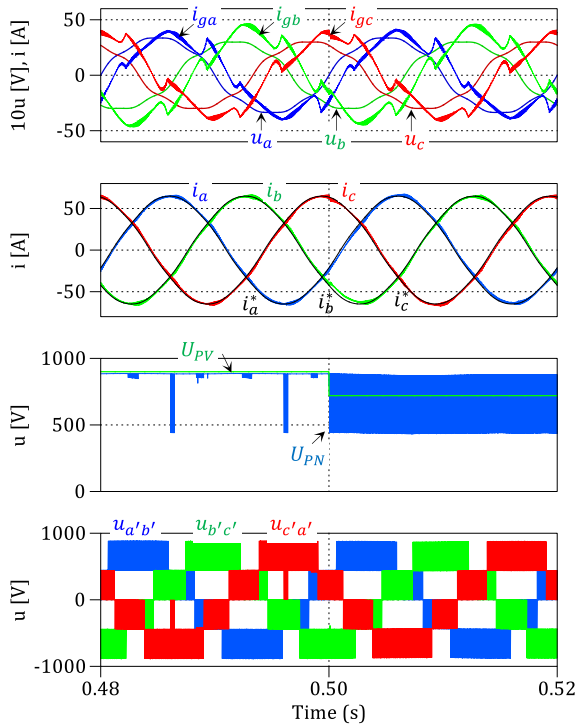
FIGURE 10. Simulation results. Buck/boost operation. $P^* = 30$ kW; $Q_1^* = 10$ kVAr. At $t = 0.5$ s, U_{PV} changes from 900 V to 720 V. From top to bottom: grid voltages (u_a, u_b, u_c) and grid currents (i_{ga}, i_{gb}, i_{gc}); inverter output currents (i_a, i_b, i_c) and references (i_a^*, i_b^*, i_c^*); PV voltage (U_{PV}) and DC-link voltage (U_{PN}); and phase-to-phase inverter output voltage before filtering ($u_{a'b'}$, $u_{b'c'}$, $u_{c'b'}$).

FIGURE 11. Simulation results. APF function. $P^* = 30$ kW; $Q_1^* = 10$ kVAr. At $t = 0.6$ s, HI function is activated. From top to bottom: grid voltages (u_a, u_b, u_c) and grid currents (i_{ga}, i_{gb}, i_{gc}); inverter output currents (i_a, i_b, i_c) and references (i_a^*, i_b^*, i_c^*); and load currents (i_{La}, i_{Lb}, i_{Lc}).

FIGURE 12. Simulation results. Setpoint changes. Initially is $P^* = 30$ kW and $Q_1^* = 10$ kVAr; at $t = 0.7$ s, active and reactive power setpoint change to 45 kW and -22 kVAr respectively. From top to bottom: grid voltages (u_a, u_b, u_c) and grid currents (i_{ga}, i_{gb}, i_{gc}); inverter output currents (i_a, i_b, i_c) and references (i_a^*, i_b^*, i_c^*).

value 900 V. The dc-link voltage is switched between $\hat{U}_{PN}$ and $\hat{U}_{PN}/2$ due to the short-circuit of only one half of the dc-link during the UST and LST states, respectively. Also, line-to-line voltages before filter preserves its waveforms during the UST and LST states to that of the non-ST operation.

Figure 11 demonstrates the correctness of the APF functionality, boosting PV voltage and following setpoints for active and reactive power simultaneously. Initially $U_{PV} = 720$ V (needing $D_0 = 0.1$ for boosting to 900 V); setpoints are $P^* = 30$ kW and $Q_1^* = 10$ kVAr and HI function is disabled. Then, at $t = 0.6$, HI function is enabled. Before HI activation, despite the unbalanced and distorted grid voltages, the inverter output currents waveforms are balanced and sinusoidal, and lagging from the fundamental component of the phase-to-neutral voltage, showing the fundamental reactive power injection. However, since load current is unbalanced and distorted, the currents injected into the grid are unbalanced and distorted. At $t = 0.6$ s, HI function is activated, consequently, inverter currents become distorted and unbalanced so that the grid currents tend to be balanced and sinusoidal. In this case, the compensation is possible because setpoints and HI compensation requirements are compatible with the inverter nominal current, i.e., the inverter rated power is not reached. Figure 12 illustrates changes in active and in reactive power setpoints and, also the saturation
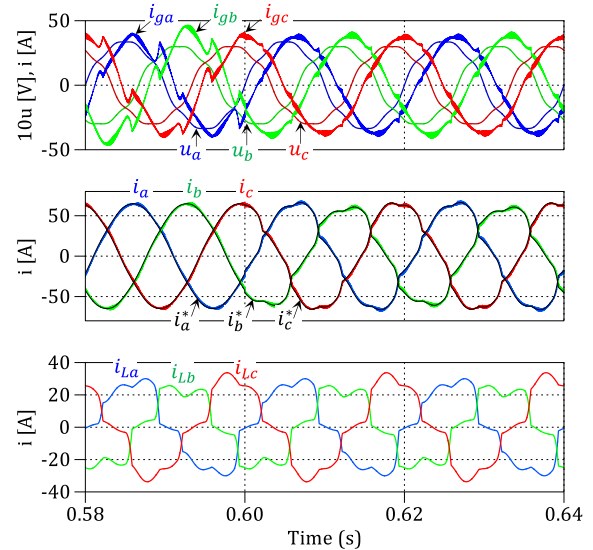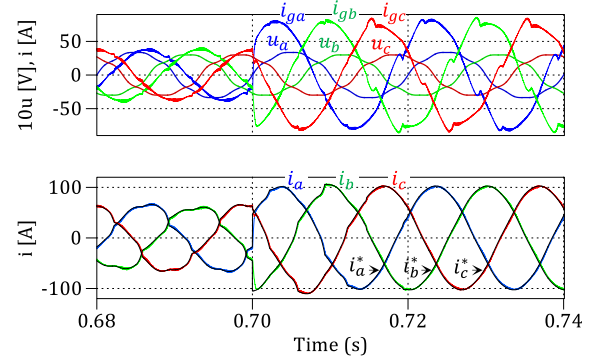
or compensation limit. Initially, conditions are the same as in Figure 11; at $t = 0.7$ s, setpoints are changed to 45 kW and -22 kVAr. With these values, the compensation requirements cannot be fulfilled without incurring equipment overload. Therefore, the inverter performs a partial compensation and grid currents are not sinusoidal nor balanced anymore.

The purpose of the simulation shown in Figs. 13 is to check the correct operation of the neutral-point imbalance compensation. The following conditions are considered for this test: $U_{PV} = 720$ V; $D_0 = 0.1$; $P^* = 30$ kW and $Q_1^* = 10$ kVAr. Since $t = 0$, a 0.5 kΩ resistor is connected in parallel to the capacitor C_3, generating a high imbalance voltage between the inner capacitors (C_2 and C_3). Before $t = 0.32$ s, the imbalance compensation is not activated, subsequently, a voltage difference of about 100 V in the inner
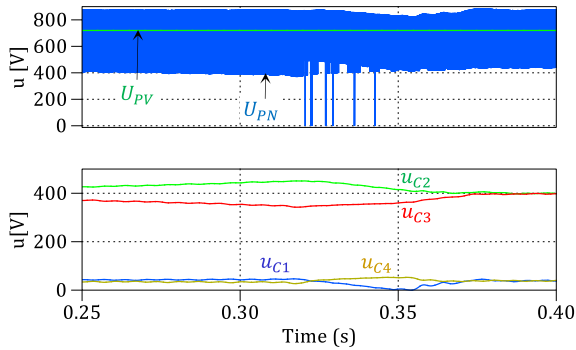
FIGURE 13. Simulation results. $D_0 = 0.1$. $U_{PV} = 720$ V; 30 kW/10 kVAr. Resistor 0.5 kΩ connected in parallel with C_3. Neutral-Point imbalance control initially disabled and then enabled at t = 0.32 s. Top: U_{PV} and U_{PN}. Bottom capacitor voltages u_{C1}, u_{C2}, u_{C3}, u_{C4}.

capacitors is observed. Once the compensation algorithm is included (time > 0.32 s), the results reach the expected values, i.e., the voltage in the inner capacitors are balanced at a value of approximately 400 V. The dc-link voltage after activating the compensation is not modified because the value of D_0 is unchanged. The transient time for the capacitor balancing is lower than 0.03 s.

IV. EXPERIMENTAL RESULTS

An experimental prototype was built to further validate the proper system performance and its main functionalities. Figure 14 shows the experimental setup implementing the system considered in Figure 1. The parameters were shown in Table 2. PV panels were emulated by the 62000H-S Solar Array Simulator from Chroma. The grid was emulated by the programmable AC Voltage Source GE 15 from CINERGIA Power Solutions. This equipment was used to create an unbalanced and distorted ac grid.
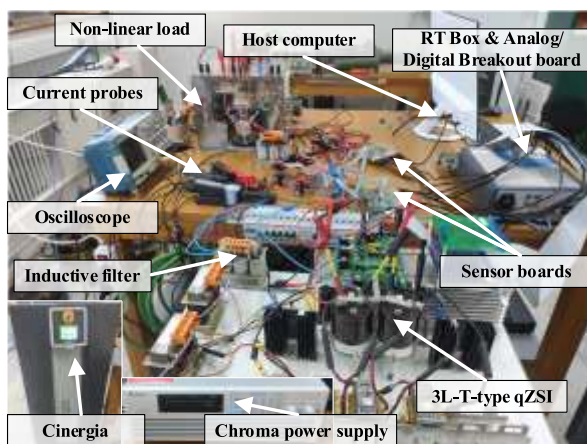

FIGURE 14. Experimental laboratory setup.

The RT Box 1 from Plexim was used as a rapid prototyping platform, equipped with analogue and digital breakout boards. The unit is based on Xilinx Zynq Z-7030

system-on-chip that embeds two CPU cores on an FPGA. The proposed strategy, current controller and modulation technique were programmed in the PLECS standalone environment in the host computer. To correctly insert the UST/LST states, digital outputs from RT Box are combined in an external PCB composed of OR and AND chips, generating the gate signals for each IGBT (S_{1a}, S_{2a}, S_{3a}, S_{4a}, S_{1b}, S_{2b}, S_{3b}, S_{4b}, S_{1c}, S_{2c}, S_{3c}, S_{4c}), which finally interface with the 3L-T-Type driver board. The driver board is the AT-NPC 3-level 12in1 provided by FUJI, based on the chip ACPE-333J from Avago Technologies with a built-in function for short-circuit protection. The power circuit is built with the 12MB150VX-120-50OGBT module from FUJI, formed by 12 RB-IGBT and designed to withstand 1200 V and 50 A in one package with reduced size and substantial low power loss.

The three grid voltages, the capacitors C_2 and C_3 voltages, the three load currents and the three output inverter currents are necessary to be measured. For this purpose, the measurement stage is equipped with two isolated voltage and current sensing modules USM-3IV from Taraz Technologies, each equipped with three voltage and three current sensors which perform with high precision, good linearity, and low common-mode disturbance. These measured quantities are analog inputs for the RT Box control unit. In addition, since the RT Box has waveform processing and display functions, the control unit itself is used to obtain the waveforms presented below.

Dynamic and steady states performance are investigated. An overview of experimental results is presented here. Figure 15 shows the behaviour when the inverter operates injecting active power to grid with unity power factor.
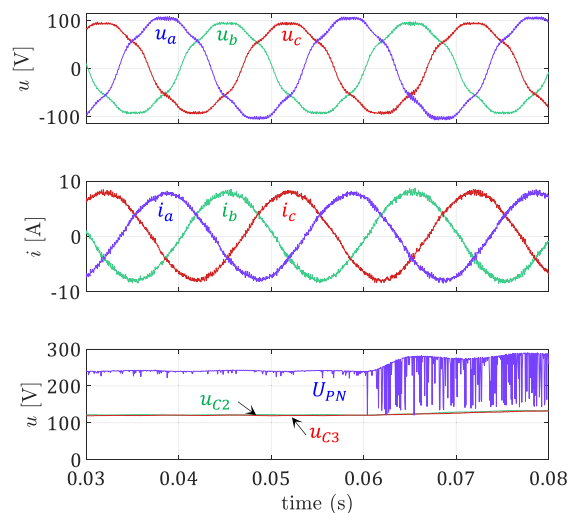

FIGURE 15. Experimental results. Load disconnected. $P^* = 1200$ W; $Q_1^* = 0$ var. At t = 0.06 s, D_0 steps from 0 to 0.1. From top to bottom: grid voltages; inverter output currents; and dc-link voltage and voltages of capacitors C_2 and C_3.

PV voltage is set to $U_{PV} = 245$ V and active and reactive power setpoints are $P^* = 1200$ W and $Q_1^* = 0$ var. The unbalanced and non-linear load is disconnected, and hence it does not provide any APF functionality. Consequently, grid injected currents are the same that inverter output currents, and they are balanced and sinusoidal. Initially, D_0 is 0 and at $t = 0.6$, it steps to 0.1. Before 0.6 s no ST states are applied and dc-link voltage is nearly constant; after 0.6 s, UST/LST states are applied, then dc-link voltage is now switching between the half and the peak value, as expected. Output current waveforms are not affected by the change. Capacitor C_2 and C_3 voltages are maintained almost equal, demonstrating a proper performance of the neutral-point imbalance control in this situation.

Figure 16 illustrates the dynamic response to a change reactive power setpoint. Voltage U_{PV} is 245 V and duty cycle D_0 is set to 0.08. Initially active power is set to 900 W and reactive power is set to 300 var. Then, at 0.06 s, Q_1^* is changed to -300 var (maintaining $P^* = 900$ W). Amplitudes of the inverter output currents do not change while the relative phase displacements change at 0.06 s from lagging to leading the respective grid voltage waveforms. Transient response time is very much lower than the grid period. Figure 17 demonstrates how the system performs its APF capability, injecting active and reactive power into the grid ($P^* = 900$ W. $Q_1^* = 300$ var) and boosting U_{PV} voltage (from 245 V with $D_0 = 0.08$). HI function is activated at $t = 0.06$ s. Before that instant, inverter output currents are balanced and sinusoidal, while grid current are unbalanced and distorted, reflecting the load currents. After that instant, the control strategy forces the inverter output currents to be unbalanced and distorted in order to make the grid currents become balanced and sinusoidal.
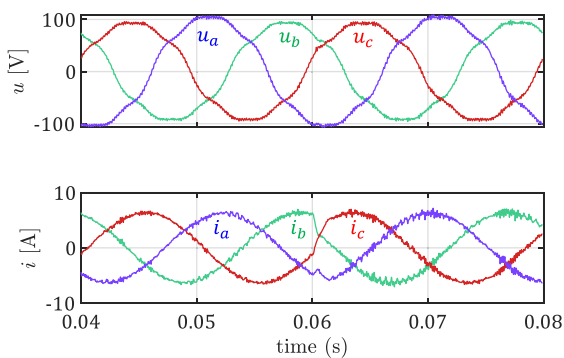

FIGURE 16. Experimental results. Load disconnected. $D_0 = 0.08$. Top: grid voltages. Bottom: inverter output currents for a Q_1^* step applied at t = 0.06 s from 300 to -300 var, with constant $P^* = 900$ W.

A Fourier analysis of the experimental measured currents in Figure 17 was performed. To summarize the results, Table 4 gathers THD calculated according to [34], and imbalance index I^-/I^+, for both cases, with and without APF functionality activated. Before APF activation, and despite the non-ideal grid voltage, the generated inverter output currents
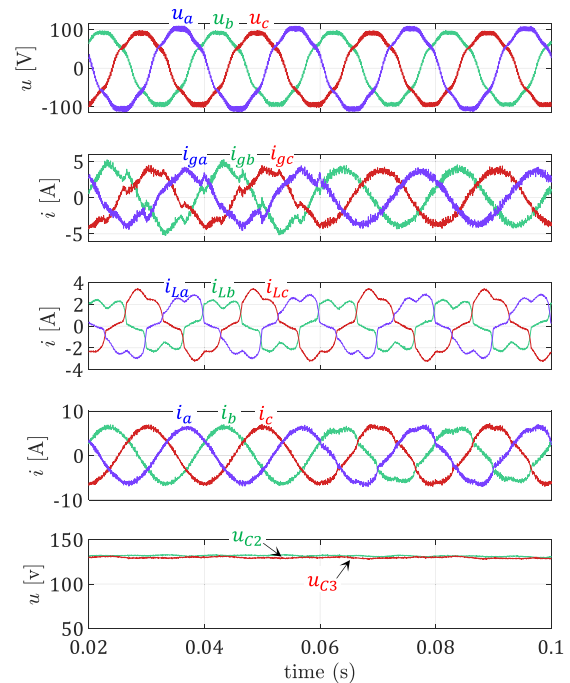

FIGURE 17. Experimental results. $P^* = 900$ W; $Q_1^* = 300$ var; $D_0 = 0.08$. At t = 0.06 s, HI compensation function is activated. From top to bottom: grid voltages; grid currents; load currents; inverter output currents; and voltages of capacitors C_2 and C_3.

TABLE 4. Quality indexes of load, inverter, and grid currents.

Current	Parameter	No APF operation	APF operation
Load currents	THD	27.37 %	
	I^-/I^+	13.17 %	
Inverter currents	THD	1.59 %	9.72 %
	I^-/I^+	0.53 %	5.06 %
Grid currents	THD	16.37 %	3.635 %
	I^-/I^+	8.94 %	1.94 %

are near balanced and undistorted, i.e., they exhibit low harmonic distortion (1.59%) and imbalance index (0.53%), while under APF operation these values increase. In contrast, the high THD value exhibited by grid currents (over 16%) when the inverter operates as a traditional PV inverter is reduced to a value below 4% and I^-/I^+ goes from about 9% to about 2% when simultaneously the system operates as an APF. Figure 18 shows a detailed view around the instant 0.06 s, showing the inverter output current for the three phases and their respective reference currents. It can be appreciated how the measured inverter currents follow the calculated references very closely, thus proving proper performance of the deadbeat controller.

In all the cases presented so far, the control of the dc-link internal voltages has proven to work well. In fact, without this control, u_{C2} and u_{C3} would progressively deviate, eventually making it impossible for the inverter to operate.
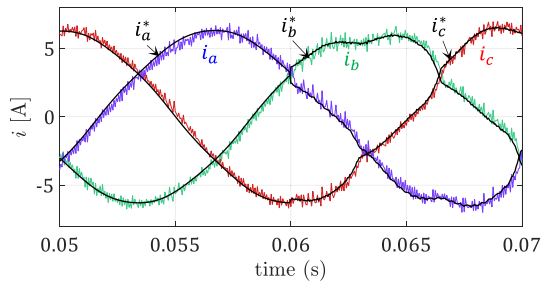
FIGURE 18. Experimental transient response of the proposed current controller to a change in HI compensation function at t = 0.06 s. Detailed view showing inverter output currents (i_a, i_b, i_c) and reference currents (i_a^*, i_b^*, i_c^*).

Even so, an additional test of this control is carried out in a different scenario, provoking an extreme unbalanced situation. Figure 19 shows the main signals before and after this control loop activation. A resistor was connected in parallel to C_3 ($R = 1$ kΩ), this produces a hard imbalance (which subsequently settles u_{C2} and u_{C3} at 150 V and 100 V, respectively, as shown in this figure). At instant-1 (0.55 s), the converter, including the neutral-point imbalance control algorithm, starts to operate and thus, u_{C2} and u_{C3} are made equal about instant-2 (0.85 s). The test was conducted in boost operation ($U_{PV} = 245$ V with $D_0 = 0.08$). In this figure, an effective voltage compensation is demonstrated, without any undesired overvoltage or overcurrent. This capability improves the entire inverter reliability. Moreover, output currents tracking is substantially improved once the voltage imbalance is eliminated. Zoomed views allow this to be seen in more detail.
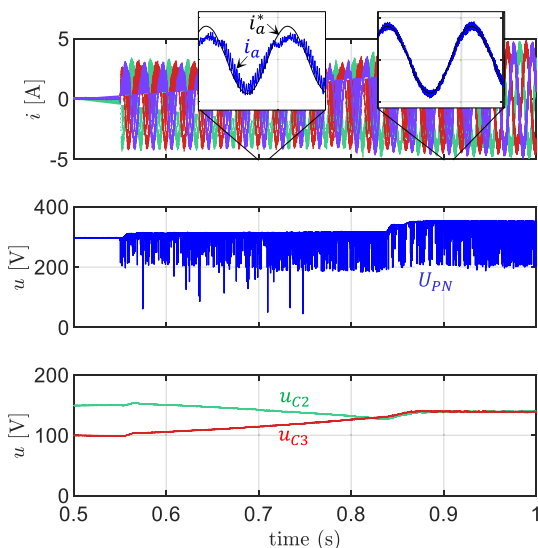

FIGURE 19. Experimental results. Dynamic response of the neutral-point imbalance control. Resistor 1 kΩ connected in parallel with C_3. Control is initially disabled and then it is enabled at t = 0.55 s. From top to bottom: inverter output currents and detailed zoom views for phase a; dc-link voltage and voltages of capacitors C_2 and C_3.

V. CONCLUSION

In this work, the single stage 3L-T-type qZS inverter topology is applied as a dual-purpose inverter: controlling the active power injected into the grid (extracting the maximum or a reference power from PV panels) and operating as a shunt active power filter simultaneously. An improved deadbeat current controller and a level-shifted carrier-based modulation technique, inserting upper and lower half dc-link ST states with inner capacitors voltage balancing, were programmed, and successfully tested. The modulation technique has proved to be a much simpler alternative to the SVM-based approach previously proposed in literature.

The performance of the inverter has been investigated extensively. Simulation study and experimental tests have proven a proper operation as an APF, under unbalanced and distorted grid voltages, in the presence of a very demanding case of unbalanced and non-linear load, for different PV voltages and different active and reactive power setpoints. Besides, the use of UST/LST states results in semiconductors withstanding half of the value of the blocking voltage with respect to the traditional full ST.

Since the characteristics of the proposed system are particularly suitable for high power applications, such as those found in commercial and industrial installations and/or in multi-megawatt PV plants, this paper reinforces the concept of using the converters in such installations for active power filtering on a 24/7 basis, providing ancillary services and improving the power quality of the grid.

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