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3-V Input, 70-V Output, Fully Integrated Hybrid Charge Pump

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ABSTRACT A novel integrated-circuit charge-pump (CP) voltage multiplier conceived for high multiplying factors is proposed. The solution exploits a mixed architecture which merges both Cockcroft-Walton and Dickson topologies, by using on-chip 12-V poly-poly capacitors and 3.3-V CMOS transistors, maximizing the output voltage at the minimum silicon size. The proposed CP has been designed to supply a fully integrated driver for miniaturized motors in Micro Electro Mechanical Systems (MEMS) technology. It is conceived to boost the power-supply voltage to values higher than those that either a Dickson (D), Fibonacci (F), Cockroft-Walton (CW) or Serial-Parallel (SP) fully integrated CPs can generate in the selected technology process. Indeed, the output voltage of the former two CPs is limited by voltage constraints of on-chip capacitors while the multiplication efficiency of the latter two is impacted by high values of on-chip stray capacitors. Specifically, the target > 70 V output voltage has to be internally generated starting from the provided minimum power-supply voltage of 3 V. Furthermore, a mathematical model is proposed to evaluate the open load output voltage and the equivalent output resistance.

INDEX TERMS Charge pumps, voltage multipliers, Cockcroft-Walton CP, Dickson CP, Fibonacci CP, serial-parallel CP.

I. INTRODUCTION

The first voltage multiplier was published by Schenkel in 1919 [1] with discrete capacitors and valve diodes. A few years later, in 1923, Marx filed a patent application [2] describing a voltage multiplier based on Serial to Parallel architecture implemented with discrete capacitors, very high value resistances and spark gap switches for generating high surge voltages. In 1932, Cockcroft and Walton [3] proposed a new voltage multiplier for generating voltages greater than those achievable with the Schenkel circuit, up to several million volts, those which could be easily handled by electromagnetic transformers for production of high velocity positive ions, using capacitors with lower operative range. In this type of application, however, the discrete capacitors can be made sufficiently large for efficient multiplication and adequate current capability while on-chip capacitors have maximum values of a few hundred pF and relatively high stray capacitances; as a result, initially, the mentioned CPs did not have large application in integrated circuits because they were very sensitive to the stray capacitances. Subsequently, in 1973, a CP based on the Schenkel topology, that is quite insensitive to parasitic capacitances, was patented for the first time in a monolithic form by Luscher [4] who replaced the valves with MOS diodes. This circuit became very popular with the article published by Dickson in 1976 [5] and is better known as the Dickson multiplier. Another popular CP using MOS switches was published by Ueno *et al.* in 1991 [6], called Fibonacci multiplier because the generated output voltage is proportional to the Fibonacci sequence.

In the last three decades, on-chip CPs, mainly based on the Dickson architecture insensitive to the bottom stray capacitance, have been widely used in smart power ICs for driving the output power transistors, in non-volatile memory circuits for programming and erasing memory cells, and in low-voltage applications such as energy harvesting [7]–[10].

On the other side, as anticipated, the Cockcroft-Walton multiplier has been used for those applications where high voltages are requested; more specifically, in converters with ac input for low current applications and when a high voltage transformer winding is not convenient [11]–[16].

More recently, Serial-Parallel [17]–[19] and Fibonacci CPs [20]–[25] have been employed for lower voltage applications in discrete and monolithic solutions, as well as new Hybrid CPs, based on a combination of Cockcroft-Walton and Dickson architectures, have been described in [26]–[28].

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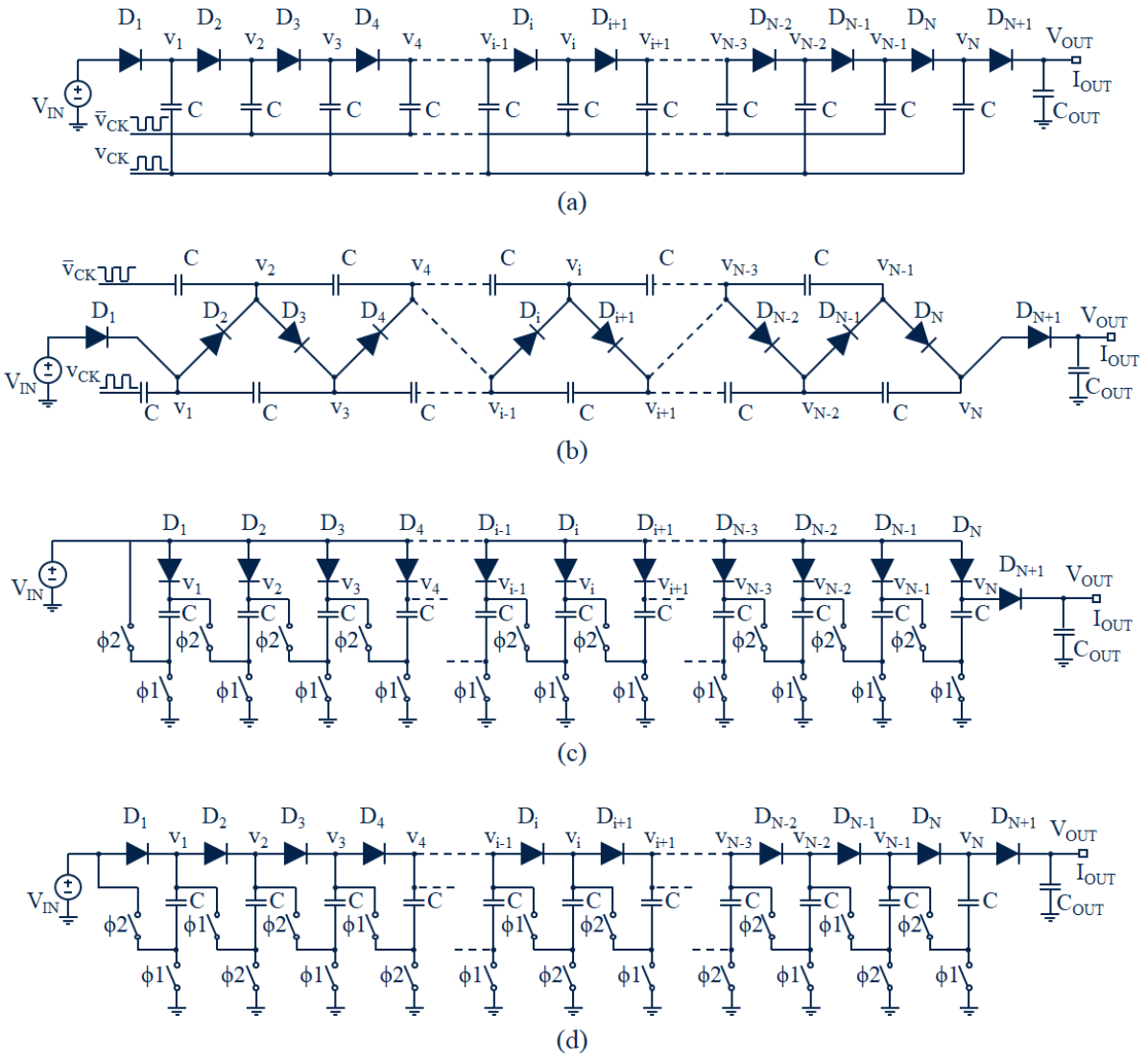

FIGURE 1. Dickson (a), Cockcroft-Walton (b), Serial-Parallel (c) and Fibonacci (d) *N*-stage CPs.

Also notable is the new on-chip Hybrid CP in which a configurable architecture of Cockcroft-Walton and Dickson stages have been devised for extremely low voltage applications [29], [30].

In this paper a novel charge pump to supply a fully integrated driver for miniaturized motors in MEMS technology is proposed. In this application, the multiplied voltage gain and the voltage efficiency are key parameters, while the power efficiency is not relevant due to the very low driving current, a few dozen μA, required to drive the motors.

Unlike previous Hybrid CPs [19], [26]–[30], where two different topologies are cascaded in series, the proposed CP merges both Dickson and Cockcroft-Walton topologies and has a completely new arrangement of the pumping capacitors which allows for the uniform distribution of the voltage on them, minimizing the stress and maximizing the multiplication factors, otherwise unfeasible with previous CPs. Indeed, a 24-stage dual branch CP, with each pumping capacitor of 25 pF, was designed and fabricated in 0.35-μm STMicroelectronics BCD process. It was demonstrated that, starting from 3 V supply, an output voltage higher than 70 V can be achieved by using medium-voltage on-chip capacitors and low-voltage CMOS transistors.

The paper is organized as follows. Sec. II summarizes the most conventional CPs. Sec. III describes the different configurations of the proposed CP, the working principle, and a comparison of the key parameters with the most popular CPs. Sec. IV illustrates the proposed CP including stray capacitors and demonstrates the matching of the mathematical model with simulation results. Sec. V describes the physical implementation. Sec. VI shows the measurement results comparing the performance with previous works and highlighting pros and cons. Finally, Sec. VII summarizes the author's conclusions. The Appendix reports the mathematical analysis.

II. MOST CONVENTIONAL CHARGE PUMPS

The most popular CPs [30]–[39] with arbitrary *N*-stage are shown in Fig. 1. They consist of *N* pumping (coupling or flying) capacitors *C* that pump the charge from the input

to the output, one storage capacitor C_{OUT} that stores the charge and makes stable the voltage at the output node V_{OUT}, $N+1$ diodes and, for the last two CPs, $2N$ switches properly driven that transfer the charge in only one direction towards the output node.

Even though the Serial-Parallel and Fibonacci CPs are commonly described with switches only, here they are drawn with diodes for uniformity with the other two CPs. The principle of operation, although well known, is summarized below. For the Dickson and Cockcroft-Walton CPs the pumping capacitors, driven by two clocks in anti-phase, are alternatively charged during each half period of the clock cycle. So, charge packets are pumped through the diode chain boosting up the output node. For the Serial-Parallel CP the pumping capacitors are all charged in parallel through the diodes and then connected in serial through the switches to transfer the charge to the output node. For the Fibonacci CP the pumping capacitors are alternatively charged through the diodes and connected among them through the switches to boost up the output node.

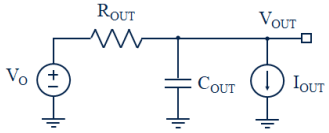

FIGURE 2. CP Equivalent Circuit.

Fig. 2 shows the simple equivalent circuit of a CP, where V_O is the voltage generated in open load condition, and R_{OUT} is the equivalent output resistance.

From the equivalent circuit the output voltage V_{OUT} can be obtained

$$V_{OUT} = V_O - R_{OUT} \cdot I_{OUT} \tag{1}$$

Parameters of (1) are summarized below for all the above-mentioned CPs, while the detailed mathematical analyses are reported in the Appendix. Hence, the open load output voltage in ideal operating condition, that happens when parasitic capacitances are negligible, is

$$V_{O,ideal} = \begin{cases} V_{IN} - (N+1)\,V_D + NV_{CK} & D, CW \\ V_{IN} - (N+1)\,V_D + NV_{IN} & SP \\ V_{IN} - \left(\sum_{i=1}^{N+1} F_i - 1\right) V_D + \sum_{i=1}^{N} F_i V_{IN} & F \end{cases} \tag{2}$$

where

V_{IN}	is the input voltage of the circuit,
V_{CK}	is the swing voltage of the clock signals,
V_D	is the forward voltage drop of the diodes,
f	is the clock or switching frequency,
F_i	is the i-th element in the Fibonacci series.

$V_{O,ideal}$ matches with results of (7) reported in [5] for Dickson CP without top stray capacitor, with results of (11) in [12] for Serial-Parallel CP replacing diodes with switches, and with results of (2) in [24] for Fibonacci CP replacing diodes with switches.

The equivalent output resistance calculated in ideal operating condition and in Slow Switching Limit (SSL), that occurs when the clock period is much longer than the time constant associated with the resistance of the diodes and the capacitance of the pumping capacitors, is

$$R_{OUT,ideal} = \begin{cases} \frac{1}{f \cdot C} N & D, SP \\ \frac{1}{f \cdot C} \cdot 2 \sum_{i=1}^{\frac{N}{2}} i^2 & CW\ N\ even \\ \frac{1}{f \cdot C} \cdot \left[\sum_{i=1}^{\frac{N+1}{2}} i^2 + \sum_{i=1}^{\frac{N-1}{2}} i^2\right] & CW\ N\ odd \\ \frac{1}{f \cdot C} \cdot \sum_{i=1}^{N} F_i^2 & F \end{cases} \tag{3}$$

$R_{OUT,ideal}$ matches with results of (8) reported in [5] for Dickson CP without top stray capacitor, with results of (11) in [12] for Serial-Parallel CP, and with results of (39) in [25] for Fibonacci CP.

It can be observed that, for $V_{CK} = V_{IN}$ and $N = 2$, all CPs have the same $V_{O,ideal}$ and the same $R_{OUT,ideal}$.

As known, these CPs can be also implemented in a Dual Branch (DB) architecture with the advantage that the voltage ripple on the output node, as well as the current peaks in the capacitors and diodes, are halved. Moreover, if the value of the pumping capacitors is halved with respect to the Single Branch (SB) configuration, the total amount of capacitance does not change since in the dual branch architecture there are $2N{\cdot}C/2$ capacitors, while in the single branch there are $N{\cdot}C$ capacitors. That said, it is known that for the Dickson, Serial-Parallel and Fibonacci dual branch CPs the open load output voltage and the equivalent output resistance remain the same as those reported in (2) and (3), while, for the dual branch Cockcroft-Walton CP, shown in Fig. 3, only $R_{OUT,ideal}$ changes as given in below

$$R_{OUT,ideal} = \frac{1}{f \cdot C} \sum_{i=1}^{N} i^2 \quad CW\ DB \tag{4}$$

In fact, it is worth noting that the dual branch architecture is by construction completely symmetric and for this reason (4) is valid for both N even and odd. Moreover, for a given number N of stages, this architecture has a double number of pumping capacitors per branch with the benefit that the voltage across each pumping capacitor is halved compared to that of the single branch architecture. On the contrary, the equivalent output resistance is much higher because it grows dramatically with the number of stacked pumping capacitors.

As anticipated, on-chip CPs have relatively high values of stray capacitances which impact the output voltage. More specifically, top plate parasitic capacitors are only considered in the Dickson CP, as bottom plate stray capacitors impact the current consumption only, because they load the clock lines. Instead, in the Cockcroft-Walton, Serial-Parallel

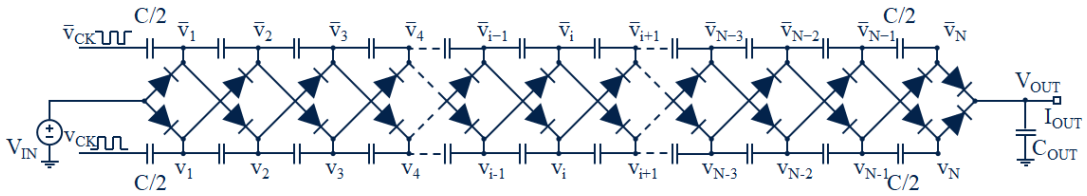

FIGURE 3. Cockcroft-Walton N-stage CP in a DB architecture.

and Fibonacci CPs, both bottom plate and top plate parasitic capacitors have to be considered. In his original paper, Dickson wrote that the Cockcroft-Walton CP has two main limitations:

1) Efficient multiplication will occur only if the pumping capacitors are much greater than the stray capacitors.
2) The output impedance increases rapidly with the number of multiplying stages.

The first limit appears also evident from (A9), where the influence of the top and bottom stray capacitors on the output voltage grows rapidly with the power of N. In fact, as the pumping capacitors are connected in series, it is hard to generate significantly high voltages if the number of multiplying stages is increased beyond a critical limit, which typically consists of a few units, heavily dependent on the ratio between the stray and pumping capacitors. The second item, according to (A10), has a direct impact on the silicon size in a monolithic integrated circuit implementation, since the total area of pumping capacitors of the Cockcroft-Walton CP increases dramatically with the number of multiplying stages.

On the contrary, the Dickson CP, when implemented in a monolithic integrated circuit, in some circumstances is not always feasible due to the well-known voltage limitations of on-chip capacitors. In fact, low voltage MOS capacitors, always available, limit the maximum voltage generated by the CP while high voltage capacitors like Metal Oxide Metal (MOM) are not so common and, when available, have very low specific value and cannot cover large silicon areas because oxide defects cannot be screened out efficiently [40].

The Serial-Parallel CP, like the Cockcroft-Walton one, is another architecture sensitive to parasitic capacitances as well as capable of using pumping capacitors with low voltage stress ratings but both switches and diodes are progressively subjected to high voltages getting closer to the output node.

The Fibonacci CP offers the highest possible boosting ratio for a given N and, with an equal area occupation, it has similar performance in many aspects compared to the Dickson one in ideal operating conditions [32]. However, it has the same limitation in that the voltage stress on pumping capacitors increases progressively getting closer to the output node. Furthermore, like the Serial-Parallel CP, the switches and diodes are progressively subjected to high voltages and the multiplication efficiency is heavily impacted by both top and bottom stray capacitors.

III. PROPOSED CHARGE PUMP

To overcome the above-mentioned limitations a novel hybrid architecture which merges both Cockcroft-Walton and Dickson CPs is proposed. Differently from the other Hybrid CPs, described in [19] and [26]–[30], where two different topologies are cascaded in series, this solution minimizes the stress on the pumping capacitors, thanks to the uniform distribution of the voltage on them. For example, in [29] and [30] the voltage on the capacitors of the Dickson stages grows as they get closer to the output node. The mix between the two topologies can be freely chosen in such a way to select any kind of on-chip capacitors exploiting the maximum voltage capability. Indeed, medium voltage on-chip capacitors, like Metal Insulator Metal (MIM) and Poly-Poly (P1P2) capacitors, have very low stray capacitances and are usually present in many technology platforms. Different configurations of the proposed novel architecture are shown in Fig. 4.

Referring to the first option, i.e. the single branch with diodes of Fig. 4a, the pumping capacitors are divided into N/M clusters. In the first two clusters, the capacitors connected to the nodes from v_1 to v_{2M} have the lower terminal connected to the clock signals, like in the Dickson CP, and the higher terminal connected to the diode chain, progressively towards the output. In the intermediate clusters, the pumping capacitors are stacked on the previous ones, like in the Cockcroft-Walton CP; they have the lower terminal connected to the higher terminal of the previous two clusters of capacitors and the higher terminal connected to the diode chain, progressively towards the output. Similarly, in the last two clusters, the pumping capacitors are stacked on the previous ones, having the lower terminal connected to the higher terminal of the previous two clusters of capacitors and the higher terminal connected to the diode chain, progressively towards the output. To summarize, the pumping capacitors belonging to their own cluster are in parallel like in the Dickson CP, while they appear stacked among different clusters like in the Cockcroft-Walton CP.

The operation is similar to the other CPs. In the first half clock period, when v_{CK} is low and $\bar{v}_{CK}$ is high, the pumping capacitors driven by v_{CK} are charged to a more positive voltage. They receive the charge packets through the odd diodes from the pumping capacitors driven by $\bar{v}_{CK}$, which are contextually discharged. In this phase, the first pumping capacitor is directly charged from the input voltage. In the second half clock period, when v_{CK} is high and $\bar{v}_{CK}$ is low, the pumping capacitors driven by v_{CK} are discharged. They

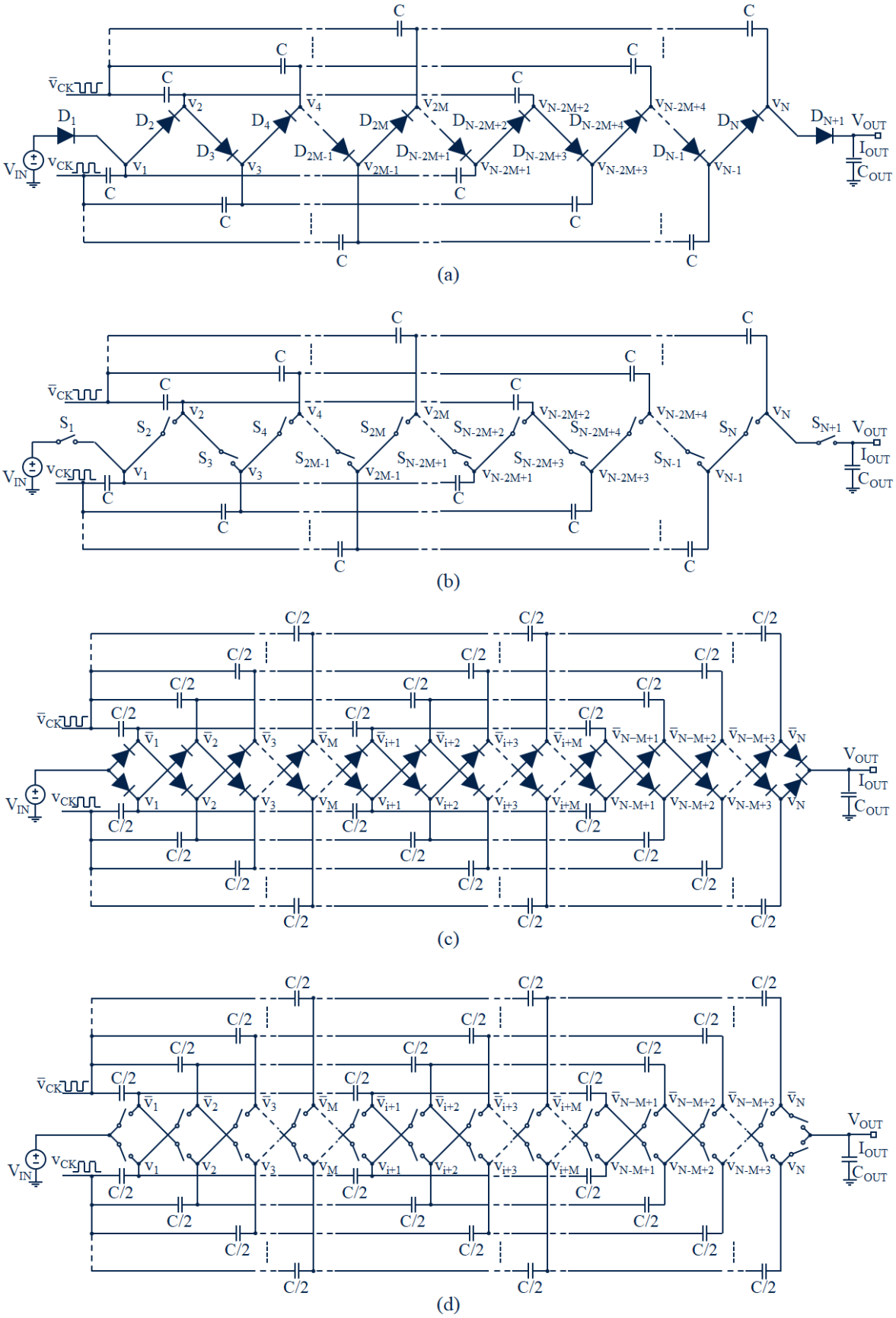

FIGURE 4. Proposed *N*-stage CP with diodes (a), with switches (b), Dual Branch with diodes (c) and Dual Branch with switches (d).

TABLE 1. Charge pump key parameters comparison in ideal conditions.

	Dickson	Cockcroft-Walton	Dual Branch CW	Serial-Parallel	Equal cap Fibonacci	Scaled cap Fibona. [32]	Sing Branch Proposed CP	Dual Branch Proposed CP
Max voltage on capacitors	$N{\cdot}V_{IN}$	$2\,V_{IN}$	V_{IN}	V_{IN}	$F_n{\cdot}V_{IN}$	$F_n{\cdot}V_{IN}$	$2M{\cdot}V_{IN}$	$M{\cdot}V_{IN}$
Max voltage on switches	V_{IN}	V_{IN}	V_{IN}	V_{OUT}	V_{OUT}	V_{OUT}	V_{IN}	V_{IN}
Ideal voltage gain $G=V_O/V_{IN}$	N+1	N+1	N+1	N+1	F_{n+2}	F_{n+2}	N+1	N+1
	25	25	25	25	21 (*)	21 (*)	25	25
Ideal eq. output resistance R_{OUT}	$\frac{N}{fC}$	$\frac{2\sum_{i=1}^{N/2} i^2}{fC}$	$\frac{\sum_{i=1}^{N} i^2}{fC}$	$\frac{N}{fC}$	$\frac{\sum_{i=1}^{n} F_i^2}{fC_n}$	$\frac{\sum_{i=1}^{n} F_i}{fC}$	$\frac{2M\sum_{i=1}^{N/2M} i^2}{fC}$	$\frac{M\sum_{i=1}^{N/M} i^2}{fC}$
	15 kΩ	812 kΩ	3062 kΩ	15 kΩ	19.5 kΩ (*)	12.5 kΩ (*)	70 kΩ	228 kΩ
Tot capacitance ratio: $C_T/C_{T\text{-}DICKSON}$	-	$\frac{2\sum_{i=1}^{N/2} i^2}{N}$	$\frac{\sum_{i=1}^{N} i^2}{N}$	1	$\frac{C\sum_{i=1}^{n} F_i^2}{N\cdot C_n}$	$\frac{\sum_{i=1}^{n} F_i}{N}$	$\frac{2M\sum_{i=1}^{N/2M} i^2}{N}$	$\frac{M\sum_{i=1}^{N/M} i^2}{N}$
	1	54	204	1	1.5 (*) (**)	1 (*) (**)	4.67	15.1

(*) $n=6$, (**) $N=20$

provide the charge packets through the even diodes to the pumping capacitors driven by $\bar{v}_{CK}$, which are contextually charged to a more positive voltage.

Referring to the first cluster of pumping capacitors driven by v_{CK}, it can be observed that the first pumping capacitor is charged to V_{IN} - V_D, the third one is charged to $V_{IN} + 2V_{CK}$ - $3V_D$, the fifth one is charged to $V_{IN} + 4V_{CK}$ - $5V_D$, and so on, up to the $(2M$ - $1)$-th pumping capacitor that is charged to $V_{IN} + (2M$ - $2)\cdot V_{CK}$ - $(2M$ - $1)\cdot V_D$. Additionally, referring to the second cluster of pumping capacitors driven by $\bar{v}_{CK}$, it happens that the second pumping capacitor is charged to $V_{IN} + V_{CK}$ - $2V_D$, the fourth one is charged to $V_{IN} + 3V_{CK}$ - $4V_D$, the sixth one is charged to $V_{IN} + 5V_{CK}$ - $6V_D$, and so on, up to the $2M$-th pumping capacitor that is charged to $V_{IN} + (2M$ - $1)\cdot V_{CK}$ - $2M\cdot V_D$. The pumping capacitors from $2M + 1$ to N are all charged to $2M\cdot(V_{CK}$ - $V_D)$; this is the voltage across the two terminals of the capacitors. The output capacitor is charged to $V_{IN} + N\cdot V_{CK}$ - $(N + 1)\cdot V_D$ as reported in (2) for the Dickson and Cockcroft-Walton CPs.

It is easy to demonstrate that the equivalent output resistance can be obtained as a combination of a $2M$-stage Dickson CP and an $N/2M$-stage Cockcroft-Walton one, as follows

$$R_{OUT,ideal} = \frac{1}{f \cdot C} \cdot 2M \sum_{i=1}^{N/2M} i^2 \tag{5}$$

The proposed CP can be also implemented in a dual branch architecture, as shown in Fig. 4c. The operation is similar to that of the single chain architecture with only a difference related to the voltages across the pumping capacitors which are now halved. This happens because the architecture is by construction completely symmetrical and, for a given N-stage, the number of pumping capacitors is doubled. Also, in this configuration R_{OUT} can be obtained as a combination of an M-stage Dickson CP and an N/M-stage Cockcroft-Walton one, as follows

$$R_{OUT,ideal} = \frac{1}{f \cdot C} \cdot M \sum_{i=1}^{N/M} i^2 \tag{6}$$

Equations (5) and (6) are respectively valid for N multiple of $2M$ and N multiple of M, and of course in SSL operating condition. Furthermore, it can be noted that for $M = N/2$ and $M = N$ the proposed CP, respectively in the single and dual branch architectures, becomes the Dickson CP as well as both (5) and (6) correspond to (3, D), while for $M = 2$ and $M = 1$ it becomes the Cockcroft-Walton one as well as (5) corresponds to (3, CW N even) and (6) corresponds to (4).

In a fully monolithic approach, CPs are normally implemented with MOS transistors arranged in several different circuit topologies. They can be either n-channel or p-channel MOS transistors as long as they are properly driven. For this reason, the diodes are replaced with switches as shown in Fig. 4b and 4d for single and dual branch architectures. In this design, assuming the voltage drop on the switches negligible, it is easy to demonstrate that R_{OUT} remains the same as that expressed in (5) and (6), while V_O simplifies to

$$V_O = V_{IN} + NV_{CK} \tag{7}$$

Key elements to be considered for proper design of CP architectures, for a given multiplication voltage gain, are the voltage ratings of the pumping capacitors, the output resistance and the silicon area occupation related to the total capacitance. Table 1 summarizes the factors mentioned for the proposed CP in single and dual branch architecture in comparison with the most popular CPs, given the following assumptions:

- All the architectures are designed with ideal switches and ideal capacitors with unlimited voltage breakdown, without diodes and with $V_{CK} = V_{IN}$.
- $N = 24$ stages, except for the Fibonacci CPs. As known, the voltage gain of Fibonacci CP corresponds to Fibonacci sequence and, for a fear comparison, $G = 21$ has been selected because it is the closest voltage gain to 25. $G = 21$ is obtained with $n = 6$ stages for Fibonacci CP and $N = 20$ stages for the other CPs.
- The ideal output resistance is calculated at the clock frequency $f = 32$ MHz and pumping capacitors $C = 50$ pF

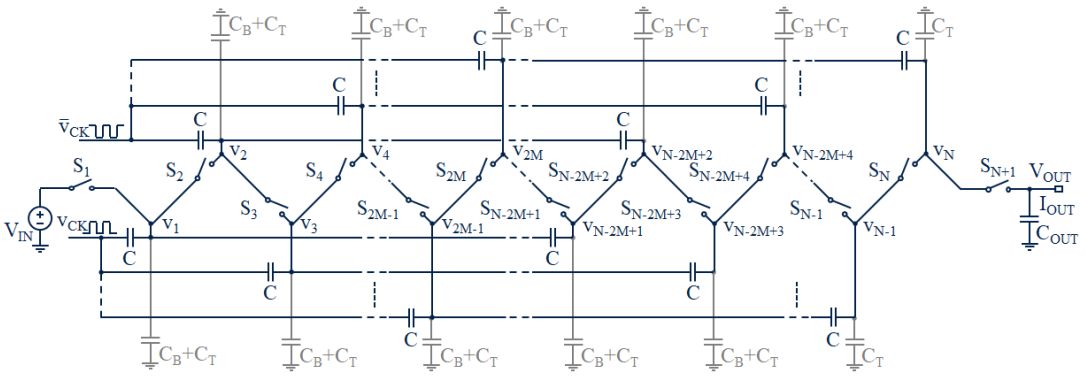

FIGURE 5. Proposed *N*-stage CP with stray capacitors.

for SB and $C = 25$ pF for DB, except for Fibonacci CPs where in the first option the pumping capacitors are $N/n = 20/6$ bigger than the Dickson's and in the second option the pumping capacitors are scaled according to [32] with the last pumping capacitor equal to the Dickson's.

- The total capacitance ratio is calculated assuming the same output resistance and voltage gain $G = 25$, except for the Fibonacci CPs where $G = 21$.
- The parameter $M = 4$ has been here arbitrarily set; in the next section the setting criteria is explained.

From this comparison it can be observed that the Dickson, Serial-Parallel and Fibonacci CPs have ideally lower output resistance and smaller area occupation than the Cockcroft-Walton and the proposed Hybrid CPs. For instance, assuming unlimited voltage capability of the pumping capacitors, the area occupation of a 24-stage dual branch Cockcroft-Walton CP is 204 times bigger than the Dickson's, as well as the area occupation of a 24-stage proposed dual branch Hybrid CP is 15.1 times bigger than the Dickson's. On the contrary, the Dickson and Fibonacci CPs require high voltage capacitors, which obviously in the real case occupy much large silicon areas and in many technologies are not available, while high voltage switches in the Fibonacci and Serial-Parallel CPs limit the switching frequency more than one magnitude order. In fact, applying the switching frequency used in [19] the equivalent output resistance of the Serial-Parallel CP becomes 192 kΩ, that is higher than that of the proposed Hybrid CP with single branch architecture.

In conclusion, the proposed architecture has the advantage to minimize the silicon area and the equivalent output resistance, thanks to the following characteristics:

- Flexile configuration to adapt the mix of the stages at any capacitor available in technology platforms, exploiting it at the highest voltage capability. No high voltage capacitors are required unlike in the Dickson and Fibonacci CPs.
- Use of low voltage CMOS, which are compact and allow for operation at the highest switching frequency. No high voltage transistors are required unlike in the Serial-Parallel and Fibonacci CPs.
- Lower impact of parasitic capacitances which allow to obtain higher multiplication gain versus the Cockcroft-Walton CP. This point will be thoroughly analyzed in the next section.

IV. PROPOSED CHARGE PUMP WITH STRAY CAPACITORS

Parasitic capacitances have relevant impact on performance tradeoff; for this reason, the proposed architecture with stray capacitors is here analyzed. For the purpose of brevity, only the single branch with switches is shown in Fig. 5.

The open load output voltage and the equivalent output resistance for both single branch and dual branch architectures can be obtained as a combination of the Cockcroft-Walton and Dickson CPs and are summarized below, while the detailed mathematical analysis is reported in the Appendix.

$$V_O = \begin{cases} V_{IN} + 2M \sum_{i=1}^{N/2M} \prod_{j=1}^{i} \dfrac{1}{1+\alpha_{SV}(j)} \cdot V_{CK} & SB \\ V_{IN} + M \sum_{i=1}^{N/M} \prod_{j=1}^{i} \dfrac{1}{1+\alpha_{SV}(j)} \cdot V_{CK} & DB \end{cases} \tag{8}$$

$$R_{OUT} = \begin{cases} \dfrac{1}{f \cdot C} \cdot 2M \sum_{i=1}^{N/2M} \sum_{j=1}^{i} \dfrac{N/2M - j + 1}{1+\alpha_{SR}(j)} & SB \\ \dfrac{1}{f \cdot C} \cdot M \sum_{i=1}^{N/M} \sum_{j=1}^{i} \dfrac{N/M - j + 1}{1+\alpha_{SR}(j)} & DB \end{cases} \tag{9}$$

with $\alpha_{SV}(j) = C_{SV}(j)/C$, $\alpha_{SR}(j) = C_{SR}(j)/C$, where $C_{SV}(j)$ and $C_{SR}(j)$, explicated respectively in (A5) and (A6), represent the contribution of top and bottom plate stray capacitors. If stray capacitors are negligible V_O and R_{OUT} are respectively simplified in (7), (5) and (6).

A specific embodiment can be obtained by using the bottom stray capacitors as pumping elements [30] as shown in Fig. 6.

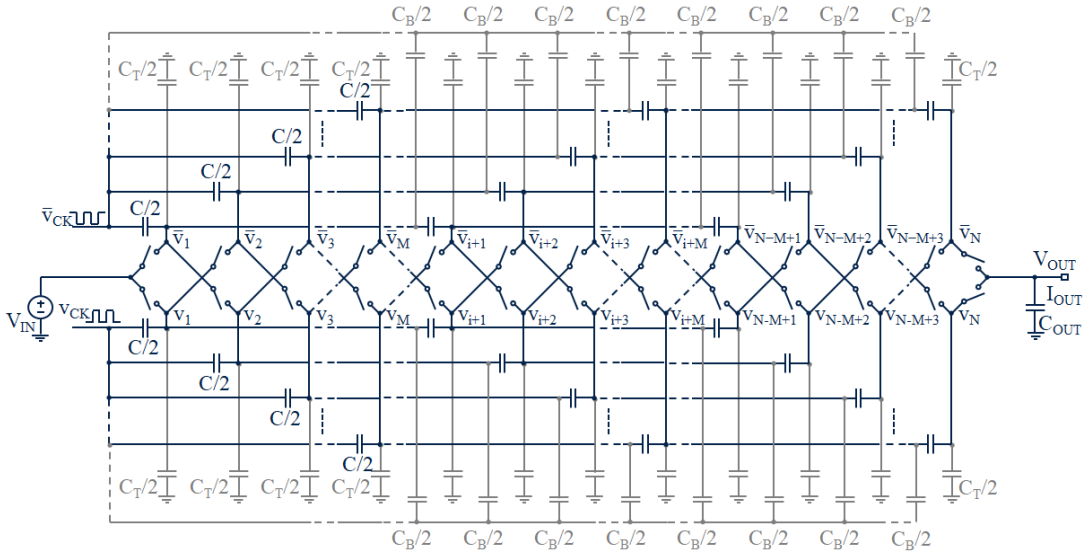

FIGURE 6. Proposed N-stage CP with bottom stray capacitors exploited as charge-pumping elements.

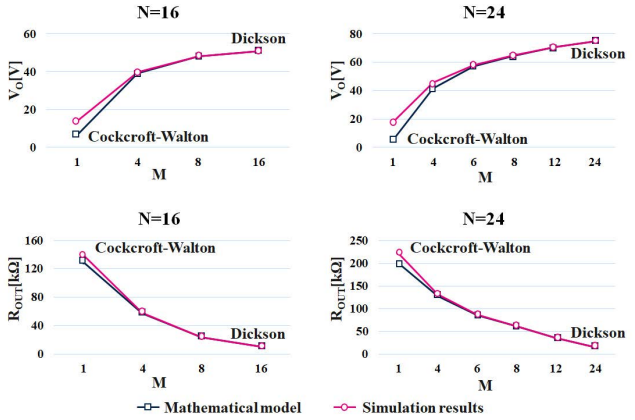

FIGURE 7. Modeled and simulated V_O and R_{OUT} of the proposed CP with 16 and 24 stages for different M.

In this implementation, these capacitors realize a Dickson topology which works in parallel to the main CP, so that the multiplication efficiency is improved. Of course, this solution introduces other parasitic capacitors connected to the bottom terminal of the stray capacitors which, nevertheless, do not have any impact on the output voltage because they only load the clock lines. The open load output voltage is summarized below

$$V_O = V_{IN} + M \sum_{i=1}^{N/M} \prod_{j=1}^{i} \times \frac{1 + \alpha_B \cdot \sum_{k=j}^{N/M-1} k}{1 + \alpha_B \cdot \sum_{k=j}^{N/M-1} k + (N/M - j + 1)\alpha_T} \cdot V_{CK} \quad (10)$$

It is easy to demonstrate that the equivalent output resistance is the same as (9, DB). Furthermore, it can be observed that setting to zero the top stray capacitor C_T, which is normally negligible, (10) becomes equal to (7).

To demonstrate the effectiveness of the mathematical model, the graphs of Fig. 7 show the comparison between the theoretical calculation and the simulation results of V_O in (8, DB) and R_{OUT} in (9, DB) for the proposed CP in dual branch architecture. The comparison is presented for $N = 16$ and 24 with different values of M: 1, 4, 6, 8, 12, 16 and 24.

The circuitries have been simulated with ELDO^{TM} simulator in CADENCE^{TM} framework, with ideal switches, $V_{IN} = 3$ V, $f = 32$ MHz, $C = 25$ pF, $\alpha_B = 6\%$ and $\alpha_T = 0.1\%$. The value of the last two parameters is typical of a P1P2 capacitor.

It can be observed that the open load output voltage increases as M grows, while the equivalent output resistance decreases. This is obvious because, as previously asserted, for $M = 1$ the architecture becomes the Cockcroft-Walton CP, where the parasitic capacitances have an increasing impact on the open load output voltage and N has an increasing impact on the output resistance, while for $M = 16$ (or 24) the architecture becomes the Dickson CP, where V_O reaches the maximum value and R_{OUT} reaches the minimum value. In summary, the mathematical model shows a good accuracy and matching with simulation results.

V. IMPLEMENTATION OF THE PROPOSED CHARGE PUMP

A specific embodiment of the proposed CP in dual branch architecture using MOS transistors in latched configuration and bottom stray capacitors as pumping elements is shown in Fig. 8.

The use of four MOS transistors in latched configuration per each multiplying stage was filed as a patent application by Pulvirenti and Gariboldi in August 1994 [41] and then published in [42] and [43]. This embodiment was later diffused in the literature under the name ''latched charge pump''. As the operation is well described in the above documents and also in many other papers [8]–[10], [34] it will not be explained here.

As anticipated in the abstract, the proposed CP has been designed to supply a fully integrated driver for miniaturized motors in MEMS technology, where the required 70-V

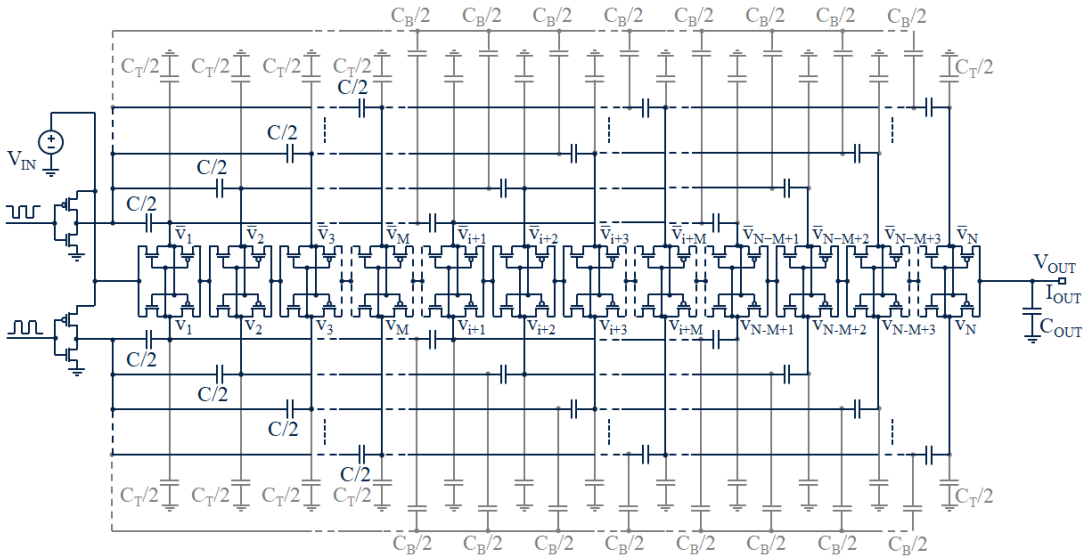

FIGURE 8. Proposed 24-stage CP with MOS transistors in latched topology and bottom stray capacitors exploited as pumping elements.

voltage must be internally generated starting from the provided power-supply of 3 V. Considering the ratio between the output and input voltages 23.3, the CP is expected to have almost 24 stages. The technology chosen for this project is the STMicroelectronics BCD in 0.35-μm lithography with 3.3-V CMOS transistors and 12-V P1P2 capacitor. In this work, M has been set to 4; it is obtained by dividing the maximum voltage capability of the P1P2 capacitor by the power supply voltage, that is 12/3, so that the maximum voltage on the pumping capacitors (that is 4·3 V) never exceeds the operating value, that is 12 V.

To target the specified output resistance of 130 kΩ, each pumping capacitor has the value of $C = 25$ pF. Furthermore, as in this technology the bottom stray capacitors are isolated from the substrate, hence they have been used as pumping elements, contributing to pumping the charge. Their value is 6% of the 12-V poly-poly capacitance.

To verify the functionality and the simulation results, a test chip has been fabricated as shown in Fig. 9.

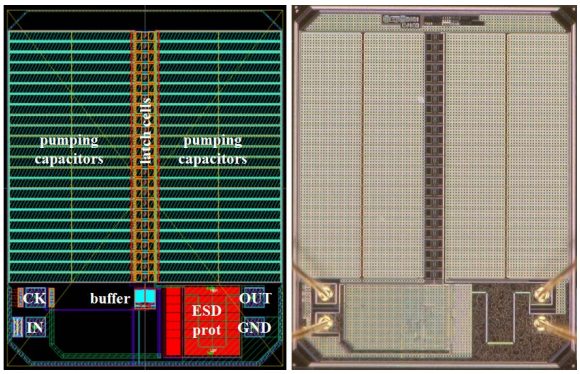

FIGURE 9. Layout and die photograph of the proposed Charge Pump with $N = 24$ stages and $M = 4$.

To better recognize the blocks which in the silicon are covered by the metal layers, the layout picture has been also enclosed. It consists of the following 3 blocks, the charge pump with 24 latch cells in the middle, 24 pumping capacitors on the left and 24 pumping capacitors on the right, the buffer stage in the bottom-center which drives the pumping capacitors, and the ESD protection in the bottom-right which protects the output voltage rail. Furthermore, it is possible to distinguish four pads, from left to right: Clock, IN, Ground and OUT. The die size is 1.3 x 1.6 mm^2.

VI. EXPERIMENTAL RESULTS

A first set of measurements has been performed applying a variable current sink to the output node with a power-supply voltage of 3.0 V and clock frequency of 32 MHz. The waveforms of the output voltage versus time for different load current values up to 40 μA are shown in Fig. 10a.

A specific setting has been arranged to measure the open load output voltage as the probe used in the measurement has an impedance of 10 MΩ; this would have charged the output node with a current of 7.3 μA. Therefore, a voltage generator and an amperemeter, connected between the output of the CP and the power supply, have been used. Consequently, the open load output voltage has been acquired increasing the voltage on the generator until the amperemeter has indicated zero current.

A second set of measurements has been performed changing the clock frequency from 4 to 32 MHz with a power-supply of 3.0 V and a load current of 10 μA. The waveforms of the output voltage versus time for different clock frequency values are shown in Fig. 10b. Although the circuit has been dimensioned for a power-supply of 3.0 V and a clock frequency of 32 MHz, it was observed to start operating at the minimum power-supply voltage of 1.1 V, generating a multiplied voltage of nearly 26 V; furthermore, the full operation was verified up to 64 MHz. It was not possible to test the multiplier at higher frequency, because of test bench limitations.

TABLE 2. Charge pump key parameters comparison in real implementations.

	Pelliconi et al. [8]	Lin et al. [21]	Abaravicius et al. [19]	Tsai et al. [30]	This work
Topology	5-Dickson	5-Fibonacci	Cross-Coupled x 4-Serial Parallel	3-Dickson + 3-Cockcroft -Walton	4-Dickson x 6 - Cockcroft -Walton
Tech lithography	0.18-µm	0.11-µm	0.13-µm	0.18-µm	0.35-µm
Ideal Gain	6	13	9	7	25
Input voltage V_{IN}	1.8 V	2.4 V	3.1 V	1.0 V	3.0 V
Pumping capacitors C	MOM 2.5 pF	Discrete 47 nF	5-V MIM 30/15 pF	MIM+MOS 6/12 pF	12-V P1P2 25 pF
Switching frequency f	100 MHz	50 kHz	20/2.5 MHz	20 MHz	32 MHz
Open load output voltage V_O	10.1 V	30 V	26 V	6.5 V	73.5 V
Equivalent output resistance R_{OUT}	8.9 kΩ	5.3 kΩ	120 kΩ	2.9 kΩ	130 kΩ
Voltage conversion efficiency $V_{O\text{-}real}/\ V_{O\text{-}ideal}$	93.5%	96.1%	93.1%	92.8%	98.0%
Max power conversion efficiency $P_{OUT}/\ V_{IN}$	50%	83.4%	42%	58%	42%
CP total silicon net area	-	-	0.086 mm²	0.5 mm²	1.4 mm²

From these curves V_O and R_{OUT} can be extracted; their value, respectively 73.5 V and 130 kΩ, is very close to that obtained with the mathematical model 74.3V and 128 kΩ. The small discrepancy is due to the fact that, in addition to the approximation described in the Appendix, the intrinsic current consumption generated by the cross conduction of the MOS switches is not considered.

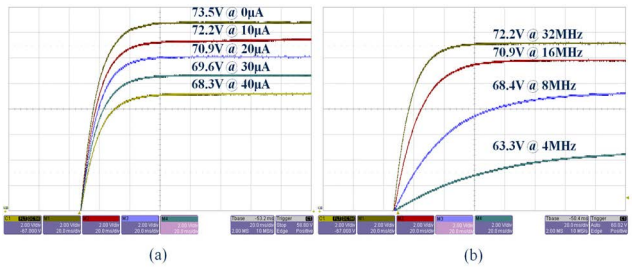

FIGURE 10. Output voltage for different output load current values (a) and different clock frequency values (b).

The measured 10%–90% rise time from zero to the open load multiplied voltage, with a 1.5 nF capacitive load, is approximately 800 μs, while the voltage ripple in steady state condition is around 1 mV at 10 μA load current.

Fig. 11 shows the power efficiency measured at a switching frequency of 16 MHz and 32 MHz, at an input voltage of 2.0 V, 2.5 V and 3.0 V, and for different load current up to 160 μA. It also includes the driver losses. It can be observed that the maximum efficiency of 42% is obtained at $V_{IN} = 3$ V, $f = 16$ MHz and $I_{OUT} = 80$ μA.

A comparison of the main parameters among the known CPs is shown in Table 2. The maximum output voltage varies significantly for the different architectures, according to the number of stages, mainly due to technology limitations or application requirements. In comparison to other

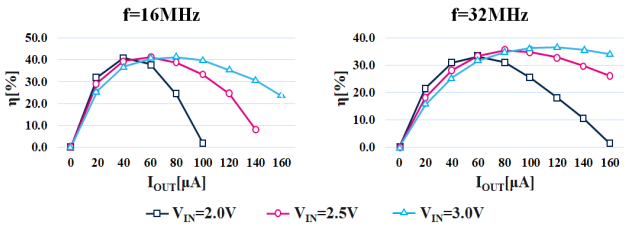

FIGURE 11. Measured conversion efficiency of the proposed CP at 16 MHz and 32 MHz switching frequency for different output load current.

implementations, the proposed CP shows a better performance tradeoff. More specifically, it offers the best voltage conversion efficiency and, considering the very high gain, a good power efficiency and a good output resistance, for a given silicon area.

VII. CONCLUSION

A novel integrated-circuit charge pump conceived to supply drivers for miniaturized motors in MEMS technology has been presented. This charge-pump is intended for high multiplying factors and is based on a mixed architecture which merges both Dickson and Cockcroft-Walton topologies, exploiting medium voltage on-chip capacitors and low-voltage CMOS transistors.

The experimental results have shown that a 24-stage dual branch CP, with each pumping capacitor of 25 pF, can generate an output voltage higher than 70 V starting from a power-supply of 3.0 V. In comparison to other implementations known in the literature, the proposed CP shows a better performance tradeoff, such as the best voltage conversion efficiency and, considering the very high gain, a good power efficiency and a good output resistance, for a given silicon area. Furthermore, it allows a reduction of the equivalent

output resistance maintaining the same area occupation or, alternatively, an area reduction for the same equivalent output resistance, as compared to a conventional Cockcroft-Walton charge pump.

Theoretical analysis of different configurations, with either diodes or MOS transistors, in single and dual branch architectures, also including stray capacitors, has been developed and described, which closely agrees with simulation and measurement results. The test chip has been fabricated in the STMicroelectronics BCD technology, with 0.35-μm lithography, 3.3-V CMOS transistors and a 12-V poly-poly capacitor.

APPENDIX

Referring to the voltage multipliers described in Sec. II, the multiplied output voltage V_{OUT} can be computed assuming the pumping capacitors and the diodes are ideally all equal. Also, C_{OUT} is assumed to be much bigger than the pumping capacitors, hence in steady state condition V_{OUT} can be considered a constant DC voltage with small superimposed voltage ripple. Furthermore, the calculation is done in SSL.

For an arbitrary N-stage Dickson Multiplier the voltages at the intermediate nodes in steady state condition are reported below. They have three contributions: the first one is the voltage level to which the pumping capacitors are charged when the clock signal is low; the second one, proportional to the clock amplitude V_{CK}, is the voltage step to which the pumping capacitors are boosted when the clock signal is switched high; while the last contribution is the voltage drop caused by the output load current I_{OUT}.

$$\begin{cases} v_1 = V_{IN} - V_D + \dfrac{C}{C+C_T}V_{CK} - \dfrac{\Delta Q}{C+C_T} \\ \quad\vdots \\ v_i = v_{i-1} - V_D + \dfrac{C}{C+C_T}V_{CK} - \dfrac{\Delta Q}{C+C_T} \quad i = 2, 3, \ldots N \\ \quad\vdots \\ V_{OUT} = v_N - V_D \end{cases} \tag{A1}$$

where

V_{IN}	is the input voltage of the circuit,
V_{CK}	is the swing voltage of the clock signals,
V_D	is the forward voltage drop of the diodes,
ΔQ	is the charge transferred in a clock period,
C_T	is the top plate stray capacitance.

The multiplied output voltage V_{OUT} can be easily obtained by solving the equations set (A1) and is given by

$$V_{OUT} = V_{IN} - (N+1)\,V_D + \frac{C}{C+C_T}NV_{CK} - \frac{\Delta Q}{C+C_T}N \tag{A2}$$

where the first three addends represent the open load output voltage, while the last one represents the voltage drop on the equivalent output resistance.

The charge transferred ΔQ is directly proportional to the clock period or inversely proportional to the clock frequency f; hence, it can be written as $\Delta Q = I_{OUT}/f$. Moreover, the top plate stray capacitor C_T can be specified as a fraction of the pumping capacitor $C_T = \alpha_T \cdot C$. So, (A2) can be rewritten as follows

$$V_O = V_{IN} - (N+1)\,V_D + \frac{1}{1+\alpha_T}NV_{CK} \tag{A3}$$

$$R_{OUT} = \frac{1}{f \cdot C} \cdot \frac{1}{1+\alpha_T}N \tag{A4}$$

Unlike the Dickson multiplier, the computation for an arbitrary N-stage Cockcroft-Walton multiplier gives different results depending on whether the architecture is single or dual, for this purpose the following calculations will be focused on the dual branch configuration and then extended to the single one. Thus, the value of pumping capacitors is halved with respect to the single branch configuration so that the total amount of capacitance does not change. Furthermore, the precise computation including both bottom and top plate stray capacitors is complex, for this reason the following simplifications are applied.

The first simplification comes from the fact that generally the parasitic capacitors are much smaller than the pumping ones, so that each pumping capacitor in series with the stray capacitor can be approximated as a short. Consequently, the equivalent parasitic capacitance loading the i-th node can be calculated by making the parallel of the cascading N - i + 1 stray capacitors. Hence, the voltage at the i-th node is obtained from the voltage at the previous node with a capacitive partitioning between the i-th pumping capacitor and the corresponding stray capacitor defined as follows.

$$C_{SV}(j) = (N-j)\cdot(C_B + C_T) + C_T \tag{A5}$$

Regarding the second approximation, looking at Fig. 12, the parasitic capacitors of circuit (a) can be arranged in a linearly growing series having same capacitive value (b) and then connected in parallel with the pumping capacitors (c).

Of course, the voltage distribution across the intermediate nodes of the stray and pumping capacitors series is not equal and the discrepancy grows with their ratio. Hence, the charge delivered from the i-th node is provided by the parallel of the i-th pumping capacitor and the corresponding stray capacitors defined in (A6), while the voltage at the related node is obtained from the voltage at the previous node subtracting the drop caused by the charge transferred.

$$C_{SR}(j) = (C_B + C_T)\cdot\sum_{k=j}^{N-1} k + N\cdot C_T \tag{A6}$$

Fig. 13a shows the clock signal attenuation caused by the stray capacitors. It can be observed that the voltage attenuation grows with the value of these capacitors, therefore they have a detrimental impact on it. Fig. 13b shows the voltage drop caused by the output load current. In this case it can be noted that the stray capacitors have a positive effect on the voltage drop because they provide part of the charge delivered to the output.

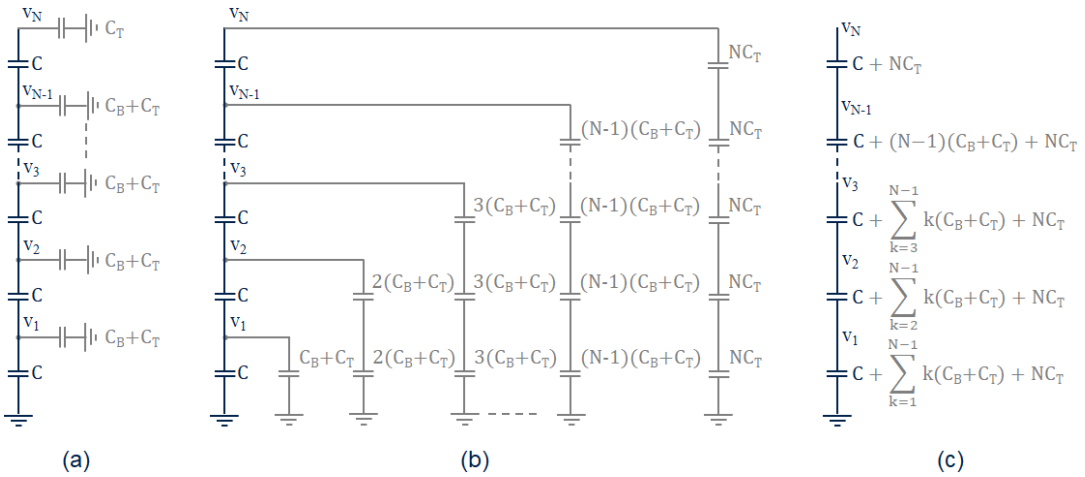

FIGURE 12. Parasitic capacitors in a N-stage Cockroft-Walton CP basic configuration (a) rearranged in a linearly growing series (b) and connected in parallel (c).

The voltages at the intermediate nodes in steady state condition have the same three contributions described for the previous CP

$$\begin{cases} v_1 = V_{IN} - V_D + \dfrac{C}{C + C_{SV}(1)} V_{CK} - \dfrac{N \cdot \Delta Q}{C + C_{SR}(1)} \\ \quad \vdots \\ v_i = v_{i-1} - V_D + \prod_{j=1}^{i} \dfrac{C}{C + C_{SV}(j)} V_{CK} \\ \quad - \sum_{j=1}^{i} \dfrac{(N - j + 1) \cdot \Delta Q}{C + C_{SR}(j)} \\ \quad \vdots \\ V_{OUT} = v_N - V_D \end{cases} \tag{A7}$$

In this case, bottom and top plate stray capacitors have been considered because both impact the output voltage, which can be obtained by solving the equations set (A7)

$$V_{OUT} = V_{IN} - (N+1) V_D + \sum_{i=1}^{N} \prod_{j=1}^{i} \frac{C}{C + C_{SV}(j)} \cdot V_{CK} - \sum_{i=1}^{N} \sum_{j=1}^{i} \frac{N - j + 1}{C + C_{SR}(j)} \cdot \Delta Q \tag{A8}$$

where the first three addends represent the open load output voltage, while the last one represents the voltage drop on the equivalent output resistance. Then, specifying the charge transferred as $\Delta Q = I_{OUT}/f$ and the stray capacitors as a fraction of the pumping capacitor (A8) can be rewritten as follows

$$V_O = V_{IN} - (N+1) V_D + \sum_{i=1}^{N} \prod_{j=1}^{i} \frac{1}{1 + \alpha_{SV}(j)} \cdot V_{CK} \tag{A9}$$

$$R_{OUT} = \frac{1}{f \cdot C} \sum_{i=1}^{N} \sum_{j=1}^{i} \frac{N - j + 1}{1 + \alpha_{SR}(j)} \tag{A10}$$

with $\alpha_{SV}(j) = C_{SV}(j)/C$ and $\alpha_{SR}(j) = C_{SR}(j)/C$; they are zero if stray capacitors are negligible.

As anticipated, in a Cockcroft-Walton dual branch architecture, there are N pumping capacitors in series on both branches. Differently, in the single branch architecture, with N even, the pumping capacitors in series are $N/2$ on both sides, while, with N odd, the pumping capacitors in series are $(N + 1)/2$ on one side and $(N - 1)/2$ on the opposite side. Hence, for a single chain configuration V_O and R_{OUT} become

$$V_O = \begin{cases} V_{IN} - (N+1) V_D + 2 \sum_{i=1}^{\frac{N}{2}} \prod_{j=1}^{i} \dfrac{1}{1 + \alpha_{SV}(j)} V_{CK} & N \text{ even} \\ V_{IN} - (N+1) V_D + [\sum_{i=1}^{\frac{N+1}{2}} \prod_{j=1}^{i} \dfrac{1}{1 + \alpha_{SV}(j)} & \\ + \sum_{i=1}^{\frac{N-1}{2}} \prod_{j=1}^{i} \dfrac{1}{1 + \alpha_{SV}(j)}] \cdot V_{CK} & N \text{ odd} \end{cases} \tag{A11}$$

$$R_{OUT} = \begin{cases} \dfrac{1}{f \cdot C} \cdot 2 \sum_{i=1}^{\frac{N}{2}} \sum_{j=1}^{i} \dfrac{N - j + 1}{1 + \alpha_{SR}(j)} & N \text{ even} \\ \dfrac{1}{f \cdot C} [\sum_{i=1}^{\frac{N+1}{2}} \sum_{j=1}^{i} \dfrac{N - j + 1}{1 + \alpha_{SR}(j)} & \\ + \sum_{i=1}^{\frac{N-1}{2}} \sum_{j=1}^{i} \dfrac{N - j + 1}{1 + \alpha_{SR}(j)}] & N \text{ odd} \end{cases} \tag{A12}$$

Assuming $V_{CK} = V_{IN}$, it can be noted that, in a single branch architecture, the pumping capacitors are charged to $2(V_{IN} - V_D)$, except for the first one which is charged up to $V_{IN} - V_D$, while in a dual branch architecture, as the number of stacked capacitors is doubled, they are charged up to $V_{IN} - V_D$. A drawback of this is that, for a given N-stage, the equivalent output resistance is much higher than that of a single branch configuration.

In those designs where the bottom stray capacitors are used as charge pumping elements, like the architecture of Fig. 6, they realize a Dickson topology which works in parallel to the main CP. Following the same reasoning of Fig. 1A, the bottom stray capacitors can be connected in parallel with the pumping capacitors. Of course, this also is an approximation

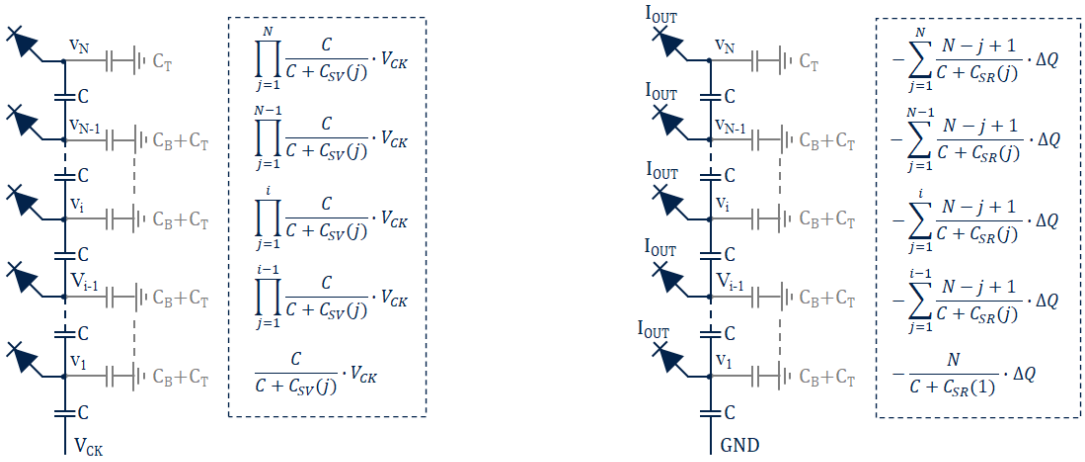

FIGURE 13. Clock signal attenuation caused by stray capacitors (a) and voltage drop caused by the output load current (b) in a Cockcroft-Walton CP.

because the voltage distribution across the intermediate nodes of the stray and pumping capacitors series is not perfectly equal since the capacitors in the two series are differently distributed.

$$\begin{cases} v_1 = V_{IN} - V_D + \dfrac{C + C_B \cdot \sum_{k=j}^{N-1} k}{C + C_B \cdot \sum_{k=1}^{N-1} k + N \cdot C_T} V_{CK} \\ \qquad - \dfrac{N \cdot \Delta Q}{C + C_{SR}(1)} \\ \vdots \\ v_i = v_{i-1} - V_D \\ \qquad + \prod_{j=1}^{i} \dfrac{C + C_B \cdot \sum_{k=j}^{N-1} k}{C + C_B \cdot \sum_{k=j}^{N-1} k + (N-j+1) \cdot C_T} \cdot V_{CK} \\ \qquad - \sum_{j=1}^{i} \dfrac{(N-j+1) \cdot \Delta Q}{C + C_{SR}(j)} \\ \vdots \\ V_{OUT} = v_N - V_D \end{cases} \tag{A13}$$

The voltages at the intermediate nodes in steady state condition are here calculated considering that the bottom stray capacitors, properly distributed, go in parallel with the pumping capacitors. Then, V_{OUT} can be easily obtained by resolving the equations set (A13)

$$\begin{aligned} V_{OUT} &= V_{IN} - (N+1)\, V_D \\ &\quad + \sum_{i=1}^{N} \prod_{j=1}^{i} \\ &\quad \times \frac{C + C_B \cdot \sum_{k=j}^{N-1} k}{C + C_B \cdot \sum_{k=j}^{N-1} k + (N-j+1) \cdot C_T} V_{CK} \\ &\quad - \sum_{i=1}^{N} \sum_{j=1}^{i} \frac{(N-j+1) \cdot \Delta Q}{C + C_{SR}(j)} \end{aligned} \tag{A14}$$

Finally, specifying the charge transferred as $\Delta Q = I_{OUT}/f$ and the stray capacitors as a fraction of the pumping capacitor (A14) can be rewritten as follows

$$\begin{aligned} V_O &= V_{IN} - (N+1)\, V_D \\ &\quad + \sum_{i=1}^{N} \prod_{j=1}^{i} \frac{1 + \alpha_B \cdot \sum_{k=j}^{N-1} k}{1 + \alpha_B \cdot \sum_{k=j}^{N-1} k + (N-j+1)\alpha_T} V_{CK} \end{aligned} \tag{A15}$$

It is easy to demonstrate that the equivalent output resistance is the same as (A10).

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