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A Novel Current Density Based Design Approach of Low-Noise Amplifiers

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ABSTRACT The input-referred noise (IRN) is one of the most crucial performance indicators for the analog front-end (AFE) of neural recording devices. In this study, we present a novel design approach for a low-noise amplifier (LNA) based on the transistor optimization method in CMOS technology. Because flicker noise is predominant in neural recording applications, AFE has been designed to meet input-referred flicker noise specifications, whereas thermal noise contributions are monitored and controlled by flicker noise corner frequencies. Transistor optimization is accomplished using a lookup table that encapsulates its performance based on its current density. Initially, transistors are optimized based on the flicker noise performance; later, they may be further optimized based on their size, power consumption, transconductance, or thermal noise contribution. The proposed approach was validated by designing a folded-cascode amplifier with IRN ranging from 2 to 8 μV_{rms}. The results of the simulation show that the errors of our design methodology are less than 10%, which is less than those of the g_m/I_D and inversion coefficient methods. The proposed LNA achieves 2.1 μV_{rms} while consuming 0.83 μW from a 1.2 V supply.

INDEX TERMS 1/f noise, current density, design methodology, flicker noise, low-noise amplifiers.

I. INTRODUCTION

A significant concern for monolithic analog front-end (AFE) designers is noise reduction. Flicker noise (FN) is a problem with MOSFETs and makes LNA design much more challenging, especially in low-frequency applications [1]. Modern transistors achieve even poorer FN performance owing to the digital focus of the CMOS technology. Therefore, low-flicker-noise AFE in modern CMOS technology has recently attracted considerable research interest, and various methods have been proposed to provide such AFE.

Compared with MOSFETs, JFET transistors produce less FN, which has led to their use as input devices for several AFEs [2]. Nonetheless, this approach is practical only when FN dominates the system resolution. A popular approach to decreasing FN is to shift its spectrum outside the frequency range of interest by using chopper stabilization [3]–[7]. However, owing to the frequency-adaptation process, this method is subject to parasitic offsets and harmonic distortions. Furthermore, more circuits must be realized, which increases the power consumption and circuit complexity.

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Several publications have demonstrated the correlated double-sampling technique as a method of reducing noise [6]–[8]. However, this was intended primarily for applications that utilize sampled-data circuits to ensure that noise-aliasing does not deteriorate the noise performance in the baseband. AFE is sometimes complemented by a low-noise preamplifier integrated with a passive load to mitigate the effect of the noise of the main amplifier on the noise characteristics of AFE [9]. The disadvantage of this method is that it increases thermal noise (TN) and power consumption. It has been demonstrated that switching MOSFETs between ON and OFF states reduces their FN, provided that the switching is performed faster than the trapping-detrapping time constant of the traps [10]. Although this technique has been utilized in some papers [11], it cannot be applied to all architectures.

Although all above-mentioned techniques are effective in reducing FN, they are limited to certain applications and add a level of complexity to the amplifier. The transistor noise performance can be managed with an appropriate size and bias. Consequently, the IRN of an amplifier can be controlled by optimizing the key transistors inside the amplifier. Several methods are available for transistor optimization.

The classic equations have been used by some authors to determine transistor size and bias [12], [13]. Nevertheless, these equations are only valid for long-channel devices that operate in strong inversion.

Currently, transistors are characterized by complex equations with many parameters. Therefore, it may be incorrect to draw a conclusion about the transistor size using classic equations. Furthermore, no closed-form equations are available to describe the behavior of transistors in the moderate inversion region. Consequently, other methods, such as g_m/I_D and inversion coefficient, have been proposed. The g_m/I_D method is based on the transconductance efficiency for estimating the device size [14]–[16]. However, this method can be useful for sizing transistors in the moderate inversion region. The inversion coefficient is the ratio between the drain forward current and the specific current, which are parameters in the EKV models [17]. Several authors have used inversion coefficient to estimate transistor sizes [18]. However, it is difficult to apply this technique to other commercial MOSFET models.

In addition to transistor size and bias, polarity also contributes significantly to the noise performance. PMOS devices have traditionally been assumed to produce less FN than NMOS devices; consequently, many authors have applied large PMOS devices to the input stage of amplifiers, particularly in cascode architectures [12], [19], [20]. It should be noted that this does not apply to all fabrication processes. Although input transistors contribute significantly to the IRN, a poor design may result in the noise of load transistors being amplified by a factor of the transconductance ratio. Therefore, all transistors should be considered by the designer.

Considering these disadvantages, the primary goals of this study are as follows: 1) identify the design variables that can be extracted from commercial models that will aid in transistor sizing; 2) develop a methodology for sizing MOSFETs according to the desired FN performance and considering other performance characteristics such as power consumption and silicon area; 3) as a case study, calculate noise equations for a folded-cascode amplifier to demonstrate how the sizing procedure is applied while avoiding noise amplification.

Following is an outline of the remaining parts of the paper: In section II, we provide a description of transistor characteristics and its design parameters, then we introduce the proposed method. The case study of the proposed design methodology is presented in section III, simulation results appear in section IV, and conclusions are the subject of section V.

II. DESIGN METHODOLOGY

The amplifier performance is determined by its internal components, each of which is intended to serve a specific purpose. Consequently, the amplifier design involves formulating performance equations and identifying the most critical components (in particular, transistors) based on the corresponding equations. Following the identification of critical transistors, their size and bias current must be designed based on the desired performance. However, some transistors may

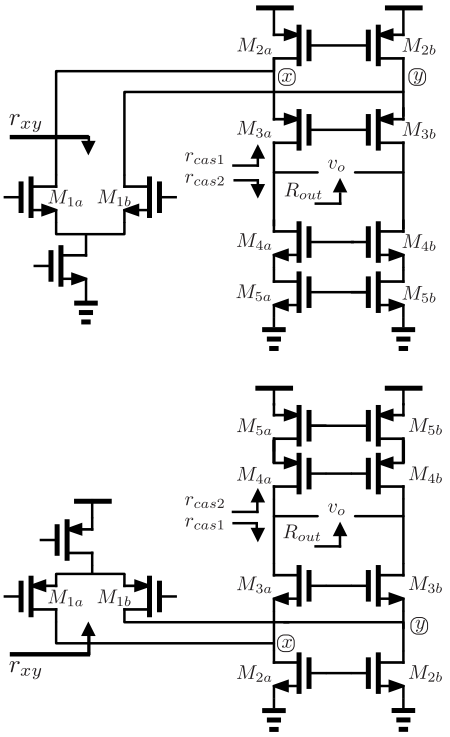

FIGURE 1. Folded cascode amplifier with (a) NMOS and (b) PMOS input pair.

interfere with or enhance the effects of other transistors, posing challenges for designers.

Among the different types of amplifier performance indicators, IRN is one of the most difficult targets to achieve. This is primarily because each transistor contains numerous noise sources with varying characteristics. Furthermore, the noise contribution of each transistor may be affected by the others, making the LNA design even more challenging. Managing different noise sources and adjusting the noise contribution of individual transistors, while considering the parameters related to those of other transistors, creates a very large design space and an extremely difficult and complex design process.

In this study, we demonstrate that the amplifier design process can be recast into a transistor sizing method while accounting for the effects of other transistors. Among the characteristics of a transistor that determine its noise performance, the g_m and gate-referred noise (GRN) are notable. By adjusting g_m and GRN of each transistor, it is possible to control the noise contribution of the transistor to the IRN of the amplifier.

To explain the proposed approach, we utilized folded-cascode topology. Despite being a common architectural choice in analog design, its noise-aware design adds a degree of complexity to the design process. Because of this, there are a sufficient number of challenges to provide us with a way to clarify our design method. Interestingly, the proposed methodology is applicable to other types of amplifiers. Two types of conventional folded-cascode amplifiers exist, as illustrated in Fig. 1. Although they have different

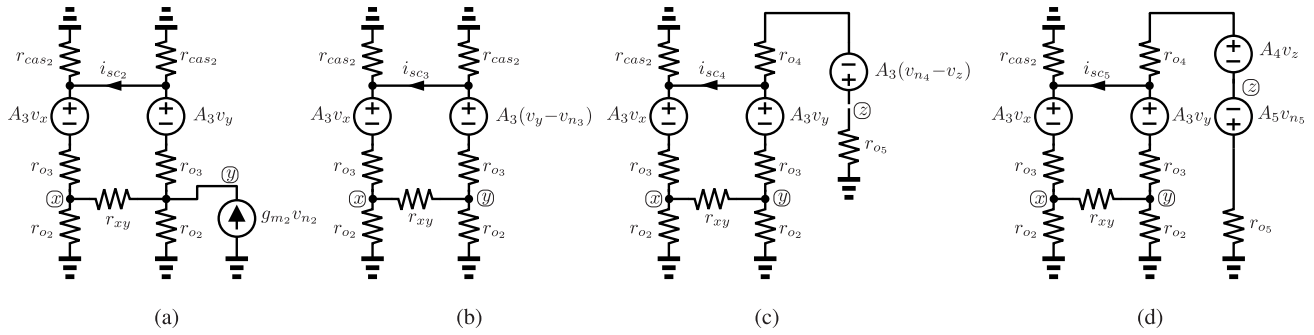

FIGURE 2. Simplified circuit diagrams used to find the noise transfer function of (a) M_2, (b) M_3, (c) M_4, and (d) M_5. In these circuits, r_{xy} is equal to $2r_{o_1}$.

configurations, they function in the same manner. The performance of the amplifier must be described by equations after its specifications have been established. In this study, we analyzed the transconductance, voltage gain, and IRN. In Fig. 1, the transconductance (G_m) is defined as the ratio of the output short-circuit current to the differential input voltage, which can be calculated using (1). If M_3 has a high intrinsic gain ($A_3 = g_{m_3}/g_{ds_3}$), then the equation simplifies to $g_{m_1}/2$.

$$G_m = \frac{g_{m_1}\left(g_{m_3} + g_{ds_3}\right)}{2\left(g_{m_3} + g_{ds_1} + g_{ds_2} + g_{ds_3}\right)} \tag{1}$$

The output impedance is determined by (2)

$$R_{out} = 2\left(r_{cas_1} \parallel r_{cas_2}\right) \tag{2}$$
$$r_{cas_1} = r_{o_3} + \left(r_{o_1} \parallel r_{o_2}\right)(1 + A_3) \tag{3}$$
$$r_{cas_2} = r_{o_4} + r_{o_5}(1 + A_4) \tag{4}$$
$$A_i = g_{m_i}/g_{ds_i} = g_{m_i} r_{o_i} \tag{5}$$

where r_{cas_1} and r_{cas_2} are the resistances observed from drains M_3 and M_4, respectively. A_i is the intrinsic voltage gain of the i-th transistor. The voltage gain of the amplifier was calculated as $G_m \times R_{out}$.

Despite the fact that the circuit introduces noise to the signal, the output noise should not be used to evaluate the noise performance of the amplifier. This is because different amplifiers have different voltage gains, which in turn cause the signal to be amplified differently. In this regard, the IRN is normally used as a measure of noise performance. An equation for IRN is obtained by determining a transfer function (TF) that transfers the GRN of each transistor to the input of the amplifier.

The circuit diagrams in Fig. 2 were used as the basis for this analysis, where some transistors were replaced by their small-signal equivalents, according to the Thevenin model. Two steps were taken in the present study to achieve the TFs. The short-circuit current noise (i_{sc_i}) produced by an individual transistor was initially determined and then divided by G_m to determine the equivalent voltage noise at the input of the amplifier.

In this case, the TF is in the form of a voltage gain, which transfers the GRN of a transistor (v_{n_i}) to the input of the amplifier.

Based on the circuit diagrams shown in Fig. 2(a), the transfer function for M_2 was calculated as follows:

$$\mathrm{TF}_2 = \frac{g_{m_2}}{g_{m_1}} \tag{6}$$

The circuit diagram of Fig. 2(b) was used in order to find TF of M_3.

$$\mathrm{TF}_3 = \frac{g_{m_3}\left(g_{ds_1} + g_{ds_2}\right)}{g_{m_1}\left(g_{m_3} + g_{ds_3}\right)} \tag{7}$$

In the case of a high intrinsic gain in M_3, this can be simplified to $\left(g_{ds1} + g_{ds2}\right)/g_{m1}$. Using the circuit in Fig. 2(c), TF_4 was derived as:

$$\mathrm{TF}_4 = \frac{g_{m_4} g_{ds_5}\left(g_{ds_1} + g_{ds_2} + g_{ds_3} + g_{m_3}\right)}{g_{m_1}\left(g_{m_3} + g_{ds_3}\right)\left(g_{m_4} + g_{ds_4} + g_{ds_5}\right)} \tag{8}$$

The high intrinsic gains of M_3 and M_4 may permit the writing of TF_4 as g_{ds_5}/g_{m_1}. Finally, the circuit diagram in Fig. 2(d) is used to calculate TF_5 as follows:

$$\mathrm{TF}_5 = \frac{g_{m_5}\left(g_{m_4} + g_{ds_4}\right)\left(g_{ds_1} + g_{ds_2} + g_{ds_3} + g_{m_3}\right)}{g_{m_1}\left(g_{m_3} + g_{ds_3}\right)\left(g_{m_4} + g_{ds_4} + g_{ds_5}\right)} \tag{9}$$

In the presence of a high intrinsic gain in M_3 and M_4, TF_5 simplifies to g_{m5}/g_{m1}.

In general, for a low-noise amplifier, transistors in the signal path must have a high g_m to amplify the signal, while transistors serving as a load must have a low g_m to produce less noisy current. When the TFs for all noise sources have been determined, the IRN of the amplifier can be calculated using the superposition of the noise power, as expressed in (10), where simplified TFs were utilized when available.

$$v_{irn}^2 = 2\left(v_{n_1}^2 + v_{n_2}^2\left(\frac{g_{m_2}}{g_{m_1}}\right)^2 + v_{n_3}^2\left(\frac{g_{ds_1} + g_{ds_2}}{g_{m_1}}\right)^2 + v_{n_4}^2\left(\frac{g_{ds_5}}{g_{m_1}}\right)^2 + v_{n_5}^2\left(\frac{g_{m_5}}{g_{m_1}}\right)^2\right) \tag{10}$$

Cascode transistors (M_3 and M_4) generate less noise because g_{ds} are usually much smaller than g_m. From another

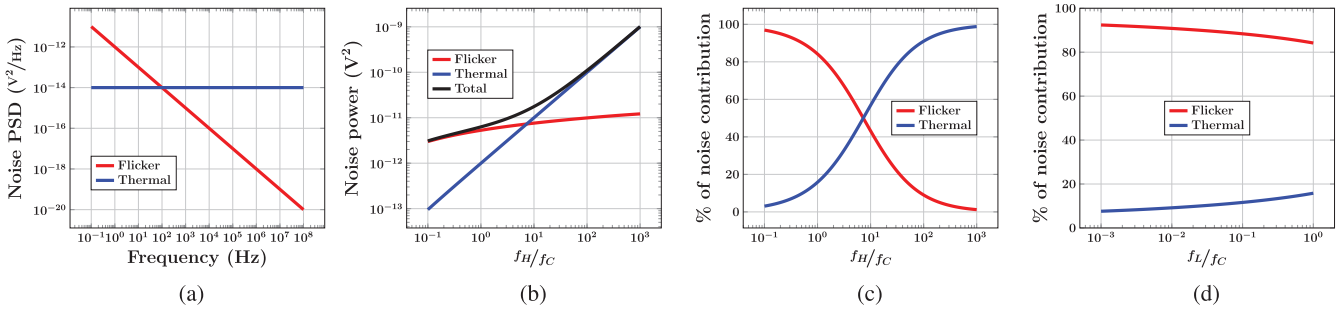

FIGURE 3. (a) Power spectral density of flicker and thermal noise obtained from simulations of a single transistor in a common-source configuration; (b) variation of integrated flicker, thermal, and total noise power with respect to f_H to f_C ratio, the variation of flicker and thermal noise contribution percentage with respect to (c) f_H to f_C ratio, and (d) f_L to f_C ratio. During this study, f_L and f_H were assumed to be 0.5 and 100 Hz respectively.

perspective, the source degeneration of these transistors reduces their effective transconductance, which results in less noise generation. Therefore, the primary sources of noise in the folded-cascode amplifiers are M_1, M_2, and M_5. Consequently, their GRN (v_{n_i}) and g_m values must be carefully designed to achieve the desired IRN (v_{irn}). Along with the GRN, the g_m ratios of M_2 and M_5 influence the noise contribution. Although a high g_{m_1} value reduces the noise, maintaining the g_m ratio is not always easy. To clarify this further, we assume that all transistors are identical in size, polarity, and properties. In the standard folded cascode, the input branch current (i_1) and load branch current (i_5) are the same; consequently, the current of M_2 (i_2) is two times greater than i_1. The noise contribution of M_5 will thus be the same as that of M_1 in this case because g_{m_5} will be equal to g_{m_1}. The problem is even more acute in the case of M_2 because i_2 exceeds i_1, g_{m_2} is larger than g_{m_1}, and therefore v_{n_2} is amplified by a factor of g_{m_2}/g_{m_1}. In other words, M_2 produces more noise than M_1.

Some researchers have tended to focus only on M_1 optimization and ignore the contributions of M_2 and M_5. However, M_2 and M_5 can contribute more noise to the amplifier input than M_1. To provide better noise characteristics and lower power consumption, i_5 should be a fraction of i_1 (current scaling technique). In this case, g_{m_5} is lower than g_{m_1}, which helps minimize the noise contribution from M_5. Additionally, i_2 is slightly larger than i_1; therefore, g_{m_2} and g_{m_1} might be approximately equal. This effectively reduces the effect of noise amplification.

It is well known that MOSFETs generate noise through a number of sources, such as FN and TN, generated by the channel, and thermal noise generated by the limited resistance of the bulk, gate, drain, and source material. In (10), v_{n_i} is the total GRN of the transistor. The channel-originating noise is more prominent in a monolithic front end, and a proper layout can diminish the noise arising from the gate resistance. Nevertheless, because the current density is relatively low in monolithic AFEs, noise sources that are not generated by the channel itself can be ignored [21], [22]. Therefore, only TN and FN can be considered for these AFEs. Although FN is the predominant noise source at low frequencies, TN can contribute a significant amount of noise, unless this contribution is properly limited. It is noteworthy that these two noise sources have remarkably different characteristics, which makes transistor sizing difficult. In contrast to coping with the two noise sources, we used the flicker-noise corner frequency (f_C) as a design variable to control the TN contribution. This is elaborated in the following sections.

Flicker-Noise Corner Frequency as a Design Variable: It has been mentioned that f_C can be used in determining FN and TN contributions. At frequencies below f_C, FN played a dominant role, whereas for frequencies above f_C, TN was dominant. To design LNAs at low frequencies, it is wise to restrict the contribution of TN. Furthermore, the bandwidth (BW) of the amplifier should be as small as possible to significantly reduce total noise. Otherwise, noise is integrated over an extended bandwidth, resulting in a reduction in the SNR. This study utilised f_C to monitor TN contribution based on the required BW. Consider a signal in the frequency range $[f_L, f_H]$ amplified by a common source amplifier with a flicker and thermal noise PSD, as shown in Fig. 3(a).

In Fig. 3(b), we show the variation in thermal, flicker, and total noise power as a function of bandwidth-to-f_C ratio (f_H/f_C). Clearly, when f_C is higher than f_H, FN becomes dominant, and with an increase in f_H (and therefore, a corresponding increase in BW), a greater amount of TN noise is introduced; thus, it becomes dominant at higher f_H/f_C ranges. Fig. 3(c) illustrates the percentage contribution from the noise sources. FN accounted for more than 84% of the total noise when $f_H/f_C \leq 1$, whereas the contribution of TN was less than 16%. Consequently, to maintain FN dominance while avoiding considerable TN, f_C should be larger than or at least equal to f_H. Fig. 3(d) depicts the variation in the noise contribution percentage according to the f_L to f_C ratio. The results indicated that f_L/f_C did not have a significant impact on the FN contribution. In this analysis, it was concluded that f_C can be viewed as a design variable to monitor TN.

A. LOOKUP TABLE PREPARATION

According to (10), the gate-referred noise (v_n) and g_m are critical parameters affect the noise properties of the amplifier. In contrast to g_m, which is well-known and easy to calculate,

v_{n_i} is composed of various sources of noise, rendering calculations difficult. However, it is still possible to control the contribution of the primary sources of noise (i.e., FN and TN) using f_C, as discussed in the preceding section. Therefore, we regarded g_m, gate-referred flicker noise (v_{fn}), and f_C as primary design variables.

Despite the availability of classical equations for calculating these variables, their accuracy is limited to long-channel devices that are biased in strong inversion. In addition, no closed-form equation describes the behavior of transistors in the moderate inversion region, whereas monolithic AFEs are typically designed to operate in weak or moderate inversion regions [22]. A lookup table approach was adopted to solve this problem, in which the behavior of transistors was represented by numerical values derived from simulations of sophisticated models.

For an amplifier to be effective, the size and operating point of each transistor must be designed according to the desired performance. In transistor-level design, the gate overdrive voltage is generally considered a design variable; however, it can only be utilized for long-channel transistors operating in strong inversion. Transistors can be designed in the moderate inversion region using the g_m/I_D method, and the inversion-coefficient approach is appropriate for EKV models. In this study, we used the drain current density ($J_D = I_D/W$) as a design variable because it has a simple definition and can be extracted from the simulation results irrespective of the type of MOSFET model used.

As a preliminary step to preparing the look-up table, we simulated both NMOS and PMOS devices with varying lengths and current densities, but with fixed widths. A length sweep was performed from 60 nm to 8 μm using a smaller step size at the short channels and a larger step size at the long channels. Our preference was for the variable step size to be able to collect sufficient data in both short- and long-channel devices, considering that short-channel devices exhibit more complex behavior. The noise appears to trade with the oxide capacitance ($C_{ox}LW$); correspondingly, low-noise transistors are usually large. Hence the width was set to 40 μm for this simulation.

Considering that monolithic front-ends typically operate at current densities lower than 1μA/μm [22], we swept the current density from 1nA/μm up to 1μA/μm with the same number of data points per decade. Consequently, the same amount of simulation data was collected at different inversion regions, resulting in a more consistent and reliable look-up table.

In addition to g_m and v_{fn}, we also recorded f_C in the lookup table as a design variable that influences the noise performance of an amplifier. Cadence IC6.18 was used to simulate both NMOS and PMOS transistors using the SMIC 55 nm technology, which employs the BSIM4 MOSFET model. We conducted both DC and noise analyses using Spectre 20.1. The f_C and v_{fn} were determined using expressions written in the ADE-Explorer environment. Finally, MATLAB R2020a was used to further analyze the noise-related information obtained from the noise analysis and DC operating point information obtained from the DC analysis. It is important to note that the noise power was integrated over a frequency range of 0.5 to 100 Hz, which corresponds to the typical frequency range for EEG recording AFEs.

Device Characterization Results: The performance results for the NMOS and PMOS transistors are shown in Fig. 4. In the first row, the results of the simulation are presented for a transistor with variable length and fixed width when it is biased at different current densities. An additional analysis was performed by simulating a transistor with a fixed length and variable width at different current densities, as shown in the second row of Fig. 4. Our primary objective was to investigate the relationship between transistor performance, transistor size, and current density.

In the first column (Fig. 4(a),(d)), it is shown that g_m is a weak function of length when the device operates in weak inversion, but the behavior is different when the device enters the strong inversion region, where g_m decreases with an increase in length. Regardless of the inversion level, g_m will vary proportionately to the width as long as the current density remains constant. Thus, current density and width are effective control variables for tuning the transconductance of the transistor, while length serves as a control variable when the transistor is biased in strong inversion.

In the second column(Fig. 4(b) and (e)), you will find the results related to the gate-referred flicker noise (GRFN). Fig. 4(b) shows that v_{fn} is not a strong function of the current density. This is especially relevant in the case of transistors biased in weak and moderate inversions, whose length is not at a minimum level, as in monolithic low-noise AFEs [22]. Based on this observation, it appears that the inversion level of the transistor can be varied within a relatively wide range without detrimental effects on the FN performance of the device.

Fig. 4(e) depicts the change in v_{fn} as a function of width when the current density is constant. As can be seen, v_{fn} decreases with an increase in W, which means that the transistor size is the most important determinant of the FN performance, particularly in low-power applications. It should also be noted that the NMOS transistors are quieter than their PMOS counterparts with the technology applied in this study. Consequently, this result contradicts the claim that PMOS transistors deliver a better FN performance than NMOS devices.

In Fig. 4(c) and (f), there is a relationship between f_C as a dependent variable and the transistor size and current density as independent variables. Although f_C is strongly influenced by the current density and length, it is not adjusted by the change in width.

1) EFFECT OF FABRICATION CORNER

Two identical NMOS and PMOS transistors were simulated at different corners to examine the influence of corners on transistor noise. During the simulation, we observed that the transistors generated less noise when they were located at the

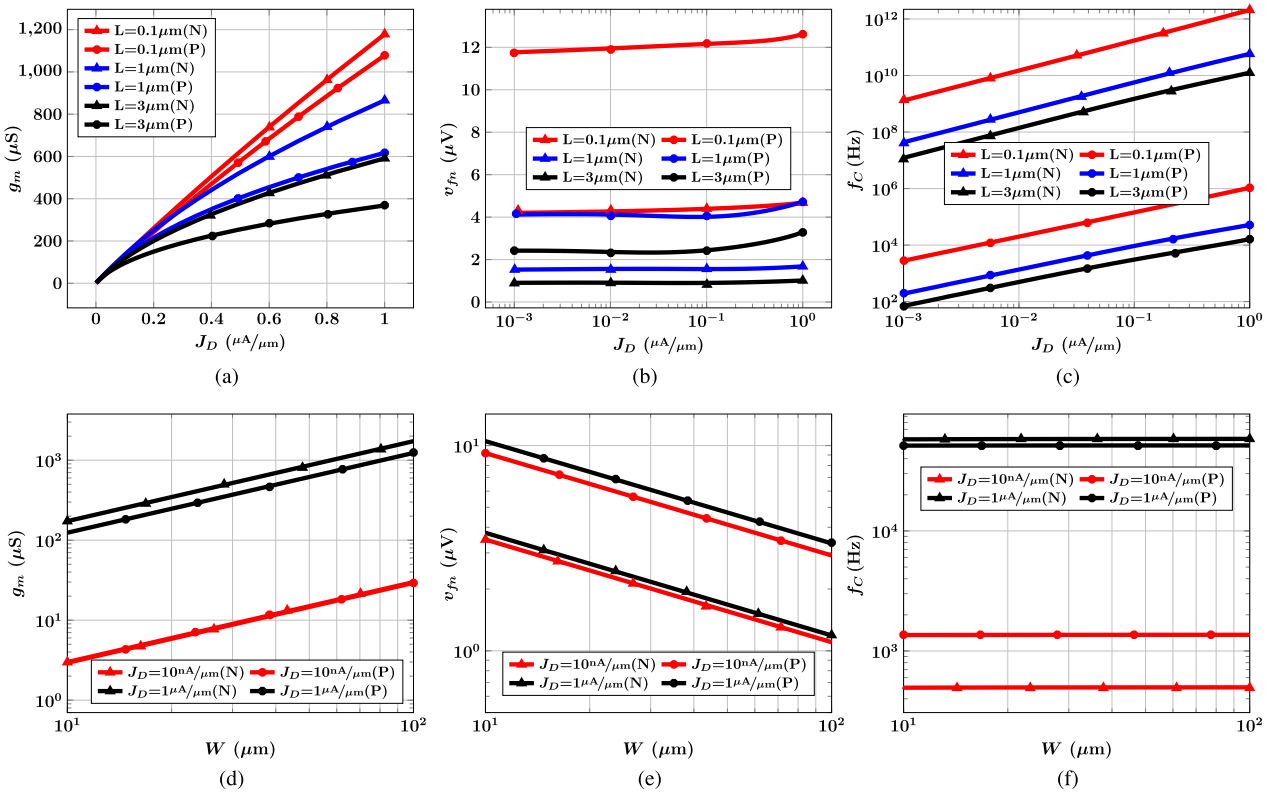

FIGURE 4. Variation of (a,d) g_m, (b,e) Integrated input-referred flicker noise (IRFN), and (c,f) f_C with respect to (a to c) Current density at different length and the width of 40 μm, and (d to f) Width at different current densities and fixed length of 1 μm.

FF corner. The noise performances in the FNSP, SNFP, and TT corners were almost similar, and in the SS corner, the noise performance was the worst. Conversely, f_C exhibits a weak relationship with the corner.

Design Table Preparation: In the previous section, we discussed a possible method for preparing lookup tables (LUTs) as well as the correlation between transistor performance and its size and bias. Every row in the lookup table includes a design point composed of information regarding the size and current density (independent variables) and their associated performance values (dependent variables). An auxiliary table, referred to as the *design table*, must be populated to design a transistor in accordance with its FN performance. Because v_{fn} is not a strong function of the current density, and it changes inversely proportional to the transistor size, for each design point in the LUT, a corresponding design point was generated in the design table by copying the value of independent variables except W. The width of the design point in the design table (W_D) is calculated using (11).

$$W_D = W_L \left(\frac{v_{fn_L}}{v_{fn_D}} \right)^2 \tag{11}$$

where W_D, W_L, v_{fn_D}, and v_{fn_L} represent the new width, width recorded in the LUT, desired GRFN, and GRFN registered in the look-up table, respectively. During this process, the remaining independent variables (g_m and f_C) in the design table are updated to reflect the change in width. In accordance with the discussion in Section II-A, f_C was copied without any changes, and g_m was updated using the following equation:

$$g_{m_D} = g_{m_L} \frac{W_D}{W_L} \tag{12}$$

where g_{m_D} is the g_m of the design point in the design table and g_{m_L} is the g_m of the corresponding row in the lookup table.

An individual row in the design table represents a unique design point with distinct size and current density information that meets the desired FN performance. It should be noted that the table was created without any simulations, thus saving considerable time in the design process. Although all the design points in the design table exhibit the desired FN performance, not all of them are suitable for use in the final circuit. In fact, other aspects such as TN contribution, g_m, area, and power consumption may also be considered when finalizing the transistor size and bias, as discussed in the following section.

III. CASE STUDY

The previous section discussed in detail the transistor optimization procedure based on the FN performance. The purpose of this section is to exploit the proposed methodology to design folded-cascode amplifiers. This method can be applied to other types of amplifiers.

As a starting point, an intuitive comparison of the two types of amplifiers shown in Fig. 1. According to (10), M_1, M_2, and

M_5 contribute the vast majority of the noise to the folded-cascode topology. Consider the case where current scaling has already been applied to the amplifier (i.e., $i_5 < i_1$), resulting in $g_{m_5} < g_{m_1}$ (for the same size), which helps control the noise contributions from M_5. However, M_1 and M_2 had approximately the same currents. Furthermore, assumed that both are of the same size, resulting in an equal current density. In accordance with the discussion presented in Section II-A, the NMOS transistors exhibit a higher g_m and lower GRFN in the technology under consideration. Consequently, for the NMOS input-type amplifier, v_{n_1} is smaller than v_{n_2}, and g_{m_1} is larger than g_{m_2}, which assists in reducing the noise contribution of M_2. However, the conditions are quite different for PMOS input types. Because g_{m_2} is larger than g_{m_1} in this case, the noise of M_2 is amplified by the factor g_{m_2}/g_{m_1}. Further consideration is that v_{n_1} is higher than v_{n_2}. Therefore, it can be deduced that the NMOS input type produces less noise than the PMOS input type in the analyzed technology. In other words, the amplifier should have a larger area to achieve the desired IRN if its input pairs are PMOS.

To design an amplifier based on its noise performance, a noise equation must be derived to identify the contributing components. Subsequently, the target IRN should be distributed among the noise contributors. For example, consider the design of a folded cascode amplifier with an IRN of 4 μV_{rms} in the frequency range of 0.5 to 100 Hz. In this case, the integrated input-referred noise power is 16 pV^2, which is twice the noise generated by the half-circuit. The half-circuit noise power (8 pV^2) must now be distributed between M1, M2, and M5. Considering power consumption and area performance, a significant noise sources should be given a higher noise budget, whereas the rest should be given a lower noise budget. Our analysis attributed a 45%, 45%, and 10% share of noise to M_1, M_2, and M_5, respectively, and the cascode transistor noise was ignored. We then used this noise budget distribution to formulate the design equations based on (10), as expressed in (13) to (15). At this stage of the design process, we ignored TN and only considered FN. Thus, we can estimate the FN contribution associated with each transistor through its noise budget. Subsequently, transistors were designed based on a noise equation and accompanying design table. It is important to note that no simulation was required at this stage of the design process.

$$v_{n_1}^2 = 3.6\ pV^2 \rightarrow v_{fn_1} \approx 1.90\ \mu V_{rms} \tag{13}$$

$$v_{n_5}^2 \left(\frac{g_{m_5}}{g_{m_1}}\right)^2 = 0.8\ pV^2 \rightarrow v_{fn_5} \frac{g_{m_5}}{g_{m_1}} \approx 0.89\ \mu V_{rms} \tag{14}$$

$$v_{n_2}^2 \left(\frac{g_{m_2}}{g_{m_1}}\right)^2 = 3.6\ pV^2 \rightarrow v_{fn_2} \frac{g_{m_2}}{g_{m_1}} \approx 1.90\ \mu V_{rms} \tag{15}$$

A. M_1 SIZING

To size a transistor, it is necessary to first determine its flicker noise power, and then its new size and performance need to be determined in the form of a design table, as discussed in Section II-A1. M_1 was sized according to (13). In the first step, a design table is created using the method outlined in the previous section to achieve v_{fn_1}. It means all the design points (rows) in the design table have GRFN equal to 1.90 μV_{rms} that is our target FN performance. The design points in the design table can be visualized as contour diagrams, as shown in Fig. 5. The first and second rows of this figure show the results for the NMOS and PMOS transistors, respectively.

Even though all the design points in the design table related to (13) meet the FN requirement, only those with f_C greater than f_H, as highlighted in Fig. 5, are acceptable. The purpose of this constraint is to maintain FN dominance; otherwise, the TN contribution would be excessive, resulting in a higher IRN than expected. The FN of the NMOS transistor in the technology we used is lower than that of the PMOS transistor; therefore, for the same GRFN, the PMOS transistor will need to be several times larger than its NMOS counterpart, as can be seen clearly in the area contours (Fig. 5(a,e)). The f_C of the PMOS is higher than that of the NMOS at the same current density, as shown in Fig. 5(b,f). This is because the PMOS is wider; hence, its current is larger than that of the NMOS (Fig. 5(c,g)), so its TN is lower.

To define the M_1 size, other criteria should be applied following the application of the f_C constraint. Suppose, for example, that the desired G_m of the amplifier is 5 μS, so g_{m_1} must be 10 μS. Based on the f_C and g_m contour diagrams (Fig. 5(d,h)), it is evident that the design points with g_m of 10 μS have f_C higher than f_H (100 Hz), and consequently, they are all possible candidates for the M_1 design. Using MATLAB, we created a multidimensional interpolation object to determine the pair of independent variables (current density and size) that achieved the desired performance ($g_m = 10$ μS in this case). The length and current density pairs were subsequently located using an optimization algorithm that minimized the error value, defined as

$$err = (g_{m_T} - g_{m_D})^2 \tag{16}$$

where g_{m_T} is the target g_m and g_{m_D} is the g_m value recorded in the design table. This optimization algorithm uses the design table as the input and produces new results that are stored in the form of a new table called the *candidate table*. Each row of a candidate table contains candidate points that achieve the desired GRFN and g_m performance.

The first row of Fig. 6 depicts the performance of candidate points having a GRFN of 1.90 μV_{rms} and a g_m of 10 μS. Based on the f_C figure (Fig. 6(a)), all candidate points have an f_C value higher than f_H, and, as a result, all of them are considered acceptable. NMOS and PMOS have similar sizes in short-channel transistors. However, as the channel length increased, the size of the NMOS transistor decreased more dramatically, as shown in Fig. 6(b). This was attributed to the lower FN of the NMOS transistors in the technology under study. In contrast, PMOS transistors achieve the desired g_m at a lower current density, which is because the PMOS transistors are wider than NMOS transistors with the same GRFN and therefore operate at a lower current

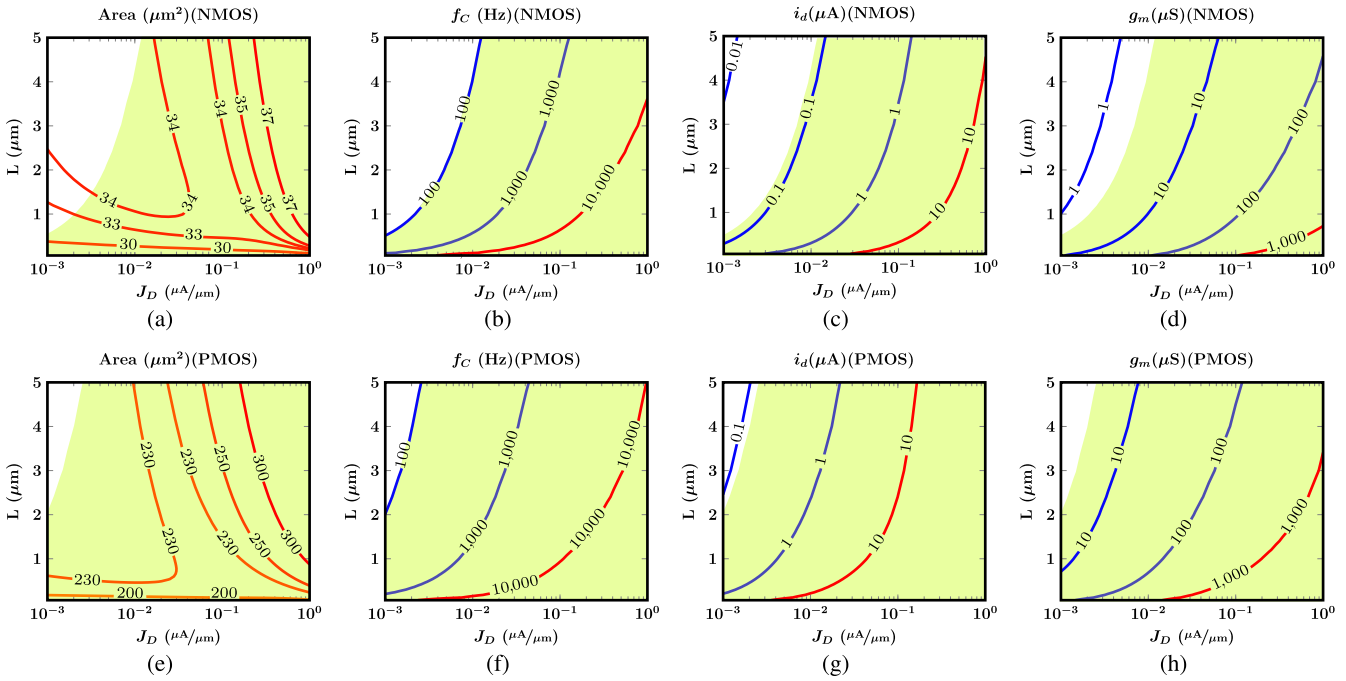

FIGURE 5. Contour diagram related to the performance of design points in a design table created for flicker noise RMS voltage equal to 1.90μV$_{\text{rms}}$ for (a to d) NMOS, and (e to h) PMOS. (a,e) Area contours, (b,f) f_C, (c,g) drain current, and (d,h) g_m contours.

level (Fig. 6(c)). While both transistors consume nearly equal amounts of power at shorter lengths, the current of NMOS increases rapidly at longer channels, suggesting that NMOS transistors are forced to operate at a higher level of inversion than PMOS transistors to achieve the desired g_m.

Designers now have the option of selecting the transistor size and bias current based on area and power consumption requirements. Additionally, the designer may select the final design point based on f_C. The TN contribution of transistors with a higher f_C was lower for a comparable GRFN. As a result, design points with a higher f_C will generate less TN, making v_{fn} closer to v_n, leading to a lower error in the final IRN value. Nonetheless, this will increase the power consumption, as the current density needs to be higher to achieve a high f_C. It was decided to have L = 1 μm for both transistors to reduce the power consumption of the amplifier. Table 1 summarizes the performance of the selected candidate points. For comparison purposes, it was intended that the input pairs of both amplifiers have an identical current of 333 nA.

B. M_5 SIZING

It is important to know the current of M_2, which varies depending on the current of M_5, if current scaling is desired. In this case, M_5 should first be sized according to (14). g_{m_5}/g_{m_1} allows for greater control over the noise contribution of this device; however, it should be less than one to prevent noise amplification. A very small g_m ratio results in a significant reduction in the M_5 current, which in turn increases its TN. Using (14), we selected $g_{m_5}/g_{m_1} = 0.1$, such that $g_{m_5} = 1$ μS and $v_{fn_5} = 8.9$ μV$_{\text{rms}}$. The design of M_5 with these specifications is accomplished in a manner similar to that of M_1. Fig. 6(d,e,f) depict the performance of the candidate points associated with this performance. A procedure similar to that described for M_1 sizing can be used to select a final candidate point based on the f_C, power consumption, or area specifications. For both NMOS and PMOS, we selected L = 1 μm, the performance of which is summarized in Table 1. i_5 was set to 33 nA for further analysis.

TABLE 1. Summary of performance of selected candidate points.

Device Name	Device Type	L (μm)	W (μm)	i_d (nA)	f_C (Hz)	v_{fn} (μV)	g_m (μS)
M1	N	1	33.71	334	493	1.9	10
M1	P	1	236.52	332	255	1.9	10
M5	N	1	1.52	34	1170	8.9	1
M5	P	1	10.70	33.5	506	8.9	1
M2	N	3	11.21	366	483	1.9	10
M2	P	6	37.95	366	256	1.9	10

C. M_2 SIZING

In (15), the design equation associated with M_2 is represented as i_2 was 366 nA when i_1 was 333 nA and i_5 was 33 nA. Similar to M_5, it is possible to control the noise contribution of this transistor by changing g_{m_2}/g_{m_1}. However, because i_2 is larger than i_1, it is challenging to size M_2 to achieve $g_{m_2} < g_{m_1}$. Under worst-case scenarios, and to avoid noise amplification, g_{m_2} can be equal to g_{m_1}. Based on of this selection, M_2 was designed for $i_2 = 366$ nA, $v_{fn_2} = 1.90$ μV$_{\text{rms}}$ and $g_{m_2} \leq 10$ μS. First, the corresponding design table for achieving v_{fn_2} is populated. Next, an optimization algorithm was used to identify candidate points. In this case, the candidate points are those

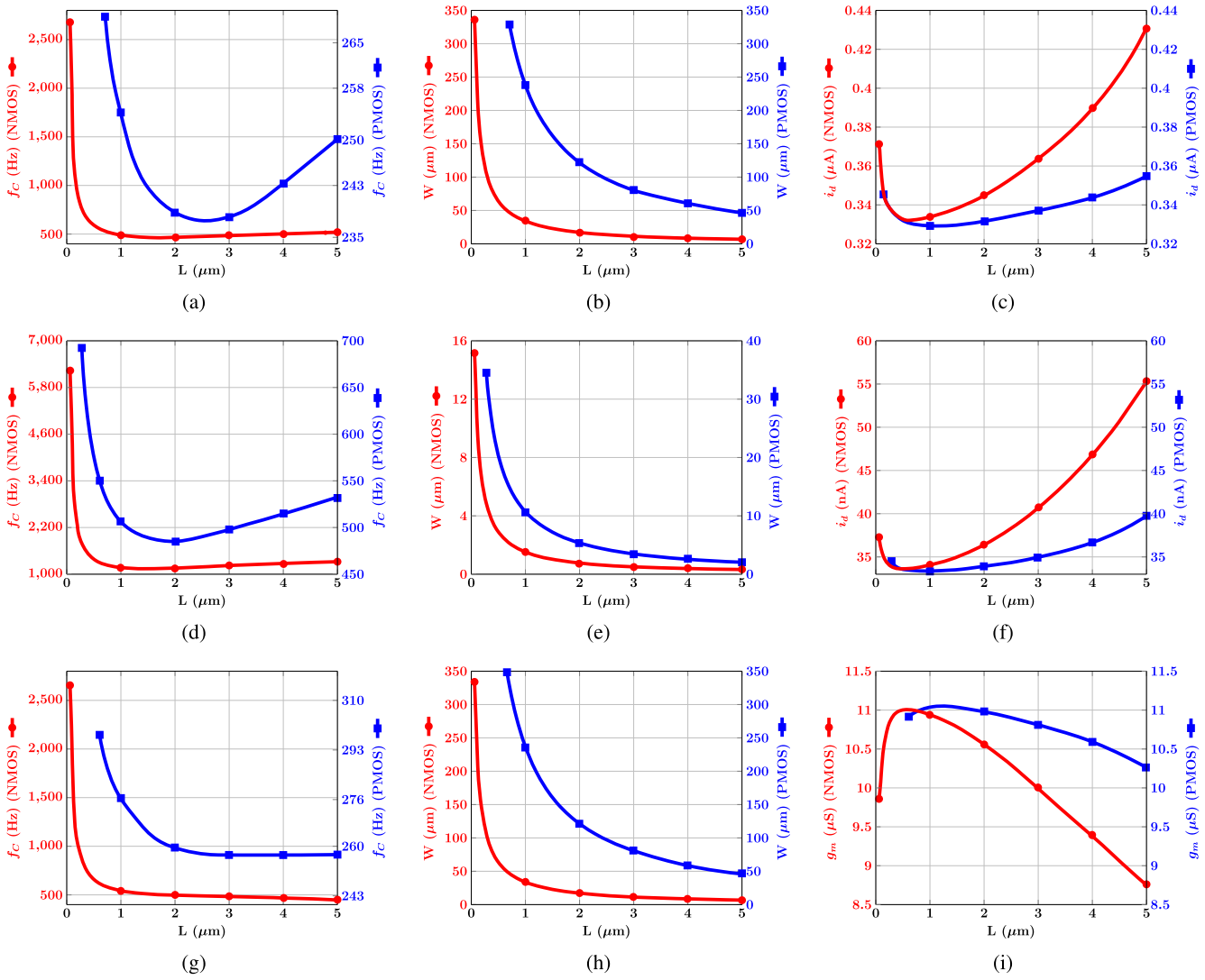

FIGURE 6. Performance of the candidate points derived from the design table for (a to c) a flicker noise of 1.90 μV_{rms} and g_m of 10 μS, (d to f) flicker noise of 8.9 μV_{rms} and g_m of 1 μS, and (g to i) flicker noise of 1.90 μV_{rms} and i_d equal to 366 nA for both NMOS (red colored) and PMOS (blue colored) transistors.

that achieve $i_2 = 366$ nA, which are plotted in Fig. 6(g,h,i). As shown in Fig. 6(g), each candidate point has f_C greater than f_H, which indicates that they are all acceptable. In the following steps, the length of M_2 is determined based on the g_m requirement. In Fig. 6(i), we can see that $g_{m_2} \leq 10$ μS only for long-channel transistors. Because a large length reduces the common-mode voltage range, we selected the shortest length that still met the g_m requirements. The corresponding transistor width can be determined from Fig. 6(h). Table 1 summarizes the results of the selected design points.

Note that if the desired g_m ratios are not achievable from the design tables, the designer can tolerate noise amplification and select g_{m_2}/g_{m_1} ratios greater than 1. However in this case, the noise power is still limited to (15). In this scenario, the transistor must be larger because its GRFN will be less than that in the case where noise amplification is avoided ($g_{m_2}/g_{m_1} \leq 1$). This scenario may also be applied to M_5. An overview of the steps involved in the proposed sizing methodology is presented in Algorithm 1.

D. EFFECT OF NOISE SHARE

The noise shares of individual transistors are also an optimization problem. Several amplifiers with NMOS inputs were designed to investigate the effect of the noise contribution of an individual transistor on the area and power consumption of the amplifier. g_{m_1} and g_{m_5} were set to 10 μS and 1 μS, respectively. Each design consisted of M_1 and M_5 sized based on the minimum current, whereas M_2 was sized to ensure $g_{m_2} \leq g_{m_1}$. The transistors were limited to length between 60 nm and 8 μm. Fig. 7(a) shows the simulation results when the noise contribution of M_1 was increased from 15 to 45% while that of M_2 was maintained at 45 percent.

TABLE 2. Comparison of different design methods for cascode amplifiers.

Desired IRN*(μV_{rms})	Open-loop voltage gain (dB)			Current (nA)			Error(%)		
	g_m/I_D	IC**	This work	g_m/I_D	IC	This work	g_m/I_D	IC	This work
2	82.68	82.69	82.60	696	695	693	34.19	26.20	6.56
3	82.85	82.90	82.79	705	704	702	25.63	18.38	4.71
4	82.90	82.95	82.96	710	711	710	19.23	13.89	3.20
5	82.80	82.85	82.99	714	715	716	14.05	10.99	2.22
6	82.70	82.75	82.96	717	718	722	11.32	9.73	1.60
7	82.50	82.60	82.90	719	721	727	9.23	9.19	0.98
8	82.30	82.40	82.76	720	722	732	8.20	8.72	0.66

* Input-referred noise
** Inversion coefficient

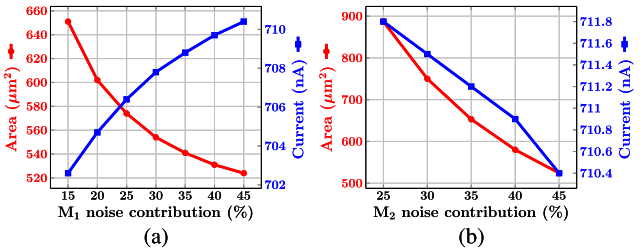

FIGURE 7. Variation in area and current of amplifier with respect to (a) M_1 noise contribution when the noise contribution of M_2 was 45% and (b) M_2 noise contribution when the noise contribution of M_1 was 45%. The target IRN was 4 μV_{rms} in this analysis.

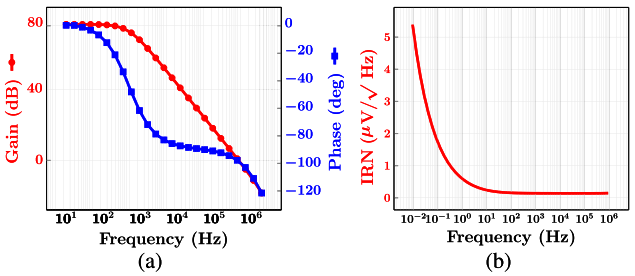

FIGURE 8. (a) Frequency response of the amplifier (f_{3dB} = 492 Hz, PM = 82°, CL = 1pF), and (b) its input-referred noise PSD.

As the noise contribution of M_1 increased, the power consumption of the amplifier increased. The opposite behavior was observed when the noise contribution of M_2 changed (Fig. 7(b)). However, the change was less than that of M_1. The results suggest that M_1 has a greater effect on the power consumption of the amplifier than M_2. Although both transistors have similar effects on the area, the amplifier designed based on the noise contribution of M_1 is smaller than that of the amplifier designed based on a similar noise contribution of M_2. Note that, as the amount of noise in M_2 is reduced, its length increases. The length of M_2 in our simulation was longer than 8 μm for contributions lower than 25%, which was beyond the design space. It can be concluded from these results that M_1 should be assigned more noise to achieve the desired power consumption, and the noise contribution of M_2 can then be adopted later to further reduce the area.

IV. RESULTS

In the previous section, a design methodology for transistor optimization was discussed primarily in terms of FN performance. We sized M_1 and M_5 based on their GRFN and g_m requirements. M_2 was designed in accordance with g_m, GRFN, and current specifications. These are almost all scenarios that a designer should consider when designing any type of amplifier based on its noise performance. Because M_3 and M_4 contribute relatively little noise, other metrics such as intrinsic gain may be used for their design. We selected $5\mu m/1\mu m$ for both.

To compare the proposed method with other state-of-the-art sizing techniques, we designed NMOS folded-cascode amplifiers with different IRN values ranging from 2 to 8 μV_{rms} and G_m of 5 μS. In each design trial, the noise was distributed at 45, 45, and 10 percent among M_1, M_2, and M_5, respectively. In addition, g_{m_1} and g_{m_5} were selected as 10 μS and 1 μS, and g_{m_2} was selected to be less than g_{m_1} to avoid noise amplification. In addition to the proposed method, we designed amplifiers based on the inversion coefficient and g_m/I_D methods. In the design process, we selected candidate points that had the lowest current among other points in the same design methodology, but had sizes similar to those of the other methods. We conducted DC, AC, and noise analyses using the Spectre 20.1 simulator and BSIM4 models.

Table 2 summarizes the performances of the amplifiers designed using various design techniques. At low noise levels, the amplifier designed using our method had a slightly lower gain than those of the other methods. However, the gain increases at high noise levels. When the noise level was low, the amplifier designed using our method consumed less current, whereas it consumed more current when the noise level was high. It should be noted that the increase in noise level will result in shrinking transistor widths, and the current needs to be increased to achieve the desired G_m.

The IRN of the designed amplifiers is evidently higher than the target value in all the methods used; hence, the error is positive. In fact, this additional noise results from both the TN generated by the transistors and noise generated by cascode transistors. The error decreases as the noise level increases because transistors have a narrower width in an amplifier with a higher IRN, which means that the current density increases and TN decreases. In contrast, the current density is low for amplifiers with less IRN; therefore, more TN is added to the input of the amplifier. The error of the g_m/I_D method

TABLE 3. Comparison of the proposed AFE with similar prior art publications.

	Prior-art Publications						
Parameter	[23]	[24]	[25]	[26]	[27]	[28]	This work
Technology (nm)	28	180	180	180	180	130	55
VDD (V)	1	1	1	1.8	1	2	1.2
power (μW)	1	2.3	2.14	13.7	0.38	6.3	0.83
gain (dB)	39.5	26	40	39.3	70	43-55	82.6
IRN (μV_{rms})	2.74[3]	2.1[3]	2.1[3]	3.36[3]	15[2] / 0.7[3]	3.45[2]	2.1[2]
Bandwidth (Hz)	1-200	1-200	1-200	200-10k	0.1-100	1-320	0.5-100
NEF	7.5	8.6	8.4	4.77	62.1[2]/ 2.9 [3]	13.2	6.7
CMRR (dB)	110	75	N/A	77	92	112	110
PSRR (dB)	103	68	N/A	60	83	101	102
THD	N/A	-70	N/A	-65	N/A	-68	-69
Sim./Meas.[1]	Meas.	Meas.	Meas.	Meas.	Sim.	Meas.	Sim.

[1] Simulation/ Measurement results
[2] Without chopper
[3] With chopper

Algorithm 1 The Proposed Low-Noise Amplifier Design Procedure

1) Formulate the input-referred noise equation of the amplifier and determine its critical transistors.
2) Prepare a lookup table by simulating the transistors with different lengths and current density and fixed width.
3) Distribute the noise of the amplifier among the critical transistors and determine their flicker noise voltage considering the g_m ratios.
4) Create a design table for each transistor based on its flicker noise performance.
5) Identify the candidate points based on their g_m or current requirements.
6) Determine the final size and bias of the selected transistor from the candidate points based on area, power consumption, transconductance, or thermal noise contribution. If the desired performance is not achievable, change the FN and repeat from step 3.
7) Repeat the procedure from step 4 for the next transistor.

decreases more rapidly than that of the IC method because transistors operate in moderate inversion regions when their current density is high. According to our experiments, our method offered a higher degree of precision by providing a more optimal size and bias current at all noise levels. In general, we can see that our proposed method is efficient, flexible, and accurate in designing amplifiers based on noise specifications. Additionally, this method delivers an amplifier with a gain, power consumption, and area comparable to those of well-known transistor sizing methods. Fig. 8(a) illustrates the frequency response of the amplifier when loaded with a 1pF capacitor. Fig. 8(b) shows the input-referred noise PSD of the amplifier.

The noise efficiency factor (NEF) captures the trade-off between the noise, current, and bandwidth and is defined as follows:

$$NEF = v_{irn}\sqrt{\frac{2.I_{tot}}{\pi.V_T.4kT.BW}} \tag{17}$$

where v_{irn} is the input-referred noise RMS voltage, I_{tot} is the current, BW is the bandwidth, k is Boltzmann's constant, and V_T is the thermal voltage. Table 3 summarizes the simulated performance of our LNA and compares its performance with that a recent state-of-the-art. Our proposed method achieves comparable or a lower noise with lower NEF while maintaining a comparable power performance. It should be noted that this performance was achieved without using chopper technique.

V. DISCUSSION AND CONCLUSION

The present work proposes a new LNA design methodology for biosignal recording applications in which flicker noise is predominant. The current density, rather than the g_m/I_D or inversion coefficient, was used as the transistor optimization variable. The transistor was optimized according to the flicker noise and g_m, while tracking their f_C to control the thermal noise contribution. We validated the proposed method by designing a LNA that achieved a 2.1 μV_{rms} input-referred noise RMS voltage while consuming 693 nA. According to our knowledge, this is the first study to investigate the effectiveness of selected design variables in LNA design in a systematic manner.

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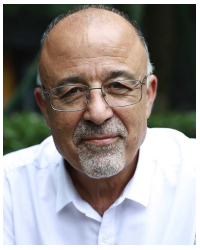

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