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Multiphase Interleaved Converter Based on Cascaded Non-Inverting Buck-Boost Converter

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ABSTRACT This paper introduces an interleaved buck-boost converter with reduced power electronics devices count in comparison with the conventional topology. The proposed converter consists of a single buck converter followed by *n* parallel interleaved boost converters. The buck switch is gated only if any of the boost switches is gated. In addition to the reduced switches count, the proposed converter offers the following advantages, soft start-up and shutdown capabilities. In addition, the buck stage gives the ability to protect the power electronic devices and to isolate the supply during load failure or overload. Moreover, the proposed converter performs as an interleaved boost converter for high voltage gain requirements with the same switching scheme. Furthermore, it offers fast dynamic performance with smooth transition from the buck mode to the boost mode. This paper investigates the eight different operating zones of the proposed three-phase interleaved buck-boost converter for non-overlapping gate signals operation. The detailed analysis and zones of operation are presented and experimentally validated. In addition, a simple control system is presented to operate the proposed converter as dc-dc converter or ac-dc converter. More study cases are carried out to evaluate the different capabilities of the proposed converter.

INDEX TERMS Interleaved buck-boost converter, ac-dc converter, and dc-dc converter.

I. INTRODUCTION

Dc-dc power electronics converters are widely used in many applications such as renewable energy sources, electric vehicles, uninterruptible power supplies, and microgrids. The buck-boost converter can increase or decrease the magnitude of the input voltage with simple circuit and control loops [1]–[4]. However, it has a limited voltage gain with inverted output voltage [5]. To increase the voltage gain, the buck-boost converter was proposed to operate under discontinues conduction mode (DCM) [6], [7]. The operation under DCM reduces the size of converter passive elements and improves the dynamic performance, but on the account of increased current stress of power electronics devices. In [8], two different topologies to reduce current stress are presented. In the first topology, two buck-boost converters inductors are charged in series and connected in parallel during the discharging in contrast to the second topology, where the inductors are connected in parallel during charging and discharging. It was concluded that the second topology succeeded to reduce the current stress on power electronics devices to half.

In the interleaving converters, two or more converters are connected in parallel, which can increase the converter rated output power as well as the output voltage. In addition, current ripple is reduced since the inductors currents, of different phases of the interleaved converter, charge a shared capacitor. Moreover, the current stress is distributed on power electronics devices of different phases that tend to reduction on the interleaved converter power losses [9]–[11]. Another advantage of interleaved converters is the reduction of the size and weight of passive components due to increase in the ripple frequency [12], [13]. For two-phase interleaved converter, the ripple frequency is double the switching frequency [14]. To increase the power density, an interphase transformer is used with a common inductor to double the

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TABLE 1. Comparison between the proposed interleaved buck-boost converter and other interleaved converters.

		[29]	[30]	[31]	[32]	[33]	Proposed
Operating mode		CCM	CCM	DCM	DCM	CCM	DCM/CCM
Semiconductor voltage stress		Low (Split)	High	High	High	High	Low (Split)
Power transistor switching		Hard switching	Hard switching	Soft off switching	Soft on switching	Hard switching	Soft on switching
Components count for two-phase interleaved converter	**Switches**	4	2	2	2	2	3
	Diodes	4	2	2	2	2	3
	Inductors	2	2	0	2	1	2
	coupled inductor	0	0	1	0	1	0
	Capacitors	1	1	1	1	1	1
Components count for three-phase interleaved converter	**Switches**	6	3	hard due to coupled inductor	3	hard due to coupled inductor	4
	Diodes	6	3		3		4
	Inductors	3	3		3		3
	coupled inductor	0	0		0		0
	Capacitors	1	1		1		1
Components count for four-phase interleaved converter	**Switches**	8	4	4	4	4	5
	Diodes	8	4	4	4	4	5
	Inductors	4	4	0	4	2	4
	coupled inductor	0	0	2	0	2	0
	Capacitors	1	1	1	1	1	1

ripple frequency [9]. The coupled inductor based interleaving converter can operates in continues conduction mode (CCM) [15], [16]. However, the operation under CCM increases the weight of the converter. In [17], [18], an interleaved converter with zero voltage switching (ZVS) capability is presented. One main disadvantage of this topology is that it requires an additional inductor to achieve ZVS which operates at CCM that leads to increase the weight and footprint size of the converter.

For the electric vehicles and PV application the size and the weight of the converter is considered. Therefore, it is preferred to operate at DCM [19]. When the interleaved converter operates under DCM, it has a higher number of operating modes during one switching cycle in comparison with CCM operation. A comprehensive analysis of the interleaved boost converter including modes of operation, voltage gain, and inductor current ripple are presented in [20], [21]. The dual interleaved buck-boost converter, which operates under DCM, was presented in [22]. However, increased number of magnetics is the main disadvantages of this topology.

The conventional interleaved buck-boost converter has a simple circuit structure, but the voltage stress on the power electronics devices is high [23], [24]. The cascaded non-inverting buck-boost converter (CNIBBC) has the following advantages: reduced voltage stress and non-inverted output voltage polarity [25]. In [6], [26], three CNIBBC are connected in parallel and was operating under DCM. However, the three converters are not operating under interleaved manner since the gate signals of each CNIBBC were not phase-shifted. In turn, the blocking diode of the boost units inherits high current stress since it carries all the discharging current. Two interleaved CNIBBC are connected in parallel to boost the PV input voltage for the grid-connected inverter [27].

This paper proposed reduced switches count non-inverting interleaved buck-boost converter shown in Fig 1. The proposed topology consists of a single buck converter cascaded with n parallel-interleaved boost converters. The proposed converter has a reduced switches count compared to the interleaved parallel CNIBBC topology presented in [28], [29]. One of the main advantages of the CNIBBC topology is that the voltage stress on the power electronics switches is splitted where the buck switch faces the supply voltage stress and the boost switches face the load voltage stress [1]. In [30]–[33], the proposed interleaved buck-boost converters are based on single-switch buck-boost topology, where the voltage stress on the power electronics switches equals to the supply voltage plus the load voltage. This disadvantage limits the maximum output voltage that can be reached by the converter. Unlike the interleaved converters shown in [33], [34], that are based on coupled inductors which decrease the flexibility in extending the number of phases, the proposed interleaved converter has a simple design, easy to increase or decrease the number of the phase, and the number of phases can be odd or even. The above comparison is summarized in the Table 1.

The paper is organized as follows. Section II introduces the proposed interleaved buck-boost converter. The detailed analysis and zones of operation are presented are presented in Sections III. Section IV presents a control system to operate the proposed interleaved buck-boost converter as dc-dc converter or ac-dc converter. The experimental evaluation of the proposed system is demonstrated in section V. Finally, the article is concluded in Section VI.

II. PROPOSED INTERLEAVED CONVERTER

Fig. 1(a) shows the proposed three-phase interleaved buck-boost converter. It consists of a single buck converter (S_0 and D_0) and three interleaved parallel connected boost converters (L_1 to L_3, S_1 to S_3, and D_1 to D_3). The three boost converter

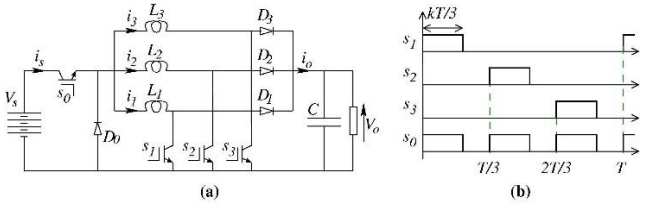


FIGURE 1. The proposed interleaved converter: (a) circuit, (b) switching signals.

switches (S_1 to S_3) operates with the same duty cycle, but each gate signal is shifted by 120° from its preceding, as shown in Fig. 1(b). The switch S_0 is turned-on simultaneously with any of S_1 to S_3. Therefore, the gate signal of the buck converter switch S_0 is obtained through OR logic-gate with input signals S_1 to S_3. As a result, the switching frequency of the buck converter is triple that of the boost converters. If the modulation index is higher than $1/n$, the proposed buck switch is turned-on continuously and the proposed interleaved converter will operate as a conventional interleaved boost converter without any adaptation in the control loop or switching pattern. This feature makes the converter has a high voltage gain with continuous input current. Moreover, the single buck switch adds soft start-up and shutdown capabilities to the proposed interleaved topology.

For non-overlapping gate signals operation, the duty cycle k must be lower than 1/3 as indicated in Fig. 1(b). If the duty cycle exceeds 1/3, S_0 becomes continuously conducting and the proposed converter operates as interleaved boost converter. This action is suitable for applications that require a high dc-voltage gain. Therefore, the proposed interleaved buck-boost converter has the capabilities of soft start-up and soft shutdown. As a result, the performance of the proposed interleaved buck-boost converter outdoes the conventional interleaved boost converter.

III. OPERATION ZONES

There are many zones of operations for the proposed interleaved converter. In this paper, the non-overlapping gate signals operation is considered. The phase inductors are assumed having the same inductance. For three-phase interleaved buck-boost converter, Fig. 2 illustrates the eight zones of operation which are determined by the converter parameters such as inductance (L), switching frequency (f), duty ratio (k), and the load resistance (R), where x = R/Lf. The following subsections present the gain equation for each operating zone and the boundaries equations with the other zones. The windings resistances are neglected and the switches are assumed ideal. These assumptions are accepted for non-overlapping gating signal operation as each inductor is energized only for one-third of the switching period.

A. ZONE 1

The on-mode and off-mode circuits for zones 1, 2, 3, and 4 are shown in Fig. 3(a) and Fig. 3(b), respectively. For zone 1, the current of the phase 1 inductor, i_1, is traced in Fig. 3(c). The

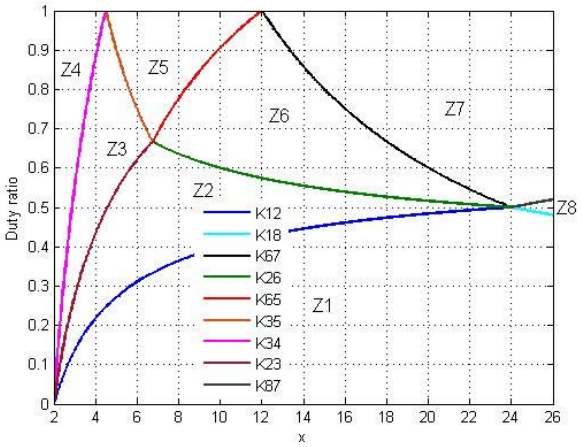


FIGURE 2. The operation zones of the proposed interleaved converter.

differential equations describing the on-mode circuit can be solved to obtain the peak currents, I_1 and I_x, as follows:

$$I_1 = kV_s/3fL \tag{1}$$

$$I_x = k(V_s - V_o)/3fL \tag{2}$$

where V_s and V_o are the supply and output voltages, respectively, and I_1 is the global peak current for DCMs. During this zone, the proposed interleaved converter behaves as a buck converter since the inductors are always charging during on-mode. This action can be revealed from (2), as I_x is a positive value. Solving the off-mode circuit, the intervals $\delta_{1,1}$ and $\delta_{2,1}$ are estimated from,

$$\delta_{1,1} = k/3fG_1 \tag{3}$$

$$\delta_{2,1} = K(1 - G_1)/3fG_1 \tag{4}$$

where $G_1 = V_o / V_s$ is the voltage gain of the converter for zone 1.

Considering the on-mode circuit, the voltage gain can be estimated by calculating the average supply current using (1) and (2),

$$G_1 = \frac{k^2 x}{6}\left(\sqrt{\frac{18}{k^2 x} + 1} - 1\right) \tag{5}$$

If the current increases, $\delta_{1,1}$ increases until it reaches $(1-k)/3f$, and operation in Zone 2, Fig. 3(d), is initiated. The boundary condition between zones 1 and 2 in the k-x plane shown in Fig. 2, K_{12}, is obtained by substituting (5) in (3) at $\delta_{1,1} = (1 - k)/3f$ as follows:

$$K_{12} = (4 - \sqrt{\frac{30}{x} + 1})/5 \tag{6}$$

B. ZONE 2

The phase 1 inductor current waveform of zone 2 is shown in Fig. 3(d). Solving the on-mode and off-mode circuits, the different peak currents and time intervals are calculated as follows:

$$I_2 = [kV_s - (1 - k)V_o]/3fL \tag{7}$$

$$I_3 = [2kV_s - V_o]/3fL \tag{8}$$

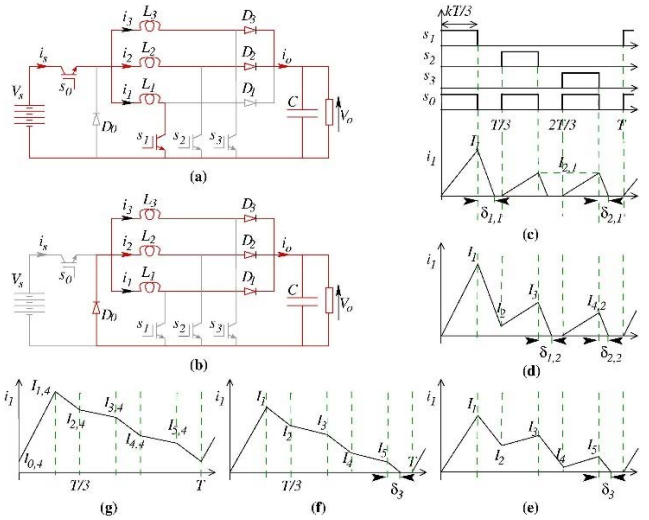


FIGURE 3. The equivalent circuits during: (a) on-mode and (b) off-mode, and the coil current of phase 1 for: (c) Zone 1, (d) Zone 2, (e) Zone 3, buck, (f) Zone 3, boost, and (g) Zone 4 of the proposed converter.

$$I_{4,2} = k(V_s - V_o)/3fL \tag{9}$$
$$\delta_{1,2} = (2k - G_2)/3fG_2 \tag{10}$$
$$\delta_{2,2} = k(1 - G_2)/3fG_2 \tag{11}$$

Similar to zone 1, the proposed converter works in buck mode during zone 2 as (9) reveals.

Referring to the on-mode circuit and calculating the average supply current using (1) and (7) to (9), the voltage gain is expressed by:

$$G_2 = \frac{kx}{6}\left(\sqrt{\frac{30}{x} + 1} - 1\right) \tag{12}$$

If the current increases, $\delta_{1,2}$ increases until it reaches (1-k)/3f, and operation in zone 3, Figs. 3(e) and (f), is initiated. At this condition, the boundary between zones 2 and 3, K_{23}, shown in Fig. 2, is derived by substituting (12) in (10),

$$K_{23} = \frac{2}{5}\left(4 - \sqrt{\frac{30}{x} + 1}\right) \tag{13}$$

C. ZONE 3

Fig. 3(e) and (f) illustrate phase 1 inductor current waveform of zone 3 for buck and boost operations, respectively. Analyzing the on-mode and off-mode circuits, the different peak currents and time interval $\delta_{1,3}$ are formulated as follows:

$$I_4 = [2kV_s - (2 - k)V_o]/3fL \tag{14}$$
$$I_5 = [3kV_s - 2V_o]/3fL \tag{15}$$
$$\delta_3 = (3k - 2G_3)/3fG_3 \tag{16}$$

The voltage gain is given by,

$$G_3 = \frac{kx}{6}\left(\sqrt{\frac{54}{x} + (3 - k)^2} - (3 - k)\right) \tag{17}$$

Inspecting (17), the condition for buck operation, in zone 3, is given by the following inequality,

$$k < \frac{3}{11}\left(1 + \sqrt{\frac{22}{3x} + 1}\right) \tag{18}$$

Continuous Current Mode (CCM) is initiated if the load is further increased, which is indicated by zone 4 in Fig. 3(g). The boundary condition between zones 3 and 4, K_{34}, is obtained by substituting $\delta_{1,3} = (1 - k)/3f$ in (16),

$$K_{34} = 3 - \sqrt{\frac{18}{x}} \tag{19}$$

It is worth mentioned that (20) gives the value of critical inductance L_C which is the minimum inductance that results in in CCM operation,

$$L_c = \frac{R}{18f}(3 - k)^2 \tag{20}$$

D. ZONE 4

As mentioned in the previous subsection, zone 4 represents the CCM of the proposed interleaved converter as illustrated in Fig. 3(g). The peak current and the voltage gain are formulated as follows:

$$I_{1,4} = \frac{V_o}{R}\left[\frac{1}{3 - k} + \frac{R}{3Lf}\left(1 - \frac{k}{3}\right)\right] \tag{21}$$
$$G_4 = \frac{3k}{3 - k} \tag{22}$$

E. ZONE 5

Fig. 4(a) and (b) illustrates the on-mode and off-mode circuits of the proposed interleaved converter during operation in zone 5. The inductor current of phase 1 is traced in Fig. 4(c). It can be noticed that the slope of the current waveform is negative during the off-mode. This action indicates that $V_s < V_o$ which reveals boost operation. The differential peak currents and the time interval δ_5 can be obtained as follows:

$$\delta_5 = [2kV_s - (2 - k)V_o]/3f(V_o - V_s) \tag{23}$$

With the aid of the above equations and the on mode circuit, the voltage gain can be expressed by:

$$G_5 = \left[\frac{1}{2} + (1 - k)(2 - k)\frac{x}{6}\right] + \sqrt{\left[\frac{1}{2} + (1 - k)(2 - k)\frac{x}{6}\right]^2 - \frac{kx}{6}(6 - 7k)} \tag{24}$$

It can be noticed that if $\delta_5 = k/3f$, operation in zone 3 is commenced and the boundary condition between zones 3 and 5, K_{35}, is obtained by solving (24) and (25),

$$K_{35} = 9/2x \tag{25}$$

F. ZONE 6

It the factor x is increased due to increase in load resistance, for example, the operation of the proposed interleaved converter is transferred from zone 5 to zone 6, as indicated in Fig. 2. For zone 6, the on-mode and off-mode circuits of the converter and the inductor current of phase 1 are shown in Fig. 4(d), (e), and (f), respectively. Similar to zone 5, boost operation is continued in zone 6. The peak currents and the time interval δ_6 are given by:

$$\delta_6 = (2k - G_6)/3fG_6 \tag{26}$$

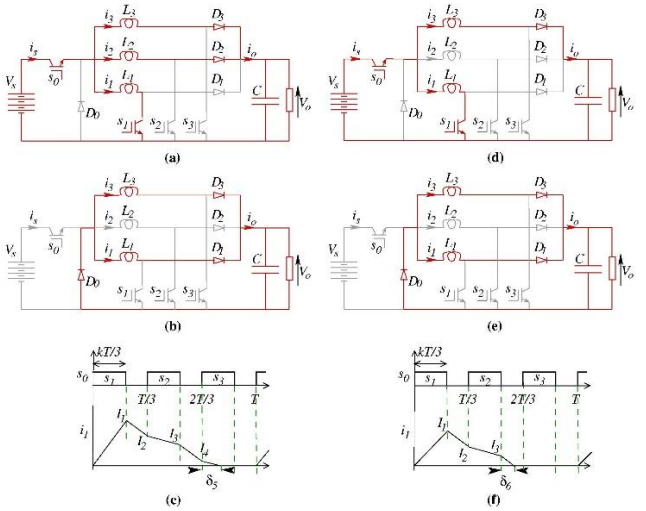


FIGURE 4. The on-mode and off-mode circuits and coil current of phase 1, for zones 5 and 6.

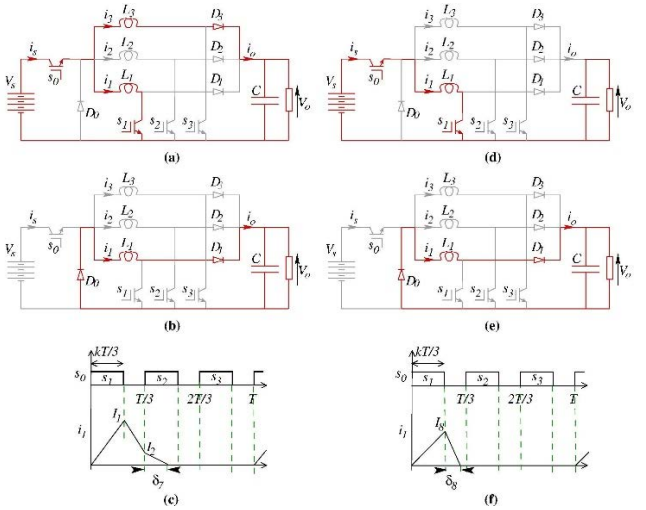


FIGURE 5. The on-mode and off-mode circuits, and coil current of phase 1, for zones 7 and 8.

As a result, the voltage gain can be obtained,

$$G_6 = \frac{kx}{12}\left(\sqrt{\frac{96}{x} + (2-k)^2} - (2-k)\right) \tag{27}$$

If the current is increased until $\delta_6 = (1-k)/3f$, operation in zone 5 is started and the boundary condition between zones 5 and 6, K_{56}, is formulated by substituting (27) in (26),

$$K_{56} = 2(1 - \sqrt{3/x}) \tag{28}$$

By inspecting the inductor current of zones 2 and 6, the boundary condition K_{26} can be derived by nulling (9), $I_{4,2} = 0$. Another way to find K_{26} is by equating the voltage gain of zone 2 (buck) or zone 6 (boost) to unity. Both methods give the following expression,

$$K_{26} = (1 + \sqrt{\frac{30}{x} + 1})/5 \tag{29}$$

G. ZONE 7

It the factor x is further increased, the operation of the proposed converter is transferred from zone 6 to zone 7, as demonstrated in Fig. 2. The on-mode and off-mode circuits of the converter during operation in zone 7 are shown in Fig. 5(a) and (b), respectively, while the inductor current of phase 1 is traced in Fig. 5(c). Boost operation can be observed as the slope of the current waveform is negative during the off-mode. The peak currents and the time interval δ_7 are calculated as follows:

$$\delta_7 = [kV_s - (1-k)V_o]/3f(V_o - V_s) \tag{30}$$

Accordingly, the voltage gain is given by,

$$G_7 = \left[\frac{1}{2} + (1-k)^2\frac{x}{12}\right] + \sqrt{\left[\frac{1}{2} + (1-k)^2\frac{x}{12}\right]^2 - \frac{kx}{6}(2-3k)} \tag{31}$$

If $\delta_7 = k/3f$, operation in zone 6 is initiated and the boundary condition between zones 6 and 7, K_{67}, is obtained by solving (30) and (31),

$$K_{67} = 12/x \tag{32}$$

H. ZONE 8

Zone 8 is the last zone for the non-overlapping gate signals operation of the proposed interleaved converter. At light loads, transfer from either zone 7 or zone 1 to zone 8 takes place as indicated in Fig. 2. The on-mode and off-mode circuits of the converter and the inductor current of phase 1 during operation in zone 8 are shown in Fig. 5(d), (e), and (f), respectively. Similar to zones 4, 5, 6, and 7, boost operation is continued in zone 8. The time interval δ_8 is given by:

$$\delta_8 = k/3fG_8 \tag{33}$$

As a result, the voltage gain is obtained from:

$$G_8 = k\sqrt{x}/6 \tag{34}$$

If $\delta_8 = (1-k)/3f$, operation in zone 7 is underway. Substituting (34) in (33), the boundary condition between zones 7 and 8, K_{78}, is obtained,

$$K_{78} = 1 - \sqrt{6/x} \tag{35}$$

Finally, the boundary condition K_{18} can be estimated by equating the voltage gain of zone 1 (buck) or zone 8 (boost) to unity which results in,

$$K_{18} = \sqrt{6/x} \tag{36}$$

At no load, $x \to \infty$. According to (35) and (36), $K_{78} = 1$ and $K_{18} = 0$, respectively. This action reveals that the proposed interleaved converter operates at zone 8 when light load is connected.

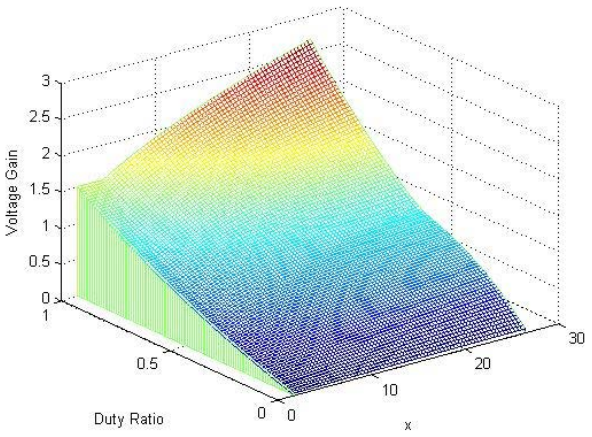


FIGURE 6. The voltage gain versus duty ratio and converter parameter.

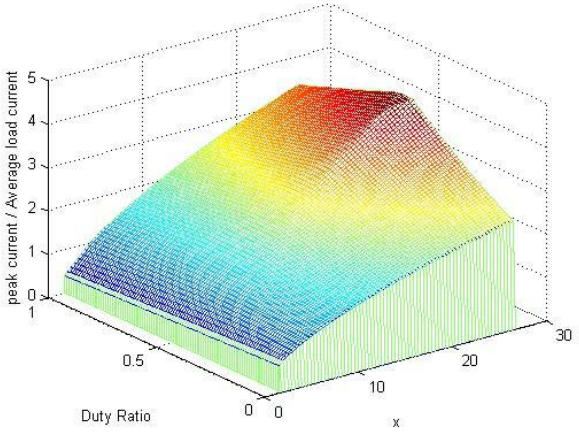


FIGURE 7. The peak current ratio versus duty ratio and converter parameter.

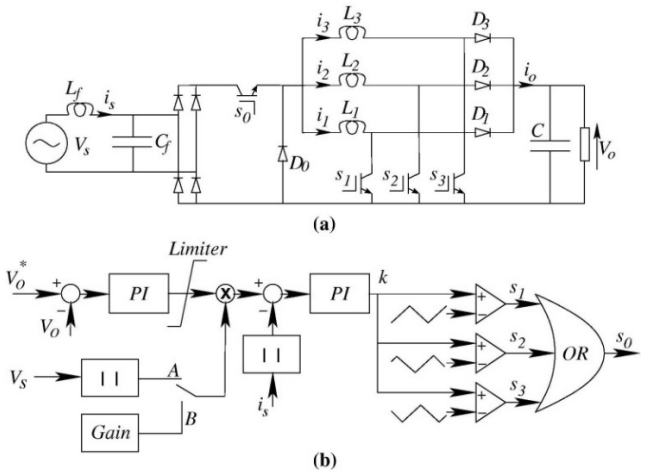


FIGURE 8. The proposed ac/dc converter system. (a) topology, (b) controller.

Referring to (1) and (21), the ratio between peak current and average load current, I_p, can be expressed as follows:

$$I_p = \begin{cases} \dfrac{xk}{3G_i} & \text{for all zones except} \\ & \text{zone } 4, (i \neq 4) \\ \dfrac{1}{3-k} + \dfrac{x}{3}\left(1 - \dfrac{k}{3}\right) & \text{for zone } 4 \end{cases} \quad (37)$$

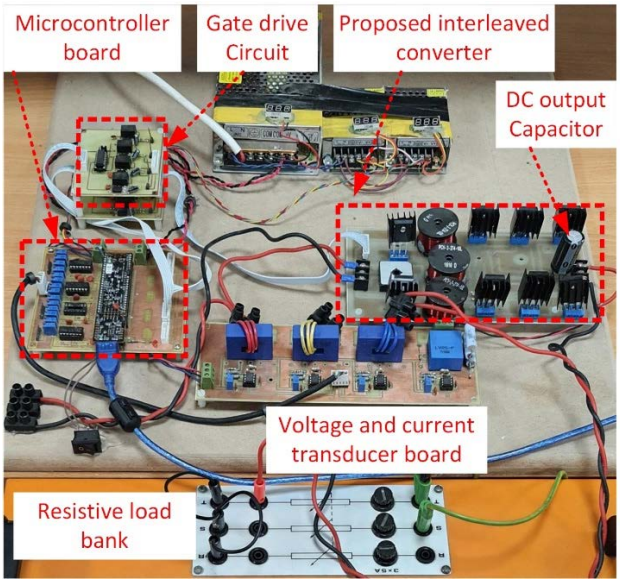


FIGURE 9. The experimental prototype.

Considering the equations of voltage gain and boundary limits for each zone, Fig. 6 shows the voltage gain surface against the load factor and duty ratio. As expected, the behavior becomes highly nonlinear when the load factor increases. The surface of the peak current ratio, given by (37), is portrayed in Fig. 7. It is obvious that the maximum value of the peak current ratio occurs at $k = 0.5$. For heavy loads, the maximum value of the peak current ratio shifts toward $k \to 0$.

IV. PROPOSED CONTROL SYSTEM

In Fig. 8(a), a rectifier with LC filter is added to the proposed interleaved dc/dc converter to work as an ac/dc converter. A cascade control system is illustrated in Fig. 8(b) which is suitable for dc/dc or ac/dc operation of the proposed converter. The outer loop regulates the output dc voltage utilizing a proportional-integral (PI) controller by setting the reference current for the inner loop. For ac/dc operation, the selector is switched to position *A* where the reference current is multiplied by the absolute value of a unity sinusoidal waveform in-phase with the supply voltage to guarantee unity power factor operation. For dc/dc operation, the selector is switched to position *B*. A current limiter is implemented to prevent overloading the converter. A PI controller is used for the inner loop to control the supply current, i_s, by setting the duty cycle for the boost switches, S_1, S_2, and S_3. Consequently, the gating signals for the boost switches are obtained by comparing the duty cycle with three carrier signals shifted by 120°. Finally, the gating signal for the buck switch, S_0, is determined as described in section II.

A digital low pass filter (LPF) is implemented to gradually increase the reference signal of the output voltage from zero to the set value to allow the proposed interleaved converter to start at buck mode, zone 1, 2, or 3 under the condition of (18). This action prevents inrush current at starting which results due to the initial charging the output capacitor. This inherent soft-stating capability is one of the advantages

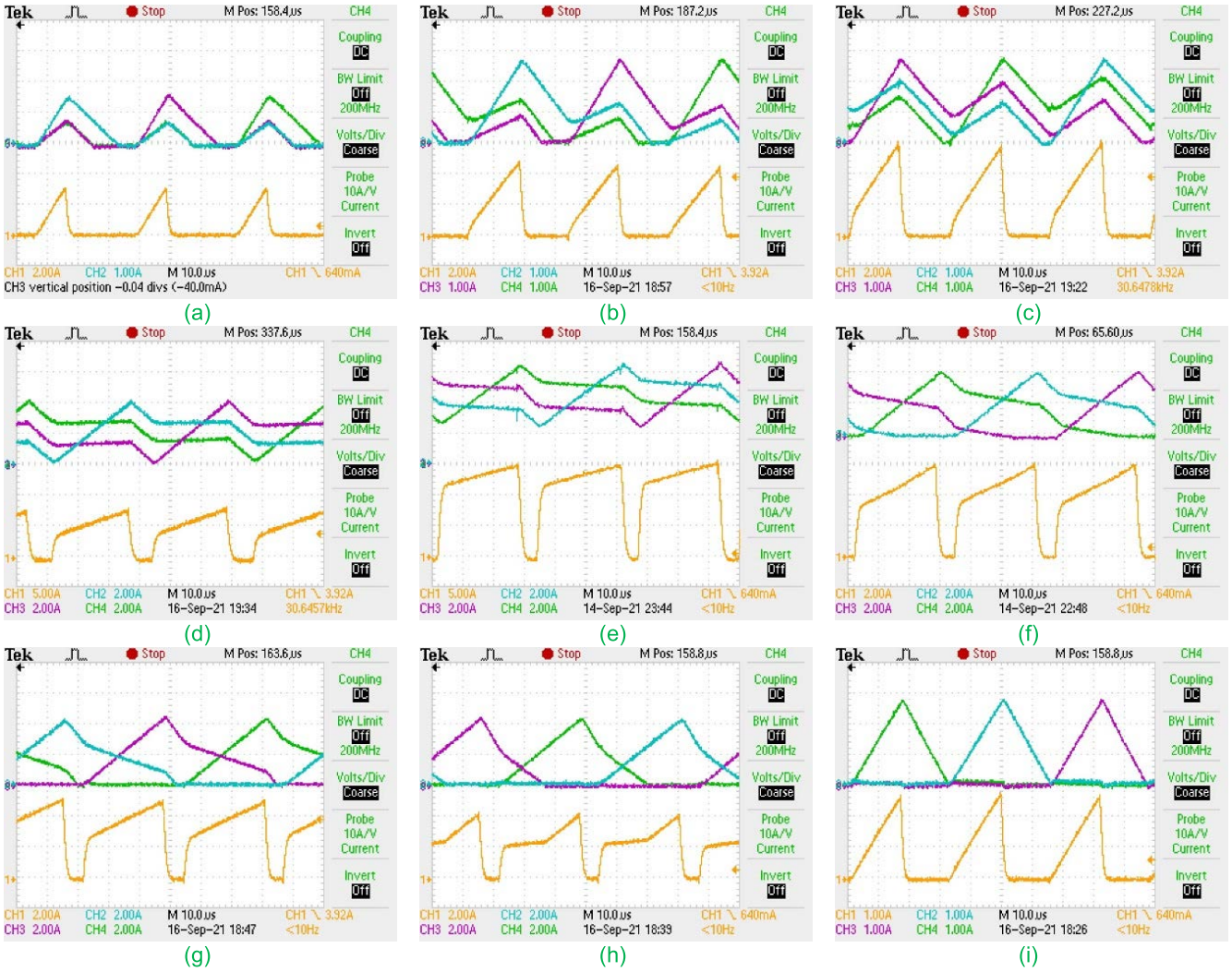


FIGURE 10. The currents of the buck switch (CH1) and three phase coils during: (a) zone 1, (b) zone 2, (c) buck operation of zone 3, (d) boost operation of zone 3, (e) zone 4, (f) zone 5, (g) zone 6, (h) zone 7, and (i) zone 8 of the proposed interleaved converter.

of the proposed interleaved buck-boost converter over the interleaved boost converter.

V. EXPERIMENTAL RESULTS

The experimental section is divided into three subsections. The first subsection is dedicated to evaluate the analyses and the different operation zones of the proposed interleaved buck-boost converter. The second subsection investigates dynamic performance of the proposed converter when works as a dc-dc converter connected to either dc-load or dc-bus. The third subsection illustrates the performance of the proposed converter for ac-dc conversion. Fig. 9 shows the laboratory prototype and the parameters are given in Table 2.

A. OPEN LOOP PERFORMANCE

The currents of the buck switch and three phase coils during operations in different zones of the proposed interleaved converter are demonstrated in Fig. 10. The eight zones of operations, which are analyzed in Section III, are recognized. For zone 3, the buck operation is illustrated in Fig. 10(c), while the unity gain operation is shown in Fig. 10(d) where

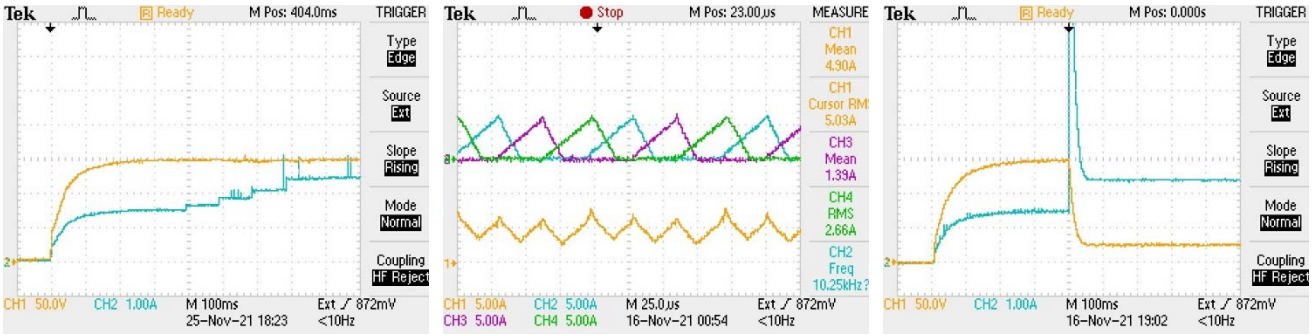
TABLE 2. System parameters.

Rated power	375W
Supply voltage, V_s	48V
Switching frequency, f	10 kHz
Inductance of phase reactors, L	0.28 mH
Output capacitance, C	220 μF

the duty ratio is set according to (18). The theoretical and experimental values of the output voltage for each case of Fig. 10 are presented in Table 3. The negligible errors between theoretical and experimental values are due to the internal coil resistance per phase. As expected, the effect of the internal coil resistance on the voltage gain can be ignored for non-overlap gate signal operation of the proposed interleaved converter. These results verify the analysis of the proposed interleaved converter.

B. DC-DC CONVERTER PERFORMANCE

Fig. 11 illustrates the dynamic performance of the proposed interleaved buck-boost converter when it is operated as a dc-dc converter. Initially, the reference output voltage is set at 150V. Fig. 11(a) demonstrates the soft start-up



(a) (b) (c)

FIGURE 11. Dynamic performance of the proposed interleaved dc-dc converter: (a) output voltage (CH1) and current (CH2) during load changes, (b) the supply current (CH1) and three coils currents (CH2, CH3, CH4) at 100Ω load, and (c) output voltage (CH1) and current (CH2) during load failure.

TABLE 3. Voltage for scenarios of Fig. 10.

	Experimental	Theoretical
(a) zone 1, $R = 30\Omega$	25.8	26.69
(b) zone 2, $R = 20\Omega$	35.4	36.78
(c) zone 3 (buck) , $R = 10\Omega$	28.3	30.4
(d) zone 3 (unity gain) , $R = 10\Omega$	46.6	48.057
(e) zone 4, $R = 5\Omega$	50.5	52.337
(f) zone 5, $R = 20\Omega$	59.6	61.38
(g) zone 6, $R = 30\Omega$	68.8	69.84
(h) zone 7, $R = 75\Omega$	91.2	92.85
(i) zone 8, $R = 75\Omega$	49.5	51.2

capability of the proposed converter where the output voltage is gradually increasing from zero to 150V without inrush current, as discussed in section IV. In addition, the load is increased in four steps from 100Ω to 60Ω where the first three steps last for 100ms. Tight voltage regulation with negligible oscillations even during step load changes is demonstrated in Fig. 11(a). Fig. 11(b) shows the three coils currents and the input supply current at 100Ω load where the duty cycle is higher than unity. Since the required voltage gain, 150V/48V, is higher than the surface given in Fig. 6, the duty cycle is expected to be higher than unity and the overlap gate signals operation is triggered. As a result, the buck-switch is turned-on and the input supply current becomes continues as indicated in Fig. 11(b). This result shows one of the features of the proposed converter, which is the operation as interleaved boost-converter for high voltage gain. To illustrate the behavior of the proposed converter under overload or load failure, Fig 11(c) shows the output current and voltage when the load is suddenly changed from 100Ω to 10Ω. It can be observed that the current limiter succeeds to limit the converter output current to it rated value, 2.5A, and protects the converter from damage. It is worth mentioning that the current spike at the overload instant results from discharging the output capacitor from the reference value, 150V, to 25V, which is corresponding to the overload resistance and current limiter setting. The efficiency of the proposed converter at different output power levels is calculated and shown in Fig. 12. It can be observed that the proposed converter has a high operating efficiency. However, the efficiency starts to drop when the output power exceeds 310W, since the

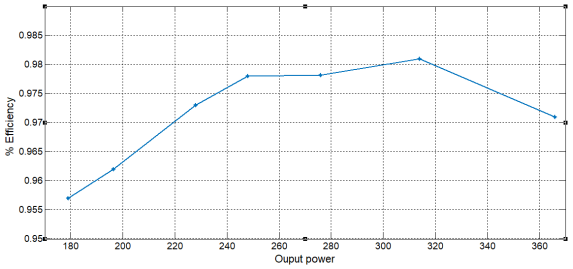


FIGURE 12. Efficiency of the proposed dc-dc converter at different output power.

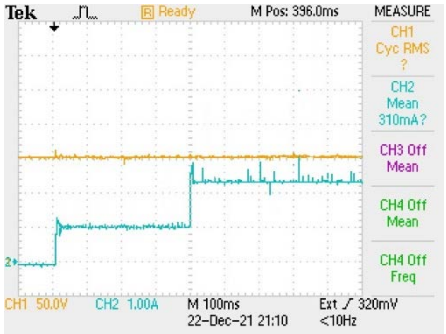


FIGURE 13. Dc-bus voltage (CH1) and load current (CH2).

inductors current becomes greater than its rated value and saturation is initiated.

Fig. 13 investigates the performance of the proposed converter when it is connected to a dc-bus of 150V to emulate the microgrids applications. During this test, the outer voltage control loop has been disabled. The reference current delivered to the dc-bus is suddenly increased from 0 to 1A and then to 2.4A. It can be observed that the proposed controller succeeds to follow the demand signal.

C. AC-DC CONVERTER PERFORMANCE

In this subsection, the proposed interleaved converter operates as an ac-dc converter. The LC filter used is 3mH and 10uF, respectively and the ac supply voltage is 50V. The supply and output voltages and currents are illustrated in Fig. 14(a). At the start-up, the reference output voltage is gradually increased, as explained in section IV, from 0 to the set point 150V. It is obvious that the proposed converter succeeds to perform a soft start-up while the supply current

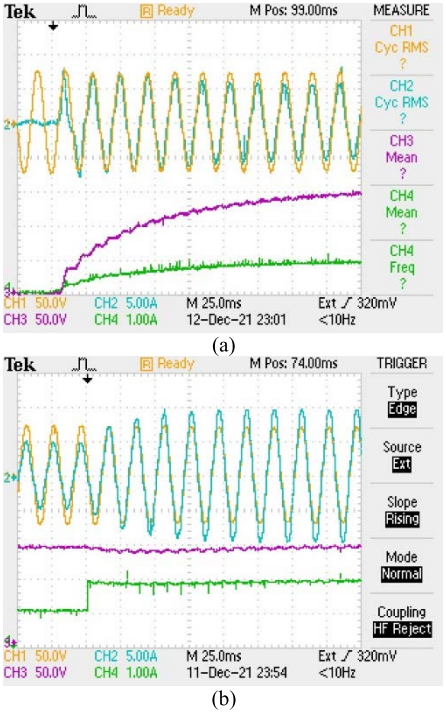


FIGURE 14. Performance of the proposed interleaved ac-dc converter where the supply voltage (CH1) and current (CH2), load voltage (CH3) and load current (CH4): (a) during start up, and (b) during step load change.

is sinusoidal and in-phase with the supply voltage. During start-up, the output voltage increases in different steps, which are governed by the gain characteristics of different zones. Successful smooth transitions between different zones are illustrated. Fig. 14(b) depicts the dynamic performance when the load resistance is suddenly changed from 150Ω to 75 Ω. It can be concluded that the proposed system succeeds to overcome the load dynamics with minimum oscillation and keeps the supply current at sinusoidal shape with unity power factor.

VI. CONCLUSION

This paper presents a reduced switch count interleaved buck-boost topology for dc-dc and ac-dc conversion systems. The buck stage offers many capabilities for the proposed converter such as soft start-up without inrush current even during overload or load failure conditions. The paper investigates the characteristics of the proposed buck-boost interleaved converter during non-overlapping gate signals operation. It has been found that the proposed converter works in boost mode during five zones, in buck mode during two zones, and buck-boost mode in one zone, Z3. For each zone, the voltage gain and peak current are derived and traced against duty cycle, converter parameters, and load resistance. Moreover, the boundary conditions between different zones are found. An experimental prototype is developed to verify the analysis and capabilities of the proposed interleaved buck-boost converter. The results validate the currents waveforms for each operating zone and the gain equations. It was found that the efficiency of the proposed converter reaches 98.5%. In addition, the soft start-up capability of the proposed converter is demonstrated for dc-dc and ac-dc operations. Moreover, the dynamic performance of the converter during load failure and dc-bus interconnection is examined. Furthermore, the results demonstrate tight voltage tracking and sinusoidal supply current with unity power factor of the proposed interleaved converter during ac-dc conversion.

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