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Performance Evaluation of an Active Neutral-Point-Clamped Multilevel Converter for Active Filtering in G2V-V2G and V2H Applications

LARA JORGE¹, (Member, IEEE), HERNANDEZ CONCEPCION¹, (Member, IEEE),
ARJONA MARCO A.¹, (Senior Member, IEEE), MASISI LESEDI², (Senior Member, IEEE),
AND CHANDRA AMBRISH³, (Fellow, IEEE)

¹División de Estudios de Posgrado e Investigación, TNM Instituto Tecnológico de La Laguna, Torreon 27000, Mexico

²School of Electrical and Information Engineering, University of the Witwatersrand, Johannesburg, Johannesburg 2000, South Africa

³Department of Electrical Engineering, École de Technologie Supérieure (ÉTS), Montreal, QC H3C 1K3, Canada

Corresponding author: Hernandez Concepcion (coni.hernandez@ieee.org)

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ABSTRACT This paper presents the performance evaluation of a proposed single-phase bidirectional active neutral-point-clamped (ANPC) five-level converter (5LC) for active filtering in grid-to-vehicle (G2V), vehicle-to-grid (V2G) and vehicle-to-home (V2H) applications. In the system, the 5LC is series-connected with an electric vehicle battery charger based on a dual active half-bridge DC-DC converter (DAHBC). A cascaded strategy with a proportional-resonant compensator controls the 5LC whereas the DAHBC is controlled by a single phase-shift technique. A performance comparison is carried out for the proposed topology versus three NPC/ANPC 5L converters found in literature with similar topologies. The simulation results obtained in MATLAB-SimPowerSystems along with the experimental results obtained from a laboratory prototype validate the following: a) the first two literature topologies have the highest efficiencies, but they are incapable of balancing the voltage of the split-capacitors what increases the total harmonic distortion of both the grid current in the G2V/V2G modes and the 5LC output voltage in the V2H mode while producing a sluggish transient response, b) the 3rd literature topology like the proposed one properly balance the capacitors voltage and achieve a faster dynamics, but at the expense of an efficiency reduction, and c) unlike the former topology that continuously applies a natural but wasting unfeedback voltage balancing strategy, the proposed one that includes a closed-loop control allows achieving an ANPC 5LC with a superior performance featured by a higher efficiency, a reduced switches stress, a flatter power losses distribution and a better power quality improving under the three modes of operation.

INDEX TERMS Five-level converter, ANPC topology, capacitor’s voltage balancing, active filter, power quality, electric vehicle, EV charger, G2V/V2G/V2H, resonant controller.

I. INTRODUCTION

Multilevel converters (MC) are fastly evolving and amazingly spreading in all power electronics applications, e.g., photovoltaics, wind generators, electric vehicles (EV), battery chargers, electrical machine drives and active power filters [1]. This is mainly due to the fact that in comparison with the traditional two-level converters, MC feature a lower dV/dt stress, a lower electromagnetic interference

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and a reduced size/cost of the required output passive filter while being capable of fault-tolerant operation as well as of handling high-voltage and high-power [2]. MC alike provide a voltage signal with a lower harmonic content and achieve it using a lower switching frequency, what represents an important advantage in terms of switching losses reduction [3]. Thus, MC are particularly a promising solution for developing more performant active filters that not only improve the power quality but also allow a more efficient power conversion [4]. The main topologies of MC are the flying capacitor (FC), the cascaded H-bridge (CHB) and

the neutral point-clamped (NPC) which also comprises the active- NPC (ANPC) subtopology [5]. Unlike the CHB, the NPC/ ANPC only requires one isolated DC source whereas in contrast with the FC, it can reliably operate at low switching frequencies and does not need pre-charging the capacitors at start-up [6]. Nevertheless, the NPC/ANPC inherently presents the voltage unbalancing phenomenon of its DC-link split-capacitors due to the non-zero average neutral current drawn over a fundamental frequency period. Therefore, it necessarily requires the implementation of voltage balancing compensating strategies [7], [8]. In spite of this requirement, three-level [9], five-level [10] and even seven-level [11] NPC/ANPC converters have been successfully applied in shunt active power filters (SAPF) for power quality improvement. In applications where these converters are further series-connected with an EV battery charger, the power transfer between the battery, the grid and the load can be controlled, thus giving rise to three possible operation modes, i.e., grid-to-vehicle (G2V), vehicle-to-grid (V2G) and vehicle-to-home (V2H) [12], [13]. The disregard of the split-capacitors voltage imbalance in the NPC/ANPC topologies results in a distorted output voltage from the converter [14]. However, under the G2V/V2G modes, this distortion is not of fairly importance since its detrimental effect on the grid current quality is in turn compensated by the active filtering algorithm. Such self-compensation also occurs in applications of pure active filters with no EV battery charger connected [15]. Nevertheless, as it will be further shown, their filtering dynamic response becomes sluggish and the converter cannot compensate for fast disturbances. In contrast, under the V2H mode, where the converter works as a conventional inverter with no power quality compensation capabilities, the voltage imbalance of capacitors becomes quite critical, since the load is being fed by a highly distorted voltage [16].

Over the last years, various NPC/ANPC five-level converters have been developed [17]–[19]. In [17], an NPC 5LC based on a topology with a reduced devices count is proposed. This single-phase converter rises from merging one leg of a conventional three-phase 2-level converter and one leg of a three-phase 3-level NPC converter. The resulting converter consisting of only six switches and two clamping diodes is advantageous in terms of a lower cost and complexity. Nevertheless, the reduction in the number of switches also eliminates the redundant switching vectors required to counteract the voltage unbalancing of split-capacitors. The distortion produced in the multilevel output voltage due to this phenomenon generally is disregarded in active filters given that the distortion produced in the grid current is concurrently improved by the implemented power quality strategy [20]. A single-phase hybrid Si/SiC ANPC 5LC is proposed in [18]. The devised topology is obtained by replacing the two clamping diodes in [17] with switches, thus having a total of eight. The addition of these two switches allows increasing the number of switching states and in turn the available current flowing paths. By selecting them according

to a particular modulation scheme, the conduction losses are properly reduced. Nevertheless, within these extra switching states there are no flowing paths neither for generating a positive voltage from the upper capacitor nor a negative voltage from the lower capacitor. Thus, when the 5LC outputs half the DC bus voltage, the charging and discharging of split-capacitors cannot be regulated, and nothing can be done to counteract the voltage imbalance. Unlike [17] and [18], the symmetrical ANPC 5LC proposed in [19] is capable of balancing the split-capacitors voltage. This topology consists of four high frequency switches commutating at twice the pulse width modulation (PWM) carrier signal and four low frequency switches that change their state with the polarity of the modulating signal. Advantageously, this ANPC 5LC has two redundant vectors to output a positive voltage from either of the capacitors and two more vectors to output a negative voltage also from either of the capacitors. Given that the modulation strategy applies the corresponding couple of redundant vectors within a switching period, thus the charging and discharging of the capacitors is the same, and consequently, the unbalancing is naturally compensated. Nevertheless, this continuous and arbitrary alternation of the redundant vectors without considering a feedback measurement, not only results in an increment of the switching power losses and a reduction of the converter efficiency but also in a higher stress of the high frequency switches.

This paper presents the performance evaluation of a proposed ANPC 5LC for active filtering in G2V, V2G and V2H applications. A performance comparison based on simulation and experimental results is carried out for the proposed topology versus three NPC/ANPC 5L converters found in literature with similar topologies [17]–[19]. The main contributions of this work are as follows:

- In contrast with [17] and [18], the proposed topology is capable of balancing the voltage of the DC-link split-capacitors. Thus, achieving a high-performance during transients in the V2G/G2V modes as well as providing a high-quality voltage signal during a power outage in the V2H mode [12], [21].
- Unlike [19], in the proposed topology, the alternation between the charging and discharging switching redundant vectors is not performed arbitrarily but as required in function of the voltage difference polarity and the direction of the 5LC current flow. As a result, a higher efficiency, a reduced switches stress and a flatter power losses distribution is achieved.
- The four presented NPC/ANPC 5L converters working as a SAPF in conjunction with a series-connected DAHB EV charger in the G2V/V2G modes and functioning within an uninterruptible power supply (UPS) unit for feeding the home loads during a power outage in the V2H mode have been neither studied nor compared in the past, thus the included analysis and results are new unpublished material.

This paper is organized as follows: section II describes the power electronics system under study, the compared four

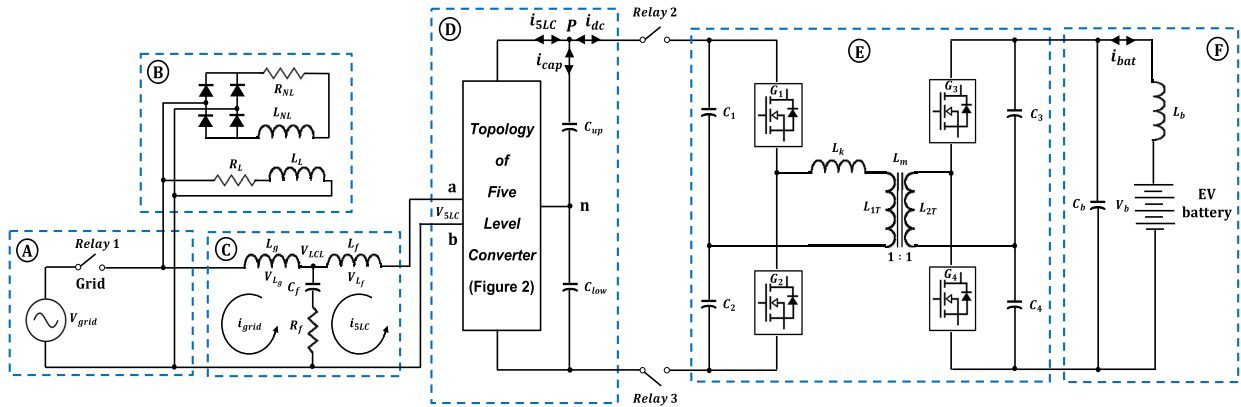


FIGURE 1. Overall diagram of the system under study: a) Single-phase grid, b) Linear/nonlinear load, c) LCL filter, d) 5LC, e) DAHBC, f) EV battery.

NPC/ANPC 5L topologies, the DAHBC and the interconnected LCL passive filter. The cascaded control strategy for the 5LC as well as the single phase-shift (SPS) control technique for the DAHBC are described in section III. Section IV presents the simulation results obtained with MATLAB-SimPowerSystems in both steady and transient state conditions. The experimental results for various scenarios under the three modes of operation as well as the power quality analysis and the power losses distribution study are presented in section V. Finally, the conclusion and some important remarks are provided in section VI.

II. POWER ELECTRONICS SYSTEM UNDER STUDY

The scheme of the overall system under study is shown in Figure 1. It consists of the 5LC, the DAHBC, the LCL filter, the EV battery, the single-phase grid as well as of the linear and nonlinear loads.

A. FIVE-LEVEL BIDIRECTIONAL CONVERTER

The electric circuit of the 5LC used as SAPF and front-end converter for regulating the transfer of energy in the three operation modes, i.e., G2V, V2G and V2H is shown in zone D of Figure 1. This 5LC works as an inverter (DC to AC) and also as a rectifier (AC to DC) depending on the operation mode and working point. It is noteworthy that due to its higher number of levels, it will inherently allow a better compensation of the grid current harmonics in comparison with 2-level and 3-level based-converter topologies [4].

Figure 2 shows the four topologies of the NPC/ANPC 5L converters analyzed in this paper [17]–[19]. The topology of the 5LC proposed in this study for working as an active filter has been previously analyzed and validated in [16]. The switching states SS_k , the state of the switches S_{1-10} and the corresponding output voltage V_{5LC} of such converter considering the voltage balancing condition always activated are shown in Table 1. Note that the voltage unbalance ΔV is defined as $V_{Cup} - V_{Cdown}$ whereas the flow direction of the battery current i_{bat} is given by the sign function sgn .

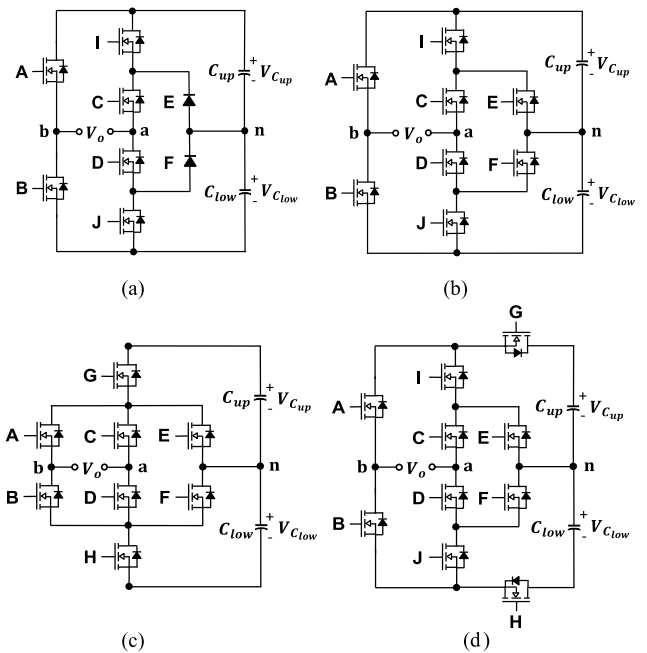


FIGURE 2. Topologies of the single-phase NPC/ANPC 5L converters under study: a) [17], b) [18], c) [19], d) Proposed.

TABLE 1. Switching states and output voltages of the proposed 5LC.

SWITCHING STATE (SS_k)	STATE OF SWITCHES										5LC OUTPUT VOLTAGE (V_{5LC})	UNBALANCE VOLTAGE (ΔV) [$sgn(i_{bat})$]	5LC OUTPUT CURRENT (i_{5LC}) [$sgn(i_{bat})$]
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}			
1	0	1	1	0	1	0	1	1	0	0	$+V_{dc}$		
2-0C	0	1	1	0	1	1	1	0	0	1	$+V_{dc}/2$	+	+
2-1C	0	1	0	1	1	0	0	1	0	0	$+V_{dc}/2$		otherwise
3	0	1	0	1	0	1	1	0	0	0	0		
4-0C	1	0	0	1	1	0	1	1	0	0	$-V_{dc}/2$		otherwise
4-1C	1	0	1	1	0	1	0	1	1	0	$-V_{dc}/2$	-	-
5	1	0	0	1	0	1	1	1	0	0	$-V_{dc}$		

The NPC 5LC from [17] and the ANPC 5LC from [18] are inherently incapable of balancing the voltage of the split-capacitors because they cannot generate a voltage of half the DC bus from either of the capacitors, thus lacking of the essential current flowing paths for carrying out the

charging and discharging process. Unlike [17] and [18], the ANPC 5LC from [19] and the proposed one are capable of balancing the capacitors voltage. In [19], the low frequency switches A-D commute twice per period of the modulating signal whereas the high frequency switches E-H commute twice per period of the triangular PWM carrier signal. At each half of this period, an opposite redundant switching vector is applied, thus alternately charging and discharging the upper and lower capacitors, what keeps them quite well balanced. In spite that the proposed topology accounts with two more switches than the one from [19], i.e., ten instead of eight, it presents a little bit higher efficiency and a better distribution of the power losses. This is because in [19], the alternation of the redundant switching vectors is continuously and indistinctly done, irrespective of the neutral current unbalancing conditions whereas in the proposed topology, the alternation between the charging and discharging switching states is carried out only when necessary, according to the sign of the voltage difference and the sign of the output current, thus reducing the stress and the switching losses.

B. DUAL ACTIVE HALF-BRIDGE DC-DC CONVERTER

Several EV charger topologies can be found in literature [22], [23]. However, the dual active full bridge (DAFB) and the dual active half bridge (DAHB) topologies are especially attractive due to the overall benefits of including a high-frequency transformer (HFT). Its main advantage is providing a galvanic isolation for safely interconnecting the EV batteries with the grid and the home load. Bearing in mind that by increasing the operating switching frequency of such converters, the physical size, weight and volume of the required HFT fairly reduce, thus the DAFB and the DAHB configurations are very suitable for EV applications [24].

Although the DAHB has limited resonance capabilities for applying zero-voltage and soft-switching techniques, it consists of only half the switches of the DAFB, what represents a smaller size and a lower cost. Another benefit is the absence of a steady-state DC magnetizing current component within the HFT due to the presence of the capacitors half-bridge [25]. Furthermore, since only half of the DC bus voltage is applied to the switching devices, their stress is lower than in the DAFB where they have to withstand the full DC bus voltage [16]. In spite that the SPS control used in the DAHB has limited degrees of liberty for carrying out the power transfer regulation, this topology is widely adopted due to its high dynamics, reduced complexity and low device count [26], [27].

According to the diagram of Figure 1, the DAHB DC-DC converter is located between the EV batteries and the 5LC. As it can be seen in zone E of this figure, the topology of such buck-boost voltage converter advantageously includes the HF isolation transformer. Besides this component, the DAHBC comprises four switches, two pairs of splitting capacitors and an optional leakage inductor. The direction and magnitude of the power flow is controlled by shifting the phase of the voltages across the terminals of the HFT. With the aim of

keeping at minimum the circulating power, the current stress and the power losses in the switching devices, the turns ratio n_r of this transformer is selected to be 1:1. The leakage and magnetization inductances of the HFT utilized in this work, the values of the splitting capacitors as well as some other design and operating parameters are provided in Table 2.

C. LCL PASSIVE FILTER

The electric diagram of the single-phase LCL passive filter used for interconnecting the 5LC to the grid and the load as well as for attenuating the HF current harmonics generated in the G2V/V2G operation mode and those of voltage in the V2H mode is shown in zone C of Figure 1.

By applying the Kirchhoff’s voltage law (KVL) in the Laplace domain s to the electrical nets on the grid and converter sides, (1)-(2) are obtained. Similarly, by applying the Kirchhoff’s current law (KCL) on the LCL node, (3) is derived [28]:

$$V_{L_g}(s) = (L_g \cdot s) \cdot i_{grid}(s) = V_{grid}(s) - V_{LCL}(s) \quad (1)$$

$$V_{L_f}(s) = (L_f \cdot s) \cdot i_{5LC}(s) = V_{5LC}(s) - V_{LCL}(s) \quad (2)$$

$$V_{LCL}(s) = [i_{5LC}(s) - i_{grid}(s)] \cdot \left(R_f + \frac{1}{C_f \cdot s} \right) \quad (3)$$

where V_{L_g} and V_{L_f} are the voltages on the inductances L_g and L_f whereas V_{LCL} is the voltage in the middle of the LCL filter as shown in zone C of Figure 1. By taking i_{grid} and V_{5LC} as the respective output and input of the system, the equivalent structure for the set of equations (1)-(3) is shown in Figure 3. By substituting (3) into (2) and equating to zero, the following expression is obtained

$$V_{5LC}(s) - (L_f \cdot s) \cdot i_{5LC}(s) - [i_{5LC}(s) - i_{grid}(s)] \cdot \left(R_f + \frac{1}{C_f \cdot s} \right) = 0 \quad (4)$$

By expanding the terms in (4) and after leaving the converter current i_{5LC} as a common factor, the former equation is rewritten as

$$(C_f \cdot s) \cdot V_{5LC}(s) = -i_{grid}(s) \cdot [R_f \cdot C_f \cdot s + 1] + i_{5LC}(s) \cdot [L_f \cdot C_f \cdot s^2 + R_f \cdot C_f \cdot s + 1] \quad (5)$$

By substituting (3) into (1) and assuming $V_{grid}(s) = 0$, the following equation is derived

$$(L_g \cdot s) i_{grid}(s) - [i_{5LC}(s) - i_{grid}(s)] \cdot \left(R_f + \frac{1}{C_f \cdot s} \right) = 0 \quad (6)$$

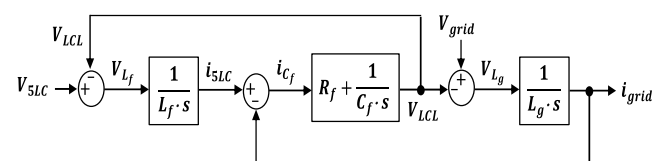


FIGURE 3. Block diagram of the LCL filter in the Laplace domain.

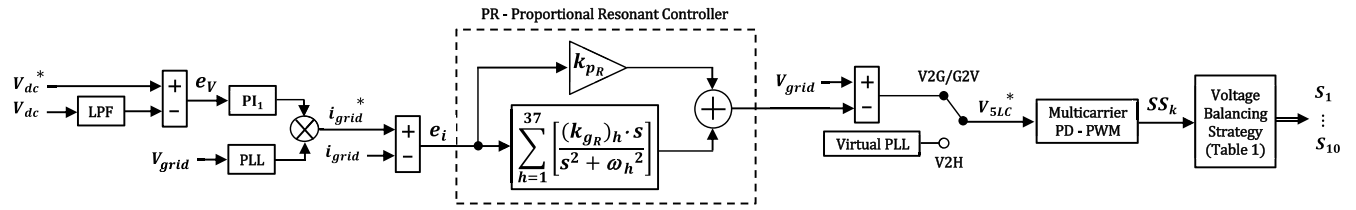


FIGURE 4. Block diagram of the cascaded control strategy for the 5LC based on PI and PR controllers and the multicarrier PD-PWM modulation [4], [16].

and by solving (6) for the converter current

$$i_{5LC}(s) = i_{grid}(s) \cdot \frac{[L_g \cdot C_f \cdot s^2 + R_f \cdot C_f \cdot s + 1]}{[R_f \cdot C_f \cdot s + 1]} \quad (7)$$

Finally, by substituting (7) into (5) and after reducing the resulting equation, the transfer function between the grid current i_{grid} and the five-level converter voltage V_{5LC} is given by [29]:

$$\frac{i_{grid}(s)}{V_{5LC}(s)} = \frac{[(R_f \cdot C_f) \cdot s + 1]}{\left[\frac{(L_f \cdot L_g \cdot C_f) \cdot s^3 + [(R_f \cdot C_f)(L_f + L_g)] \cdot s^2 + (L_f + L_g) \cdot s}{(R_f \cdot C_f) \cdot s + 1} \right]} \quad (8)$$

The parameters in (8) have been selected for achieving a fairly reduced ripple while bearing in mind the following trade-offs: a) the inductances L_f and L_g small enough for avoiding large voltage drops in the filter, b) the filter capacitance C_f small enough for avoiding a high amount of reactive power interchanged, and c) the value of the damping resistance R_f high enough for attenuating the gain at the resonance frequency but not too much in order to limit the power losses of the filter. The numerical values have been obtained following the design procedure presented in [29]–[31]. Table 2 shows the resulting values for the LCL passive filter components. Since the resonance frequency is approximated as [30]:

$$f_{resonance} \approx \frac{1}{2} \sqrt{\frac{(L_f + L_g)}{L_f \cdot L_g \cdot C_f}} \quad (9)$$

when substituting in (9) the obtained design parameters, it is found that $f_{resonance} \approx 2.25$ kHz, thus being properly lower than half the switching frequency $f_{sw/5LC} = 5$ kHz.

III. CONTROL STRATEGIES OF POWER CONVERTERS

A. CASCADED CONTROL OF 5LC

The block diagram of the cascaded control strategy for the 5LC is shown in Figure 4. According to this scheme, the DC bus voltage is regulated by means of the current demanded from the grid or supplied to the grid [4], [16]. Bearing in mind that the proportional-integral (PI) compensator is designed for linear control and acts on DC quantities, the measurement of the DC bus voltage is first low-pass filtered. This also helps to minimize the introduction of oscillations to the control loop that can give rise to instability issues due to the feedback of the same periodical components.

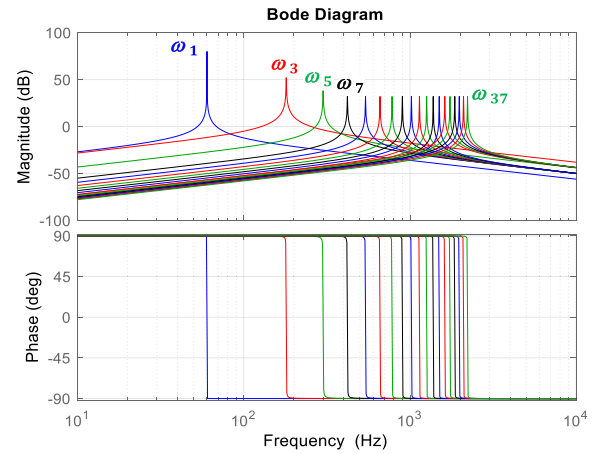


FIGURE 5. Frequency- and phase- response of the 37 transfer functions included in the PR controller of Figure 4.

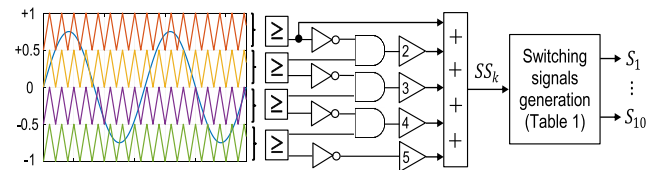


FIGURE 6. Block diagram of the multicarrier phase-disposition PWM technique.

In order to generate the grid current reference i_{grid}^* in the G2V/V2G operation modes, a PI controller and a phase-locked-loop (PLL) are used. Note that unlike V_{dc}^* , i_{grid}^* is not a constant value but a sine wave synchronized with the grid voltage V_{grid} . Given that a PI controller has a limited bandwidth, and hence a poor performance for tracking the sinusoidal harmonic signals found in the grid current, it has been replaced with a proportional-resonant (PR) controller, which has a theoretical infinite gain at the resonance frequency and also a zero steady-state error [17]. In order to properly compensate the grid current distortion, this PR controller has been tuned for the first 37 harmonics. The gains of the controllers PI₁ and PR included in Figure 4 are provided in Table 5 of the appendix. The design and stability analysis of this controller as well as the details about its implementation can be found in [32]. The frequency and phase responses for the resulting set of transfer functions are shown in Figure 5.

In the G2V/V2G operation modes, the voltage reference V_{5LC}^* of the five-level converter is obtained by subtracting

the output of the PR controller from the grid voltage V_{grid} . In the V2H mode, V_{5LC}^* is simply obtained from a virtual PLL that outputs a 60Hz sine wave with the same peak voltage of the grid operating in normal conditions. The classical multicarrier phase-disposition (PD) PWM has been used for generating the ten switching signals S_{1-10} [4], [14]. A detailed scheme of the PD-PWM block included on the right-hand side of Figure 4 is shown in Figure 6. Note that in this modulation technique, the amplitude of the voltage reference also called modulating signal is first normalized, then divided into fourth vertical sections and finally each of the resulting waveforms is accordingly compared with one of the four synchronized triangular carriers.

Figure 7 shows the closed-loop control scheme with the transfer functions involved in the cascaded strategy for regulating the DC bus voltage V_{dc} and the grid current i_{grid} by means of two series-connected controllers [4], [16]. For this, the PLL first synchronizes with the grid voltage V_{grid} and provides a unit sinusoidal signal. Then, it multiplies with the output from the compensator $H_{Cv}(s)$ of the outer voltage loop for generating the grid current reference i_{grid}^* that becomes the input of the cascaded inner current loop. Later, the output from the compensator $H_{Ci}(s)$ becomes the voltage reference V_{5LC}^* of the converter. This voltage is assumed to be ideally synthesized with the ANPC 5LC by means of the multicarrier PD-PWM [4], [14]. Note that the resulting state SS_k is sent to the voltage balancing block that finally outputs the switching signals S_{1-10} of the converter. The maths behind these cascaded controllers is described in the following.

The outer loop voltage error e_v and the inner loop current error e_i are defined as [16]:

$$e_v = V_{dc}^* - V_{dc} \quad (10)$$

$$e_i = i_{grid}^* - i_{grid} \quad (11)$$

where the superscript * means a reference signal. Bearing in mind that the middle branch of the LCL filter (see zone C of Figure 1) is a low impedance path for the high-frequency harmonics, it is assumed that they are totally filtered out and thus, the low-frequency (LF) currents flowing through the inductances L_f and L_g are equal. The analysis shown below dealing with only low-frequency signals is a valid approximation since under such condition, the low-frequency

harmonics are much more significant than the high-frequency ones, which are ideally attenuated and absorbed by the middle branch of the LCL filter. Hence, by applying the KVL to the simplified power circuit of Figure 1 consisting of the 5LC connected to the single-phase grid through two series inductors, the following equation is obtained:

$$(L_f + L_g) \frac{di_{grid}(t)}{dt} - V_{grid}(t) + V_{5LC}(t) = 0 \quad (12)$$

where t means time whereas the terms L_f and L_g represent the line inductance on the converter side and the grid side, respectively. The variables i_{grid} , V_{grid} and V_{5LC} are the grid current, the grid voltage and the 5LC output voltage. This voltage can be represented as a function of the duty cycle δ as [4]:

$$V_{5LC}(t) = \delta(t) \cdot V_{dc}(t) \quad (13)$$

By substituting (13) in (12) while assuming an average value for the grid current and the respective duty cycle, the small signal model of the grid current is given by:

$$i_{grid}(s) = \frac{V_{grid} - \delta \cdot V_{dc}(s)}{(L_f + L_g) \cdot s} \quad (14)$$

Assuming that the inner current loop is at least ten times faster than the outer voltage loop, V_{grid} can be seen as a constant value that does not vary with time, thus, $V_{grid}(s) = 0$. Hence, the transfer function $H_i(s)$ for the inner current loop is written as:

$$H_i(s) = \frac{i_{grid}(s)}{\delta \cdot V_{dc}(s)} = -\frac{1}{[(L_f + L_g) \cdot s]} \quad (15)$$

Bearing in mind that the inner loop deals with the grid current that is an AC quantity, thus a PR controller with a zero steady-state error and a theoretical infinite gain at the resonance frequency has been used. The transfer function $H_{Ci}(s)$ of this current controller is given by [32]:

$$H_{Ci}(s) = k_{PR} + \sum_{h=1}^{37} \left[\frac{(k_{GR})_h \cdot s}{s^2 + \omega_h^2} \right] \quad (16)$$

where ω_h is the angular frequency of the harmonics, and the index h is an odd integer number. After applying the KCL at the node P in the power circuit of Figure 1, the following equations are obtained [16]:

$$i_{dc}(t) - i_{cap}(t) - i_{5LC}(t) = 0 \quad (17)$$

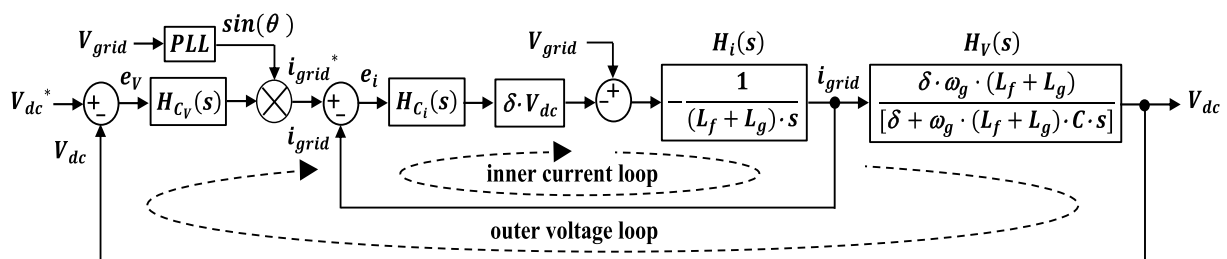


FIGURE 7. Scheme of cascaded control strategy for the grid-tied five-level converter [4], [16].

$$i_{dc}(t) = \delta(t) \cdot i_{grid}(t) \quad (18)$$

$$i_{cap}(t) = C \cdot \frac{d[V_{dc}(t)]}{dt} \quad (19)$$

$$i_{5LC}(t) = \frac{V_{5LC}(t) - V_{grid}(t)}{\omega_g \cdot (L_f + L_g)} \quad (20)$$

where i_{dc} is the DC bus current, i_{cap} is the split-capacitors current and $C = C_{up}/2 = C_{low}/2$ whereas ω_g is the grid angular frequency. By substituting (13) into (20), and the resulting (18)-(20) into (17) while assuming an average value for the grid current and the duty cycle, the small signal model that links up the DC bus voltage with the grid current is found as:

$$\begin{aligned} & \delta \cdot \omega_g \cdot (L_f + L_g) \cdot i_{grid}(s) \\ & - [\omega_g \cdot (L_f + L_g) \cdot C \cdot V_{dc}(s)] \cdot s \\ & - V_{5LC}(s) + V_{grid}(s) = 0 \end{aligned} \quad (21)$$

By considering in (21) the same assumption as in the inner loop, i.e., $V_{grid}(s) = 0$, the transfer function $H_V(s)$ for the outer voltage loop is expressed as:

$$H_V(s) = \frac{V_{dc}(s)}{i_{grid}(s)} = \frac{\delta \cdot \omega_g \cdot (L_f + L_g)}{[\delta + \omega_g \cdot (L_f + L_g) \cdot C \cdot s]} \quad (22)$$

Bearing in mind that this outer loop deals with the bus voltage that is a DC quantity, thus a classical PI controller has been used. The transfer function $H_{C_V}(s)$ of this voltage controller is given by [4]:

$$H_{C_V}(s) = k_{p5LC} + \frac{k_{i5LC}}{s} \quad (23)$$

By programming the transfer functions of the plants (15), (22) as well as the compensators (16), (23) in MATLAB code and using the single-input single-output (SISO) design tool, the gains of the controllers have been accurately tuned until obtaining a good response [4], [16], [32]. The gains of the controllers PR and PI₁ included in (16) and (23) can be found in Table 5 of the appendix.

B. SINGLE-PHASE-SHIFT CONTROL OF DAHBC

The block diagram of the classical SPS control strategy applied to the DAHBC DC-DC converter is shown in Figure 8. In the V2G operation mode, the battery discharging is regulated by using only the current control mode whereas in the G2V mode by changing the state of selector 1 also the voltage control mode is used, thus fully implementing the classical constant current (CC) – constant voltage (CV) battery charging technique [13]. It is important to note that in the three modes of operation, e.g., G2V, V2G and V2H, the switching signals $G_1 = \bar{G}_2$ are obtained from the SPS technique whereas $G_3 = \bar{G}_4$ are simply derived from a 50% fixed-duty cycle block.

As it is shown in Figure 8, the selector 2 allows choosing the phase Φ from either the G2V/V2G modes or the V2H mode, respectively. In both cases, the output from either of the PI controllers corresponds to the angle that exists between the pulses G_1 and G_3 . During the G2V mode, the pulses G_1/G_2

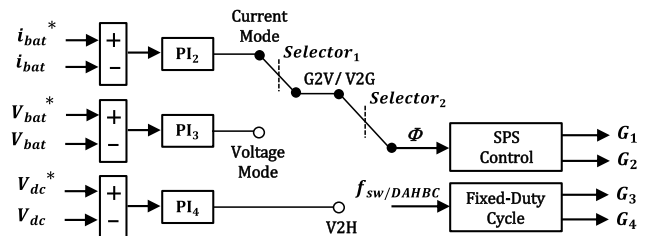


FIGURE 8. Control block diagram of the DAHBC DC-DC converter based on the SPS technique and PI compensators.

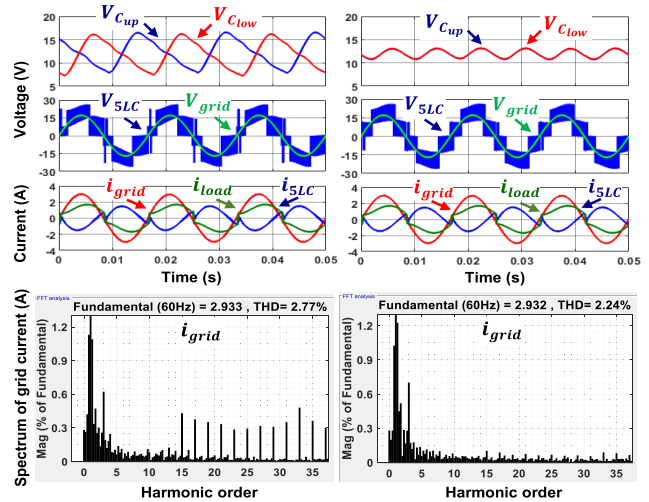


FIGURE 9. Time and frequency domain curves of the four NPC/ANPC 5L converters under the G2V mode. (Left) [17] and [18], (Right) [19] and proposed.

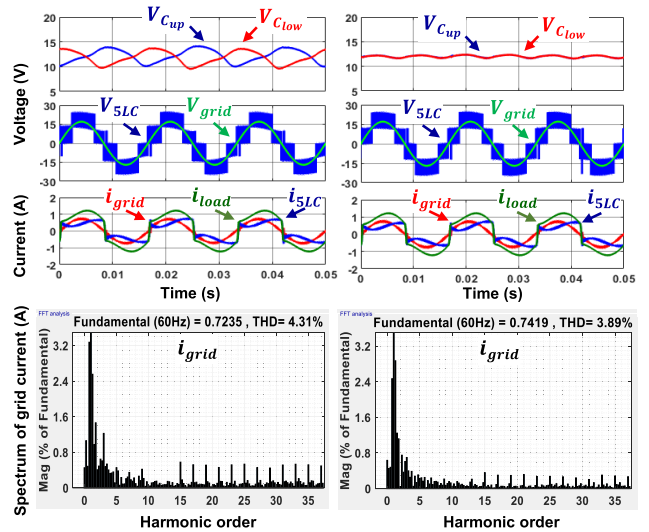


FIGURE 10. Time and frequency domain curves of the four NPC/ANPC 5L converters under the V2G mode. (Left) [17] and [18], (Right) [19] and proposed.

lead G_3/G_4 , whereas in the V2G/V2H modes, the pulses G_1/G_2 lag G_3/G_4 , respectively. It is important to note also that during the G2V/V2G modes, the cascaded control strategy regulates the DC bus voltage V_{dc} through the 5LC, whereas in the V2H mode, it is controlled by the SPS strategy by means

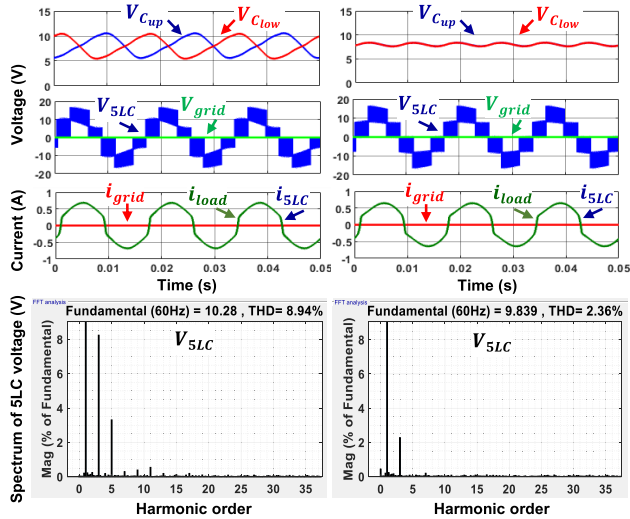


FIGURE 11. Time and frequency domain curves of the four NPC/ANPC 5L converters under the V2H mode. (Left) [17] and [18], (Right) [19] and proposed.

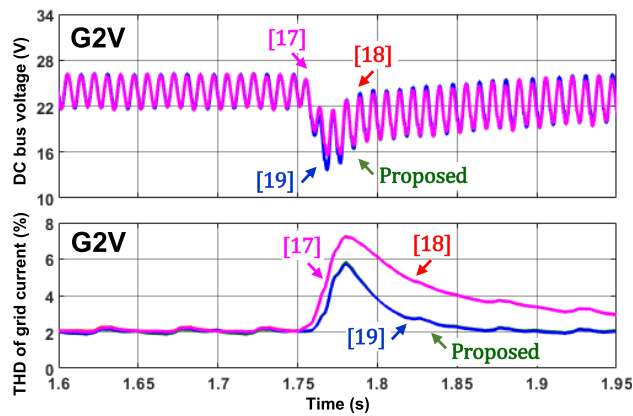


FIGURE 12. Comparison of the transient state response during a step-change in load under the G2V mode.

of the DAHBC [12]. The gains of the controllers PI_2 , PI_3 and PI_4 included in Figure 8 can be found in Table 5 of the appendix.

IV. SIMULATION RESULTS

A. STEADY-STATE IN G2V, V2G AND V2H MODES

Figures 9-11 show the steady-state results obtained from the four NPC/ANPC 5L converters under study when operating in the G2V, V2G and V2H modes, respectively. The displayed curves are the voltage of upper and lower split-capacitors $V_{C_{up}}$ and $V_{C_{low}}$, the output voltage of the converter V_{5LC} , the grid voltage V_{grid} , the grid/load/converter currents i_{grid} , i_{load} , i_{5LC} as well as the spectrum of either i_{grid} or V_{5LC} .

In Figure 9, it can be observed how under the G2V mode, a quite big voltage unbalancing of capacitors is generated with the topologies [17] and [18], and how it is properly compensated with the topology [19] and also with the proposed one. This compensation allows reducing the total harmonic distortion (THD) of the grid current from about 2.8% to 2.2%.

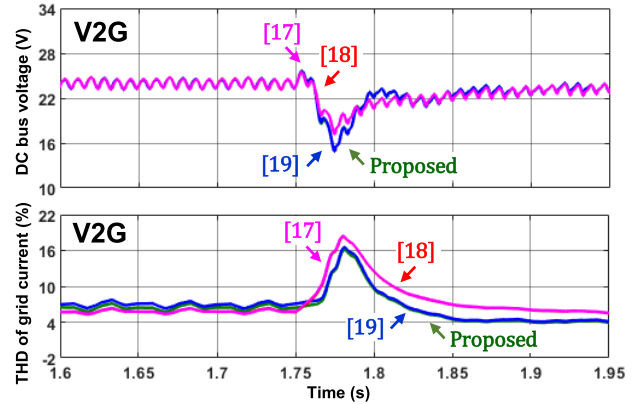


FIGURE 13. Comparison of the transient state response during a step-change in load under the V2G mode.

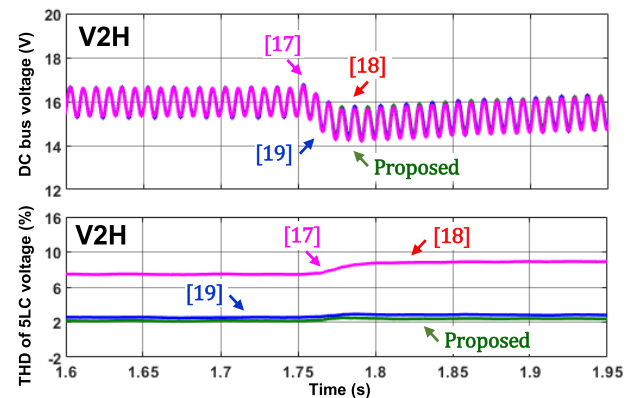


FIGURE 14. Comparison of the transient state response during a step-change in load under the V2H mode.

Under the V2G mode, the voltage unbalancing is alike present in [17] and [18] whereas in [19] and the proposed, the voltage of split-capacitors properly overlaps. As a result, the voltage signal provided by both of these 5LC has symmetrical levels as it shown in Figure 10. In this operation mode, the balancing compensation techniques have allow reducing the THD from around 4.3% to 3.9%.

Bearing in mind that under the V2H mode, the full system is off-the-grid, thus no grid voltage and consequently no grid current are available. Hence, Figure 11 shows instead the spectrum of the output voltage from the 5LC. It can be observed how in [17] and [18], the THD of V_{5LC} is near 8.9% whereas in [19] and the proposed, it is reduced to only 2.4%. Note that under the V2H mode, the waveform of the current supplied by the 5L converter i_{5LC} becomes the same as that of the load current i_{load} since $i_{grid} = 0$.

B. TRANSIENT-STATE IN G2V, V2G AND V2H MODES

Figures 12-14 show the transient-state results obtained from the four NPC/ANPC 5L converters during a step-change in load under the G2V, V2G and V2H modes, respectively. The displayed curves are the DC bus voltage V_{dc} and the THD of either i_{grid} or V_{5LC} . It can be observed that the transient

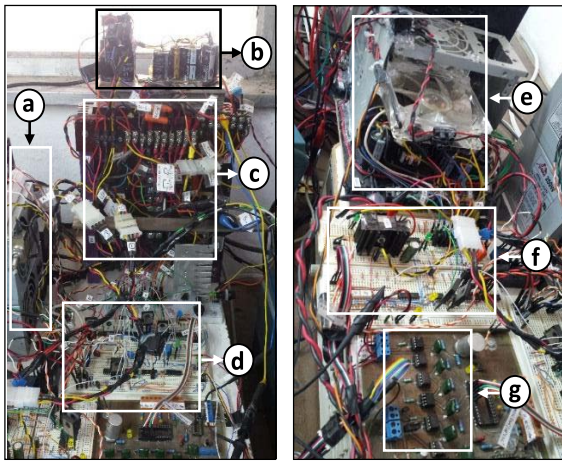


FIGURE 15. Prototypes of power converters: a) Isolated DC sources, b) DC-link capacitors, c) NPC/ANPC 5LC, d) Drivers of 5LC, e) DAHBC, f) Drivers of DAHBC, g) Optocouplers.

of the DC bus voltage regulation during the step-change in load is very similar for the four 5L converters. However, in [19] and the proposed, the dynamic response of the THD not only presents a lower value but also reaches faster the steady-state conditions. Note also how the responses in [17] and [18] present a higher THD peak value as well as a sluggish dynamics. Given that in the V2H mode, the 5L converters work as a conventional inverter without any active filtering capability, thus [17] and [18] are not able of compensating its self-distortion produced by the voltage unbalancing of the split-capacitors. Therefore, under the V2H operation mode, they provide an output voltage V_{5LC} with a fairly high THD. In contrast, the balancing strategies applied in [19] and the proposed 5LC allow keeping such THD much below 5%, thus providing a high-quality voltage signal for properly supplying the home loads while fulfilling the standard IEEE 519.

V. EXPERIMENTAL RESULTS

In order to evaluate and validate the performance of the four NPC/ANPC 5L converters, the DAHBC and their control strategies under the three operation modes, they have been implemented and exhaustively tested.

Figure 15 shows a close-up view of the prototypes built in laboratory, i.e., the five-level converters, the dual active half bridge DC-DC converter and their drivers.

Figure 16 shows the full experimental setup whereas Table 2 provides its design and operating parameters.

Figure 17 shows the experimental results obtained from the prototype built in laboratory. With the aim of straightforwardly comparing all of them, they have been organized and presented in three rows having three graphs each. The top and middle rows group the results for the G2V and V2G operation modes whereas the bottom row groups the results for the V2H mode. The particular tests conditions as well as the results for each operation mode are described below.

TABLE 2. Parameters of the experimental setup built in laboratory.

	PARAMETER	SYMBOL	VALUE	UNITS
Switching frequency	5LC	$f_{sw/5LC}$	5	kHz
	DAHBC	$f_{sw/DAHBC}$	10	
LCL filter	damping resistance	R_f	6.8	Ω
	capacitance	C_f	4	μF
	inductance (5LC side)	L_f	2.5	mH
	inductance (grid side)	L_g	2.5	
HF transformer	magnetization inductance	L_m	8.3	mH
	leakage inductances	L_{1T}, L_{2T}	0.082	
Inductance of the battery inductor		L_b	5	
Grid frequency		f_{grid}	60	Hz
Grid voltage (peak)		V_{grid}	22 12 9 *	
DC bus voltage		V_{dc}	24 16 *	V
Battery	nominal voltage	$V_{bat/nom}$	21	
	rated current capacity	$i_{bat/Ah}$	120	Ah
Capacitance	5LC split-capacitors	C_{up}, C_{low}	128	μF
	DAHBC split-capacitors	C_1, C_2 C_3, C_4	680 165	
battery side capacitor		C_b	100	
Linear RL load	resistance	R_L	26 38 **	Ω
	inductance	L_L	15	mH
Nonlinear RL load	resistance	R_{NL}	4 8 **	Ω
	inductance	L_{NL}	35	mH
Sampling time / Time-step		T_s	100	μs

* Note 1: $V_{dc} = 24\text{V}$ with $V_{grid} = 22\text{V}$ in the G2V mode and $V_{grid} = 12\text{V}$ in the V2G mode whereas $V_{dc} = 16\text{V}$ with $V_{grid} = 9\text{V}$ in the V2H mode, respectively.

** Note 2: The variation of the linear/nonlinear loads for increasing/decreasing the load current has been done by interchanging between the resistance values on the left and right sides of the symbol |.

A. G2V: GRID-TO-VEHICLE

The results shown in Figure 17a correspond to the following sequence of events:

- At $t = 3\text{s}$, the battery current reference i_{bat}^* is step-changed from -0.2A to -0.4A , where the negative sign of i_{bat} implies that the battery is charging.
- At $t = 7\text{s}$, i_{bat}^* is returned back to -0.2A .

It can be observed how the battery current properly follows the desired reference. Likewise, the grid current i_{grid} accurately remains in-phase with the grid voltage V_{grid} , thereby confirming that the grid is sending power to the battery. It is noteworthy that in spite of the current step-changes, the voltage unbalancing of split-capacitors is fairly well compensated by maintaining $V_{C_{up}}$ overlapped with $V_{C_{low}}$ at half the DC bus voltage $V_{dc}^* = 24\text{V}$.

Figure 17b shows the results obtained from a grid voltage sag of 18% while the battery current is regulated at a constant value of -0.4A . From $t = 5\text{s}$, the peak value of V_{grid} is gradually decreased from 22V to 18V. It can be noted that this sag event practically has no influence neither on the DC bus voltage regulation nor in the battery current control.

Figure 17c shows the results obtained from a 17% increment in the DC bus voltage. At $t = 5\text{s}$, V_{dc}^* is step-changed from 24V to 28V. Due to the voltage balancing strategy, the upper and lower capacitors properly keep the same voltage during the full test, even when the DC bus voltage variation occurs. Note that the output voltage from the 5LC not only increases quite fast, but also does it while always maintaining its voltage levels accurately symmetric.



FIGURE 16. Experimental setup built in laboratory: a) Dual active half-bridge DC-DC converter, b) Drivers of power converters, c) Single-phase NPC/ANPC five-level converters, d) DC voltage sources, e) Auxiliary passive battery charger, f) Grid connectors board, g) LCL passive filter, h) Linear and nonlinear loads, i) Single-phase variable autotransformer for grid interfacing, j) Tektronix Hall current probes, k) Lead-acid rechargeable battery bank, m) Voltage/current hall sensors and signal conditioning stage, n) DSP/FPGA-based control cards, p) Control dashboard, q) Power quality analyzer Fluke 43B, r) PC - Windows 10 /i7/8Gb RAM, s) Tektronix and Agilent digital scopes, t) Multimeters.

Furthermore, the magnitude of the output current from the 5LC does not undergo any visible disturbance in spite of the sudden increment in the DC bus voltage.

B. V2G: VEHICLE-TO-GRID

The results shown in Figure 17d correspond to the following sequence of events:

- At $t = 3s$, i_{bat}^* is step-changed from $+0.2A$ to $+0.4A$. Given that the sign of i_{bat} is positive, thus the battery is discharging.
- At $t = 7s$, i_{bat}^* is returned back to $+0.2A$.

It can be noted that the results are very similar to the ones obtained in the G2V mode. The only noticeable difference is that the magnitude of i_{grid} is lower than in the G2V mode since the battery is now contributing to feed the load.

Figure 17e shows the results obtained from a grid voltage swell of 25% while i_{bat}^* and V_{dc}^* remain at $+0.4A$ and $24V$, respectively. From $t = 2.5s$, the peak value of V_{grid} is gradually increased from $16V$ to $20V$. As with the grid voltage sag, in the G2V mode, this grid voltage swell event has no effect on the battery current while the DC bus voltage alike only undergoes a small disturbance and fastly reaches steady-state.

Figure 17f shows the results obtained from a 14% decrement in the DC bus voltage. At $t = 1.25s$, V_{dc}^* is step-changed from $28V$ to $24V$. It is noteworthy how even during this fast DC bus voltage transient that lasts less than two cycles of the grid frequency, V_{5LC} remains symmetrical. Under these conditions, the battery current regulation loop and the active filtering control also remain unaffected, thus

maintaining a high-quality grid current accurately in-phase with the grid voltage.

C. V2H: VEHICLE-TO-HOME

The results shown in Figure 17g correspond to the following event:

- At half the time scale, i.e., $t = 0.1s$, the active filtering algorithm is activated. Therefore, from there on the PR controllers start compensating for the grid current harmonics.

Note that during the full test, the grid is still connected at the point of common coupling (PCC) but the battery current flow is maintained at zero. Hence, under such conditions, the proposed 5LC behaves as a pure active filter that compensates the harmonics generated by the nonlinear load. It can be observed how from $t = 0.1s$, the grid current i_{grid} becomes a sinusoidal waveform while it remains accurately in-phase with the grid voltage V_{grid} . These results mean that the grid is only providing active power whereas the active filter is supplying the reactive power demanded by the nonlinear home load.

Figure 17h shows the results obtained from a sudden power outage. At half the time scale, i.e., $t = 100ms$, the grid is abruptly disconnected from the PCC. It is noteworthy how the V2H operation mode is immediately activated, thereby the battery supplies the power required by the load while the 5LC provides a high-quality voltage signal V_{5LC} with a very low harmonic content. During this power failure and its restoration, the load is seamlessly and uninterruptedly fed from either of the available power sources [12], [21].

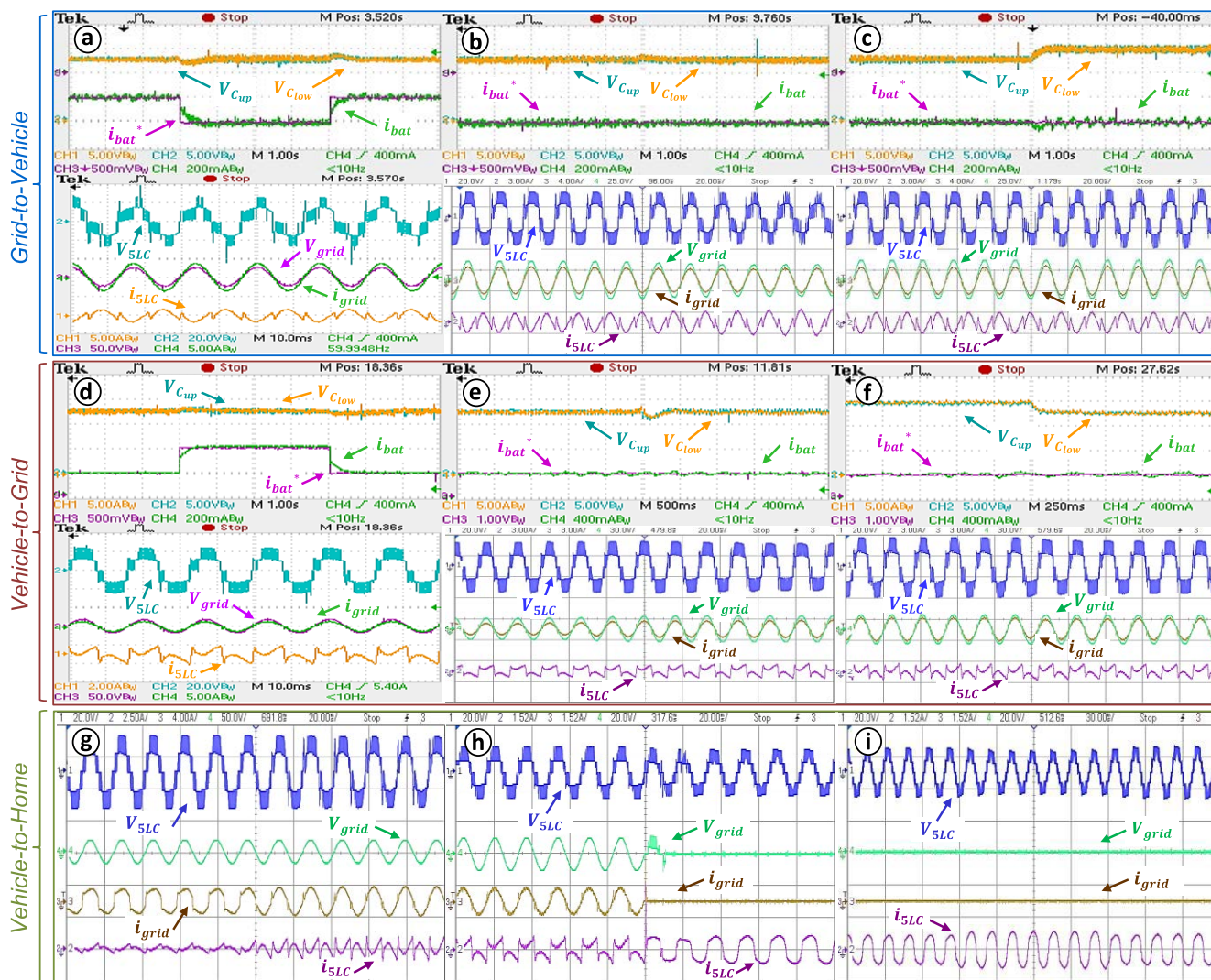


FIGURE 17. Experimental results: (Top row) G2V: a) Step-change in current i_{bat}^* , b) Grid voltage sag, c) Increment of V_{dc}^* , (Middle row) V2G: d) Step-change in current i_{bat}^* , e) Grid voltage swell, f) Decrement of V_{dc}^* , (Bottom row) V2H: g) Active filter activation while $i_{bat} = 0$ and the grid is still connected, h) Sudden power outage, i) Increment and decrement of load current with the grid disconnected.

Note that before the transition to the V2H mode, the load voltage waveform V_{load} is the same as that of the grid voltage V_{grid} due to its shunt connection whereas after this transition, the load current i_{load} is equivalent to the converter current i_{5LC} since they are series connected and the grid current is zero. Thus, the load voltage and load current waveforms are also implicitly shown in this figure.

Figure 17i shows the results obtained from an incremental and a decremental step-change in the load current. During the full test, the grid remains disconnected from the PCC while the battery supplies the total power drawn by the load. At $t = 90\text{ms}$, the load is step-changed for producing an increment of 28% in the peak current, thus going from +0.7A to +0.9A. Later, at $t = 210\text{ms}$, the load is changed to its former value so that the peak current returns back to +0.7A, equivalent to a current variation of 22%. From the multilevel voltage signal it can be inferred that the voltage of the DC-link

is slightly disturbed by these load changes but it properly reaches steady-state conditions while maintaining V_{dc}^* at around 16V. It is also noteworthy how the voltage balancing of split-capacitors is practically unaffected since they keep fairly well its voltage at half of V_{dc} .

D. POWER QUALITY ANALYSIS

Figure 18 shows the experimental results obtained from a power quality analysis carried out with the Fluke 43B for a set of exhaustive tests under the three modes of operation, e.g., G2V, V2G and V2H.

Figure 18a shows the output voltage V_{5LC} and current i_{5LC} from the five-level converter during the G2V operation mode whereas Figure 18b shows the resulting grid voltage V_{grid} and grid current i_{grid} . Note that they are in-phase because the energy is flowing from the grid to the load and the battery. For this reason, the power factor (PF) is also positive. The spectra

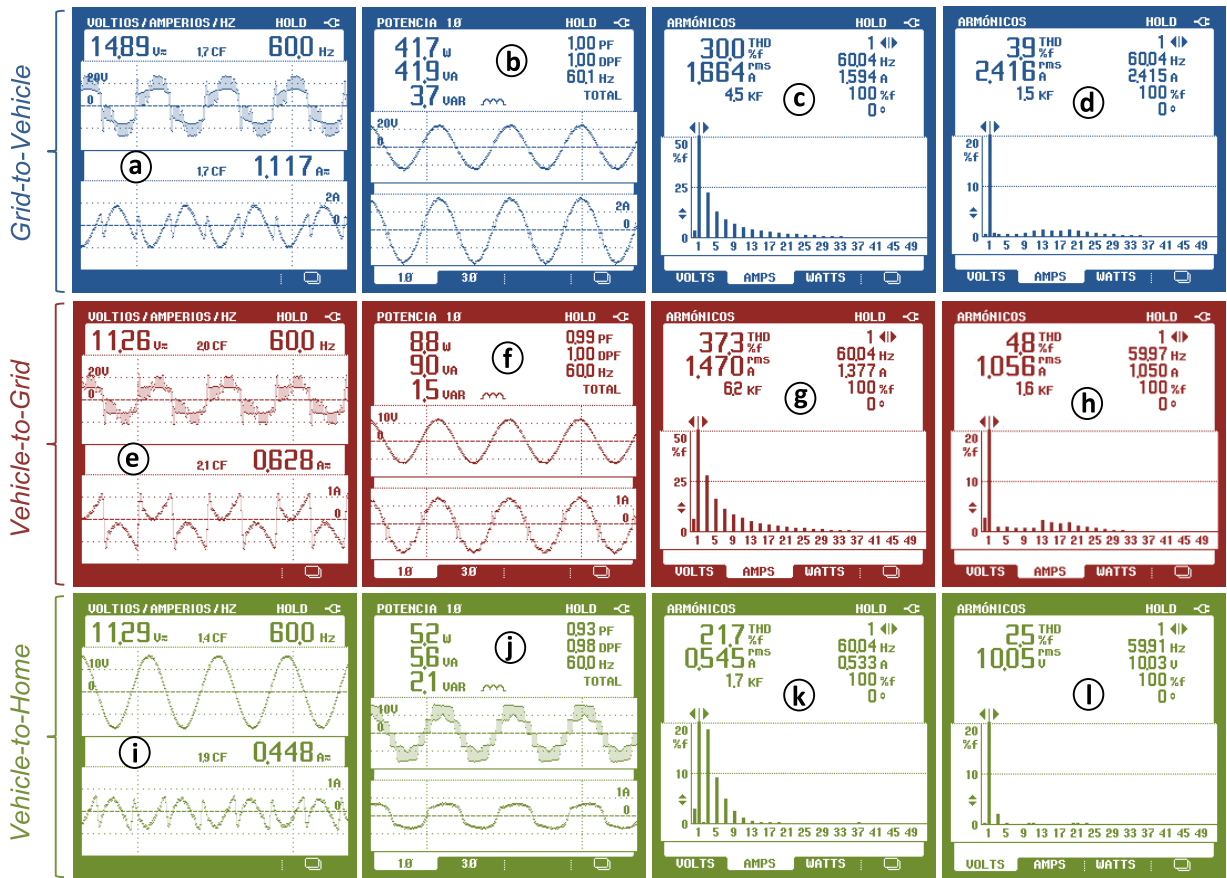


FIGURE 18. Experimental results: (Upper row) G2V: a) V_{5LC} and i_{5LC} , b) V_{grid} and i_{grid} , c) Spectrum of i_{load} , d) Spectrum of i_{grid} . (Middle row) V2G: e) V_{5LC} and i_{5LC} , f) V_{grid} and i_{grid} , g) Spectrum of i_{load} , h) Spectrum of i_{grid} . (Bottom row) V2H: i) V_{grid} and i_{5LC} , j) V_{5LC} and i_{5LC} , k) Spectrum of i_{5LC} , l) Spectrum of V_{5LC} .

of i_{load} and i_{grid} are shown in Figures 18c and 18d, respectively. It is noteworthy how due to the active filtering capabilities of the 5LC, the THD of the grid current is reduced from 30% to only 3.9% while the PF is unity.

Figure 18e shows the waveforms of V_{5LC} and i_{5LC} obtained during the V2G operation mode whereas Figure 18f shows the resulting V_{grid} and i_{grid} . Given that the battery is contributing to feed the load, thus the power provided by the grid is lower than in the G2V mode. Under this condition, the PF remains at 0.99. The spectra of i_{load} and i_{grid} are shown in Figures 18g and 18h, respectively. Observe that the distortion of the grid current is quite good compensated by decreasing its THD from 37.3% to 4.8%. Take into account that in order to send more power from the battery to the grid, the peak magnitude of the grid voltage has been reduced from around 22V to 12V.

Note that the grid voltage conditions are different in the V2G and G2V modes. It has been possible by adjusting the knob of the grid interfacing variable autotransformer shown in Figure 16i. It is important to remark that the magnitude of this voltage has been set only once before starting either the V2G or the G2V tests, and from there on, the knob remained fixed during their progress. Hence, the peak value of the grid

TABLE 3. Efficiency of the four NPC/ANPC 5L topologies under study.

FIVE - LEVEL TOPOLOGY	EFFICIENCY (%)		
	G2V	V2G	V2H
[17]	97.4	97.3	97.4
[18]	97.5	97.3	97.5
[19]	94.3	94.3	94.5
Proposed	94.9	94.6	94.6

voltage was properly kept constant during each of the tests for both operation modes.

Figure 18i shows the signals of V_{grid} and i_{5LC} obtained when the active filtering task carried out by the PR controllers is turned on while the battery current is regulated at zero. Note that these waveforms have been captured with the grid still connected at the PCC.

Figure 18j shows the voltage V_{5LC} and current i_{5LC} from the five-level converter right after the power outage occurs.

Figures 18k and 18l show the spectra of i_{5LC} and V_{5LC} , respectively. Given that under the V2H mode, the converter

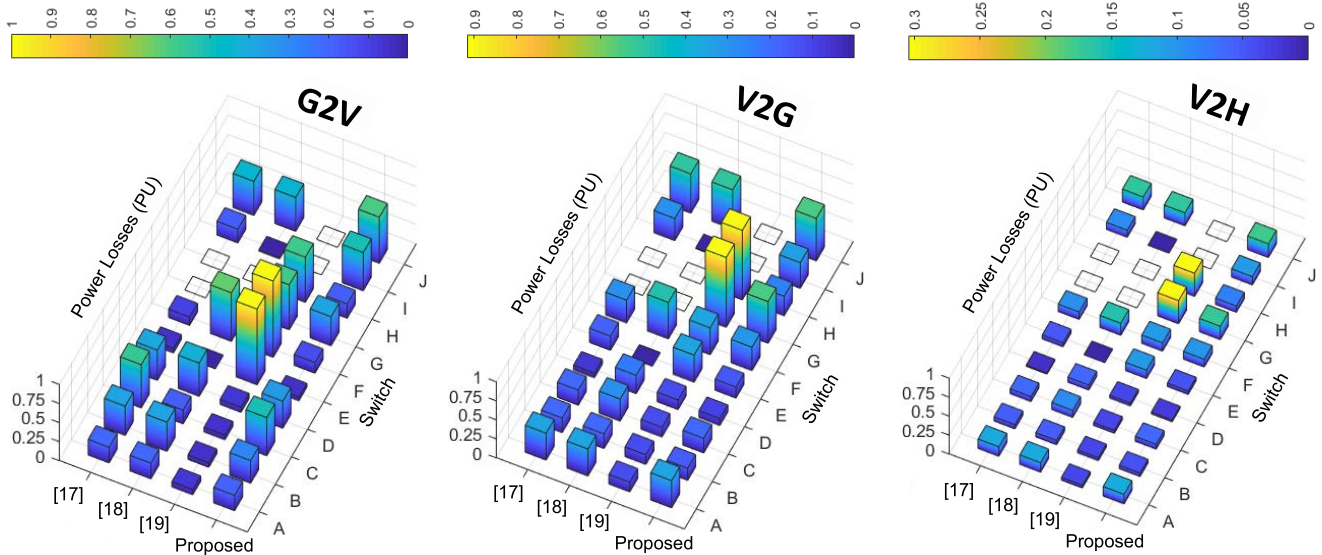


FIGURE 19. Power losses distribution of the four NPC/ANPC 5L converters in the three operation modes: (Left) G2V. (Middle) V2G. (Right) V2H.

current i_{5LC} and the load current i_{load} are the same, its spectrum is also implicitly shown in Figure 18k, thus demonstrating the high harmonic content of the load current waveform formerly presented in the second half of the time scale in Figure 17h as well as in Figure 17i. It is noteworthy that even though the 5LC is feeding this highly nonlinear home load, its output voltage has a THD of only 2.5%.

It can be observed that in the three operation modes, the output voltage V_{5LC} from the 5LC is a high-quality signal with symmetric levels due to the good performance of the balancing strategy for keeping the split-capacitors at the same voltage in spite of the disturbances and testing conditions.

Likewise, the transition from the V2G/G2V modes to the V2H mode is seamless for the load since the output from the 5LC is always ready for generating a voltage signal with the same magnitude as that of the grid and also accurately phase-synchronized. Note that the voltage feeding the load before and after the power outage is equal in magnitude but it is generated by the converter once the grid is off.

It is also important to remark that the detection of the power outage has been carried out automatically. For this, the grid voltage signal is first rectified, later low-pass filtered and finally, the obtained DC component is compared with a threshold value.

E. POWER LOSSES DISTRIBUTION

Figure 19 shows the normalized power losses distribution of the four NPC/ANPC 5L converters under study when operating in the G2V, V2G and V2H modes. Take into account that the letters from A to J included on the y-axis label of these 3D graphs allow identifying the corresponding switch within the topologies presented in Figure 2. Bear alike in mind that in the NPC topology [17], I and F are not switches but diodes. Additionally, the blank squares found among the 3D bars mean that such topology does not have that particular switch.

TABLE 4. Comparison of the four NPC/ANPC 5L topologies under study.

FIVE-LEVEL TOPOLOGY	NUMBER OF COMPONENTS				FEATURE	
	Split Capacitors	Power Switches	Clamping Diodes	Voltage Balancing	Switches Stress	Overall Efficiency
[17]	2	6	2	NO	LOW	HIGH
[18]	2	8	0	NO	LOW	HIGH
[19]	2	8	0	YES	HIGH	LOW
Proposed	2	10	0	YES	MIDDLE	MIDDLE

According to Table 3, the 5L topologies [17] and [18] present the highest efficiencies in the three modes of operation. Nevertheless, both of them are incapable of balancing the voltage of the split-capacitors since the resulting converters lack of redundant vectors for generating a voltage of half the DC bus, and consequently, the upper and lower capacitors cannot be charged and discharged as required. Unlike [17] and [18], the topology in [19] and the proposed one properly balance the split-capacitors voltage but at the expense of a little bit efficiency reduction.

It is noteworthy that even though the proposed topology consists of two more switches than [19], it presents a slightly higher efficiency as well as a better distribution of the power losses. This is because in the proposed 5L converter, the voltage balancing algorithm changes among the charging and discharging switching states only if it is necessary according to the sign of the capacitors voltage difference and the sign of the 5LC output current. On the contrary, in [19], the capacitors are kept balanced by continuously and indistinctly alternating the charging/discharging switching states at a high frequency rate, i.e., twice per period of the carrier signal. Therefore, the highest stress and losses occur in switches E and F under the G2V mode as well as in switches G and H under the V2G and V2H operation modes. Note also how in [19], the lowest power losses occur in the four switches A-D since they commute at a low frequency rate, i.e., twice per period of the modulating signal.

A comparison of the four topologies considering the number of components, the voltage balancing capability, the switches stress and the overall efficiency is summarized in Table 4.

VI. CONCLUSION

The performance evaluation of the proposed single-phase bidirectional ANPC 5LC for active filtering in G2V, V2G and V2H applications has been presented in this paper. The comparison carried out among the four NPC/ANPC 5L converters showed that the proposed one not only is capable of properly balancing the split-capacitors voltage but also does it optimally by continuously monitoring the sign of the capacitors voltage difference and the direction of the 5LC current. It is noteworthy that in contrast with the literature topologies, the proposed converter achieved a faster dynamics, a higher efficiency, a reduced switches stress and a flatter power losses distribution under the three modes of operation. The PR compensator included in the cascaded control strategy fairly attenuated the harmonics generated by the nonlinear load while maintaining a high-quality grid current with a THD below 5%, an almost zero reactive power and a PF very close to unity in the V2G/G2V modes. Furthermore, when the power outage suddenly occurred, the linear and nonlinear home loads correctly drew the EV battery’s energy and they were seamlessly and uninterruptedly supplied. Under this V2H mode, both loads were fed through the 5LC with a five-level voltage signal having a THD of only 2.5%. It is important to remark that the obtained simulation and experimental time domain results along with the indexes and spectra from the power quality analysis, validate the superior performance of the proposed ANPC 5LC functioning as an active filter for improving the power quality when cascaded with an EV charger.

APPENDIX

TABLE 5. Parameters of the controllers used in the 5LC and the DAHBC.

CONVERTER	PARAMETER	CONTROLLER	OPERATION MODE			SYMBOL	VALUE
			G2V	V2G	V2H		
5LC	DC bus voltage	PI ₁	X	X		k_{PSLC}	0.1
	Power quality	PR	X	X		k_{ISLC}	1
						k_{PR}	1
						k_{BR}	60
DAHBC	Battery current	PI ₂	X	X		k_{PC}	1
	Battery voltage	PI ₃	X			k_{IC}	10
						k_{PV}	0.1
						k_{IV}	0.5
DC bus voltage	PI ₄			X	k_{PDHBC}	0.05	
					k_{DAHBC}	1	

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Eléctricas, from 1991 to 2000. Her research interests include artificial intelligence, power electronics, electrical machines, and renewable energy.



of electrical engineering with the Instituto Tecnológico de la Laguna. His research interests include electrical machines, power electronics, and renewable energy.



the University of the Witwatersrand, South Africa, since May 2017. His research interests include electric machines, drives, power electronics, and transportation electrification.



the Director of Multidisciplinary Graduate Program on renewable energy and energy efficiency at ÉTS. Currently, he is the Director of Master Program in electrical engineering. The primary focus of his work is related to the advancement of new theory and control algorithms for power electronic converters for power quality improvement in distribution systems and integration of renewable energy sources. He has coauthored John Wiley book *Power Quality: Problems and Mitigation Techniques*. He is a fellow of many organizations, including the Canadian Academy of Engineering, the Institute of Engineering and Technology U.K., and the Engineering Institute of Canada. He registered as a Professional Engineer in Quebec. He was a recipient of the IEEE Canada P. Ziogas Electric Power Award 2018 and the IEEE Power and Energy Society Nari Hingorani Custom Power Award 2021.



LARA JORGE (Member, IEEE) received the B.E. degree in electronics and communications and the M.S. degree in electrical engineering from the Faculty of Mechanical, Electronic, and Electrical Engineering (FIMEE), University of Guanajuato (UG), Guanajuato, Mexico, in 2006 and 2008, respectively, and the Ph.D. degree in electrical engineering from Université du Québec–École de Technologie Supérieure (ÉTS), Montreal, Canada, in 2017.

From 2011 to 2014, he worked as a Research and Development Engineer at TM4 Inc., Boucherville, QC, Canada. In 2016, he participated in a NSERC Research Partnerships Program at Power Survey International Inc., Montreal. From 2017 to 2018, he worked at the Specialized Unit of Renewable Energies (UEER), Technological Institute of La Laguna (ITL) / National Technological of Mexico (TecNM), Torreón, Coahuila, Mexico. Currently, he is doing a Postdoctoral Research Internship funded by the National Council of Science and Technology (CONACYT) of Mexico at ITL/TecNM. His research interests include power electronics, wind and photovoltaic renewable energies, power quality, active filtering, electrical machine and drives, electric vehicles, and DSP-based real-time control.

Dr. Lara is a member of the National Researchers System (SNI) of Mexico. He is an active Reviewer of IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON POWER ELECTRONICS, and IEEE TRANSACTIONS ON ENERGY CONVERSION.