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0.5 V Differential Difference Transconductance Amplifier and Its Application in Voltage-Mode Universal Filter

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ABSTRACT This paper presents an innovative CMOS structure for Differential Difference Transconductance Amplifiers (DDTA). While the circuit operates under extremely low voltage supply 0.5 V, the circuit's performance is improved thanks to using the multiple-input MOS transistor (MI-MOST), the bulk-driven, self-cascode and partial positive feedback (PPF) techniques. As a result, the DDTA structure is less complex, with high gain of 93 dB, wide input voltage range nearly rail-to-rail, and wide transconductance tunability. As an example of application, a second-order voltage-mode universal filter using three DDTAs and two 6 pF integrated capacitors is presented. The filter is designed such that no matching conditions are required for the input and passive components, and the input signals need not be inverted. The natural frequency and the quality factor can be set orthogonally while the natural frequency can be electronically controlled. The circuit was designed and simulated in Cadence environment using 0.18 μm TSMC technology. The simulation results including intensive Monte-Carlo (MC) and process, temperature, voltage (PVT) analysis confirm the stability and the robustness of the design to process, mismatch variation and PVT corners.

INDEX TERMS Mixed-mode filter, universal filter, differential difference transconductance amplifier, analog signal processing.

I. INTRODUCTION

In modern portable electronics, wireless sensors, biomedical and energy harvesting applications the reduction of the voltage supply and the power consumption is a continuing demand that leads to prolong the operation period of the applications. Therefore, CMOS designers still have to innovate techniques that permit improving the performance of the analogue circuits operating under extremely low-voltage supply ($\leq$0.5 V). Circuits operating in subthreshold region along with non-conventional techniques such as bulk-driven (BD) [1]–[15], floating-gate (FG), quasi-floating-gate (QFG) [16]–[19] and multiple-input MOS transistor (MI-MOST) [13], [20]–[28] are promising solutions for low-voltage supply and low frequency applications. The MI-MOST can further lead to decrease the complexity of the CMOS structure by reducing the number of transistors and current branches. This results in optimized chip area and reduced power consumption of the applications. The symbol and the realization of the bulk-driven MI-MOST are shown in Fig. 1.

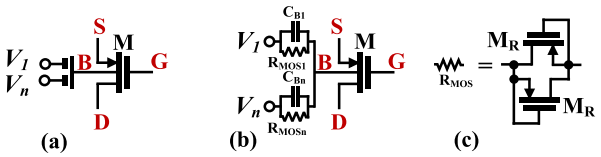

FIGURE 1. The BD MI-MOST: a) symbol, b) realization and c) realization of R_{MOS}.

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This BD MI-MOST can be realized in any standard CMOS technology; hence, no extra fabrication steps are needed. From a conventional MOS transistor, multiple-inputs ($V_1, \ldots, V_n$) are created by a set of parallel connection of input capacitor C_B and high-resistance R_{MOS} that are implemented by two transistors M_R operating in cut-off region.

In this paper, the BD MI-MOST has been used to design the Differential Difference Transconductance Amplifiers (DDTA). The DDTA comprises the advantage of the Differential Difference Amplifier (DDA) such as high input impedance and arithmetic operation capability, and of the Transconductance Amplifier (TA) such as electronic tunability. Unlike the previous standard structures of the DDTA [29]–[32], the proposed structure is compact, innovative and optimized to work under extremely low voltage supply 0.5 V with enhanced performance. While the input stage of a standard DDTA (i.e. DDA) uses two differential pairs, the proposed structure uses one differential pair based on bulk-driven multiple-input MOS transistor technique. This leads to reduced design complexity from one side and to increased range of the input voltage nearly rail-to-rail from other side. In addition, and to the best of the authors' knowledge, the input stage comprises, for the first time, two partial positive feedbacks (PPF) to achieve high performance like high gain around 93 dB with lower sensitivity to transistor mismatch. The second stage of the proposed DDTA (i.e. TA) is based on the BD technique and self-cascode transistors that increase the output resistance and the gain of the TA.

This paper is organized as follows: in Sec. 2 the innovative CMOS structure of the DDTA is presented, Sec. 3 presents the filter application of the voltage-mode universal filter, Sec. 4 presents the simulation results and finally Sec. 5 concludes the paper.

II. CMOS STRUCTURE OF DDTA

The symbol of the DDTA is shown in Fig. 2. Internally it consists of the DDA, followed by the TA. In ideal case, the DDTA is described by the following set of equations:

$$\left.\begin{aligned} V_w &= V_{y1} - V_{y2} + V_{y3} \\ I_o &= g_m V_w \end{aligned}\right\} \tag{1}$$

The CMOS structure of the proposed DDTA is shown in Fig. 3. As mentioned above, the circuit consists of two main blocks. The first one is the differential-difference amplifier stage DDA operating in a unity-gain configuration, thus realizing a low-impedance output W.

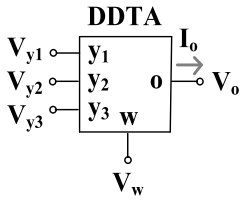

FIGURE 2. Symbol of DDTA.

The second block is the transconductance stage TA, based on a classical BD differential pair with DC voltage gain enhanced thanks to the use of self-cascode composite transistors.

The DDA block consists of two stages, the input differential stage operating in a current mirror configuration M_1-M_{15} and the output stage M_{13}-M_{16} with the frequency compensation capacitance C_C. Similar structure has previously been applied in [10], [11]. The input differential stage consists of the non-tailed differential pair M_1-M_2, biased with the current sinks M_3-M_4, and the partial positive feedback (PPF) circuit, $M_{5,6}$, $M_{9,10}$, applied as a load of the input pair. The cross-coupled transistors M_9-M_{10} generate the negative resistances $-g_{m9}$ and $-g_{m10}$, which partially compensate the positive conductances of the diode-connected transistors M_5 and M_6 (g_{m5} and g_{m6}). This way the load resistance is increasing and the overall voltage gain is improved [10]. However, two modifications have been made as compared to the original design. First, the input BD transistors M_1-M_2 have been replaced by BD MI-MOS transistors that allowed simplification of the overall structure, namely removing one differential stage, since summation of signals is realized by the passive capacitances C_{Bi}. The second modification is the addition of the second PPF circuit M_7-M_8, applied directly to the input non-tailed differential pair, in the same configuration as previously described in [33], [34]. To the best of the authors' knowledge, the application of two PPF circuits instead of one is the original solution proposed in this DDA structure. As it is widely known, the sensitivity of the circuits with PPF to transistor mismatch increase with the amount of positive feedback that can even lead to instability. This effect limits the maximum amount of feedback and consequently the voltage gain enhancement factor. As will be shown below, application of two PPF circuits with a weaker feedback instead of one with stronger feedback allows achieving the same voltage (transconductance) gain enhancement, with lower sensitivity to transistor mismatch. This is the main advantage of the proposed approach.

The low-frequency voltage gain of the DDA, from one differential input, with the second input grounded for AC signals, in open-loop configuration, can be expressed as follows:

$$A_{vo} = \frac{\beta A_o}{(1 - m_1)(1 - m_2)} \tag{2}$$

where A_o is the DC open-loop voltage gain of the DDA, without PPF circuits, calculated directly from the bulk terminals of M_1, and given as:

$$A_o = 2g_{mb1}\left(r_{ds15} || r_{ds12}\right) g_{m16}\left(r_{ds16} || r_{ds13}\right) \tag{3}$$

The coefficient β is the AC gain of the input capacitive divider, composed of the capacitances C_{Bi} in MI-BD MOS transistors, assuming equal capacitances C_{Bi} and neglecting the impact of the input capacitance of a MOS transistor seen from its bulk terminal is equal to 1/2. The factors m_1 and m_2

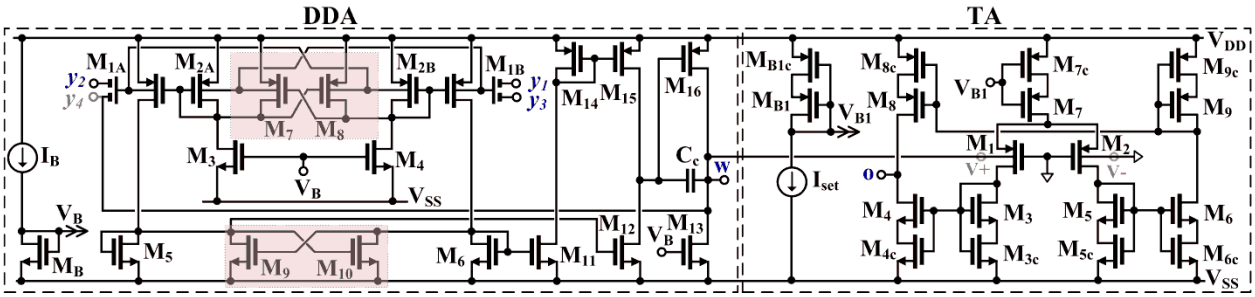

FIGURE 3. CMOS structure of the proposed DDTA.

can be expressed as:

$$m_1 = \frac{g_{m9,10}}{g_{m5,6} + g_{ds2} + g_{ds3,4} + g_{ds7,8}} \cong \frac{g_{m9,10}}{g_{m5,6}} \quad (4)$$

$$m_2 = \frac{g_{m7,8}}{g_{m2} + g_{ds1} + g_{ds5,6} + g_{ds9,10}} \cong \frac{g_{m7,8}}{g_{m2}} \quad (5)$$

Thus, the factors m_1 and m_2 can be considered as the ratios of the absolute values of the negative to positive conductances in "bottom" PPF_1 and "upper" PPF_2. The factors can range from zero (lack of positive feedback) to unity (100% positive feedback). Note that, the overall voltage gain A_{vo} increases from βA_o to infinity, as m_1, m_2 increase from 0 to 1. The maximum values of the factors are however limited by two effects. First, the circuit sensitivity to transistor mismatch increase, as m_1, m_2 tend to unity, which limits the maximum reliable voltage gain, and increases also the variations of the transconductance of the first stage of the DDA. This entails increased variations of the phase margin of the overall structure, thus affecting the circuit instability, even if the circuit is not yet overcompensated, i.e. when the absolute values of the negative conductances in PPF are not larger than the positive ones.

The sensitivities of the voltage gain A_{vo} to the values of the coefficients m_1 and m_2 are given as:

$$S_{m_1}^{A_{vo}} = \frac{m_1}{1 - m_1} \quad (6)$$

$$S_{m_2}^{A_{vo}} = \frac{m_2}{1 - m_2} \quad (7)$$

thus, both sensitivities are nonlinear functions of m_1 (m_2), and their values tend to infinity, as m_1 (m_2) tend to unity. Note that, considering linear approximation, the relative variation of the voltage gain A_{vo}, caused by the relative variations of m_1 and m_2 in a two PPF circuit can be expressed as:

$$\frac{dA_{vo}}{A_o} = \frac{m_1}{1 - m_1} \cdot \frac{dm_1}{m_1} + \frac{m_2}{1 - m_2} \cdot \frac{dm_2}{m_2} \quad (8)$$

It can be concluded from (6)-(8) and (2) that using two PPF with lower values of m can provide the same voltage gain with lower overall sensitivity than using only one PPF circuit with larger value of m. For instance, assuming $m_1 = m_2 = 0.5$ (as in the proposed design), according to (2) the voltage gain is improved by 12 dB, compared to the version without PPF, with $S_{m_1}^{A_{vo}} = S_{m_2}^{A_{vo}} = 1$ Using (8), and assuming 1% variations of m_1 and m_2, results in 2% variation of A_{vo}. In order to obtain the same enhancement of the voltage gain with one PPF circuit, say PPF1, we should chose $m_1 = 0.75$, which, according to (6), gives the sensitivity equal to 3, namely 1% variation of m_1 results in 3% variation of A_{vo}. This improvement would even be more apparent when assuming larger values of m_1, m_2.

The second important factor, limiting the maximum values of m_1, m_2, is the location of the parasitic poles, associated with PPF_1 and PPF_2. Neglecting the second-order effects, the poles can be respectively expressed as:

$$p_{PPF1} = -\frac{g_{m5,6}\,(1 - m_1)}{C_{O1}} \quad (9)$$

$$p_{PPF2} = -\frac{g_{m2}\,(1 - m_2)}{C_{O2}} \quad (10)$$

where C_{O1} and C_{O2} are the total capacitances associated with the drain/gate nodes of M_2 and $M_{5,6}$, respectively. As it can be noticed, the frequencies of the poles decrease with increasing m_1 and m_2. In order to mitigate their impact on the phase margin of the DDA, the poles should be located well above the gain-bandwidth product (GBW) of the DDA. This limits the maximum values of m_1 and m_2 and consequently the achievable voltage gain. The phase shift associated with these poles for the cutoff frequency ω_{GBW} can be expressed as:

$$\Delta\varphi = arctg\left(\frac{\omega_{GBW}}{\omega_{pPPF1}}\right) + arctg\left(\frac{\omega_{GBW}}{\omega_{pPPF2}}\right) \quad (11)$$

where:

$$\omega_{GBW} = \frac{2\beta g_{mb1}}{(1 - m_1)\,(1 - m_2)\,C_C} \quad (12)$$

Note that for ω_{pPPF1} and $\omega_{pPPF2} \gg \omega_{GBW}$ we can apply the linear approximation arctg(x) = x. Consequently, the phase shift can be approximated as:

$$\Delta\varphi \cong \left(\frac{\omega_{GBW}}{\omega_{pPPF1}}\right) + \left(\frac{\omega_{GBW}}{\omega_{pPPF2}}\right) \quad (13)$$

Assuming for simplicity that $\omega_{pPPF1} = \omega_{pPPF2} = \omega_{pPPF1,2}$, and $m_1 = m_2$, the corresponding pole for a circuit with one

PPF, providing the same A_{vo}, can be calculated as:

$$\omega_{pPPF} = \frac{1 - m_{1,2}\left(2 - m_{1,2}\right)}{\left(1 - m_{1,2}\right)}\omega_{pPPF1,2} \tag{14}$$

Using (13) and (14) we can conclude that the phase shift for a system with one PPF is lower for $m_{1,2} < 0.5$ and larger for $m_{1,2} > 0.5$, compared to its counterpart with two PPFs. In the proposed design we chose $m_{1,2} = 0.5$, that provides the same phase shift in both cases.

Finally, since DDA operates with a 100% negative feedback, the voltage at the W terminal for low frequencies can be expressed as:

$$V_w = \frac{\beta A_{vo}}{1 + \beta A_{vo}}\left(V_1 - V_2 + V_3\right) \tag{15}$$

while the output resistance at the W terminal is:

$$r_{outW} = \frac{r_{ds16} || r_{ds13}}{1 + \beta A_{vo}} \tag{16}$$

Thus, since PPF allows improving the voltage gain A_{vo}, then both the accuracy of the basic function given by (1) as well as the output resistance at W terminal are improved. At the same time, applying two PPFs instead of one allows decreasing the circuit sensitivity to mismatch, compared to the circuit with one PPF and the same A_{vo}.

The second block of the proposed DDTA circuit, namely the transconductance amplifier TA, operates in the so-called current mirror configuration, with the input BD differential pair. The self-cascode composite transistors M_3-M_9 are used to improve its DC voltage gain. The biasing current I_{set} can be adjusted independently, that allows regulating the circuit transconductance g_m. Assuming unity-gain current mirrors, its DC transfer characteristic in a weak inversion in given by:

$$I_O = I_{set} \tanh\left(\frac{\eta V_w}{2n_p U_T}\right) \tag{17}$$

where $\eta = g_{mb}/g_m$ is the bulk to gate transconductance ratio, n_p is the subthreshold slope factor and U_T is the thermal potential. The small-signal transconductance of the OTA is:

$$g_m = \eta \frac{I_{set}}{2n_p U_T} \tag{18}$$

while its DC voltage gain:

$$A_{vTA} \cong g_m \left(g_{m6} r_{ds6} r_{ds6c}\right) || \left(g_{m9} r_{ds9} r_{ds9c}\right) \tag{19}$$

Thus, as mentioned previously, the voltage gain is enhanced due to the application of self-cascode connections, improving the output resistance of the TA stage.

III. APPLICATION OF THE DDTA

The proposed universal filter using three DDTAs and two integrated capacitors is shown in Fig. 4. The input voltages V_{in1}, V_{in2}, V_{in3}, V_{in4} are applied to high impedance terminals while the output voltages V_{o1}, V_{o2}, V_{o4} possess low impedance terminals.

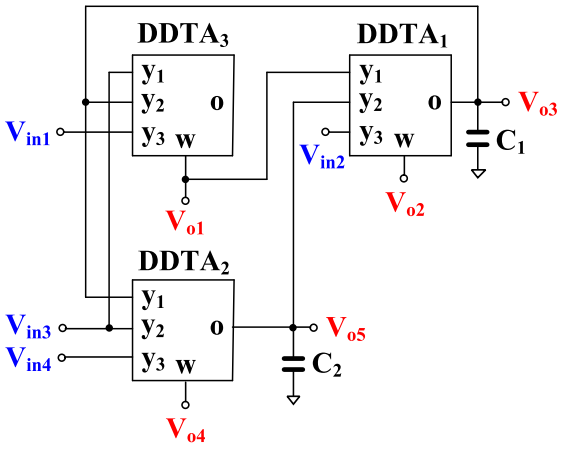

FIGURE 4. Proposed universal filter using DDTAs.

Using (1) and nodal analysis, the output voltages of Fig. 4 can be expressed by:

$$V_{o1} = \frac{\left(s^2 C_1 C_2 + g_{m1} g_{m2}\right) V_{in1} - sC_2 g_{m1} V_{in2} + s^2 C_1 C_2 V_{in3} + g_{m1} g_{m2} V_{in4}}{s^2 C_1 C_2 + sC_2 g_{m1} + g_{m1} g_{m2}} \tag{20}$$

$$V_{o2} = \frac{s^2 C_1 C_2 V_{in1} + s^2 C_1 C_2 V_{in2} + \left(s^2 C_1 C_2 + sC_2 g_{m1}\right) V_{in3} - sC_2 g_{m1} V_{in4}}{s^2 C_1 C_2 + sC_2 g_{m1} + g_{m1} g_{m2}} \tag{21}$$

$$V_{o3} = \frac{sC_2 g_{m1} V_{in1} + sC_2 g_{m1} V_{in2} + \left(sC_2 g_{m1} + g_{m1} g_{m2}\right) V_{in3} - g_{m1} g_{m2} V_{in4}}{s^2 C_1 C_2 + sC_2 g_{m1} + g_{m1} g_{m2}} \tag{22}$$

$$V_{o4} = \frac{sC_2 g_{m1} V_{in1} + sC_2 g_{m1} V_{in2} - s^2 C_1 C_2 V_{in3} + \left(s^2 C_1 C_2 + sC_2 g_{m1}\right) V_{in4}}{s^2 C_1 C_2 + sC_2 g_{m1} + g_{m1} g_{m2}} \tag{23}$$

$$V_{o5} = \frac{g_{m1} g_{m2} V_{in1} + g_{m1} g_{m2} V_{in2} - sC_1 g_{m2} V_{in3} + \left(sC_1 g_{m2} + g_{m1} g_{m2}\right) V_{in4}}{s^2 C_1 C_2 + sC_2 g_{m1} + g_{m1} g_{m2}} \tag{24}$$

From (20)-(24), it is evident that various filtering functions such as low-pass filter (LPF), band-pass filter (BPF), high-pass filter (HPF), band-stop filter (BSF), and all-pass filter (APF) can be obtained by appropriately applying the input signals as well as appropriately choosing the output signals. The unused input terminal should be connected to ground. The input and output conditions and various filtering functions realized can be shown in Table 1. It should be noted from Table 1 that no inversion of input signal is necessary to obtain all filtering transfer functions, and additional buffers are therefore not required.

The natural frequency (ω_o) and the quality factor (Q) can be expressed by:

$$\omega_o = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \tag{25}$$

$$Q = \sqrt{\frac{g_{m2} C_1}{g_{m1} C_2}} \tag{26}$$

TABLE 1. Input and output conditions and various filtering functions realized.

Filtering Function		Input	Output
LPF	Non-inverting	V_{in4}	V_{o1}
	Inverting	V_{in4}	V_{o3}
	Non-inverting	V_{in1}	V_{o5}
	Non-inverting	V_{in2}	V_{o5}
	Non-inverting	$V_{in3} = V_{in4}$	V_{o5}
BPF	Inverting	V_{in2}	V_{o1}
	Inverting	V_{in4}	V_{o2}
	Non-inverting	V_{in1}	V_{o3}
	Non-inverting	V_{in2}	V_{o3}
	Non-inverting	$V_{in3} = V_{in4}$	V_{o3}
	Non-inverting	V_{in1}	V_{o4}
	Non-inverting	V_{in2}	V_{o4}
	Non-inverting	$V_{in3} = V_{in4}$	V_{o4}
	Inverting	V_{in3}	V_{o5}
HPF	Non-inverting	V_{in3}	V_{o1}
	Non-inverting	V_{in1}	V_{o2}
	Non-inverting	V_{in2}	V_{o2}
	Non-inverting	$V_{in3} = V_{in4}$	V_{o2}
	Inverting	V_{in3}	V_{o4}
BSF	Non-inverting	V_{in1}	V_{o1}
	Non-inverting	$V_{in3} = V_{in4}$	V_{o1}
APF	Non-inverting	$V_{in1} = V_{in2}$	V_{o1}
	Non-inverting	$V_{in2} = V_{in3} = V_{in4}$	V_{o1}

Eqs. (25) and (26) show that the natural frequency can be controlled by g_m ($g_m = g_{m1} = g_{m2}$) and the quality factor can be given by C_1/C_2 while keeping $g_{m1} = g_{m2}$. Thanks to electronic tuning ability, the natural frequency can be retuned if the ratio C_1/C_2 deviates the natural frequency.

IV. NON-IDEALITIES ANALYSIS

Considering non-idealities of the DDTA, its characteristics can be rewritten as:

$$\left.\begin{aligned} V_w &= \beta_{j1} V_{y1} - \beta_{j2} V_{y2} + \beta_{j3} V_{y3} \\ I_o &= g_{mnj} V_w \end{aligned}\right\} \tag{27}$$

where $\beta_{j1} = 1 - \varepsilon_{j1v}$ and $\varepsilon_{j1v}(|\varepsilon_{j1v}| \ll 1)$ denotes the voltage tracking error from V_{y1} to V_w of j-th DDTA, $\beta_{j2} = 1 - \varepsilon_{j2v}$ and $\varepsilon_{j2v}(|\varepsilon_{j2v}| \ll 1)$ denotes the voltage tracking error from V_{y2} to V_w of j-th DDTA, and $\beta_{j3} = 1 - \varepsilon_{j3v}$ and $\varepsilon_{j3v}(|\varepsilon_{j3v}| \ll 1)$ denotes the voltage tracking error from V_{y2} to V_w of j-th DDTA. The non-ideal transconductance gain g_{mnj} is given by:

$$g_{mnj}(s) = \left(\frac{\omega_{gmj}}{s + \omega_{gmj}}\right) g_{mj} \tag{28}$$

where ω_{gmj} denotes the first-order pole frequency that includes parasitic elements such as C_{oj} and R_{oj} at o-terminal of j-th DDTA, and g_{mj} denotes the open-loop transconductance gain of j-th DDTA.

In the frequency range of interest of this paper, g_{mnj} can be approximated as:

$$g_{mnj}(s) \cong g_{mj}\left(1 - \mu_j s\right) \tag{29}$$

where $\mu_j = 1/\omega_{gmj}$.

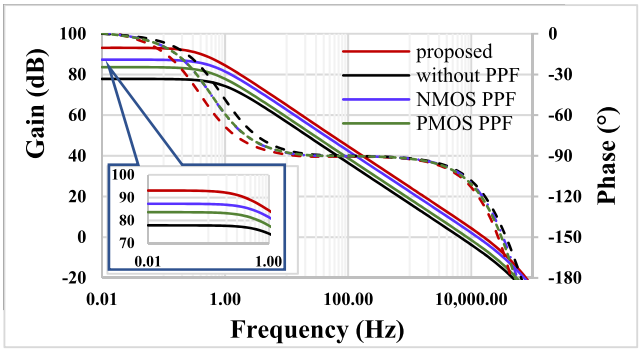

FIGURE 5. The gain and phase characteristics of the proposed DDA.

Using (27), the denominator of the transfer function can be expressed as:

$$D(s) = s^2 C_1 C_2 + s C_2 g_{mn1} \beta_{11} \beta_{32} + g_{mn1} g_{mn2} \beta_{12} \beta_{21} \tag{30}$$

Using (29), (30) becomes:

$$\begin{aligned} D(s) &= s^2 C_1 C_2 \left(1 - \frac{C_2 g_{m1} \mu_1 \beta_{11} \beta_{32} - g_{m1} g_{m2} \beta_{12} \beta_{21} \mu_1 \mu_2}{C_1 C_2}\right) \\ &\quad + s C_2 g_{m1} \beta_{11} \beta_{32} \\ &\quad \times \left(1 - \frac{g_{m1} g_{m2} \beta_{12} \beta_{21} \mu_1 + g_{m1} g_{m2} \beta_{12} \beta_{21} \mu_2}{C_2 g_{m1} \beta_{11} \beta_{32}}\right) \\ &\quad + g_{m1} g_{m2} \beta_{12} \beta_{21} \end{aligned} \tag{31}$$

From (31), the non-idealities of the DDTAs affect the circuit characteristics, which depart from ideal values. The parasitic effects from the DDTA can be made negligible by satisfying the following conditions:

$$\frac{C_2 g_{m1} \mu_1 \beta_{11} \beta_{32} - g_{m1} g_{m2} \beta_{12} \beta_{21} \mu_1 \mu_2}{C_1 C_2} \ll 1 \tag{32}$$

$$\frac{g_{m1} g_{m2} \beta_{12} \beta_{21} \mu_1 + g_{m1} g_{m2} \beta_{12} \beta_{21} \mu_2}{C_2 g_{m1} \beta_{11} \beta_{32}} \ll 1 \tag{33}$$

Therefore, the non-ideal natural frequency (ω_{on}) and the non-ideal quality factor (Q_n) can be obtained respectively by:

$$\omega_{on} = \sqrt{\frac{g_{m1} g_{m2} \beta_{12} \beta_{21}}{C_1 C_2}} \tag{34}$$

$$Q_n = \frac{1}{\beta_{11} \beta_{32}} \sqrt{\frac{g_{m2} C_1 \beta_{12} \beta_{21}}{g_{m1} C_2}} \tag{35}$$

The sensitivity of ω_{on} and Q_n with respect to circuit components and non-ideal parameters are given as follows:

$$S_{g_{m1}}^{\omega_{on}} = S_{g_{m2}}^{\omega_{on}} = S_{\beta_{12}}^{\omega_{on}} = S_{\beta_{21}}^{\omega_{on}} = -S_{C_1}^{\omega_{on}} = -S_{C_2}^{\omega_{on}} = \frac{1}{2} \tag{36}$$

$$S_{\beta_{11}}^{Q_n} = S_{\beta_{32}}^{Q_n} = -1 \tag{37}$$

$$S_{g_{m2}}^{Q_n} = S_{C_1}^{Q_n} = S_{\beta_{12}}^{Q_n} = S_{\beta_{21}}^{Q_n} = -S_{g_{m1}}^{Q_n} = -S_{C_2}^{Q_n} = -\frac{1}{2} \tag{38}$$

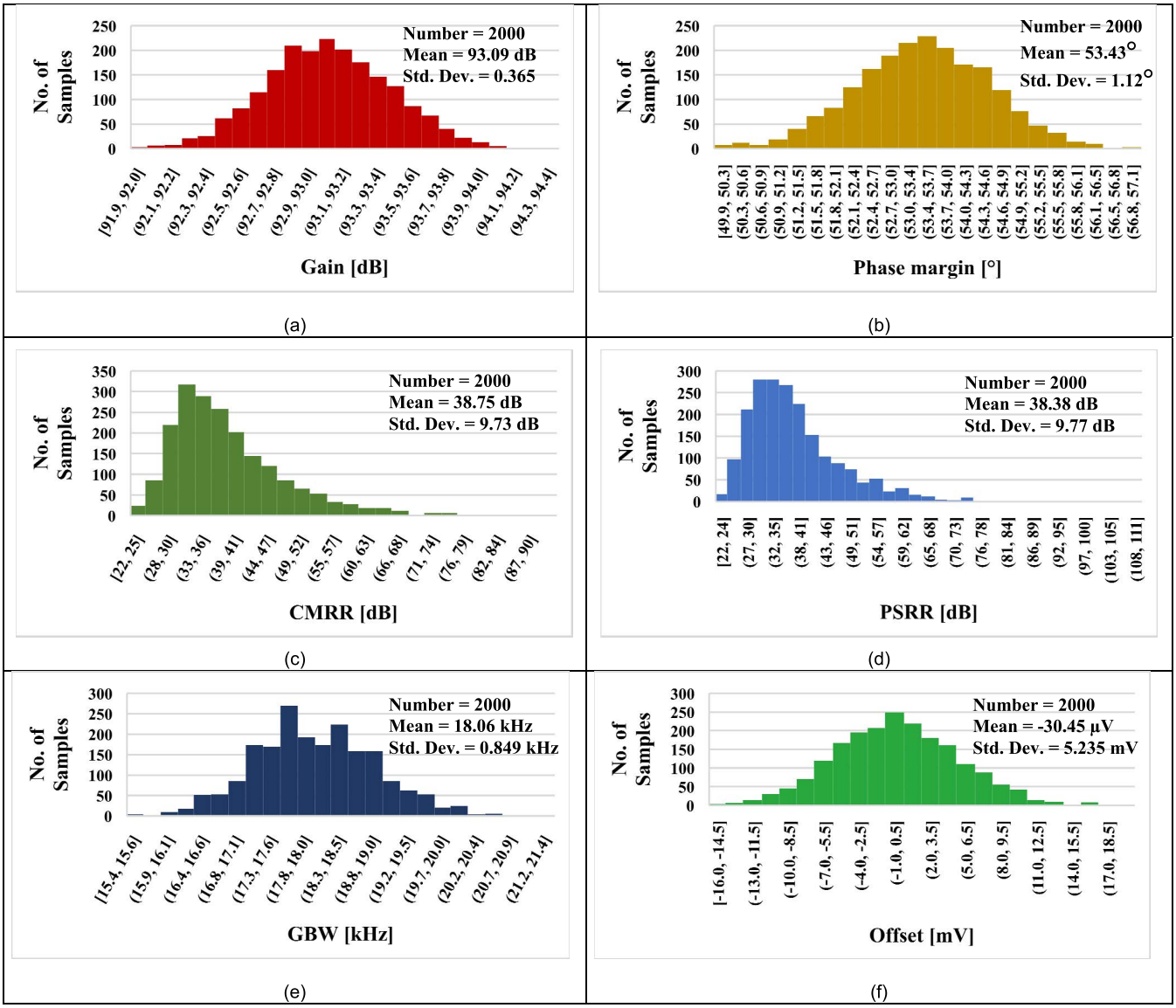

FIGURE 6. Histogram of gain (a), phase margin (b), CMRR (c), PSRR (d), GBW (e) and offset (f) of the proposed DDA.

It can be concluded from (36)-(38) that all the sensitivities are within unity in magnitude. Thus, the proposed filter enjoys good active and passive sensitivities.

The filter behavior may be affected at low frequencies by parasitic resistances R_1 and R_2 acting in parallel to integrating capacitors C_1 and C_2. The error analysis reveals finite parasitic DC attenuation Att_0 in high-pass and particularly in band-pass outputs. For the band-pass filter in V_{in2} and V_{o1} configuration, this attenuation is:

$$Att_0 = 1 + g_{m2}R_2 + \frac{1}{g_{m1}R_1} \tag{39}$$

It is obvious that the $g_m \times R$ product must be kept as high as possible to maintain high attenuation, and that this issue is critical for the parasitic resistance R_2 near $DDTA_2$. Note that for the attenuation of at least 40 dB, the $g_m \times R$ should be approximately 99. For low transconductances, typically below 100nS, this condition imposes challenging demands on high resistances acting at TA output.

V. SIMULATION RESULTS

The proposed DDTA circuit and the filter application were designed and simulated in Cadence environment using 0.18 μm CMOS technology from TSMC. The voltage supply was 0.5V ($\pm$0.25V). The bias current I_B was set to 40 nA and the I_{set} is adjustable. For $I_{set} = 1$ nA, the total power consumption of the DDTA is 205.5 nW (DDA = 203 nW and TA = 2.5 nW). The transistor's aspect ratio of the DDTA are shown in Table 2.

The high performance linear metal-insulator-metal (MIM) capacitor that is available in TSMC technology has been used in the DDTA design.

TABLE 2. Transistor aspect ratio of the DDTA.

DDA	W/L (μm/μm)	TA	W/L (μm/μm)
M_{1A}, M_{2A}, M_{1B}, M_{2B} M_{14}, M_{15}	16/3	M_1, M_2	2×15/1
M_3-M_8, M_{11}-M_{12}, M_B	8/3	M_3-M_6	2×10/1
M_9, M_{10}	4/3	M_{3c}-M_{6c}	10/1
M_{16}	6×16/3	M_8, M_9, M_{B1}	2×15/1
M_{13}	6×8/3	M_{8c}, M_{9c}, M_{B1c}	15/1
M_R	4/5	M_7	2×30/1
MIM capacitor: C_B= 0.5 pF, C_c= 6 pF		M_{7c}	30/1

TABLE 3. The gain, phase margin and GBW for the DDA with and without PPF.

	Proposed DDA (with two PPFs)	DDA without PPF	DDA with NMOS PPF	DDA with PMOS PPF
Gain (dB)	93	77.81	87.29	83.59
Phase margin (°)	53.47	77.78	64.84	71.96
GBW (kHz)	18.02	6.92	13.78	9.06

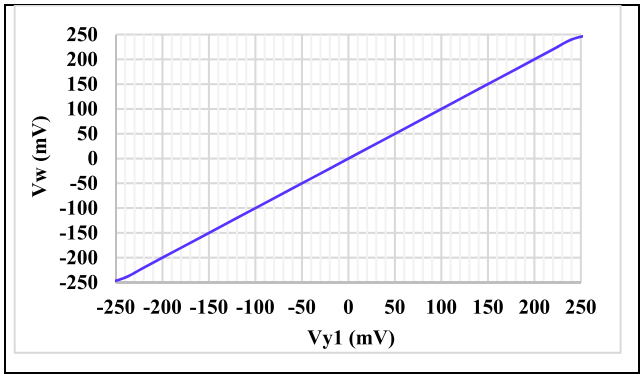

FIGURE 7. The output voltage V_W versus V_{y1}.

The DDA was simulated in the open-loop configuration, with load capacitance 20 pF, to confirm the impact of the used techniques, mainly the two PPFs, on the performance of the proposed structure. As it is evident from Fig. 5 that shows the frequency and the phase characteristics of the DDA, the proposed DDA offers the highest gain around 93 dB, while the lowest gain is for the DDA structure without PPF, where the gain is around 77.81 dB. The detailed results of the gain, phase margin and gain bandwidth product (GBW) of the proposed DDA, DDA without PPF, with NMOS PPF and with PMOS PPF is shown in Table 3, that confirm our expectation.

To confirm the robustness of the design with process and mismatch variation, the Monte-Carlo (MC) analysis with 2000 runs was performed. The histogram of the DDA gain, phase margin, common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), voltage offset and GBW is shown in Fig. 6. The DDA enjoys small deviations for most of these parameters. For instance, the mean value of the phase margin is 53.43° and standard deviation is only 1.12°.

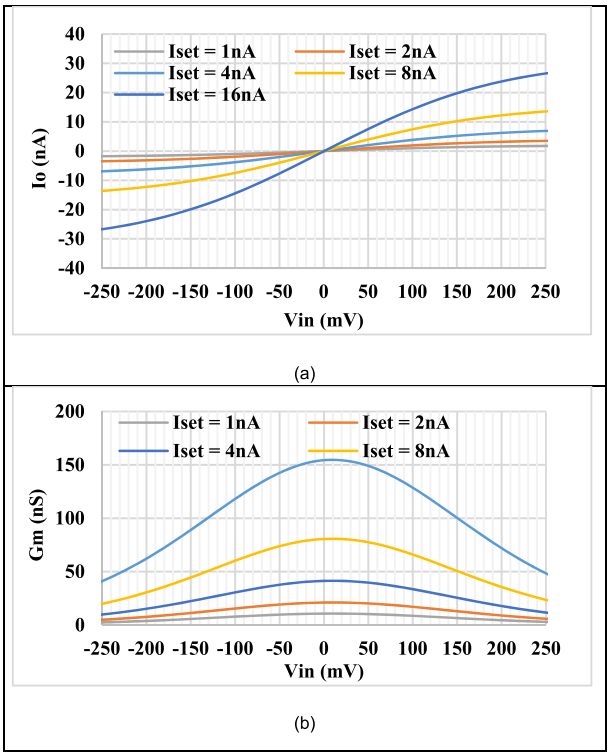

FIGURE 8. The DC (a) and transconductance (b) characteristics of the TA versus input voltage.

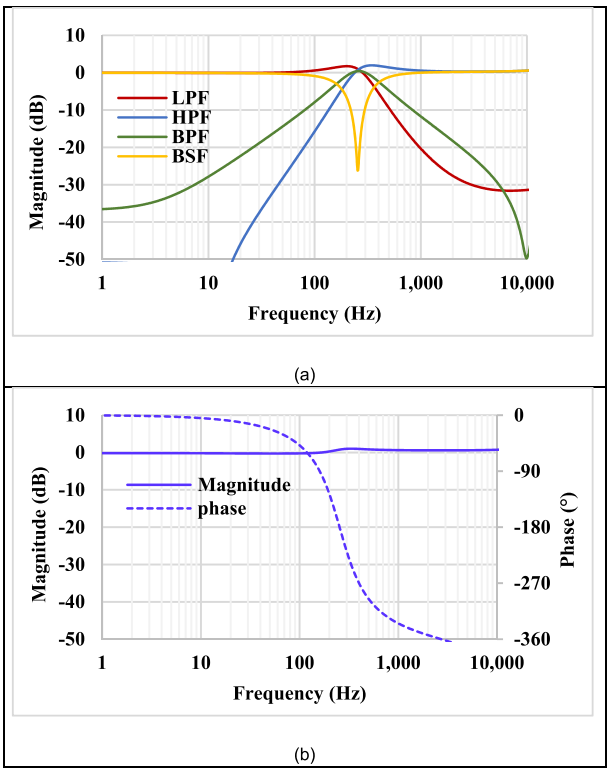

FIGURE 9. The magnitude and phase characteristics of the universal filter.

Larger variations were observed only for CMRR and PSRR, which were significantly lower than their nominal values (67.2 dB, 81.5 dB, respectively) shown in Table 4. The impact

TABLE 4. DDA PVT corners analysis.

Process corners

MOS corner	SS	SS	SF	SF	TT	FS	FS	FF	FF
MIM corner	SS	FF	SS	FF	TT	SS	FF	SS	FF
Gain (dB)	91.01	94.59	94.14	94.14	93.09	91.56	91.56	91.01	94.58
Phase margin (◦)	56.5	54.72	55.89	51.67	53.46	55.58	50.66	51.67	49.59
CMRR (dB)	66.51	66.51	69.2	69.21	67.19	66.73	66.73	70.07	70.07
PSRR (dB)	70.84	70.84	78.43	78.43	81.52	75.2	75.2	78.65	78.65
GBW (kHz)	13.7	18.04	17.14	23.13	18.05	14.2	19.15	18.48	24.34

Voltage corners

V_{DD} (mV)	450	500	550
Gain (dB)	90.35	93.09	93.49
Phase margin (◦)	54.18	53.46	52.9
CMRR (dB)	70.38	67.19	65.42
PSRR (dB)	60.6	81.52	69.05
GBW (kHz)	19.11	18.05	16.34

Temp. corners

Temp (°C)	-20	27	80
Gain (dB)	88.9	93.09	89.71
Phase margin (◦)	55.05	53.46	53.36
CMRR (dB)	65.99	67.19	75.42
PSRR (dB)	55.53	81.52	76.96
GBW (kHz)	15.26	18.05	10.9

TABLE 5. TA PVT corners analysis.

Process corners

MOS corner	SS	SF	TT	FS	FF
Gain (dB)	39.65	38.71	39	39.49	38.56
Phase error (◦)	0.097	0.198	0.152	0.107	0.209
GBW (Hz)	86.44	83.04	85.06	87.07	83.83
G_m (nS)	10.86	10.44	10.7	10.94	10.54
G_m BW (kHz)	14.3	14.4	14.3	14.21	14.33
CMRR (dB)	116.96	99.63	104	125.11	98.91
PSRR (dB)	40.01	39.37	39.6	39.89	39.23

Voltage corners

V_{DD} (mV)	450	500	550
Gain (dB)	38.59	39	39.23
Phase error (◦)	0.19	0.152	0.143
GBW (Hz)	84.18	85.06	85.28
G_m (nS)	10.59	10.7	10.72
G_m BW (kHz)	14.16	14.3	14.33
CMRR (dB)	128.14	104	102.92
PSRR (dB)	39.05	39.6	39.23

Temp. corners

Temp (°C)	-20	27	80
Gain (dB)	39.96	39	37.8
Phase error (◦)	0.101	0.152	0.262
GBW (Hz)	97	85.06	74.16
G_m (nS)	12.18	10.7	9.33
G_m BW (kHz)	16.54	14.3	12.77
CMRR (dB)	85.28	104	113
PSRR (dB)	40.05	39.6	38.8

TABLE 6. Comparisons of the proposed filter with some previous filters.

Features	Proposed	Ref [35]	Ref [36]	Ref [37]	Ref [38]	Ref [39]	Ref [23]	Ref [40]
Active and passive elements	3 DDTA, 2 C	1 FDCCII, 1 DDCC, 2 R, 2 C	1 DO-OTA, 3 OTA, 2 C	6 DDA, 6 C	16 MOS, 8 C	8 OTA, 8C	4 OTA, 1 R, 2 C	8 OTA, 2 C (Fig.3)
Technology (nm)	180	350	commercial IC	180	180	180	180	180
Threshold voltage: V_{TH} (V)	0.5	0.55	-	0.5	0.5	0.5	0.5	0.5
Power supply voltages (V)	0.5	±1.65	±15	1.8	1.8	1	0.5	0.6
Resistorless topology	Yes	No	Yes	Yes	Yes	Yes	No	Yes
Order (N)	2	2	2	6	4	4	2	2
Number of filtering functions	23	10	9	1 (LP)	1 (LP)	1 (LP)	5	20
Offering five standard biquad filter functions	Yes	Yes	Yes	No	No	No	Yes	Yes
Electronic control of ω_o	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes
Bandwidth (BW, Hz)	254	1×10^6	144.7×10^3	65×10^6	33×10^6	100	10	5×10^3
Power consumption (µW)	0.616	-	1.23×10^6	8070	1380	0.208	0.0533	5.77
DR (dB)	49.7	-	-	-	70.96	49.26	63	53.2
FOM=P/(N*BW*DR) (pJ)	24.39	-	-	-	0.147	10.4	42.3	10.84
LV operation capability=(V_{TH}/V_{DD})*100 (%)	100	16.67	-	27.78	27.78	50	100	83.33
Obtained results	Simulation	Simulation	Measured	Measured	Measured	Simulation	Simulation	Simulation

of mismatch could be mitigated employing larger transistor channel sizes. Fig. 7 shows the output voltage V_W versus the input voltage V_{y1} of the DDA connected in unity gain configuration. It can be observed that the circuit enjoys nearly rail-to-rail operation under 0.5V supply voltage. The TA was simulated for different set current I_{set} = 1, 2, 4, 8, 16 nA.

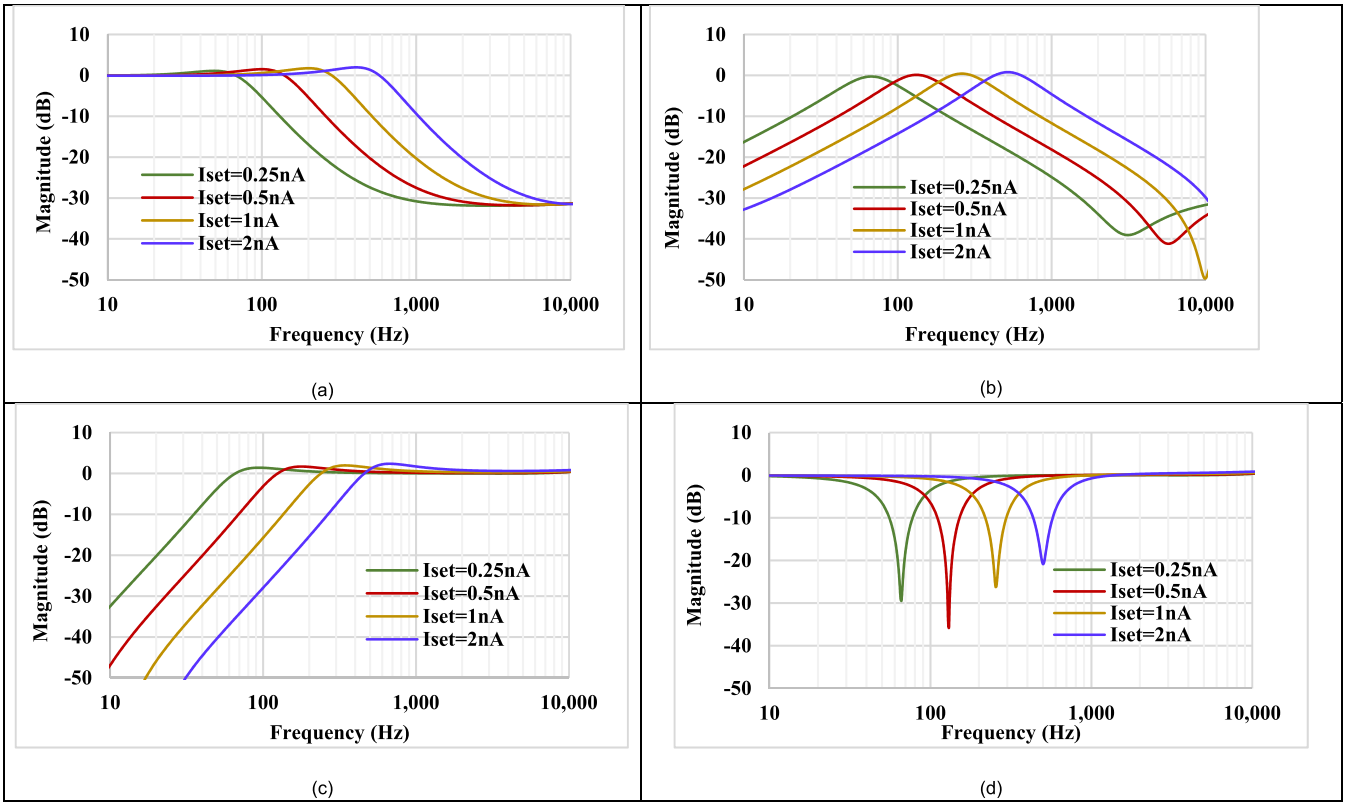

FIGURE 10. Magnitude characteristics of the LPF (a), BPF (b), HPF (c) and BSF (d) with different bias.

The DC characteristic of the output current I_o versus differential input voltage V_{in} ($V_{in} = V_+ - V_-$) is shown in Fig. 8(a) while the transconductance G_m is shown in Fig. 8 (b). The transconductance has 10% variation from the nominal value in the range of ± 75 mV.

The PVT corners analysis for the DDA and TA are depicted in Tables 4 and 5. The MOS transistor corners were slow-slow (SS), slow-fast (SF), fast-slow (FS) and fast-fast (FF), the voltage corners were $V_{DD} \pm 10\%$ and the temperature corners were $-20°C$ and $80°C$. Since the MIM capacitors are used in the design, their corners (SS) and (FF) have been also performed. As it is shown from these tables, the performance of the DDTA is still acceptable with all PVT corners. For on-chip integration, the filter with small capacitors is preferred. Therefore, for the filter application in Fig. 4, the value of capacitors for integration was selected low $C_1 = C_2 = 6$ pF. For $I_{set1,2,3} = 1$ nA, the transfer characteristics of the LPF, HPF, BPF and BSF are shown in Fig. 9 (a). The simulated natural frequency (f_o) is 254 Hz. Fig. 9 (b) shows the magnitude and phase characteristics of the APF. It can be confirmed that the proposed filter can provide five standard filtering responses within a single topology.

Fig. 10 shows the magnitude characteristics of the LPF, BPF, HPF, BSF with $I_{set1} = 1$ nA and different bias currents $I_{set} = I_{set2,3} = 0.25$ nA, 0.5 nA, 1 nA, 2 nA. The f_o was 66 Hz, 130.3 Hz, 254 Hz, 501.1 Hz, respectively. This confirms that the proposed filter enjoys electronic tuning ability. Fig. 11 (a) and (b) show the magnitude characteristics of the LPF, HPF, BPF and BSF with process corners and MC analysis, respectively, obtained for the same bias condition as for Fig. 9 (a), this way confirming the robustness of the filter. The transient response of the LPF for $I_{set1,2,3} = 1$ nA is shown in Fig. 12. A sine-wave signal with 100 mV_{pp} @ 10 Hz has been applied to the input of the filter as shown in Fig. 12 (a). The output signal is shown in Fig. 12 (b). The nominal total harmonic distortion (THD) was 0.62%. The THD simulation was repeated using the MC analysis with 200 runs. The result of the histogram is shown in Fig. 13. The mean value of the THD was 1.37% while the standard deviation was 0.98%. The THD of the LPF with different input voltage and different frequencies 10 Hz and 100 Hz is shown in Fig. 14. The LPF shows THD below 1.2% for 120 mV_{pp}.

The output noise characteristic of the LPF is shown in Fig. 15. The RMS value of the integrated noise was 116 μV, which results in the dynamic range (DR) around 49.7 dB. The mean value of the DR stays around 47.4 dB with worst case of MC and process corner analysis.

Finally, Table 6 compares the proposed filter with some previous filters. The versatile universal filters in [35], [36], biquad-based high-frequency high-order filters in [37], [38], biquad-based low-power high-order filters in [39], and

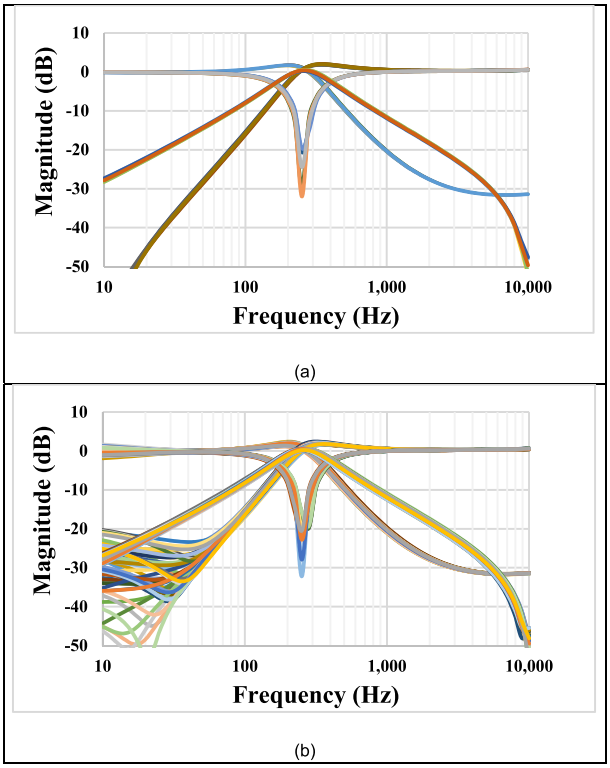

FIGURE 11. Magnitude characteristics of the LPF, HPF, BPF, BSF with process corner analysis (a) and MC (b).

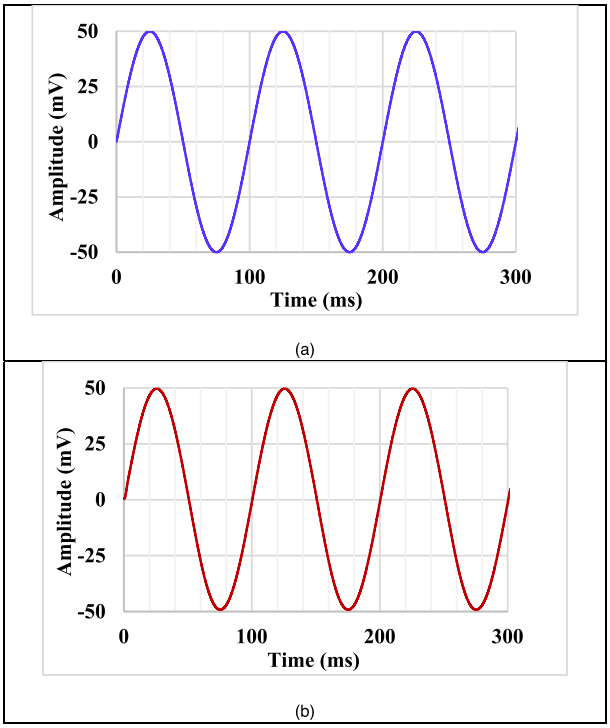

FIGURE 12. Transient response for the LPF: (a) input and (b) output.

low-voltage low-power universal filters in [23], [40] have been used for a comparison. It is evident that the proposed filter offers the highest number of filtering functions (i.e. 23),

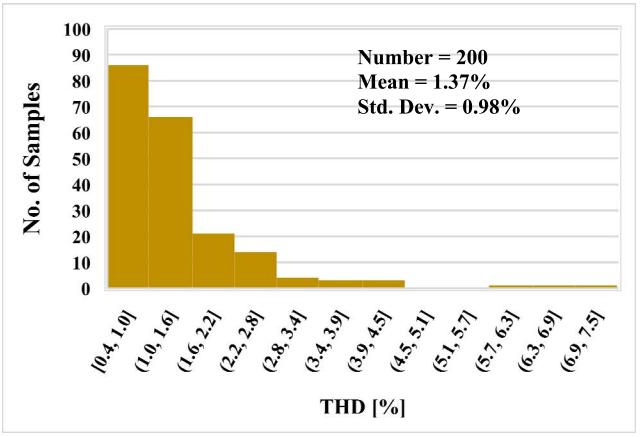

FIGURE 13. The histogram of the THD of the LPF with MC simulation.

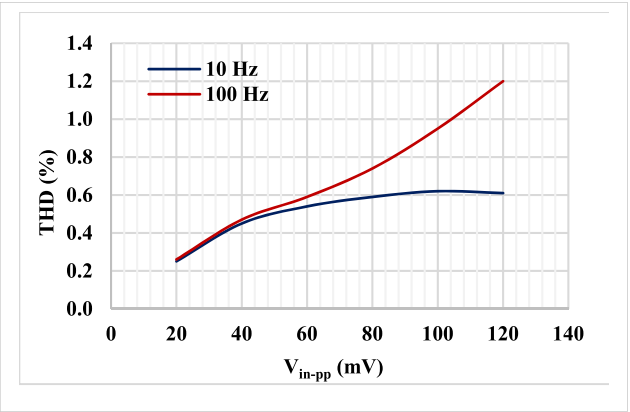

FIGURE 14. The THD of the LPF with different input voltage and different frequencies.

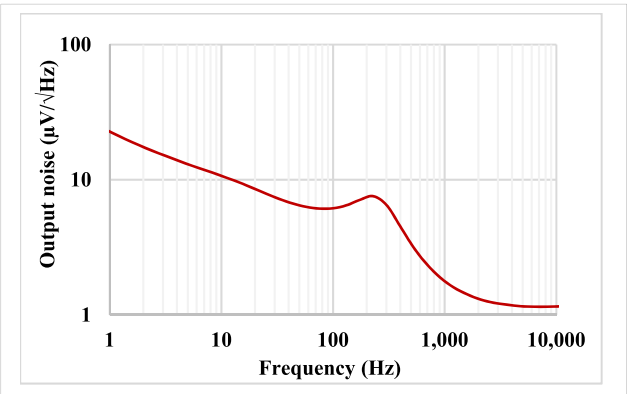

FIGURE 15. The voltage noise at the LPF output.

resistorless topology, electronic control of ω_o, and, with one exception from [23], the lowest voltage supply and power consumption. The figure-of-merit (FOM), dynamic range and low-voltage (LV) capability of the filters have been also considered in Table 6. It is notable that the proposed filter and the one in [23] are the only filters that offer 100% LV operation capability (V_{TH}/V_{DD}). Although the filter

in [38] shows better DR and FOM, this filter along with those in [37], [39] offer only low-pass function. Furthermore, the filters in [37], [38] use power-hungry structures with much higher voltage supply, making them inappropriate for extremely low-voltage low-power applications. Compared with the low-voltage low-power filters in [23], [39], [40], the proposed filter has better LV operation capability than the filters in [39], [40] and better FOM than the filter in [23].

VI. CONCLUSION

This paper presents an innovative structure for DDTA based on bulk-driven multiple-input DDA followed by bulk-driven transconductance amplifier capable to work under 0.5 V supply voltage. The DDA structure employs two PPFs, which results in high performance parameters. Bulk-driven techniques along with MI-MOST increase the input voltage range of the circuit. The universal filter application employs 3 DDTAs and two grounded capacitors with low value for circuit integration. The simulated results confirm the futures of the design.

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