Received March 18, 2022, accepted March 31, 2022, date of publication April 11, 2022, date of current version April 20, 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3166533

Reconfigurable and Storable Chaotic Logic Operations in Drive-Response VCSELs With Optical Feedback

GELIANG XU, SONG YE, AND JIAN XU

School of Electronic Engineering, Chaohu University, Hefei 238000, China

Corresponding author: Geliang Xu (xugeliang1027@163.com)

This work was supported in part by the Industrial Process Control Optimization and Automation Engineering Research Center, Chaohu University, under Grant kj21gczx02; in part by the Natural Science Foundation of the Higher Education Institutions of Anhui Province under Grant KJ2019A0685; and in part by the School-Level Scientific Research Project of Chaohu University under Grant XLY-202001.

ABSTRACT Based on the system of drive-response vertical cavity surface emitting lasers (VCSELs) with optical feedback and the new electro-optic (EO) modulation theory, we propose a novel reconfigurable and storable logic operations scheme to perform the behaviors of flexible switching and delayed storage among different logic operations. Here, the optical feedback intensity is modulated into logic input, the applied electric field in drive system and response system are modulated into logical control signals, the logic output is decoded by threshold mechanism. When the logical control signal in drive system and response system remain equal and both of them satisfy different logic operation relationships with the logic inputs, the system can perform the mutual conversion and delayed storage among the logic operations such as AND, NAND, OR, NOR, XOR and XNOR. Furthermore, the half adder logic operations are also being realized. Finally, the influence of bit duration time and noise intensity on the reliability of the logic operations is analyzed, and the results indicate that the logic operations have good anti-noise performance.

INDEX TERMS Vertical cavity surface emitting laser, reconfigurable, chaotic logic operations, success probability.

I. INTRODUCTION

It is well known that the chaotic laser signal is not only extremely sensitive to the initial conditions of the system and external interference, but also has the characteristics of aperiodic and high randomness, which makes it widely used in the field of optical communication, such as high-speed physical random number generators, high-speed key distribution and signal carrier, etc. In recent years, optical chaotic logic operations based on semiconductor laser has attracted widespread attention since it provides a scheme to realize reconfigurable logic operation, where different logic operations such as AND, OR, XNOR, NAND, NOR, XOR, etc., are flexibly converted by the slight change of the parameters in a chaotic system. And optical chaotic logic operations are the most critical technology in future optical chaotic network secure communication, however, the technology of the optical chaotic logic operations still lags behind. For most of the logic processing of optical chaotic signals, such as multiplexing, demultiplexing, switching, regeneration, storage and calculation, it is necessary to implement all-optical chaotic logic devices and sequential logic ones with low power consumption and high speed. Compared to edge emitting laser, vertical cavity surface emitting laser (VCSEL) exhibits many advantages such as large modulation bandwidth, low threshold current, round beam output and easy coupling with fiber, etc. [1]–[4]. Under the conditions of external light injection or bias current injection, the VCSEL is easy to emit mutually orthogonal chaotic x-polarized light (x-PL) and chaotic y-polarized light (y-PL), and it can also exhibit rich dynamic behaviors such as polarization switch and polarization bistability [5]–[14]. Based on the dynamic characteristics of VCSEL's polarization bistability, the C. Masoller's research group successfully implemented stochastic logic gates with different technical schemes [1], [2], [15]. In 2013, Yan put forward a feasible plan to implement all-optical logic gates based on "master-slave-response" synchronization system of chaotic multiple-quantum-well lasers [16].

The associate editor coordinating the review of this manuscript and approving it for publication was Yang Yue.

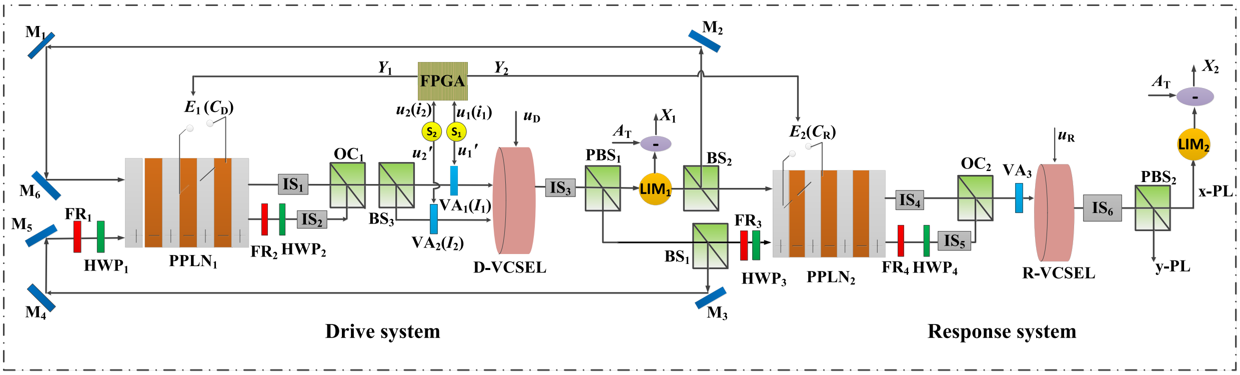


FIGURE 1. The diagram of system composition and detailed light path. D (R)-VCSEL: drive (response) vertical cavity surface emitting laser; IS: isolator; μ_D: normalized injection current of D-VCSEL; μ_R: normalized injection current of R-VCSEL; BS: beam splitter; PBS: polarization beam splitter; OC: optocoupler; HWP: half-wave plate; FR: faraday rotator; VA: variable attenuator; M: mirror; PPLN: periodic poled LiNbo$_3$; E_1 (E_2): applied electric field; *x* (*y*)-PL: *x* (*y*)-polarized light; FPGA: field programmable gate array; LIM: light intensity meter; A_T: threshold; X_1 (X_2): logic output; I_1 (I_2): logic input; C_D (C_R): control signal.

In 2015, Zhong's team obtained optoelectronic composite logic gates based on electro-optic (EO) modulation theory and the VCSEL subjected to external optical injection [17]. In 2016, all-optical stochastic logic gates and their delay storages were successfully implemented based on generalized chaotic synchronization and polarization switch in system of the cascaded VCSELs with optical-injection [18]. In 2017, based on polarization bistability, the reconfigurable all-optical chaotic logic gates were firstly being successfully realized by the scheme for VCSEL subject the injection of light from tunable sampled grating distributed Bragg reflector laser [19]. In 2020, my research group use a simple technical scheme for the VCSEL subject the optical feedback to implement the reconfigurable optoelectronic chaotic logic gates [20]. Next year, a novel scheme for the reconfigurable optical chaotic logic operations with fast rate of picoseconds scale were proposed in our laboratory [21].

However, the most of logic operations implemented by the above schemes are static, the development of dynamic and reconfigurable chaotic logic operations are still in the initial stage. Since the VCSEL with external optical feedback or external optical injection, as a nonlinear system with high dimension has rich nonlinear dynamic behaviors, it is great prospect that reconfigurable chaotic logic operations are implemented. In this paper, we put forward a novel implementation scheme for reconfigurable and storable chaotic logic operations in a chaotic polarization system of drive-response VCSELs with optical feedback. And the half adder logic operations can also be performed based on this system. Finally, the reliability of logic operations is further analyzed.

II. THEORY AND MODEL

The composition of the drive-response system and detailed light path are displayed in Figure 1. In the drive system, the light emitted by D-VCSEL first passes through the isolator 3 (IS$_3$), and then is separated into x-PL and y-PL by polarization beam splitter 1 (PBS$_1$). The x-PL passes through the light intensity meter 1 (LIM$_1$) and then is divided into two beams by beam splitter 2 (BS2). One beam of the x-PL is feedback into the periodic poled LiNbo$_3$ 1 (PPLN$_1$) crystal by the plane mirror 1 (M$_1$), M$_2$ and M$_6$ in the feedback cavity, and the other beam of x-PL is directly injected into the PPLN$_2$ crystal. The *y*-PL from PBS$_1$ is divided into two beams by BS$_1$. One beam of *y*-PL is reflected by M$_3$, M$_4$, M$_5$ and then passes through the faraday rotator 1 (FR$_1$) and half wave plate 1 (HWP$_1$), and finally is injected into the PPLN$_1$ crystal. The other beam of *y*-PL is directly injected into the PPLN$_2$ crystal through FR$_3$ and HWP$_3$. The above FR and HWP are mainly used to convert the polarized direction of y-PL to the z-axis direction of the crystal. The x-PL and y-PL injected into the crystal are regarded as the initial input of o-light and e-light respectively. The electric fields applied to PPLN$_1$ and PPLN$_2$ are denoted by E_1 and E_2, respectively. The x-PL and y-PL from the PPLN$_1$ crystal (e-light is converted into y-PC by FR$_2$ and HWP$_2$) pass through IS$_1$ and IS$_2$ respectively, and then are injected into optocoupler 1 (OC$_1$) together. The light output from OC$_1$ is divided into two beams by BS$_3$, and then these two beams are injected into D-VCSEL through polymer tunable diffraction grating variable attenuator 1(VA$_1$) and VA$_2$, respectively. The x-PL and y-PL from the PPLN$_2$ crystal pass through IS$_4$ and IS$_5$respectively, and then are combined by OC$_2$ into a beam of light, which is injected into the R-VCSEL through VA$_3$. Here, μ_D and μ_R are the normalized injection currents of D-VCSEL and R-VCSEL, respectively.

In order to implement dynamic switching between different logic operations, the logical control signal needs to meet the different logic operation relationships with the logic inputs synchronously. To solve this problem, we give the following technical solutions: the time-varying current source S_1 and S_2 output the current u_1, u_1', u_2 and u_2'. Here, the current $u_1$and u_2, in turn, are encoded into two electric logic inputs of the field programmable gate array (FPGA) such as i_1 and i_2. Because the polymer tunable diffraction grating VA is controlled by the current, the optical feedback intensity k_{f1} and k_{f2} are determined by u_1' and u_2' respectively (see Fig. 1). Here, the k_{f1} and k_{f2} are encoded into optical logic inputs I_1 and I_2, respectively. Due to $u_1 = u_1$', $u_2 = u_2$', the logic sets of the signals i_1 and i_2 are synchronized with those of the signals I_1 and I_2. The two logic outputs of the FPGA are defined as Y_1 and Y_2, which respectively control the E_1 and E_2. Here, $Y_1 = Y_2 = 0$ is encoded in the low level E_{01}, $Y_1 = Y_2 = 1$ is encoded in the high level E_{02}. Namely if $Y_1 = Y_2 = 0$, we obtain $E_1 = E_2 = E_{01}$ and $C_D = C_R = 0$; when $Y_1 = Y_2 = 1$, we have $E_1 = E_2 = E_{02}$ and $C_D = C_R = 1$. Using the FPGA, $Y_1$and Y_2 both can perform different logic operations with i_1 and i_2, so that C_D and C_R can implement different logic operations with I_1 and I_2 indirectly.

The D-VCSEL in the drive system is injected by the light from the $PPLN_1$ crystal, its rate equations are derived as:

$$\begin{aligned}\frac{d}{dt}\begin{pmatrix}E_{Dx}(t)\\E_{Dy}(t)\end{pmatrix} &= k\,(1+ia)\{[N_D(t)-1]\}\begin{pmatrix}E_{Dx}(t)\\E_{Dy}(t)\end{pmatrix}\\ &\quad \pm k\,(1+ia)\,in_D(t)\begin{pmatrix}E_{Dy}(t)\\E_{Dx}(t)\end{pmatrix}\\ &\quad \mp(\gamma_a+i\gamma_p)\begin{pmatrix}E_{Dx}(t)\\E_{Dy}(t)\end{pmatrix}+k_f\begin{pmatrix}E_{Px1}(t-\tau_1)\\E_{Py1}(t-\tau_1)\end{pmatrix}\\ &\quad \times\exp(-i\omega_0\tau)+\begin{pmatrix}\sqrt{\beta_{sp}\gamma_e N_D}\zeta_x\\ \sqrt{\beta_{sp}\gamma_e N_D}\zeta_y\end{pmatrix} \qquad (1)\end{aligned}$$

$$\begin{aligned}\frac{dN_D(t)}{dt} &= -\gamma_e\{N_D(t)-\mu_D+N_D(t)(|E_{Dx}(t)|^2+|E_{Dy}(t)|^2)\\ &\quad +in_D(t)[E_{Dy}(t)E^*_{Dx}(t)-E_{Dx}(t)E^*_{Dy}(t)]\} \qquad (2)\end{aligned}$$

$$\begin{aligned}\frac{dn_D(t)}{dt} &= -\gamma_s n_D(t)-\gamma_e\{n_D(t)(|E_{Dx}(t)|^2+|E_{Dy}(t)|^2)\\ &\quad +iN_D(t)[E_{Dy}(t)E^*_{Dx}(t)-E_{Dx}(t)E^*_{Dy}(t)]\} \qquad (3)\end{aligned}$$

Similarly, the rate equations of the R-VCSEL in the response system can be expressed as:

$$\begin{aligned}\frac{d}{dt}\begin{pmatrix}E_{Rx}(t)\\E_{Ry}(t)\end{pmatrix} &= k\,(1+ia)\{[N_R(t)-1]\}\begin{pmatrix}E_{Rx}(t)\\E_{Ry}(t)\end{pmatrix}\\ &\quad \pm k\,(1+ia)\,in_R(t)\begin{pmatrix}E_{Ry}(t)\\E_{Rx}(t)\end{pmatrix}\\ &\quad \mp(\gamma_a+i\gamma_p)\begin{pmatrix}E_{Rx}(t)\\E_{Ry}(t)\end{pmatrix}+k_{inj}\begin{pmatrix}E_{Px2}(t-\tau_2)\\E_{Py2}(t-\tau_2)\end{pmatrix}\\ &\quad \times\exp(-i\omega_0\tau_c)+\begin{pmatrix}\sqrt{\beta_{sp}\gamma_e N_R}\zeta_x\\ \sqrt{\beta_{sp}\gamma_e N_R}\zeta_y\end{pmatrix} \qquad (4)\end{aligned}$$

$$\begin{aligned}\frac{dN_R(t)}{dt} &= -\gamma_e\{N_R(t)-\mu_R+N_R(t)(|E_{Rx}(t)|^2+|E_{Ry}(t)|^2)\\ &\quad +in_R(t)[E_{Ry}(t)E^*_{Rx}(t)-E_{Rx}(t)E^*_{Ry}(t)]\} \qquad (5)\end{aligned}$$

$$\begin{aligned}\frac{dn_R(t)}{dt} &= -\gamma_s n_R(t)-\gamma_e\{n_R(t)(|E_{Rx}(t)|^2+|E_{Ry}(t)|^2)\\ &\quad +iN_R(t)[E_{Ry}(t)E^*_{Rx}(t)-E_{Rx}(t)E^*_{Ry}(t)]\} \qquad (6)\end{aligned}$$

In the above rate equations, the subscripts x, y, D, and R respectively mean the x-PL, y-PL, D-VCSEL and R-VCSEL; E represents the complex amplitude of light; N is the total carrier concentration; n is the difference in concentration between carriers with spin-up and carriers with spin-down; k_f represents the optical feedback intensity; τ_1 is the round-trip time in the external cavity; τ_2 is the propagation time of light from the $PPLN_2$ to the R-VCSEL; ω_0 represents the center frequency of D-VCSEL and R-VCSEL; ζ_x and ζ_y are a pair of gaussian white noises that are independent of each other and obey the standard normal distribution. E_{Px1} and E_{Py1} are the complex amplitudes of the x-PL and y-PL output from the $PPLN_1$ crystal; similarly, E_{Px2} and E_{Py2} are the those of x-PL and y-PL from the $PPLN_2$ crystal. The meanings and values of other physical parameters are presented in Table 1 below.

Considering the x-PL and y-PL from D-VCSEL as the original inputs of the o-light and the e-light in $PPLN_1$ crystal, respectively, we have

$$E_{o,e}(0,t-\tau_1)=\sqrt{\frac{\hbar\omega_0 V}{S_A T_L v_c n_{1,2}}}E_{Dx,Dy}(t-\tau_1) \qquad (7)$$

In the same way, the amplitude of the original inputs of the o-light and e-light in $PPLN_2$ crystal satisfy

$$E_{o,e}(0,t-\tau_2)=\sqrt{\frac{\hbar\omega_0 V}{S_A T_L v_c n_{1,2}}}E_{Dx,Dy}(t-\tau_2) \qquad (8)$$

In the above formula, E_o and E_e represent the amplitude of o-light and e-light respectively; $\hbar$ is the Planck constant; S_A denotes the effective area of the light spot; V is volume of the active layer; T_L is the round trip time in the laser cavity and $T_L = 2n_g o_c/L_v$, L_v is the length of the laser cavity, n_g represents the effective refractive index of active layer, $o_c$is the speed of light in vacuum; v_c is the light velocity in a vacuum, n_1 and n_2 are the undisturbed refractive indices of the o-light and the e-light, respectively. Due to the phase mismatch and the weak second-order nonlinear effect, the analytical solutions of the wave-coupling equations of the linear EO effect for the light in the $PPLN_1$ and the $PPLN_2$are written as:

$$E_{o,e}(L,t-t_0)=\rho_{x,y}(L,t-t_0)\exp(i\beta_0 L)\exp\left[i\phi_{x,y}(L,t-t_0)\right] \qquad (9)$$

where $t_0 = \tau_1$ orτ_2, the meanings and mathematical expressions of other physical parameters are present in Ref. [18]. When the D-VCSEL are subject to the injection of the output x-PL and y-PL from the $PPLN_1$ crystal, we have:

$$E_{Px1,Py1}(t-\tau_1)=\sqrt{\frac{S_A T_L v_c n_{1,2}}{\hbar\omega_0 V}}U_{o,e}(L,t-\tau_1) \qquad (10)$$

Similarly, while the output x-PL and y-PL from the $PPLN_2$ crystal are injected into the R-VCSEL, we obtain

$$E_{Px2,Py2}(t-\tau_2)=\sqrt{\frac{S_A T_L v_c n_{1,2}}{\hbar\omega_0 V}}U_{o,e}(L,t-\tau_2) \qquad (11)$$

TABLE 1. The parameters of the system.

Parameters	value	Parameters	value
Line-width enhancement factor a	3	Effective refractive index of active layer n_g	3.6
field decay rate k	300	Polar angle θ/π	1/2
Spin relaxation rate γ_s	50 ns^{-1}	Azimuth φ	0
Nonradiative carrier relaxation γ_e	1 ns^{-1}	Normalized injection current μ_D	1.5
Dichroism γ_a	-0.1 ns^{-1}	Poled period of crystal Λ	5.8×10^{5}m^{-1}
Birefringence γ_p	2 ns^{-1}	Crystal length L	15 mm
Delay time τ_1	2 ns	Refractive index of o-light n_1	2.24
Delay time τ_2	4 ns	Normalized injection current μ_R	1.5
Effective area of light spot S_A	38.485 um^2	Refractive index of e-light n_2	2.17
Length of the laser cavity L_V	10 um	Optical injection intensity k_{inj}	1.13 ns^{-1}
Volume of the active layer V	384.85 um^3	Central wavelength λ_0	1550 nm
Differential material gain g	2.9×10^{-12} s/m^3	Field confinement factor to the active region Γ	0.05
The bit duration time T	10 ns	The noise intensity β_{sp}	2×10^9

III. RESULTS AND DISCUSSION

Here, we suppose that the optical feedback intensity equals to the sum of two square waves that encode the two logic inputs, i.e., $k_f = k_{f1} + k_{f2}$. Here, the logic input for the optical feedback intensity k_{f1} is defined as I_1, and that for the optical feedback intensity k_{f2} is defined as I_2. In this case, there are four logic input sets: (0, 0), (0, 1), (1, 0), and (1, 1). Representing the (0, 1) and (1, 0) with the same optical feedback intensity k_{fII}, we can encode the four inputs with the three-level signals k_{fI}, k_{fII}, and k_{fIII}, where k_{fI} accounts for the set (0, 0), and k_{fIII} represents the set (1, 1). The three-level signal used to vary k_f is constant during a time interval T, defined as the bit duration time. We suppose that $I_1 = I_2 = 0$ when $k_{f1} = k_{f2} = 0.56\text{ns}^{-1}$ ($k_{fI} = 1.12\text{ns}^{-1}$); when $k_{f1} = k_{f2} = 0.57\text{ns}^{-1}$, $I_1 = I_2 = 1$ ($k_{fIII} = 1.14\text{ns}^{-1}$); $I_1 = 0, I_2 = 1$ if $k_{f1} = 0.56\text{ns}^{-1}$ and $k_{f2} = 0.57\text{ns}^{-1}$ ($k_{fII} = 1.13\text{ns}^{-1}$), similarly $k_{f1} = 0.57\text{ns}^{-1}$, $k_{f2} = 0.56\text{ns}^{-1}$ ($k_{fII} = 1.13\text{ns}^{-1}$) indicate that $I_1 = 1$, $I_2 = 0$. The applied electric field E_1 and E_2 in drive-response system are modulated into the logical control signal C_D and C_R respectively, it means that, if $E_1 = E_2 = E_{01} = 0.3\text{kV/mm}$, $C_D = C_R = 0$; else if $E_1 = E_2 = E_{02} = 0.75\text{kV/mm}$, $C_D = C_R = 1$. The logic output X_1 of the drive system is demodulated by the difference between the average value A_D of the x-PL intensity from the D-VCSEL and the threshold A_T; similarly, the logic output X_2 of the response system is demodulated by the difference between the average value A_R of that from the R-VCSEL and the threshold A_T. Namely, if A_D-$A_T > 0$, $X_1 = 1$, else $X_1 = 0$; in the same way $X_2 = 1$ if A_R-$A_T > 0$, else $X_2 = 0$.

The threshold value A_T determines the reliability of the logic operations. In order to obtain a suitable threshold, we adopt the following technical solutions: since C_D and C_R can perform different logic operations with I_1 and I_2 by FPGA, such as AND, OR, XOR, etc. For different cases of logic operation $C_{D,R}$, we have calculated the maximum value A_{Dmax} of A_D when $C_D = 0$, and the minimum value A_{Dmin} of that under $C_D = 1$. The maximum value A_{Rmax} of A_R when $C_R = 0$, and the minimum value A_{Rmin} of that under $C_R = 1$ also have been calculated. The specific calculation results are displayed in table 2. From the table, we obtain that the maximum value of A_{Dmax} equals to 0.0053, and the minimum value of A_{Dmin} equals to 0.016. Therefore, the threshold A_T needs to satisfy the following condition: $0.0053 < A_T < 0.016$. Hence, we take A_T as 0.01, that is, if $A_D < 0.01$ and $A_R < 0.01$, $X_1 = X_2 = 0$; else $X_1 = X_2 = 1$ when $A_D > 0.01$ and $A_R > 0.01$.

The system can realize different logic operations when the logical control signal meets different logic operation relationships with the logic inputs. In this paper, relying on FPGA to convert the logic operation relationships between the logical control signals C_D (C_R) and I_1, I_2, the response system has the same logic outputs as the drive system when C_R remains equal to C_D, i.e., $X_2(t) = X_1(t\text{-}\tau_2 + \tau_1)$, so as to realize the reconfigurable and storable logic operations.

Figure 2 shows the numerical simulation results of logic operations. The blue dotted line in Fig. 2(a) represents the applied electric field E_1 (encoded into C_D), and the red dotted line represents the three-level signals k_{fI}, k_{fII} and k_{fIII} (encoded into the logic inputs), the solid black line in Fig. 2(b) denotes the intensity I_{Dx} of x-PL from the D-VCSEL, and $I_{Dx} = |E_{Dx}|^2$. The logic output X_1 obtained by the threshold mechanism as shown in Fig. 2(c). From Figs. 2(a), 2(b) and 2(c), it is found that when the noise intensity β_{sp} is 2×10^9, the different logic operations at different time periods can be implemented, controlling the logic operation between C_D and two logic inputs. For example,

TABLE 2. For different cases of logic operations $C_{D,R}$ between I_1 and I_2, the maximum average value A_{Dmax} and A_{Rmax} of the x-PL intensity from D-VCSEL and R-VCSEL respectively under $C_{D,R} = 0$, and their minimum average value $A_{Dmin}$and A_{Rmin} under $C_{D,R} = 1$.

Logic operations	$(I_1, I_2) = (0, 0)$		$(I_1, I_2) = (0, 1) / (1, 0)$		$(I_1, I_2) = (1, 1)$	
	$C_{D,R}$	A_{Dx}, A_{Rx}	$C_{D,R}$	A_{Dx}, A_{Rx}	$C_{D,R}$	A_{Dx}, A_{Rx}
$C_{D,R} = I_1 \cdot I_2$	0	A_{Dmax}=0.0051 A_{Rmax}=0.0039	0	A_{Dmax}=0.0052 A_{Rmax}=0.003	1	A_{Dmin}=0.025 A_{Rmin}=0.019
$C_{D,R} = \overline{I_1 \cdot I_2}$	1	A_{Dmin}=0.03 A_{Rmin}=0.021	1	A_{Dmin}=0.022 A_{Rmin}=0.019	0	A_{Dmax}=0.0048 A_{Rmax}=0.0024
$C_{D,R} = I_1 + I_2$	0	A_{Dmax}=0.0053 A_{Rmax}=0.0042	1	A_{Dmin}=0.031 A_{Rmin}=0.02	1	A_{Dmin}=0.034 A_{Rmin}=0.018
$C_{D,R} = \overline{I_1 + I_2}$	1	A_{Dmin}=0.022 A_{Rmin}=0.019	0	A_{Dmax}=0.005 A_{Rmax}=0.004	0	A_{Dmax}=0.005 A_{Rmax}=0.002
$C_{D,R} = I_1 \oplus I_2$	0	A_{Dmax}=0.005 A_{Rmax}=0.002	1	A_{Dmin}=0.034 A_{Rmin}=0.021	0	A_{Dmax}=0.0048 A_{Rmax}=0.0031
$C_{D,R} = I_1 \text{ e } I_2$	1	A_{Dmin}=0.0195 A_{Rmin}=0.016	0	A_{Dmax}=0.0049 A_{Rmax}=0.002	1	A_{Dmin}=0.023 A_{Rmin}=0.019

if $C_D = I_1 \cdot I_2$when the time t is between 10 ns and 50 ns, we obtain the logic AND operation, i.e., $X_1 = I_1 \cdot I_2$; while t is between 50 ns and 90 ns, the logic OR operation can be performed when $C_D = I_1+I_2$, i.e., $X_1 = I_1+I_2$; with t varying from 90 ns to 130 ns, $X_1 = I_1 \odot I_2$ if $C_D = I_1 \odot I_2$, the logic output is logic XNOR operation; In the case that $C_D = \overline{I_1 \cdot I_2}$, the logic output is of logic NAND operation, i.e., $X_1 = I_1 \bar{\cdot} I_2$, and when 130 ns$\leq t \leq$ 170 ns; If $C_D = \overline{I_1+I_2}$, it is converted into the XNOR operation, i.e., $X_1 = \overline{I_1+I_2}$ in the time period from 170 ns to 210 ns. Finally, with t being between 210 ns to 250 ns, the logic output is further converted into logic XOR operation due to the fact that $C_D = I_1 \oplus I_2$. When the logical control signals C_D and C_R remain equal at all times, the logic operations performed by the response system are the same as that of the drive system, as shown in Figs. 2(d), 2(e) and 2(f), indicating that the system has the ability to reconstruct and store logic operations.

Controlling the logic operation between the logical control signals and two logic inputs, the reconfigurable and storable logic operations such as XOR, AND, XNOR, OR, NAND and NOR are further implemented as shown in Fig. 3.

Depending on FPGA, we have $C_D = I_1 \cdot I_2$ and $C_R = I_1 \oplus I_2$ (see Figs. 4(a) and 4(d)) at the same time, thus the drive system can implement the logic AND operation, i.e., $X_1 = I_1 \cdot I_2$, and the response system can realize the logic XOR operation, i.e., $X_2 = I_1 \oplus I_2$, as shown in Figs. 4(b), 4(c), 4(e) and 4(f). Therefore, the half adder logic operations are also successfully implemented.

The reliability of logic operations depends strongly on some system parameters. In the following we calculate the success probability P_1 and P_2 (as the ratio between the number of correct bits to the total number of bits) to quantify the reliabilities of the logic operations performed by the drive system and the response system, respectively. Here, we take the logic operations shown in Fig. 2 as an example to calculate the evolutions of P_1 and P_2in the space of noise intensity β_{sp} and bit duration T, as shown in Fig 5. It is found that the area of $P_1 < 0.8$ in Fig. 5(a) accounts for a larger proportion when T varies from 0ns to 1ns, indicating that the reliability of logic operations is poor; As T gradually increases from 1ns to 2ns, the area with $P_1 > 0.9$ accounts for a larger proportion, denoting that the reliability of logic operations is enhanced; when T continues to increase from 2ns to 10ns, the proportion of the area with $P_1 = 1$ increases rapidly. It can also be seen that as the noise intensity β_{sp} increases from 0 to 4×10^9, the proportion of area with $P_1 = 1$ is gradually shrinking, showing that reliability is slowly getting worse. The evolution trajectory of P_2 in Fig. 5(b) is similar to that of P_1 in Fig. 5(a).

.

.

In order to show the local changes of P_1 and P_2in Fig. 5 in more detail, we further analyze the dependence of the success probability on the β_{sp} for different T, as displayed in Fig. 6. As we can see from the Fig. 6(a) that if $T = 4$ns, the value of P_1 is always equal to 1 when $0 < \beta_{sp} < 1 \times 10^9$, which indicates that the reliability of the logic operations is strong, and no error appeared in logic outputs; as β_{sp} exceeds 1×10^9, the value of P_1 begins to fluctuate, but is still above 0.9. When $0 < \beta_{sp} < 3.75 \times 10^9$, the P_1 is always equal to 1 if $T = 8$ns, denoting that the logic operations are of reliability and stability; P_1 varies in a small range when β_{sp} exceeds 3.75×10^9, the reliability of the logic operations gets slightly worse. When β_{sp} varies from 0 to 4×10^9, the logic operations are so reliable that P_1 is always equal to 1 if $T = 10$ns. From Fig. 6(b), one sees that value of P_2 oscillates severely with β_{sp} increasing if $T = 4$ns. When β_{sp} increases from 0 to 2.7 $\times$

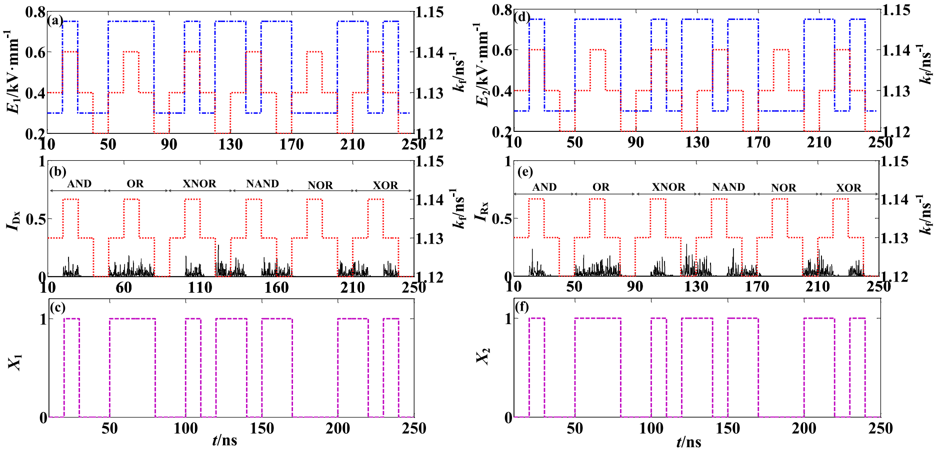


FIGURE 2. Reconfigurable chaotic logic operations and their delayed storage.

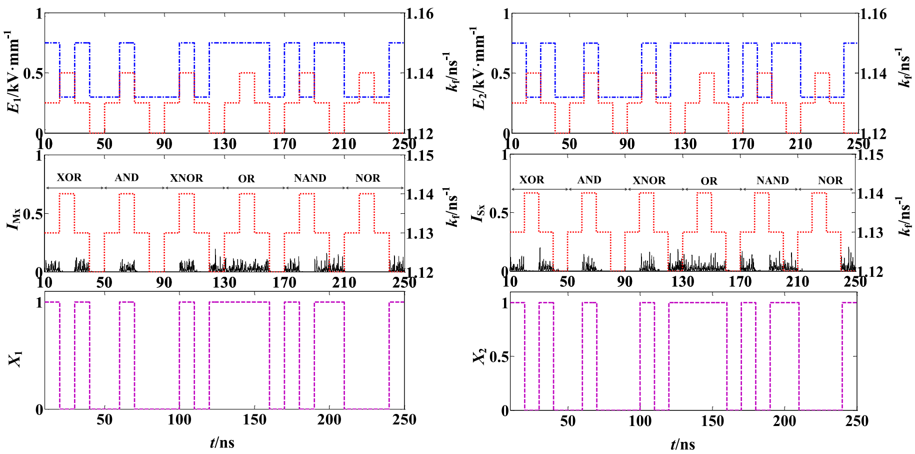


FIGURE 3. Reconfigurable chaotic logic operations and their delayed storage.

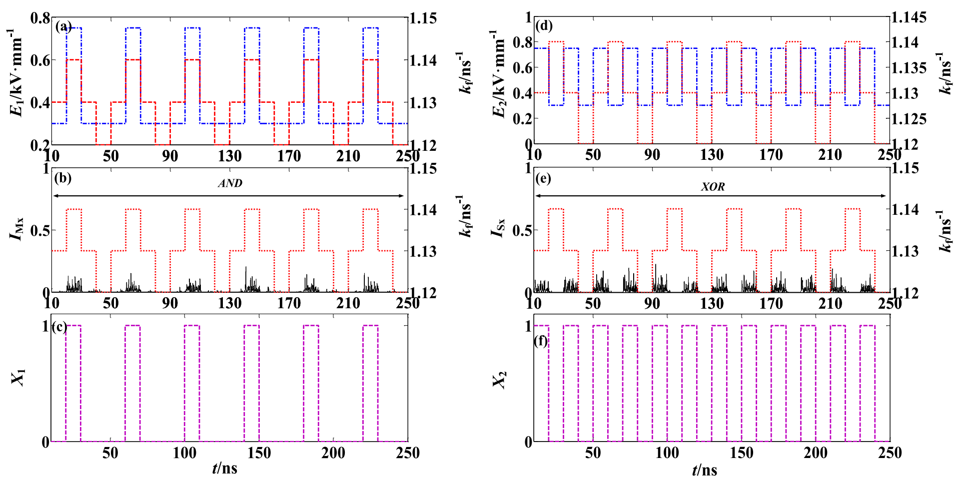


FIGURE 4. Half adder logic operations.

10^9, the value of P_2 always equals to 1 since $T = 8$ns; with β_{sp} further increasing from 2.7×10^9 to 4×10^9, P_2 begin to fluctuate. The β_{sp} within the range of 4×10^9 will not cause errors to the logic outputs due to the P_2 is always equal to 1 when $T = 10$ns.

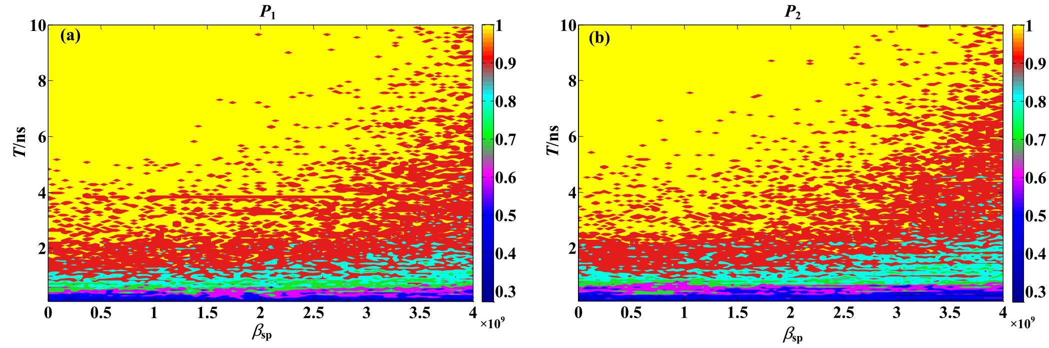


FIGURE 5. The evolution of P_1 and P_2 in the space of bit duration time T and noise intensity β_{sp}

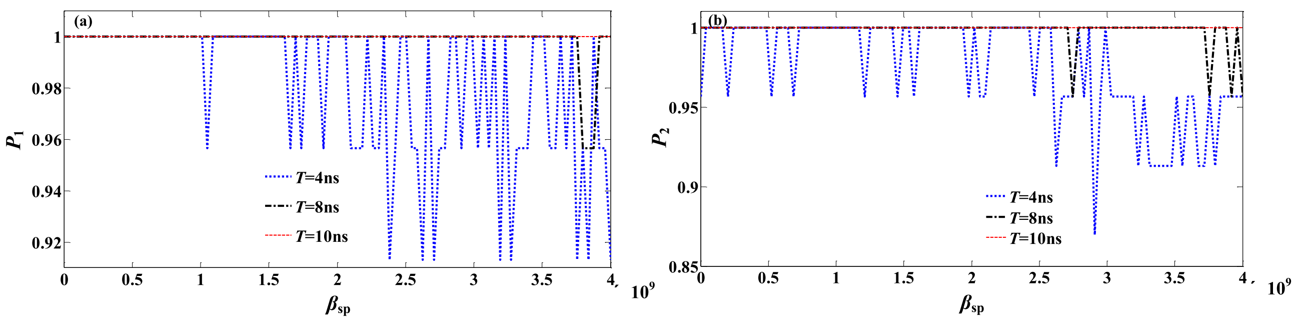


FIGURE 6. The dependence of the success probability on the noise intensity β_{sp} for different bit duration time T

From the above results, it is concluded that the success probability P_1 and P_2 for logic operations implemented by the drive system and response system respectively are seriously dependent on the noise intensity β_{sp} and bit duration time T. The values of P_1 and P_2 will become small and unstable if the value of T is too small or the value of β_{sp} is too large. It is noted that the logic operations are highly reliable that both P_1 and P_2 are always equal to 1 under appropriate conditions such as $T = 8$ns and $\beta_{sp} < 2.7 \times 10^9$, or $T = 10$ns and β_{sp} within the 4×10^9.

IV. CONCLUSION

We propose a novel reconfigurable and storable chaotic logic operations scheme by using the drive-response VCSELs with optical feedback, based on the EO modulation theory. Here, the optical feedback intensity is modulated into logic input, the applied electric field in drive system and response system are modulated into logical control signals, and logic outputs are demodulated by the threshold mechanism. Relying on FPGA to convert the logic operation relationships between the logical control signals and logic input, the system can perform the reconfigurable and storable processing of logic operations. Furthermore, the system can also implement the half adder logic operations when the chaotic logic AND and XOR operations are performed by the drive system and the response system, respectively. It is noted that the bit duration time and noise intensity have an impact on success probability of logic operations. And the reliability of logic operations are so strong that the success probability can be always equal to 1 even though the noise intensity is as high as 4×10^9, indicating that the logic operations have good anti-noise performance. These results have potential application in the reconfigurable and storable chaotic logic computing system with high speed, security and low power cost.

REFERENCES

[1] J. Zamora-Muntand and C. Masoller, "Numerical implementation of a VCSEL-based stochastic logic gate via polarization bistability," *Opt. Exp.*, vol. 18, no. 16, pp. 16418–16429, Aug. 2010.

[2] S. Perrone, R. Vilaseca, and C. Masoller, "Stochastic logic gate that exploits noise and polarization bistability in an optically injected VCSEL," *Opt. Exp.*, vol. 20, no. 12, pp. 22692–22699, Sep. 2012.

[3] X. X. Zhang, S. H. Zhang, T. A. Wu, and W. Y. Sun, "Polarization switching characteristics of polarization maintaining optical feedback and orthogonal optical injection of 1550 nm-VCSEL," *Acta. Phys. Sinica*, vol. 65, no. 21, Nov. 2016, Art. no. 214206.

[4] D. Z. Zhong, G. Q. Xia, F. Wang, and Z. M. Wu, "Vectorial chaotic synchronization characteristics of unidirectionally coupled and injected vertical-cavity surface-emitting lasers based on optical feedback," *Acta Phys. Sinica*, vol. 56, no. 6, pp. 3279–3291, Mar. 2007.

[5] S. Xiang, W. Pan, L. Yan, B. Luo, N. Jiang, K. Wen, X. Zou, and L. Yang, "Variable-polarization optical feedback induced hysteresis of the polarization switching in vertical-cavity surface-emitting lasers," *J. Opt. Soc. Amer. B, Opt. Phys.*, vol. 27, no. 12, pp. 2512–2517, 2010.

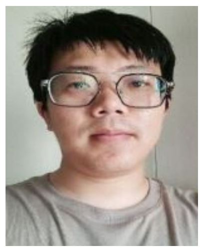
[6] W. Li Zhang, W. Pan, B. Luo, M. Yao Wang, and X. Hua Zou, "Polarization switching and hysteresis of VCSELs with time-varying optical injection," *IEEE J. Sel. Topics Quantum Electron.*, vol. 14, no. 3, pp. 889–894, Jun. 2008.

[7] K. H. Jeong, K. H. Kim, S. H. Lee, M. H. Lee, B. S. Yoo, and K. A. Shore, "Optical injection-induced polarization switching dynamics in 1.5 μm wavelength single-mode vertical-cavity surface-emitting lasers," *IEEE Photon. Technol. Lett*, vol. 20, no. 10, pp. 779–781, Apr. 1, 2008.

[8] H. Y. Qiu, Z. M. Wu, T. Deng, Y. He, and G. Q. Xia, "Polarization switching characteristics in a 1550 nm VCSEL subject to circularly polarized optical injection," *Chin. Opt. Lett*, vol. 14, no. 2, pp. 33–37, 2016.
[9] Z.-Q. Zhong, S.-S. Li, S.-C. Chan, G.-Q. Xia, and Z.-M. Wu, "Polarization-resolved time-delay signatures of chaos induced by FBG-feedback in VCSEL," *Opt. Exp.*, vol. 23, no. 12, pp. 15459–15468, Jun. 2015.
[10] P. Guo, W. Yang, D. Parekh, C. J. Chang-Hasnain, A. Xu, and Z. Chen, "Experimental and theoretical study of wide hysteresis cycles in 1550 nm VCSELs under optical injection," *Opt. Exp.*, vol. 21, no. 3, pp. 3125–3132, Feb. 2013.
[11] T. Deng, Z. M. Wu, Y. Y. Xie, J. G. Wu, X. Tang, L. Fan, P. Krassimir, and G. Q. Xia, "Impact of optical feedback on current-induced polarization behavior of 1550 nm vertical-cavity surface-emitting lasers," *Appl. Opt.*, vol. 52, no. 16, pp. 3833–3837, Jun. 2013.
[12] J. J. Chen, G. Q. Xia, and Z. M. Wu, "Power-induced polarization switching and bistability characteristics in 1550-nm VCSELs subjected to orthogonal optical injection," *Chin. Phys. B*, vol. 24, no. 2, pp. 186–190, Feb. 2015.
[13] T. Deng, Z.-M. Wu, and G.-Q. Xia, "Two-mode coexistence in 1550 nm VCSELs with optical feedback," *IEEE Photon. Technol. Lett.*, vol. 27, no. 19, pp. 2075–2078, Oct. 1, 2015.
[14] D. Z. Zhong and Z. M. Wu, "Manipulation of the vector chaotic polarization of VCSEL output with external optical feedback by electro-optic modulation," *Acta. Phys. Sinica*, vol. 61, no. 3, pp. 355–367, 2012.
[15] M. F. Salvide, C. Masoller, and M. S. Torre, "All-optical stochastic logic gate based on a VCSEL with tunable optical injection," *IEEE J. Quantum Electron.*, vol. 49, no. 10, pp. 886–893, Oct. 2013.
[16] Y. Sen-Lin, "Chaotic laser parallel synchronization and its application in all-optical logic gates," *Acta Phys. Sinica*, vol. 62, no. 23, 2013, Art. no. 230504.
[17] D. Zhong, Y. Ji, and W. Luo, "Controllable optoelectric composite logic gates based on the polarization switching in an optically injected VCSEL," *Opt. Exp.*, vol. 23, no. 23, p. 29823, Nov. 2015.
[18] D. Z. Zhong, W. Luo, and G. L. Xu, "Controllable all-optical stochastic logic gates and their delay storages based on the cascaded VCSELs with optical-injection," *Chin. Phys. B*, vol. 25, no. 9, pp. 342–354, 2016.
[19] D.-Z. Zhong, G.-L. Xu, W. Luo, and Z.-Z. Xiao, "Reconfigurable dynamic all-optical chaotic logic operations in an optically injected VCSEL," *Chin. Phys. B*, vol. 26, no. 12, Dec. 2017, Art. no. 124204.
[20] G. Xu, C. Da, Q. Ni, S. Zhou, and F. Cheng, "Reconfigurable optoelectronic chaotic logic gates in vertical cavity surface emitting laser with optical feedback," *Chin. J. Lasers*, vol. 47, no. 12, 2020, Art. no. 1206003.
[21] G. L. Xu, J. Xu, L. L. Kong, Q. F. Huang, X. T. Qiu, Y. Y. Guo, and F. Cheng, "Reconfigurable optical chaotic logic operations with fast rate for picosecond scale," *Acta. Photonica Sinica*, vol. 50, no. 5, May 2021, Art. no. 0506008.

GELIANG XU received the master's degree in information and communication engineering from Wuyi University, in 2018. He participated in the National Natural Science Foundation of China during the postgraduate study. Since 2018, he has been working as a Teacher with Chaohu University. His research interests include nonlinear optics, chaos computing, and chaos lidar ranging.

SONG YE received the Ph.D. degree in optical engineering from the Sichuan University. He is a Professor with Chaohu University. He has presided over a number of national, provincial, and ministerial projects. His research interests include micro-nano optical technology and chaos computing.



JIAN XU received the Ph.D. degree in optical engineering from Fujian Normal University, in 2018. He is currently a Teacher with Chaohu University. His main research interests include chaos and the application of laser in biomedicine.