

Received February 23, 2022, accepted March 28, 2022, date of publication April 7, 2022, date of current version April 14, 2022. *Digital Object Identifier* 10.1109/ACCESS.2022.3165561

A New Approach to Fourth-Order Quadrature Signal Generation for a Fast and Noise-Free PLL Output Under Non-Ideal Grid Voltage Conditions

BISHAL MONDAL[®] AND B. ARUN KARUPPASWAMY[®], (Member, IEEE)

Department of Electrical Engineering, IIT Madras, Chennai 600036, India

Corresponding author: Bishal Mondal (ee16d406@ee.iitm.ac.in)

This work was supported by the New Faculty Scheme, IIT Madras, under Project ELE1617686NFSCAKAR.

ABSTRACT Dual quadrature signal generator (QSG) along with a positive sequence calculator (PSC) eliminates the negative sequence components from unbalanced grid voltages. The QSGs also offer attenuation to harmonics and dc-offset present in the sensed input voltages. Fourth-order QSGs offer superior harmonic attenuation with complete dc-offset rejection compared to lower-order QSGs. Therefore, dual fourth-order QSG + PSC is an apt solution for pre-filtering in phase-locked loops (PLLs) under non-ideal grid voltage conditions. Two fourth-order QSGs (FO-QSGs) namely, second-order SOGI-QSG (SO-SOGI-QSG) and cascaded SOGI-QSG have been proposed in the literature. Parameter selection for these FO-QSGs to achieve a faster dynamic response is challenging due to the higher order of the transfer functions. The response time of the QSGs directly impact the response time of the PLL. This paper proposes a new approach to fourth-order quadrature signal generation that achieves a lower settling time for the QSG parameters using equations that directly relate to the system settling time. Using the proposed method, the QSG settles within 25.4 ms while maintaining a low total harmonic distortion.

INDEX TERMS Phase-locked loop, non-ideal grid, second-order generalized integrator, quadrature signal generator.

I. INTRODUCTION

A phase-locked loop (PLL) provides voltage magnitude, frequency, and phase angle information of the utility grid for synchronization and reference current generation in gridtie converter applications [1]. The commonly used PLL structure is the synchronous reference frame based PLL (SRF-PLL). The SRF-PLL utilizes a synchronously rotating direct-quadrature axis (dq axis) along with a proportionalintegral (PI) controller for its implementation [2], [3]. The PI controller of the SRF-PLL is designed to achieve a required bandwidth (BW) that gives desired transient and steady-state response.

Under non-ideal grid voltage conditions, the fundamental positive-sequence voltage of the utility appears as a dc

The associate editor coordinating the review of this manuscript and approving it for publication was Zhigang Liu^(D).

component in the dq frame while the abnormalities like harmonics, unbalance and dc-offset appear as ac components [2]. The fundamental positive-sequence voltage is the information of interest for synchronization and controls. Two broad approaches are used in literature to handle the effect of abnormalities [4]–[6], [9]–[13]. While [4] and [5] handle the abnormalities inside the PLL, [6], [9]–[13] handle the same outside the PLL using a pre-filter.

For a three-phase SRF-PLL, the pre-filter approach based on dual quadrature signal generator (QSG) with a positive sequence calculator (PSC) implemented in the $\alpha - \beta$ reference frame [6], [9], [10], [13] provides better results [14] as compared to [4], [5]. Fig. 1 shows the block diagram of a pre-filter with a dual-QSG and PSC. The QSG can be implemented using transfer functions of varying orders. While the QSGs eliminate the dc component and provide attenuation to the harmonics of the sensed grid voltage, the PSC handles



FIGURE 1. Block diagram of dual-QSG with PSC [9].

the unbalance. Therefore, the extracted positive sequence voltage components $(\nu_{\alpha}^+, \nu_{\beta}^+)$ allow selection of higher BW for the SRF-PLL [15], [16].

In [6], second-order generalized integrator QSGs (SOGI-QSGs) are used for realizing the dual-QSG of Fig. 1. The transfer function of the QSGs relating the in-phase component (v') to input (v) is a second-order band-pass filter (BPF) while the same relating the quadrature-phase component (qv')to v is a second-order low pass filter (LPF) [7]. Due to the LPF nature of the qv' to v transfer function, the method in [6] is incapable of complete dc-offset elimination. In [8] the dcoffset from qv' is eliminated by subtracting it from qv'. The dc component is obtained by low pass filtering of the error voltage, v - v'. The BW of the LPF must be low enough to ensure that no harmonics appear at qv' and therefore it results in a slower dynamics for the QSG. Method in [9] offers complete dc-offset elimination using a mixed second-(v' to v) and third-order (qv' to v) transfer function based BPFs as QSGs. An improved QSG is proposed in [10] and [12] for implementing the dual-QSG + PSC structure where both transfer-functions v' to v and qv' to v are third-order BPFs.

Dual-QSG followed by PSC eliminates the negative sequence components arising from the unbalance in the input voltages [6], [9], [10], [13]. Therefore the total harmonic distortion (THD) of v_{α}^+ and v_{β}^+ voltage components depend only on the harmonic attenuation and dc-offset elimination capability of the QSGs. Fourth-order QSGs [11], [13] offer higher harmonic attenuation and complete dc-offset elimination as compared to second- [6], mixed- (second- and third-) [9] and third-order [10], [12] QSGs. Two such fourth-order QSGs (FO-QSGs) – second-order SOGI-QSG (SO-SOGI-QSG) and cascaded SOGI-QSG – are proposed in [11] and [13] respectively.

A standard second-order system (SOS) can be built with two standard first-order systems (FOS) such that the SOS and FOS have same settling time [11]. By viewing SOGI-QSG as a standard FOS for ac inputs and following the above analogy, a FO-QSG named SO-SOGI-QSG is proposed in [11]. The parameters for the SO-SOGI-QSG are selected based on the settling time of the system. The method outlined in [11], for the selection of parameters, in effect approximates the fourthorder system to a lower-order system. This approximation leads to a large error between the expected and the actual settling times for several combinations of damping factor and settling time, an example of which is indicated in Section VI.

In [13] two SOGI-QSGs with identical parameters are cascaded to obtain a FO-QSG named cascaded SOGI-QSG (CSOGI-QSG). The first SOGI-QSG of the cascaded structure is used to eliminate the dc-offset from the sensed grid voltage while the two cascaded SOGI-QSGs together are used to give fourth-order attenuation to harmonics. The parameter selection outlined in [13] is primarily based on harmonic attenuation. The harmonic attenuation of the overall cascaded structure is set to be the same as that of a single SOGI-QSG. This is expected to lead to a faster dynamics for the individual SOGI-QSGs of the cascaded structure as compared to that of a single SOGI-QSG. The method is good in terms of harmonic attenuation performance. However, it suffers from certain flaws which are not addressed in [13]. Since the harmonic attenuation of the cascaded SOGI-OSGs and the single SOGI-QSG are equated, the damping factor of SOGI-QSGs of the cascaded structure has an empirical relation with the damping factor of a single SOGI-QSG. If the damping factor of the single SOGI-QSG is not selected carefully, the SOGI-OSGs of the cascaded structure can become overdamped and result in a slower response than the single SOGI-QSG, negating the basic premise of the design. Secondly, even though the settling time of each SOGI-QSGs is known, the combined effect of the cascaded structure on the settling time of the overall system has not been examined in [13]. The method is useful if a high attenuation is required and the settling time is of secondary importance.

The dual-QSG + PSC structure with the existing FO-QSGs [11], [13] gives a good steady-state performance with regard to harmonic attenuation and complete negative sequence and dc-offset elimination. However, their transient response in terms of the settling time is slow and unpredictable. In order to achieve a lower settling time for the dual-QSG + PSC structure, a new approach is proposed for the FO-QSG in this paper. The proposed approach ensures faster transients while maintaining a good steady-state performance. Further, the proposed approach helps to closely predict the settling time of the QSG at the design stage.

The proposed approach uses a cascaded structure as in [13] but with non-identical parameters for the individual SOGI-QSGs, and is referred to as cascaded non-identical SOGI-QSG (CNISOGI-QSG) in this paper. The non-identical parameters of the SOGIs offer higher degree of freedom for achieving better settling time as compared to [13]. Further, a novel parameter selection procedure that closely predicts the overall settling time of the cascaded system is developed. Conventionally, dominant closed-loop pole method is used to analyse higher-order systems. However, it requires the poles to be well separated in the frequency plane so that a simplifying assumption of neglecting the far away poles can be employed. This leads to a slower response for the system. The proposed method utilises an approximation which ensures that the actual and the approximated transfer functions have a close match of the transients only around the 2% settling limit. In this manner, unlike the dominant closedloop pole method, the proposed approach is able to achieve

faster dynamics since it allows the ratio of the real part of the poles to be lower than 5. Further, the method leads to a simple equation relating the settling time of the fourth-order system with its parameters which allows for a simple design procedure.

The proposed CNISOGI-QSG gives fourth-order attenuation to harmonics with complete dc-offset elimination while improving the dynamic response. The error between the expected and obtained settling times for the proposed approach is 1.7 ms for a damping factor choice of 0.7 and 0.645 for the two SOGI-QSGs of the CNISOGI-QSG. In comparison, the error for the SO-SOGI-QSG is 35.6 ms for a damping factor of 0.707 when designed using the method in [11]. Also, unlike CSOGI-SQG in [13], the proposed method is capable of estimating the settling time of the overall structure at the design stage. The proposed CNISOGI-QSG offers better overall speed of response when compared to existing FO-QSGs.

Finally, the performance of the CNISOGI-QSG with the proposed design method is tested along with a three-phase SRF-PLL. A fixed-frequency QSG based three-phase SRF-PLL is employed to ensure perfect decoupling between the QSGs and the SRF-PLL. In this manner, since the dynamics of the QSGs are unaffected by the dynamics of the PLL, the proposed design method of the CNISOGI-QSG is valid even with a SRF-PLL. The fixed-frequency QSG based threephase SRF-PLL used in this work follows [15], where the SRF-PLL is shown to be capable of error-free tracking of the grid phase angle even when the grid frequency is different from the QSG's corner frequency. The hardware result for a representative operating condition showed a settling time of around 25 ms for the CNISOGI-QSG with K_1 = 1.452 and $K_2 = 1.8$, while the frequency tracking of the same CNISOGI-QSG based SRF-PLL shows a settling time of 26 ms.

II. STRUCTURE OF THE PROPOSED CNISOGI-QSG

The proposed structure consists of two SOGI-QSGs like the one proposed in [13] but with non-identical parameters K_1 and K_2 as shown in Fig. 2. The transfer functions relating the outputs v' and qv' to the input v are represented as $G_1(s)$ and $H_1(s)$ respectively as

$$G_{1}(s) = \left(\frac{K_{1}\omega_{o}s}{s^{2} + K_{1}\omega_{o}s + \omega_{o}^{2}}\right) \left(\frac{K_{2}\omega_{o}s}{s^{2} + K_{2}\omega_{o}s + \omega_{o}^{2}}\right) (1)$$

$$H_{1}(s) = \left(\frac{K_{1}\omega_{o}s}{s^{2} + K_{1}\omega_{o}s + \omega_{o}^{2}}\right) \left(\frac{K_{2}\omega_{o}^{2}}{s^{2} + K_{2}\omega_{o}s + \omega_{o}^{2}}\right). (2)$$

Transfer functions (1) and (2) are fourth-order band-pass filters with corner-frequency as ω_o rad/s. The damping factors ζ_1 and ζ_2 of the constituent transfer functions of (1) and (2) are related to K_1 and K_2 as $K_1 = 2\zeta_1$ and $K_2 = 2\zeta_2$ and are different for SOGI-QSG-I and SOGI-QSG-II.



FIGURE 2. Block diagram of the proposed CNISOGI-QSG.

III. PARAMETER SELECTION FOR THE PROPOSED CNISOGI-QSG

The parameter selection procedure aims at reducing the settling time of the CNISOGI-QSG. It is desirable to obtain a settling time equation for the system in terms of its parameters K_1 and K_2 such that the system can be tuned during the design stage to attain a chosen settling time.

A. CONVENTIONAL DOMINANT CLOSED-LOOP POLE METHOD

Closed form expression for settling time is not defined for fourth-order systems. A conventional approach is to reduce the fourth-order system into an equivalent second-order system using the dominant closed-loop pole approach and use the settling time equation of a SOS to design the fourth-order system [17]. To apply the dominant closed-loop pole method, the transfer function (1) is rearranged as

$$G_1(s) = K \left\{ \frac{s}{s^2 + 2\zeta_1 \omega_o s + \omega_o^2} - \frac{s}{s^2 + 2\zeta_2 \omega_o s + \omega_o^2} \right\}$$
(3)

where

$$K = \frac{2\zeta_1\zeta_2\omega_o}{\zeta_2 - \zeta_1}; \quad 0 < \zeta_2 < 1 \text{ and } 0 < \zeta_1 < 1.$$

The complex pole pairs of the transfer-function (3) are

$$-\zeta_1 \omega_o \pm j \omega_o \sqrt{1-\zeta_1^2}$$
 and $-\zeta_2 \omega_o \pm j \omega_o \sqrt{1-\zeta_2^2}$. (4)

To reduce (3) using the dominant closed-loop pole method, it is required to have $\zeta_1 = \frac{\zeta_2}{\alpha}$ with $\alpha > 5$ [17]. Therefore (3) can be reduced to

$$G_{1}'(s) = \frac{2\zeta_{1}\omega_{o}s}{s^{2} + 2\zeta_{1}\omega_{o}s + \omega_{o}^{2}}$$
(5)

where $G'_1(s)$ is approximated equivalent of (3) with settling time

$$t'_s = \frac{4.4}{\zeta_1 \omega_o}.\tag{6}$$

Fig. 3 shows the step response of (3) $[s_{G_1}(t)]$ and (5) $[s_{G'_1}(t)]$ for an example setting of $\zeta_2 = 0.9$ ($K_2 = 1.8$) and $\zeta_1 = 0.15$ ($K_1 = 0.3$) considering $\alpha = 6$. A close match can be observed between $s_{G_1}(t)$ and $s_{G'_2}(t)$.

Table 1 shows the estimated (t'_s) and the simulated $(t'_{s,sim.})$ settling times for the fourth-order system (3) using the dominant closed-loop pole method for practical values of



FIGURE 3. Step response comparison of actual transfer function $G_1(s)$ and dominant pole based reduced transfer function $G'_1(s)$ for $\zeta_2 = 0.9$, $\alpha = 6$.

TABLE 1. Comparison of estimated (t'_s) and simulated $(t'_{s,sim.})$ settling time for proposed CNISOGI-QSG when designed using dominant closed-loop pole method.

ζ_2	α	$\zeta_1 = \zeta_2 / \alpha$	t'_s (ms)	$t'_{s,sim.}$ (ms)	Error (ms)
0.9	6	0.15	93.4	57.6	35.8
0.8	6	0.13	105.0	66.4	38.6
0.7	6	0.12	120.0	67.3	52.7
0.6	6	0.1	140.0	76.6	63.4
0.5	6	0.08	168.1	86.1	82.0

 ζ_2 (0.5 to 0.9) and a fixed $\alpha = 6$. The system response can be observed to be slow. The slow response is due to lower value of ζ_1 as a result of the requirement of the dominant closed-loop pole method. Also, as seen from Table 1, the error between the actual and estimated settling time is high. Therefore, the parameter evaluation of the proposed CNISOGI-QSG using the dominant closed-loop pole method becomes in-effective in terms of the settling time. An alternative approach is proposed in this work to improve the settling time.

B. PROPOSED METHOD

In the dominant pole approach, the reduced-order transfer function tries to match the original transfer function at every instant. To achieve this, the poles need to be well separated. The separation ensures that except for the small initial duration when the transients due to the ignored poles are still effective, the response of the reduced-order transfer function closely matches the original transfer function. Since only the 2% settling time instant is of interest in the parameter selection of the CNISOGI-QSG, the proposed approach is to allow lesser separation between the poles. The suggested separation of the poles is such that the fast decaying transient reaches negligible magnitude before the slower transient reaches its 2% value. This helps achieve a overall faster transient response for the system while simplifying the analysis of the settling time by considering only the slow transient envelop.



FIGURE 4. Step response of $G_1(s)$ for $K_2 = 1.8$ and $\sigma = 2$ along with the envelops of SOGI-QSG-I and SOGI-QSG-II.

For the proposed design method, K_1 ($2\zeta_1$) and K_2 ($2\zeta_2$) are selected such that the constituent SOGI-QSGs of the CNISOGI-QSG are always under-damped. Associating K_1 with the slower transient, we have,

$$K_1 = \frac{K_2}{\sigma}; \quad 0 < K_2 < 2 \text{ and } 1 < \sigma < 5.$$
 (7)

The range of K_2 and σ in (7) have been chosen to ensure that the SOGI-QSGs are under-damped as stated above. The upper limit on σ in (7) sets the boundary between the proposed method of parameter selection and the conventional dominant closed-loop pole method. The lower limit on σ in (7) is the value at which CNISOGI-QSG becomes cascaded SOGI-QSG of [13]. An example is considered to demonstrate the proposed design method of the CNISOGI-QSG with $K_2 =$ 1.8 ($\zeta_2 = 0.9$) and $\sigma = 2$. The value of K_1 is calculated as 0.9 ($\zeta_1 = 0.45$) using (7). This setting results in a faster settling time for SOGI-QSG-II when compared to SOGI-QSG-I of the CNISOGI-QSG. In this manner, the envelop of SOGI-QSG-II decays to zero before the CNISOGI-QSG response reaches around its 2% steady state. Therefore, the response of the CNISOGI-QSG from around 2% of its steady state is tracked completely by the envelop of SOGI-QSG-I as shown in Fig. 4. In this manner, the envelop of SOGI-QSG-I alone can be considered for determining the settling time of the proposed CNISOGI-QSG. The difference between the dominant closed-loop pole method and the proposed method can be clearly visualized from Fig. 3 and Fig. 4 respectively.

IV. SETTLING TIME EQUATION OF THE PROPOSED CNISOGI-QSG

The analytical expression for the step response of (1) is given by:

$$s_{G1,A}(t) = \frac{2\zeta_1\zeta_2}{\zeta_2 - \zeta_1} \left[\frac{e^{-\zeta_1\omega_0 t}}{\sqrt{1 - \zeta_1^2}} \sin \omega_{d1} t - \frac{e^{-\zeta_2\omega_0 t}}{\sqrt{1 - \zeta_2^2}} \sin \omega_{d2} t \right],$$

$$t \ge 0 \tag{8}$$

where

$$\omega_{d1} = \omega_o \sqrt{1 - \zeta_1^2}; \quad \omega_{d2} = \omega_o \sqrt{1 - \zeta_2^2}$$

and

$$0 < \zeta_1 < 1$$
 $0 < \zeta_2 < 1$.

The settling time equation of the CNISOGI-QSG is obtained by identifying the expression of the slowest envelop guiding the step response of (1). It can be seen from (8) that the step response of (1) is guided by the two envelops

$$env_{1} = \frac{2\zeta_{2}}{(\sigma - 1)\sqrt{1 - \left(\frac{\zeta_{2}}{\sigma}\right)^{2}}}e^{-\left(\frac{\zeta_{2}}{\sigma}\right)\omega_{0}t}$$
(9)
$$env_{2} = \frac{2\zeta_{2}}{(\sigma - 1)\sqrt{1 - \zeta_{2}^{2}}}e^{-\zeta_{2}\omega_{0}t}.$$
(10)

From (9), (10) and (7) it is clear that env_1 is slower than env_2 . Therefore, env_1 is considered for deriving the settling time equation for (1). The 2% settling time of (1) is computed by equating (9) to 0.02, which is obtained as

$$t_{s} = \frac{\sigma}{\zeta_{2}\omega_{o}} \ln\left[\frac{\zeta_{2}}{0.01(\sigma-1)\sqrt{1-\left(\frac{\zeta_{2}}{\sigma}\right)^{2}}}\right]; \quad 1 < \sigma < 5.$$
(11)

From (11), the proposed CNISOGI-QSG with a fixed ζ_2 can be designed to achieve different settling times for $1 < \sigma < 5$. An optimal value of σ ($\sigma_{opt.}$) in the range $1 < \sigma < 5$ for which the proposed CNISOGI-QSG attains a minimum settling time for a fixed ζ_2 is established in the following discussion.

 $\sigma_{opt.}$ for a fixed ζ_2 is obtained graphically by plotting (11) versus σ as shown in Fig. 5 with $\omega_o = \omega_{o,nom.} = 2\pi 50$ rad/s, considering a fixed 50 Hz corner-frequency CNISOGI-QSG. From Fig. 5 it is seen that $\sigma_{opt.} \approx 1.24$ for $\zeta_2 = 0.3$ to $\zeta_2 = 0.9$ and $\omega_o = \omega_{o,nom.}$. The value of $\sigma_{opt.}$ can be found to be close to 1.24 for all ζ_2 in the range $0 < \zeta_2 < 1$. Substituting $\sigma = \sigma_{opt.}$ in (11), the expression of the minimum expected settling time $(t_{s,min})$ for $0 < \zeta_2 < 1$ is obtained as

$$t_{s,min} = \frac{\sigma_{opt.}}{\zeta_2 \ \omega_{o,nom.}} \ln \left[\frac{\zeta_2}{0.01(\sigma_{opt.} - 1)\sqrt{1 - \left(\frac{\zeta_2}{\sigma_{opt.}}\right)^2}} \right].$$
(12)

Table. 2 shows the error between the expected $(t_{s,min})$ and actual $(t_{s,sim})$ settling time for the CNISOGI-QSG when parameters are selected using the proposed design method. The actual settling time matches very closely with the expected value. Also, from Table 1 and Table. 2 it is evident that the proposed method is better than the conventional dominant closed-loop pole approach for parameter selection of the CNISOGI-QSG in terms of predicting the system's response time and achieving a faster settling time.



FIGURE 5. Plot of t_s versus σ for various values of ζ_2 .

TABLE 2. Comparison of expected $(t_{s,min})$ and obtained $(t_{s,sim})$ settling time for the Proposed CNISOGI-QSG using the proposed method of parameter evaluation.

ζ_2	$\sigma_{opt.}$	ζ_1	$t_{s,min}$ (ms)	$t_{s,sim}$ (ms)	Error (ms)
0.9	1.24	0.726	27.6	25.4	2.2
0.8	1.24	0.645	30.0	29.7	0.3
0.7	1.24	0.564	33.1	31.4	1.7
0.6	1.24	0.484	37.2	31.2	6
0.5	1.24	0.403	42.8	39.4	3.4

V. EFFECT OF CORNER-FREQUENCY VARIATION

The proposed mathematical model for the parameter selection of the CNISOGI-QSG is obtained for a fixed cornerfrequency $\omega_o = \omega_{o,nom.} = 2\pi 50$ rad/s. Therefore, (12) can no longer be used to estimate the settling time of the CNISOGI-QSG for a general application where ω_o is different from $2\pi 50$ rad/s.

It can be observed form (11) that the settling time of the CNISOGI-QSG for any corner-frequency ω_o depends on σ for a chosen ζ_2 . Therefore, for $\omega_o \neq 2\pi 50$ rad/s, the expression of minimum expected settling time $(t_{s,min})$ can be obtained by determining the new optimal value for σ corresponding to the new ω_o . Analytically, the new optimal σ ($\sigma'_{opt.}$) can be derived by setting the derivative of (11) w.r.t σ to zero in the interval $1 < \sigma < 5$. We have

$$\frac{dt_s}{d\sigma} = \frac{1}{\zeta_2 \omega_o} \frac{d}{d\sigma} \left[\sigma \ln \left(\frac{\zeta_2}{0.01(\sigma - 1)\sqrt{1 - \left(\frac{\zeta_2}{\sigma}\right)^2}} \right) \right].$$
(13)

Equation (13) can be rewritten as

$$\frac{dt_s}{d\sigma} = \frac{1}{\zeta_2 \omega_o} f(\sigma) \tag{14}$$

where

$$f(\sigma) = \frac{d}{d\sigma} \left[\sigma \ln \left(\frac{\zeta_2}{0.01(\sigma - 1)\sqrt{1 - \left(\frac{\zeta_2}{\sigma}\right)^2}} \right) \right].$$

Equating (14) to zero, we get

$$f(\sigma'_{opt.}) = 0. \tag{15}$$

From (14) and (15) it is observed that the optimum σ is independent of corner-frequency ω_o . So, from (11) and Fig. 5, the generalized expression for the minimum expected settling time $(t_{s,min}^g)$ for $0 < \zeta_2 < 1$ and $1 < \sigma < 5$ can be written as

$$t_{s,min}^{g} = \frac{\sigma_{opt.}}{\zeta_{2}\omega_{o}} \ln \left[\frac{\zeta_{2}}{0.01(\sigma_{opt.} - 1)\sqrt{1 - \left(\frac{\zeta_{2}}{\sigma_{opt.}}\right)^{2}}} \right].$$
(16)

VI. COMPARISON WITH SO-SOGI-QSG [11]

The design principle of SO-SOGI-QSG is introduced briefly in Section I. The transfer-functions describing the system are

$$G_2(s) = \frac{K_1 K_2 \omega_o^2 s^2}{(s^2 + \omega_o^2)(s^2 + K_2 \omega_o s + \omega_o^2) + K_1 K_2 \omega_o^2 s^2}$$
(17)

$$H_2(s) = \frac{K_1 K_2 \omega_o^3 s}{(s^2 + \omega_o^2)(s^2 + K_2 \omega_o s + \omega_o^2) + K_1 K_2 \omega_o^2 s^2}.$$
 (18)

For a SOS with a chosen ζ and settling time t_s , $\omega_n = \frac{4.4}{t_s \zeta}$. Using the same ζ and ω_n values, [11] sets $K_1 = \frac{\omega_n}{\zeta \omega_o}$ and $K_2 = \frac{4\zeta \omega_n}{\omega_o}$. This setting is expected to give SO-SOGI-QSG

the same settling time as the SOS. In effect, the method approximates the fourth-order system to be of lower-order. As a design example in [11], the values of K_1 and K_2 are computed as 1.56 and 3.11 respectively for $\zeta = 0.707$ and $t_s = 18$ ms, assuming $\omega_o = 2\pi 50$ rad/s.

The step response of the in-phase component of the SO-SOGI-QSG with the above values of K_1 and K_2 is plotted in Fig. 6 along with the step response of the in-phase component of the proposed method for an expected settling time of 27.6 ms ($K_1 = 1.452$ and $K_2 = 1.8$). From Fig. 6 it can be observed that the actual settling time for the in-phase component of the SO-SOGI-QSG is around 54 ms against an expected value of 18 ms, however, the settling time (25.4 ms) of the in-phase component of the CNISOGI-QSG is much closer to the expected value (27.6 ms). Fig. 7 shows the same for the quadrature-phase components of the SO-SOGI-QSG and CNISOGI-QSG. Here too, the quadrature-phase of the CNISOGI-QSG settles within 23 ms which is much closer to the expected value of 25.4 ms while the quadrature-phase component of the SO-SOGI-QSG settles at 53.7 ms against an expected settling time of 18 ms.

Fig. 8 and Fig. 9 compare the bode plots of the in- and quadrature-phase components of SO-SOGI-QSG with the CNISOGI-QSG for the aforementioned values of K_1 and K_2 . It is observed from Fig. 8 and Fig. 9 that the CNISOGI-QSG offers higher attenuation to harmonic components when compared to the SO-SOGI-QSG. From Fig. 6, Fig. 7, Fig. 8 and Fig. 9 it is clear that the proposed CNISOGI-QSG is better compared to SO-SOGI-QSG in terms of the dynamics, settling time estimation and harmonic attenuation.



FIGURE 6. Step response comparison of in-phase components of CNISOGI-QSG (K_1 =1.452 and K_2 =1.8), SO-SOGI-QSG (K_1 =1.56 and K_2 =3.11) and CSOGI-QSG (K = 2.66).



FIGURE 7. Step response comparison of quadrature-phase components of CNISOGI-QSG (K_1 =1.452 and K_2 =1.8), SO-SOGI-QSG (K_1 =1.56 and K_2 =3.11) and CSOGI-QSG (K = 2.66).



FIGURE 8. Bode plot comparison of in-phase components of CNISOGI-QSG (K_1 =1.452 and K_2 =1.8), SO-SOGI-QSG (K_1 =1.56 and K_2 =3.11) and CSOGI-QSG (K = 2.66).

VII. COMPARISON WITH CSOGI-QSG [13]

In [13] a fourth-order QSG is proposed by cascading two identical SOGI-QSGs. The transfer-functions of the



FIGURE 9. Bode plot comparison of quadrature-phase components of CNISOGI-QSG (K_1 =1.452 and K_2 =1.8), SO-SOGI-QSG (K_1 =1.56 and K_2 =3.11) and CSOGI-QSG (K = 2.66).

CSOGI-QSG are

$$G_{3}(s) = \left(\frac{K\omega_{o}s}{s^{2} + K\omega_{o}s + \omega_{o}^{2}}\right)^{2}$$
(19)
$$H_{3}(s) = \left(\frac{K\omega_{o}s}{s^{2} + K\omega_{o}s + \omega_{o}^{2}}\right) \left(\frac{K\omega_{o}^{2}}{s^{2} + K\omega_{o}s + \omega_{o}^{2}}\right).$$
(20)

The parameter *K* in (19) and (20) is computed by equating $|G_3(jh\omega_o)| = |G_o(jh\omega_o)|$ where, $|G_o(jh\omega_o)|$ is the magnitude offered to h^{th} -order harmonic component by a single SOGI-QSG ($G_o(s)$) [13]. This results in a higher damping factor for the SOGI-QSG units of the CSOGI-QSG as compared to $G_o(s)$, that is

$$\zeta = \sqrt{h\zeta_o} \tag{21}$$

where $\zeta = \frac{K}{2}$ and $\zeta_o = \frac{K_o}{2}$ are the damping factors of the SOGI-QSGs of the CSOGI-QSG and $G_o(s)$ respectively. ζ_o in (21) is estimated from

$$t_{so} = \frac{4.4}{\zeta_o \omega_o}, \quad \zeta_o < 0 \tag{22}$$

where t_{so} represents the chosen settling time of $G_o(s)$. The settling times of the SOGI-QSGs of the CSOGI-QSG are

$$t_{s1} = t_{s2} = \frac{4.4}{\zeta \omega_o}, \quad \zeta < 0.$$
 (23)

Clearly, from (21), (22) and (23) the SOGI-QSGs of the CSOGI-QSG will have lower settling times than that of $G_o(s)$. The combined effect of cascading on the settling time is not discussed in [13]. Also, a careful choice of ζ_o is required. The use of (21) can lead to $\zeta > 1$ if ζ_o is not selected appropriately for a fixed harmonic-order *h*. This results in higher settling times for the SOGI-QSGs of the CSOGI-QSG when compared to the single SOGI-QSG, negating the basic premise of the design. As an example, for $t_{so} = 18$ ms and $\omega_o = 2\pi 50$,

 ζ_o is calculated as 0.707 using (22). With $\zeta_o = 0.707$ and h = 5, the damping factor of SOGI-QSGs of the cascaded structure is computed to be $\zeta = 1.33$ (K = 2.66) using (21). Step response of the in- and quadrature-phase components of the CSOGI-QSG with the above setting shows a settling time of 44 ms (Fig. 6) and 51.6 ms (Fig. 7) respectively, much higher than the settling time of the individual SOGI-QSG ($G_o(s)$). An appropriate range of ζ_o for a chosen value of h is not considered in [13]. Also, for K = 2.66, the harmonic attenuation offered by the in- and quadrature-phase components of the CSOGI-QSG are lower than the in- and quadrature-phase components of the CNISOGI-QSG with $K_1 = 1.452$ and $K_2 = 1.8$. Clearly, from Fig. 6, Fig. 7, Fig. 8, Fig. 9 and above discussion, the CNISOGI-QSG is superior than the CSOGI-OSG for a correct settling time estimation along with a sufficiently higher harmonic attenuation.

VIII. QUANTITATIVE COMPARISON OF VARIOUS QSGs

Table. 3 presents a quantitative comparison of the proposed CNISOGI-QSG with the various QSGs [7]–[13]. To have a fair comparison, the system parameter (*K* for [7]–[10] and K_1 for [11], [13] and proposed CNISOGI-QSG) is considered as 1.414. The comparison in Table. 3 is based on the settling time and THD of the in-phase [v'(t)] and quadrature-phase [qv'(t)] components of the QSGs. The settling times are obtained by applying a step input while the THD values are obtained by applying a harmonic distorted voltage described in (24). The total harmonic distortion (THD) in the input voltage is 17.32%. Due to higher filtering ability, a fourth-order QSG may be slower than lower-order QSGs. Therefore, along with the settling time, it is important to consider the THD of the outputs as an important factor for comparing the performance of fourth-order QSGs with lower-order ones.

From Table. 3, it is clear that the proposed QSG shows superior performance in terms of settling time, percentage THD and a correct estimation of system settling time when compared to other QSGs.

IX. EXPERIMENTAL RESULTS

Experimental results are conducted on a digital signal processor (DSP) platform built around the processor TMS320F2812. The QSGs are implemented in the DSP using trapezoidal method of discretization with the computations done every 100 μs , corresponding to a sampling frequency of 10 kHz.

A. DYNAMIC PERFORMANCE COMPARISON

Fig. 10 and Fig. 11 compare the dynamic performance of the CNISOGI-QSG ($K_1 = 1.452$ and $K_2 = 1.8$) with SO-SOGI-QSG ($K_1 = 1.56$ and $K_2 = 3.11$) and CSOGI-QSG (K = 2.66). Fig. 10 shows the dynamic response of the in-phase component [v'(t)] for the QSGs to a unit step input, whereas, Fig. 11 considers the dynamic response of the output space-vector [$v'_s(t) = \sqrt{(v'(t))^2 + (qv'(t))^2}$] of the QSGs to a sinusoidal input of frequency 50 Hz (2π 50 rad/s) which experiences a step change in magnitude from 0.5 p.u to 1 p.u

Method	t_s (ms) [expected]	Parameter	$t_{s,v'(t)}$ (ms) [obtained]	$\begin{array}{c}t_{s,qv'(t)} \text{ (ms)}\\ \text{[obtained]}\end{array}$	$\begin{array}{c} THD_{v'(t)} \\ (\%) \end{array}$	$\begin{array}{c} THD_{qv'(t)} \\ (\%) \end{array}$
SOGI-QSG [7]	20	K = 1.414	21	24	3.7	0.65
SOGI-QSG + LPF [8]	20	$K=1.414, \omega_{LPF}=2\pi 10$ rad/s	21	72	3.7	0.98
MSTOGI-QSG [9]	20	K = 1.414	21	20	3.7	3.71
Third-order SOGI-QSG [10]	*	$K = 1.414, K_{dc} = 0.22$	39	41	3.67	0.64
Novel two-phase generator [12]	*	$K_i = 85.313$	27	26	2.64	0.46
SO-SOGI-QSG [11]	20	$K_1 = 1.414, K_2 = 2.827$	51	49	1.94	0.36
CSOGI-QSG [13]	*	K = 1.414	30	30	0.94	0.18
Proposed CNISOGI-QSG	28	$K1 = 1.414, K_2 = 1.753$	25	28	1.11	0.21

TABLE 3. A quantitative comparison of the proposed CNISOGI-QSG with existing QSGs [7]–[13]. Except [7] all the other QSGs are capable of dc-offset elimination.

* Settling time equation for the QSGs are not proposed in [10], [12], [13].



FIGURE 10. Hardware result comparing the step response of v'(t) of the CNISOGI-QSG (K_1 =1.452 and K_2 =1.8), SO-SOGI-QSG (K_1 =1.56 and K_2 =3.11) and CSOGI-QSG (K = 2.66) to a unit step input. X-axis: 10 ms/div and Y-axis: 0.2 p.u/div.



FIGURE 11. Dynamic response comparison of $v'_{s}(t)$ of the CNISOGI-QSG (K_1 =1.452 and K_2 =1.8), SO-SOGI-QSG (K_1 =1.56 and K_2 =3.11) and CSOGI-QSG (K = 2.66) to a sinusoidal voltage with a step change. X-axis: 10 ms/div and Y-axis: 0.2 p.u/div for $v'_{s}(t)$ and 0.5 p.u/div for v(t).

at 20 ms. Since the settling time of the in-phase components of the QSGs are closer to the settling time of the quadraturephase components, the in-phase components alone are shown in the experimental results. It is observed from Fig. 10 and Fig. 11 that the settling time of the CNISOGI-QSG is around 25 ms and is close to the estimated value of 27.6 ms. Whereas, the settling time of the SO-SOGI-QSG is observed as 54 ms while [11] estimates the same to be 18 ms for the above settings. The settling time of the CSOGI-QSG is observed as 44 ms.

B. STEADY-STATE PERFORMANCE COMPARISON

A harmonic distorted single-phase input is considered for comparing the sinusoidal steady-state performance of the CNISOGI-QSG with SO-SOGI-QSG and CSOGI-QSG as discussed in Section IX-A. The input voltage in per-unit is given by

$$v(t) = 0.1 + 1.0\sin(\omega_o t) + 0.1\sin(5\omega_o t) + 0.1\sin(7\omega_o t) + 0.1\sin(11\omega_o t)$$
(24)

where $\omega_o = 2\pi 50$ rad/s. The THD in v(t) is 17.32%.



FIGURE 12. Steady-state sinusoidal response of in-phase component [v'(t)] of the CNISOGI-QSG (K_1 =1.452 and K_2 =1.8), SO-SOGI-QSG (K_1 =1.56 and K_2 =3.11) and CSOGI-QSG (K = 2.66) to a non-ideal input voltage [v(t)]. X-axis: 10 ms/div and Y-axis: 0.2 p.u/div.

The input voltage [v(t)] and steady-state in-phase output voltage [v'(t)] of the QSGs are shown in Fig. 12. In fourthorder QSGs, a comparison of the bode plots would indicate that the in-phase component offers lower attenuation to harmonics when compared to the quadrature-phase component. So, Fig. 9 considers the in-phase output voltage alone for analyzing the steady-state performance of the QSGs. In this manner, the worst-case harmonic elimination ability of the QSGs can be assessed. It is observed from Fig. 12 that the harmonics are well attenuated at the outputs. A simulation result shows that the THD in v'(t) and qv'(t) for (i) CNISOGI-QSG is 1.16% and 0.22% (ii) SO-SOGI-QSG is 2.34% and 0.44% and (iii) CSOGI-QSG is 2.75% and 0.51% respectively. From the above discussion and Section IX-A, it is clear that the CNISOGI-QSG with the proposed method of parameter selection shows superior dynamicand steady-state performance in terms of settling time and percentage THD.



FIGURE 13. Block diagram of frequency-fixed dual FO-QSG (FFDFO-QSG) + PSC based three-phase SRF-PLL.

X. FREQUENCY-FIXED DUAL FO-QSG BASED THREE-PHASE SRF-PLL

A frequency-fixed dual FO-QSG (FFDFO-QSG) + PSC based three-phase SRF-PLL (FFDFO-OSG SRF-PLL) is implemented by replacing the QSGs of Fig. 1 with fixed corner-frequency ($\omega_o = 2\pi 50 \text{ rad/s}$) CNISOGI-QSGs as shown in Fig. 13. For performance comparison of the CNISOGI-QSG based FFDFO-QSG SRF-PLL, a SO-SOGI-QSG and CSOGI-QSG based FFDFO-QSG SRF-PLL were also implemented in the DSP. It is shown in [15] that a frequency-fixed SOGI-QSG based SRF PLL (FFSOGI-QSG SRF-PLL) is superior when compared to frequency-adaptive SOGI-QSG SRF-PLL [18] in terms of system stability. Higher stability in FFSOGI-QSG SRF-PLL is due to the decoupling between the QSG and SRF-PLL. The decoupled nature of QSGs allows for higher bandwidth/faster response for the SRF-PLL [15]. Also, due to decoupling, the settling time of the QSGs are unaffected by the PLL dynamics.

A FFSOGI-QSG SRF-PLL requires additional compensator ($C(\theta)$) for correcting the error in tracked phase angle (θ') when the grid frequency (ω_{in}) is different from the SOGI-QSG corner-frequency (ω_o) [15]. Similar compensators are employed for the CNISOGI-QSG and SO-SOGI-QSG based FFDFO-QSG SRF-PLLs too, following the design principle outlined in [15]. Since the frequency of the grid voltage (ω_{in}) is unaffected by the QSG during the steady state, the tracked frequency of the FFDFO-QSG SRF-PLL (ω_{PLL}) remains same as ω_{in} in the steady-state. The PI controller gains of the CNISOGI-QSG, SO-SOGI-QSG and CSOGI-QSG based FFDFO-QSG SRF-PLLs are calculated as $K_p = 2.546$ p.u and $K_i = 1019$ p.u for achieving a settling time of 10 ms with $\zeta = 0.707$ for the PLL($V_{base} = V_m$ and $\omega_{base} = \omega_o = 2\pi 50$ rad/s).

Fig. 14 is considered to demonstrate the phase tracking capability of a FFDFO-QSG SRF-PLL while ω_{in} is different from the QSG corner-frequency ($\omega_o = 2\pi 50 \text{ rad/s}$). The phase tracking is shown only for the CNISOGI-QSG based FFDFO-QSG SRF-PLL. The grid frequency (ω_{in}) is changed from $2\pi 50 \text{ rad/s}$ (50 Hz) to $2\pi 55 \text{ rad/s}$ (55 Hz) at 30 ms. It is observed that the FFDFO-QSG SRF-PLL tracks the



FIGURE 14. Phase tracking of the CNISOGI-QSG (K_1 =1.452 and K_2 =1.8) based FFDFO-QSG SRF-PLL for a step change in the input frequency. X-axis: 10 ms/div and Y-axis: 0.5 p.u/div.



FIGURE 15. Three-phase input voltage for testing the dynamic behaviour of the CNISOGI-QSG and SO-SOGI-QSG based FFDFO-QSG + PSC structure. X-axis: 10 ms/div and Y-axis: 0.5 p.u/div.



FIGURE 16. Dynamic response of the CNISOGI-QSG based FFDFO-QSG + PSC structure with K_1 =1.452 and K_2 =1.8 to the input of Fig. 15. X-axis: 10 ms/div and Y-axis: 0.5 p.u/div.

phase angle with zero error $[\theta_{in} - \theta_{PLL}]$ despite ω_{in} being different from the QSG corner-frequency. Ideal three-phase grid voltages are considered as input for Fig. 14 to strictly focus on the phase tracking capability. Similar results are expected under non-ideal grid scenario also.

Fig. 16 shows the dynamic behaviour of the CNISOGI-QSG based FFDFO-QSG + PSC structure in generating the positive sequence $\alpha - \beta$ components $[v_{\alpha}^+(t), v_{\beta}^+(t)]$. Fig. 17 and Fig. 18 show the same for the SO-SOGI-QSG and CSOGI-QSG based FFDFO-QSG + PSC structures. The parameters of CNISOGI-QSGs, SO-SOGI-QSGs and CSOGI-QSG are the same as in Section. IX-A. The input for Fig. 16, Fig. 17 and Fig. 18 is shown in Fig.15. The three-phase input voltages in Fig.15 considers a 30% negative sequence component with 10% 5th-, 7th- and 11th-order harmonics in each phases. Also, a dc-offset of 10%, 20% and 30% are added in $v_a(t)$, $v_b(t)$ and $v_c(t)$ respectively. All the percentages are expressed w.r.t the fundamental positive sequence voltage component. The fundamental positive



FIGURE 17. Dynamic response of the SO-SOGI-QSG based FFDFO-QSG + PSC structure with K_1 =1.56 and K_2 =3.11 to the input of Fig. 15. X-axis: 10 ms/div and Y-axis: 0.5 p.u/div.



FIGURE 18. Dynamic response of the CSOGI-QSG based FFDFO-QSG + PSC structure with K=2.66 to the input of Fig. 15. X-axis: 10 ms/div and Y-axis: 0.5 p.u/div.



FIGURE 19. Frequency tracking of the CNISOGI-QSG (K_1 =1.452 and K_2 =1.8) based FFDFO-QSG SRF-PLL. $\omega_o = 2\pi 50$ rad/s. X-axis: 10 ms/div and Y-axis: 0.1 p.u/div.



FIGURE 20. Frequency tracking of the SO-SOGI-QSG (K_1 =1.56 and K_2 =3.11) based FFDFO-QSG SRF-PLL. $\omega_0 = 2\pi$ 50 rad/s. X-axis: 10 ms/div and Y-axis: 0.1 p.u/div.

sequence space-vector experiences a 50% dip in magnitude at 40 ms. It is observed that the CNISOGI-QSG based FFDFO-QSG + PSC structure tracks the change in input within 22 ms (Fig. 16) whereas, the SO-SOGI-QSG and CSOGI-QSG based FFDFO-QSG + PSC structure take around 45 ms (Fig. 17) and 30 ms (Fig. 18) respectively for the same.



FIGURE 21. Frequency tracking of the CSOGI-QSG based FFDFO-QSG SRF-PLL with system parameter K=2.66. $\omega_0 = 2\pi 50$ rad/s. X-axis: 10 ms/div and Y-axis: 0.1 p.u/div.

Fig. 19 to Fig. 21 considers the frequency tracking capability of the CNISOGI-QSG, SO-SOGI-QSG and CSOGI-QSG based FFDFO-QSG SRF-PLL respectively. The parameters of the QSGs are same as discussed above. The grid frequency (ω_{in}) in Fig. 19, Fig. 20 and Fig. 21 experiences a step change from 2π 50 rad/s (50 Hz) to 2π 52 rad/s (52 Hz) at 20 ms. The CNISOGI-QSG based FFDFO-QSG SRF-PLL tracks the change in ω_{in} within 26 ms (Fig. 19) while the SO-SOGI-QSG and CSOGI-QSG based FFDFO-QSG SRF-PLL take a relatively longer time of 50 ms (Fig. 20) and 42 ms (to Fig. 21) respectively. Ideal three-phase grid voltages are considered for Fig. 19, Fig. 20 and Fig. 21 to strictly focus on the dynamic frequency tracking ability of the PLLs. Similar results are expected under non-ideal grid scenario also.

XI. CONCLUSION

A fourth-order QSG, cascading two non-identical SOGI-QSGs is proposed. A novel method of parameter selection based on settling time is developed by identifying and utilising the slower envelop around the 2% settling time limit. This approach allows for lesser separation between the poles of the fourth-order transfer function and helps achieve a faster overall response. The proposed method is analysed for the effect of variation in corner frequency. A brief comparison with existing methods are provided. The proposed parameter selection approach allows the QSG to achieve lower setting times when compared to the existing fourth-order QSGs. The proposed method shows a faster response of 25.4 ms settling time. For a sample input voltage with a THD of 17.32%, the THD in the output voltages (v' and qv') are shown to be 1.16% and 0.22% respectively. The proposed method is useful in frequency-fixed QSG based single- and three-phase PLLs under non-ideal grid voltage conditions.

REFERENCES

- L. Shi and M. L. Crow, "A novel phase-locked-loop and its application in STATCOM system," in *Proc. North Amer. Power Symp.*, Arlington, TX, USA, Sep. 2010, pp. 1–5.
- [2] S.-K. Chung, "A phase tracking system for three phase utility interface inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 3, pp. 431–438, May 2000, doi: 10.1109/63.844502.
- [3] V. Kaura and V. Blasko, "Operation of a phase locked loop system under distorted utility conditions," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 58–63, Jan./Feb. 1997, doi: 10.1109/28.567077.
- [4] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich, "Decoupled double synchronous reference frame PLL for power converters control," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 584–592, Mar. 2007, doi: 10.1109/TPEL.2006.890000.

- [5] A. Ghoshal and V. John, "A method to improve PLL performance under abnormal grid conditions," in *Proc. NPEC*, 2007, pp. 17–19.
- [6] P. Rodriguez, R. Teodorescu, I. Candela, A. V. Timbus, M. Liserre, and F. Blaabjerg, "New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions," in *Proc. 37th IEEE Power Electron. Spec. Conf.*, Jeju, South Korea, Jun. 2006, pp. 1–7.
- [7] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase PLL structure based on second order generalized integrator," in *Proc. 37th IEEE Power Electron. Spec. Conf.*, Jeju, South Korea, Jun. 2006, pp. 1–6.
- [8] M. Ciobotaru, R. Teodorescu, and V. G. Agelidis, "Offset rejection for PLL based synchronization in grid-connected converters," in *Proc. 23rd Annu. IEEE Appl. Power Electron. Conf. Expo.*, Austin, TX, USA, Feb. 2008, pp. 1611–1617.
- [9] C. Zhang, X. Zhao, X. Wang, X. Chai, Z. Zhang, and X. Guo, "A grid synchronization PLL method based on mixed second- and third-order generalized integrator for DC offset elimination and frequency adaptability," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1517–1526, Sep. 2018, doi: 10.1109/JESTPE.2018.2810499.
- [10] J. Li, J. Zhao, J. Wu, and P.-P. Xu, "Improved dual second-order generalized integrator PLL for grid synchronization under non-ideal grid voltages including DC offset," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Pittsburgh, PA, USA, Sep. 2014, pp. 136–141.
- [11] Z. Xin, X. Wang, Z. Qin, M. Lu, P. C. Loh, and F. Blaabjerg, "An improved second-order generalized integrator based quadrature signal generator," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8068–8073, Dec. 2016, doi: 10.1109/TPEL.2016.2576644.
- [12] S. Lubura, M. Šoja, S.-A. Lale, and M. Ikic, "Single-phase phase locked loop with DC offset and noise rejection for photovoltaic inverters," *IEE Power Electron.*, vol. 7, no. 9, pp. 2288–2299, Sep. 2014, doi: 10.1049/iet-pel.2013.0413.
- [13] J. Matas, M. Castilla, J. Miret, L. G. de Vicuna, and R. Guzman, "An adaptive prefiltering method to improve the speed/accuracy tradeoff of voltage sequence detection methods under adverse grid conditions," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2139–2151, May 2014, doi: 10.1109/TIE.2013.2274414.
- [14] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Three-phase PLLs: A review of recent advances," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1894–1907, Mar. 2017, doi: 10.1109/TPEL.2016.2565642.
- [15] F. Xiao, L. Dong, L. Li, and X. Liao, "A frequency-fixed SOGIbased PLL for single-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1713–1719, Mar. 2017, doi: 10.1109/TPEL.2016.2606623.
- [16] A. A. Nazib, D. G. Holmes, and B. P. McGrath, "Decoupled DSOGI-PLL for improved three phase grid synchronisation," in *Proc. Int. Power Electron. Conf. (IPEC-Niigata -ECCE Asia)*, Niigata, Japan, May 2018, pp. 3670–3677.

- [17] K. Ogata, Modern Control Engineering, vol. 3, 5th ed. London, U.K.: Pearson, 2015, pp. 189–192.
- [18] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Dynamics assessment of advanced single-phase PLL structures," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2167–2177, Jun. 2013, doi: 10.1109/TIE.2012.2193863.



BISHAL MONDAL received the B.Tech. degree in electrical and electronics engineering from NIT, Puducherry, India, in 2014. He is currently pursuing the M.S. + Ph.D. degree in electrical engineering with IIT Madras, Chennai, Tamil Nadu, India.

His research interests include single- and three-phase PLLs under non-ideal grid voltage conditions, LCL filter using passive damping techniques, and design/control of grid-tie converters.



B. ARUN KARUPPASWAMY (Member, IEEE) received the B.E. degree in electrical and electronics engineering from CEG, Anna University, Chennai, in 2003, the M.Tech. degree in power electronics from NIT, Calicut, in 2007, and the Ph.D. degree in electrical engineering from IISc, Bangalore, in 2015, all from India.

From 2014 to 2016, he was a Senior Engineer at Design with Bloom Energy India Pvt. Ltd. Since 2016, he has been an Assistant Professor of elec-

trical engineering with IIT Madras, India. His research interests include grid-connected inverters, wireless charging of electric vehicles, and power electronics in general. He works closely with the industries in India.