

Received January 19, 2022, accepted March 28, 2022, date of publication April 5, 2022, date of current version April 13, 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3165033

Wideband, Millimeter Wave Domain SI Canceling (> 50 dB) In-Band Full-Duplex Circulator Receiver

ROBIN GARG^{ID}, (Member, IEEE), SANKET JAIN^{ID}, (Member, IEEE),
AND ARUN S. NATARAJAN, (Member, IEEE)

School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR 97330, USA

Corresponding author: Robin Garg (robingarg388@gmail.com)

This work was supported in part by the U.S. Defense Advanced Research Projects Agency (DARPA) Young Faculty Award (YFA) Program.

ABSTRACT This paper describes a 26-GHz fully integrated In-band Full-duplex Circulator (IBFD) Receiver (RX), which employs passive and active Self-interference Cancellation (SIC) techniques in the mm-wave domain. Coverage of wireless networks at mm-wave frequencies can be enhanced by deploying a large number of base stations economically based on Integrated Access and Backhaul (IAB) relays and repeaters. However, to retain the channel capacity, IAB needs to be implemented using full-duplex schemes that suffer from a strong Transmitter (TX) to RX SI. This SI leakage can significantly impact the receiver sensitivity and increase the baseband/ADC dynamic range requirements. Canceling SI at mm-wave applications is particularly challenging given the high frequency of operation, wide bandwidth, and antenna (ANT) impedance sensitivity to the surroundings. Proposed mm-wave RX with a shared ANT interface based on a circulator with active SI cancelers provide ~53 dB SIC over 400 MHz and ~40 dB SIC over 400 MHz in mm-wave domain to meet the link budget requirements. Proposed architecture achieves SIC by (i) introducing a shared ANT interface based on a hybrid-coupler and a non-reciprocal delay line that provides wideband SIC and additionally creates a SI replica (ii) subsequent active cancellation using SI replica processed with variable gain amplifiers and phase shifters. This system also accommodates SI channel variations due to surroundings. Proposed 26-GHz circulator RX has >100x better SIC at high TX power (>10 dBm) levels in comparison to the state-of-the-art and it consumes ~111 mW power. The system is implemented in 45nm SOI CMOS and has an active area of 4.54 mm². Stand-alone RX NF is ~5.8 dB and TX to ANT insertion loss (IL) is ~3.1 dB. Over-the-air measurements with modulated TX (128 QAM 2.1 Gb/s) and RX (128 QAM 4.2 Gb/s) signals show an EVM of 3.3%.

INDEX TERMS Circulators, integrated access and backhaul, full-duplex receiver, self-interference cancellation, shared antenna interface, 5G-NR.

I. INTRODUCTION

Millimeter-wave frequency bands with wide spectrum allocations promise multi-Gb/s wireless data rates targeted in 5G and beyond. However, higher propagation-loss and shadowing at mm-wave limits coverage [1]–[4]. Therefore, achieving ubiquitous mm-wave coverage requires the deployment of a large number of base stations economically with wireless backhauling [2], [5]–[9]. Potentially, combining base-stations with repeater/relay nodes with spectrum reuse can provide efficient increase in coverage and wireless backhaul, makes network densification economically viable [10]–[13] (Fig. 1).

The associate editor coordinating the review of this manuscript and approving it for publication was Wenjie Feng.

Integrated mm-wave relays/repeaters can be implemented based on half-duplex (HD), or full-duplex (FD) links, as shown in Fig. 2(a). HD links based on time-division duplexing (TDD), frequency-division duplexing (FDD) or spatial/polarization duplexing minimize transmitter (TX) to receiver (RX) self-interference by separating them in time, frequency, or spatial/polarization domains, resulting in trade-offs between network capacity and interference. In-band full-duplex circulator (IBFD) links, provide superior channel capacity through spectrum reuse. However, IBFD links have to handle strong TX to RX self-interference (SI) as shown in Fig. 2(b) and therefore require self-interference cancellation (SIC) > 100 dB [11], [12], [14], [15].

SI leakage in IBFD systems from TX to RX path occurs through direct coupling and/or antenna reflections and such

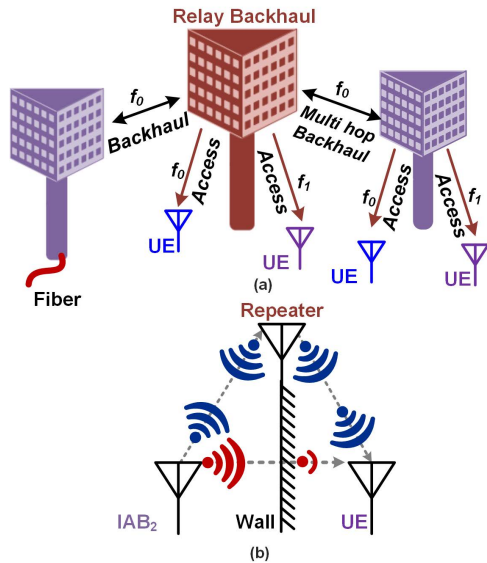


FIGURE 1. Simultaneous transmit and receive for repeaters in mm-wave links.

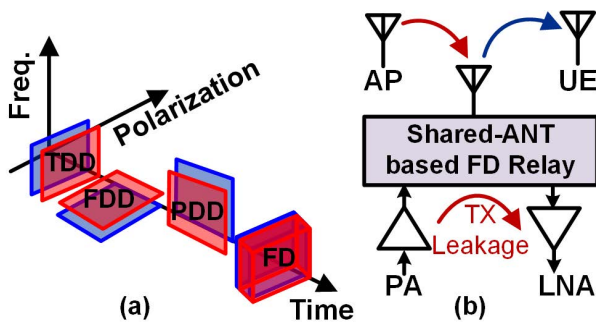


FIGURE 2. (a) Time/Frequency/Spatial spectrum of mm-wave half-duplex and full-duplex links (b) TX to ANT leakage associated with shared antenna interface-based FD links.

in-band SI cannot be filtered frequency-selective frontend filters. However, SI suppression is necessary to prevent saturation in the RX front-end and reduce required ADC dynamic range. An example of SIC required from a mm-wave RX with TX power, P_{TX} , RX noise figure (NF) of 10 dB over 800 MHz instantaneous bandwidth, BW and assuming $SNR_{min} = 20\text{ dB}$, is given by (1),

$$SIC_{reqd.} > 174 - 10\log_{10}(BW) - NF + SNR + P_{TX}$$

$$SIC_{reqd.} > P_{TX} + 95 \tag{1}$$

The high SIC requirement requires distribution of SI suppression across RF, IF and baseband domains along the RX chain [12], [14], [16]–[20]. Digital and baseband cancellation techniques have demonstrated 66 dB suppression of the leakage [20], [21], and hence mm-wave front-end should be able to provide additional ~40 dB suppression over 800 MHz bandwidth.

Several SIC architectures have been proposed in prior work to enable simultaneous transmit and receive (STAR)

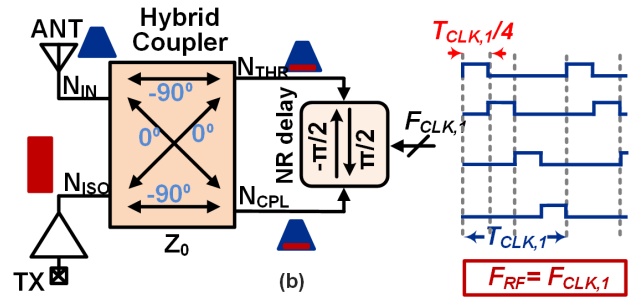


FIGURE 3. Prior art: Full-duplex circulator RX based on hybrid coupler requiring non-overlapping clocks.

at RF and mm-wave. STAR operation with non-reciprocal on-chip circulators using N-path mixers were proposed at RF frequencies in [22] with subsequent works focused on increasing bandwidth, increased power handling and MIMO operation [14], [19], [20], [23]–[25]. Shared-antenna interfaces based on electrical-balance duplexers (EBD) have also been demonstrated at RF in [18], [26]–[30]. However, applying such SIC techniques at mm-wave with shared ANT interface is particularly challenging due to the high operation frequency. Polarization-based cancellation techniques have been demonstrated for mm-wave STAR with multiple feed networks and/or multiple antennas [16], [31], [32].

An FD RX architecture with N-path mixers interfaced to a 90°-hybrid coupler was proposed in [19]. This architecture (Fig. 3) had > 40 dB TX to RX baseband cancellation, but does not scale well to higher operating frequency as non-overlapping clocks with a duty cycle of 100%/N are required for the N-path mixer.

A three-port wideband mm-wave IBFD circulator is proposed in [33], [34] based on non-reciprocal delays. These circulators utilize 50% duty cycle quadrature clocks to drive non-reciprocal T-lines or bandpass filters instead of capacitors used in [19], [20], thus ensuring wideband functionality. Non-reciprocity is analytically derived in [33] for all clock signals that are odd sub-harmonics of the mm-wave/RF input signal driving the non-reciprocal delay. This property enables this architecture to be applied for mm-wave IBFD using sub-harmonic clock signals. While these IBFD circulators provide low TX-to-ANT IL and wideband SIC, SIC achieved for small signal operation is limited to ~20 dB at 28 GHz [33] and 40 dB (22 dB at +10 dBm TX SI power) at 60 GHz [34], respectively. Typically, >40 dB SIC at mm-wave is required to meet the link budget at high P_{TX} as shown in 1, and a single stage cancellation is insufficient for targeted SIC.

In this work, we propose a fully integrated full-duplex circulator RX with wideband ‘passive’ and ‘active’ SIC techniques in mm-wave domain. SI is first canceled ‘passively’ with a shared ANT interface based on 90° hybrid coupler followed by a non-reciprocal transmission line (NTL) delay. Subsequently, ‘active’ cancellation is achieved by creating a faithful replica of TX and aligning it with the leakage using

programmable pseudo-differential phase shifter and variable gain amplifier (VGA). Multi-stage cancellation facilitates high SI suppression in bands of interest and the system provides integrated SIC of 40 dB over 800 MHz and 50 dB over 400 MHz instantaneous bandwidth for high $P_{TX} > 10$ dBm. Similar to the approach in [33], the proposed architecture scales well to higher frequencies since the clock frequency required is F_{RF}/N , where F_{RF} is the input RX frequency, and N is an odd integer.

This manuscript expands on [35] to detail the motivation, analysis, system implementation and additional measurements. Prior art is discussed elaborately to place the presented work in perspective of current state-of-the-art. Subsequently, detailed analysis is presented to explain the working principle. Additional sub-block level implementation details are also discussed. Further, measurements in the presence of realistic EM environment are added to demonstrate the efficacy of this work. The organization of the manuscript is as follows. Literature and state-of-art IBFD systems based on shared ANT interface along with their challenges at mm-wave frequencies are discussed in Sec. I. The proposed 26-GHz IBFD circulator RX architectural analysis is then presented in Sec. II along with conceptual insights. Sec. III details system implementation in 45nm SOI and the device level architectures of various building blocks of the circulator RX. Measured results are presented in Sec. IV followed by conclusion and future research in Sec. V.

II. PROPOSED MM-WAVE IBFD CIRCULATOR RECEIVER

In this section, the proposed mm-wave SI canceling IBFD circulator-RX capable of providing wideband SIC with high TX power handling, is presented. The section also details approaches that can provide higher SIC utilizing additional avenues for further SI suppression. The proposed architecture is shown in Fig. 4, where, a ‘passive’ SI canceler is followed by an ‘active’ one. The following sub-sections present the theoretical analysis of these cancelers.

A. PASSIVE SI CANCELER

Passive SIC is achieved by employing a cascade of two differential quadrature hybrid couplers along with a NTL-based delay proposed in [33]. The working principle of NTL delay and detailed analysis has already been elaborately covered in [33]. In the proposed system, the NTL is driven with a clock frequency of $F_{RF}/5$ with 50% duty cycle.

Detailed mechanism for supporting simultaneous transmission of the TX through the *shared* ANT port while receiving the signal incident at ANT port is shown in Fig. 5 and Fig. 6. The TX signal is applied to the isolated port, and ANT is attached to the input port of the hybrid coupler (HC1). Under the assumption of matched input and isolated ports and balanced termination at through and coupled ports, the voltages at N_{THR1} and N_{CPL1} can be written as;

$$V_{CPL1,RX} = (1 + \Gamma_{R,RX})(0.7 \times V_{IN}) \quad (2)$$

$$V_{THR1,RX} = (1 + \Gamma_{R,RX})(-0.7j \times V_{IN}) \quad (3)$$

$$V_{CPL1,TX} = (1 + \Gamma_{R,TX})(-0.7j \times V_{ISO}) \quad (4)$$

$$V_{THR1,TX} = (1 + \Gamma_{R,TX})(0.7 \times V_{ISO}), \quad (5)$$

where, $\Gamma_{R,TX}$ and $\Gamma_{R,RX}$ are reflection coefficients for TX and RX signals at balanced ports, N_{THR1} and N_{CPL1} . In the following discussion, it will be shown that different $\Gamma_{R,TX}$ and $\Gamma_{R,RX}$ can be achieved through different loading at N_{THR1} and N_{CPL1} with respect to signals incident at N_{IN} and N_{ISO} .

Quadrature relationship between N_{THR1} and N_{CPL1} can be established from (2)-(5) as long as ports are balanced, irrespective of the absolute termination magnitude/phase. Hence, the presence of a NTL delay line does not disrupt this quadrature phase relation at the N_{THR1} and N_{CPL1} . Furthermore, the NTL delay can be described using the following S-parameters (from [33]):

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0 & e^{j\frac{\pi}{2}} \\ e^{-j\frac{\pi}{2}} & 0 \end{bmatrix} \quad (6)$$

The presence of NTL delay leads to $V_{CPL1,TX}$ combining with $jV_{THR1,TX}$ at N_{CPL1} and $V_{THR1,TX}$ combines with $-jV_{CPL1,TX}$ at N_{THR1} (6). From (4-6), the combined signals at N_{CPL1} and N_{THR1} observe nulling ($V_{THR1,TX,EFF} = 0$ and $V_{CPL1,TX,EFF} = 0$) of strong undesired TX signal from PA incident on the isolated port. Nulling of the TX signal creates an effective ‘short’ across N_{CPL1} and N_{THR1} , which leads to reflection of the TX signal to input/ANT port. Consequently, the PA output is transmitted through antenna.

Fig. 6 shows the signal-path phase of RX signals incident on the antenna. The RX signal analysis is similar to the TX, but with the important difference that RX signals from ANT port arrive at N_{THR1} and N_{CPL1} with phase shifts of $-\frac{\pi}{2}$ and 0, respectively. This leads to constructive addition for the RX signals, which is equivalent to an ‘open’ circuit (in the absence of HC2). The RX signal, is hence available at N_{THR1} and N_{CPL1} for further amplification.

In the following, non-idealities will be taken into consideration and the proposed scheme for further SIC to address these non-idealities will be discussed. The discussion of TX leakage cancellation so far has assumed ideal NTL delay, infinite quality factors and ideal switches. In practice, TX nulling is finite and limited by the parasitic capacitance, and resistance, which leads to TX leakage residue at N_{CPL1} and N_{THR1} . While the cancellation depth of the leakage depends on the parasitics, TX residue phase $\Delta(\Phi_{THR1,EFF} - \Phi_{CPL1,EFF})$ is independent of parasitics as long as N_{CPL1} and N_{THR1} have balanced loading.

Assuming residual TX leakage at N_{CPL1} and N_{THR1} to be $\delta V_{CPL1,TX}$ and $\delta V_{THR1,TX}$ respectively, these can be described as;

$$\delta V_{CPL1,TX} = \epsilon_{1,TX} \times e^{-j\frac{\pi}{2}} \quad (7)$$

$$\delta V_{THR1,TX} = \epsilon_{1,TX} \quad (8)$$

where, $\epsilon_{1,TX}$ is the magnitude of the residual TX leakage. Quadrature relationship between $\delta V_{CPL1,TX}$ and $\delta V_{THR1,TX}$, allows the addition of a residual 90° hybrid coupler (HC2) at N_{CPL1} and N_{THR1} to provide further suppression of the

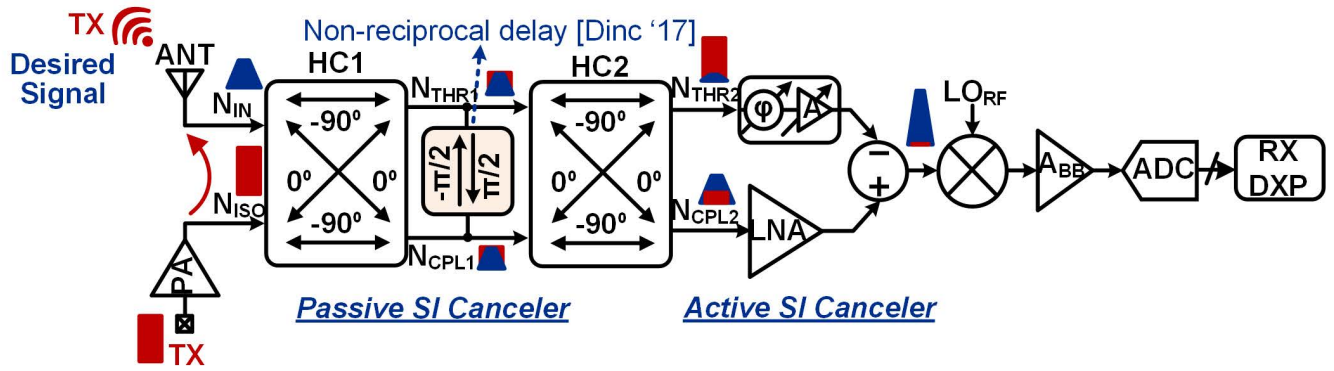


FIGURE 4. Proposed architecture of 26-GHz IBFD circulator RX capable of providing wideband self-interference cancellation for high TX power.

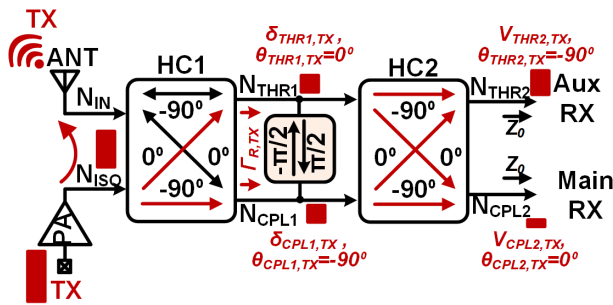


FIGURE 5. Phase progression for the TX leakage through the shared ANT interface to the auxiliary and main RX.

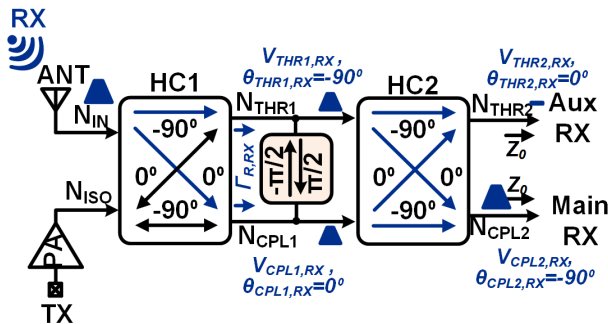


FIGURE 6. Phase progression for signal incident on the ANT port through the shared ANT interface.

residual TX leakage. Further suppression of the residue is possible because RX and residual TX signals have different relative phase shift between N_{CPL1} and N_{THR1} equal to $+\frac{\pi}{2}$ and $-\frac{\pi}{2}$ respectively. The addition of a hybrid coupler does change the ‘open’ across N_{CPL1} and N_{THR1} to 50Ω for the RX, but quadrature phase relationship still holds. This can also be ascertained from (4-5) where balanced loads at CPL and THR ports ensure same reflection coefficient (Γ) at these ports, leading to quadrature phase relationship irrespective of exact value of Γ .

The residual TX leakage is further canceled by the residual hybrid coupler (HC2) on N_{CPL2} because of destructive

addition of phase-shifted $\delta V_{CPL1,TX}$ and $\delta V_{THR1,TX}$. Additionally, residual TX adds constructively at N_{THR2} as shown in (9) and (10).

$$V_{CPL2,TX} = 0 \quad (9)$$

$$V_{THR2,TX} = -2 \times 0.7j \times \epsilon_{1,TX} \quad (10)$$

Similar analysis can be performed for the desired RX signal incident on the ANT port. RX and residual TX signals have relative phase shift between N_{CPL1} and N_{THR1} equal to $+\frac{\pi}{2}$ and $-\frac{\pi}{2}$, respectively, and this leads to RX cancellation at N_{THR2} and RX constructive addition at N_{CPL2} . Availability of stronger residual TX opens up another avenue for further SIC in the RF domain considering there is enough isolation between TX signals at Main and Aux nodes (Fig. 6). Isolation of TX residue between N_{CPL2} and N_{THR2} is desired if any active auxiliary path is to be used for further cancellation.

The ‘passive’ SIC scheme discussed above provides additional TX leakage cancellation while ensuring no fundamental power loss for RX signals.

B. ACTIVE SI CANCELER

From Sec. II-A, TX leakage residue cancellation is possible since a stronger TX residue is available at N_{THR2} . As shown in Fig. 7, N_{CPL2} connected a Low Noise Amplifier (LNA), and a passive down-conversion mixer followed by a baseband amplifier. Additionally, an auxiliary path through N_{THR2} phase shifter and auxiliary LNA is proposed. Auxiliary and main paths of RX are combined in the current domain to allow further SIC.

Theoretically, very high suppression is possible through the SI-canceller’s ‘passive’ stage. However, in practice due to finite insertion loss (IL) and phase matching between through and coupled ports, and layout parasitics, SIC is limited, which leads to non-zero $V_{CPL2,TX}$. Therefore, an auxiliary path for additional cancellation is required.

The auxiliary path is designed to align the amplitude and invert the phase with respect to the main path TX residue using a programmable gm-cell and a wideband RTPS as shown in Fig. 4. Coarse gain programmability in the auxiliary

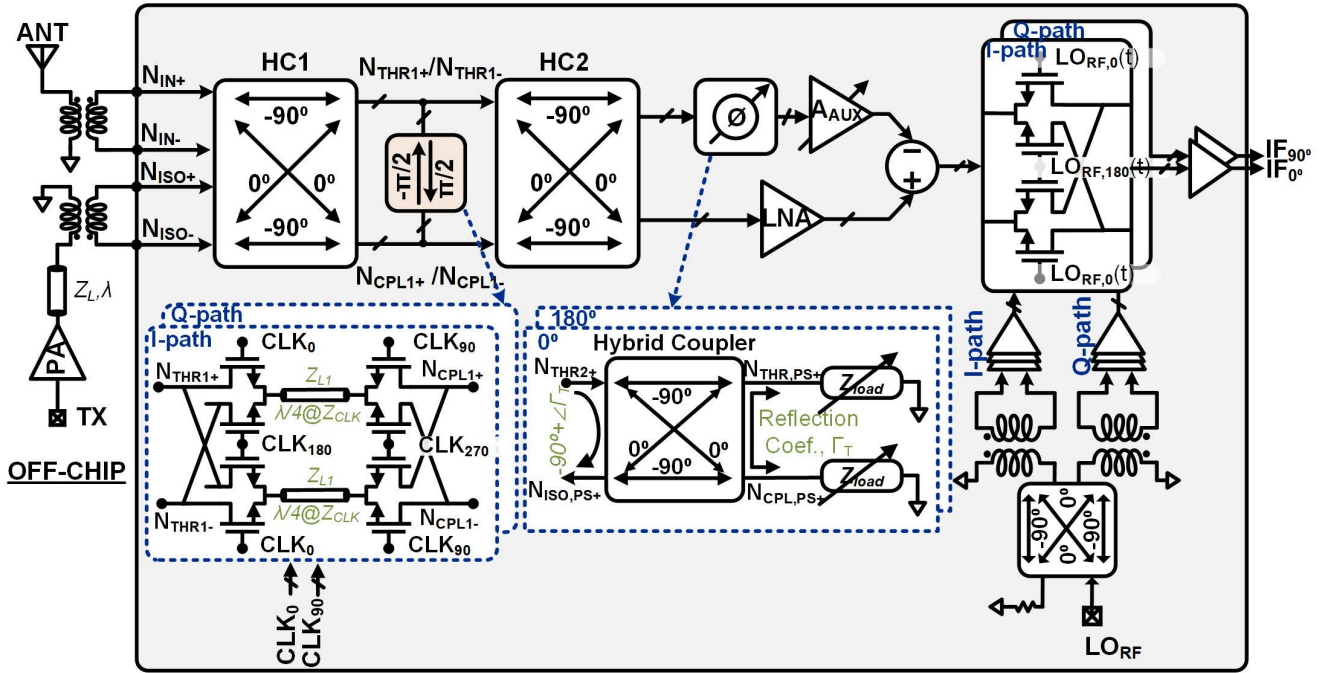


FIGURE 7. Implementation of mm-wave FD circulator RX based on a hybrid coupler and non-reciprocal delay-based shared ANT interface.

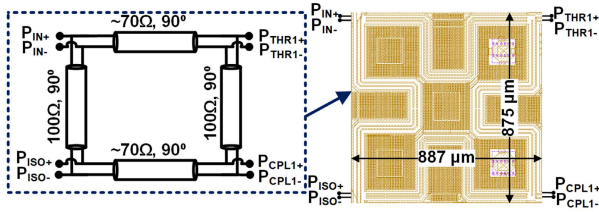


FIGURE 8. Schematic and layout of branch line 90 degree differential hybrid coupler (modeled with EM simulations [36]).

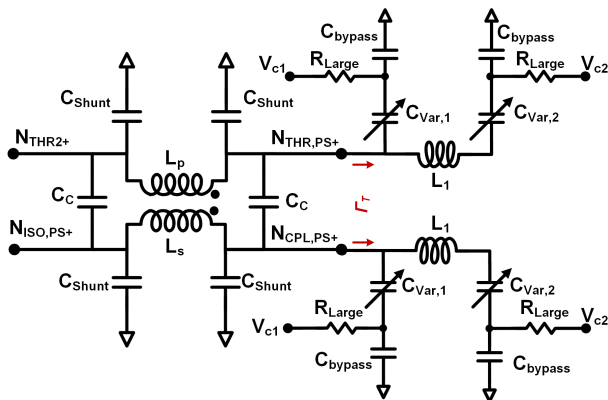


FIGURE 9. Architecture of a RTPS for pseudo-differential auxiliary path phase alignment.

path is provided by 6-level differential LNA. Phase shifter should be capable of providing 360° phase shift to ensure cancellation for any possible phase of TX residue. Reflection-type phase shifter based on [37] can provide 360° phase-shift

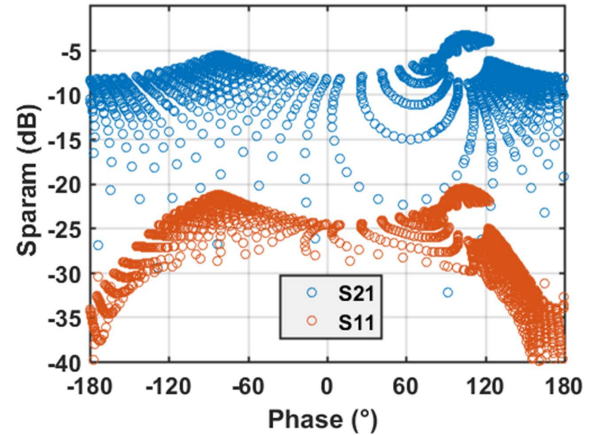


FIGURE 10. Simulated phase shift vs insertion loss plot for the RTPS.

and fine amplitude control over the phase-shift range with analog control of varactors.

Auxiliary and main paths are current summed at their output to allow better power handling. Residual TX leakage current after summation can be expressed as following:

$$I_{Leak,TX} = V_{THR2,TX} \times |\Gamma_T| \times e^{-j\frac{\pi}{2} + \Gamma_T} \times G_{m,Aux} + V_{CPL2,TX} \times G_{m,Main} \quad (11)$$

where, $I_{Leak,TX}$ is the residual TX leakage current after addition of main and auxiliary paths, $V_{THR2,TX}$ and $V_{CPL2,TX}$ are the residual TX leakages at N_{THR2} and N_{CPL2} respectively due to non-idealities, Γ_T is reflection coefficient at through and coupled ports of the RTPS and $G_{m,Main}$ and $G_{m,Aux}$

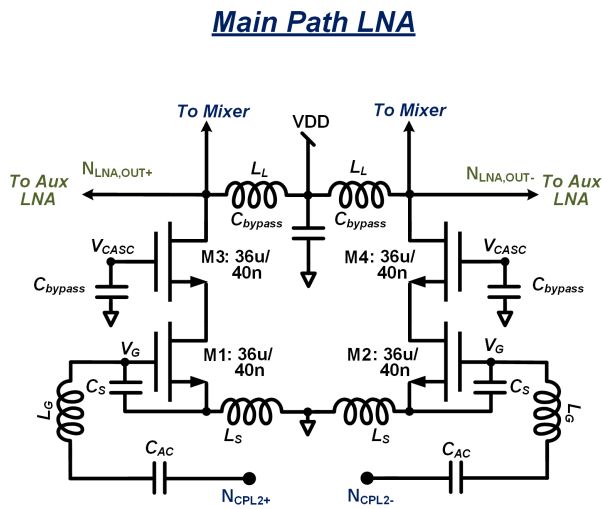


FIGURE 11. Implementation of a common-source low-noise amplifier(LNA) with inductive degeneration.

are transconductances of the main path and aux path LNAs respectively. To ensure a low $I_{Leak,TX}$, fine gain and phase resolution of the auxiliary path has been provided through the RTPS and variable transconductance.

III. 26-GHz SI CANCELING IBFD CIRCULATOR RX DESIGN IN 45nm SOI CMOS

In this section, the implementation of the proposed mm-wave SI cancellation RX, as shown in Fig. 7, is detailed. The IC is implemented in 45nm RFSOI which provides simulated $R_{on}C_{off}$ of < 200 fs and inductor quality factor >15 due to high substrate resistivity. Block-level circuit implementations of the shared ANT interface and the subsequent RX are discussed in the following:

A. HYBRID COUPLER (HC1) WITH NON-RECIPROCAL DELAY LOAD

The proposed architecture is implemented differentially with an on-chip branch line 90° hybrid coupler (Fig. 8) designed based on differential 100 Ω and 70 Ω transmission lines. EM simulations were performed to verify mm-wave impedance and wavelength [36]. In this work, T-line based distributed approach is used to design HC1 for increased EM modeling predictability; however lumped components can be used for reducing area. The insertion loss of HC1 when loaded with HC2 is ~1.45 dB.

Implementation of the switching network for the NTL delay loading the branch-line hybrid coupler is shown in Fig. 7. This design is based on [33], and the NTL delay is clocked at $F_{RF}/5$ with 50% duty cycle square waves with four quadrature phases. Low-frequency operation assists in two ways; i) reducing the dynamic power consumption of switches, ii) improving the switch performance. Switch resistance is chosen to target TX-ANT IL ~3 dB. The parasitic capacitance of the switch is absorbed in the T-lines around

Auxiliary Path LNA

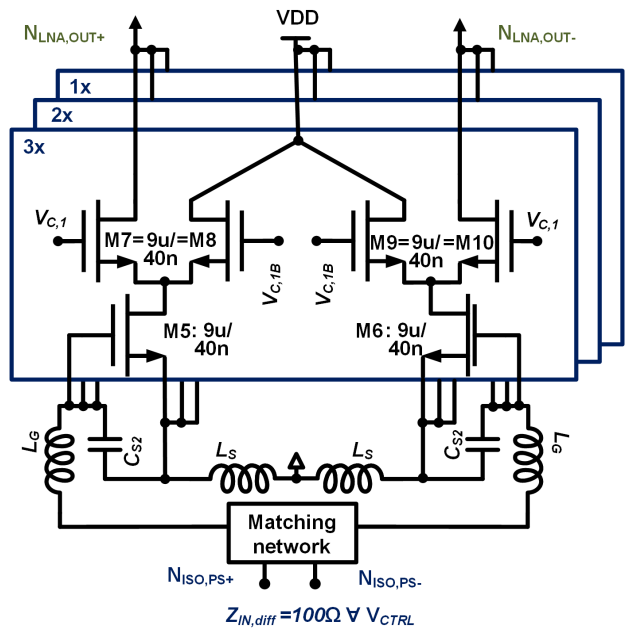


FIGURE 12. Implementation of a programmable auxiliary LNA with input matching across variable gain and current summing with the main path LNA through the LC load.

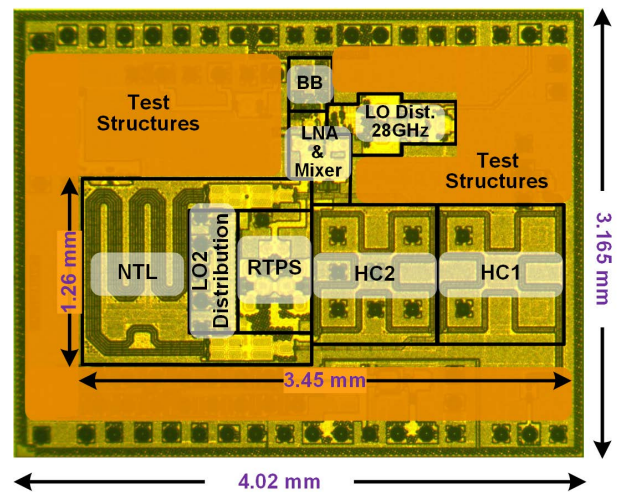


FIGURE 13. Chip microphotograph of a 26-GHz fully integrated FD circulator RX implemented in 45nm SOI.

the switches. Differential T-line between the switches has a length of $\lambda/4$ at $F_{RF}/5$.

B. RESIDUE CANCELING 90° HYBRID COUPLER (HC2)

Due to finite switch resistance and quality factor of passive elements, TX residue remains at $N_{THR,1}$ and $N_{CPL,1}$ of Fig. 5. Since these nodes are placed symmetrically in the circuit, leakage amplitudes on these nodes are comparable. Additional branch-line differential 90° hybrid coupler (HC2) based on Fig. 8 is added to N_{THR1+}/N_{THR1-} and

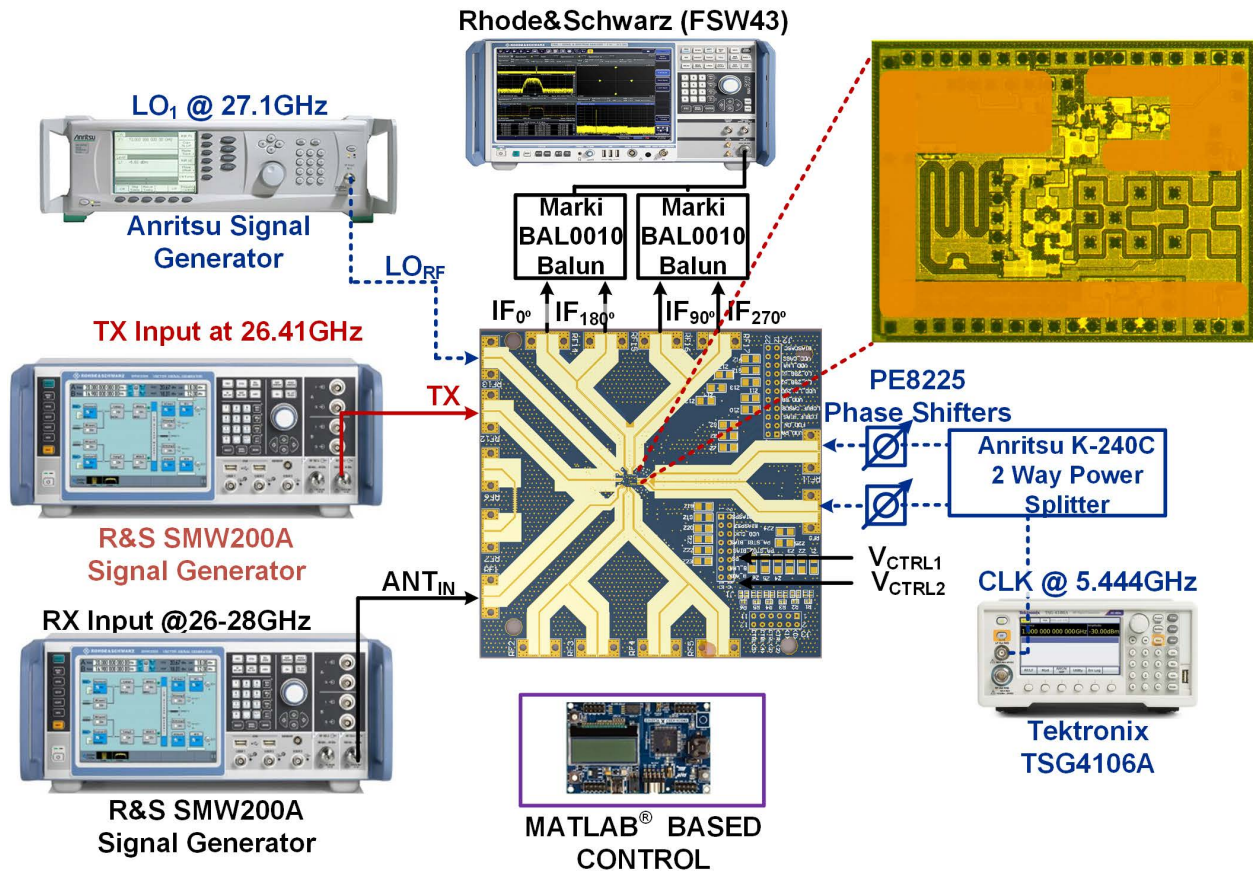


FIGURE 14. Setup for connectorized measurements using flip-chip mounted on a 3-layer Rogers 4350B PCB and external signal generators as RX and TX inputs to the system.

N_{CPL1+}/N_{CPL1-} . With HC2, RX signal witnesses a differential $100\ \Omega$ match instead of an ‘open’ across N_{THR1+}/N_{THR1-} and N_{CPL1+}/N_{CPL1-} .

C. PSEUDO-DIFFERENTIAL REFLECTION-TYPE PHASE SHIFTER

As described in Sec. II, the residue canceling 90° hybrid coupler (HC2) drives a phase shifter for further TX leakage suppression. The RTPS is implemented based on the single-ended phase-shifter proposed in [37]. In this work, two stand-alone RTPS are used in a pseudo-differential configuration. To achieve a compact footprint, a transformer-based lumped-element hybrid coupler (Fig. 9) is used to implement the RTPS. Each RTPS is matched to $50\ \Omega$ both at input and output. A variable LCL- Π network is used as the termination, Γ_T , at the through and coupled ports with the use of varactors providing variable phase (and resultant variable amplitude). Fig. 10 shows the simulated RTPS amplitude and phase shift (S_{21}) for the RTPS as varactors, $C_{Var,1}$ and $C_{Var,2}$ in Fig. 9 are varied, demonstrating phase and amplitude tunability. Since the input and output ports of the RTPS are matched (S_{11} in Fig. 10), TX-leakage reflections are not created that can propagate back to main signal path through the residue-canceling hybrid coupler (HC2).

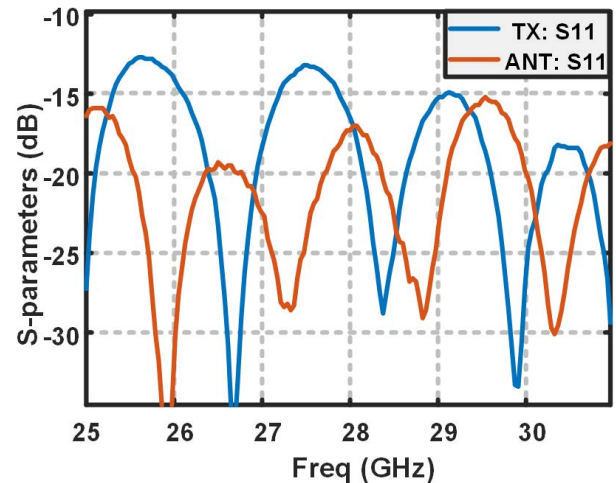


FIGURE 15. Measured input matching at ANT and TX ports.

D. 26 GHz ‘MAIN’ AND ‘AUXILIARY’ PATH LOW-NOISE AMPLIFIERS (LNA)

Common-source differential LNA with inductive degeneration topology is used for low stand-alone NF of ~ 2.45 dB and higher power gain in this work. Fig. 11 shows the

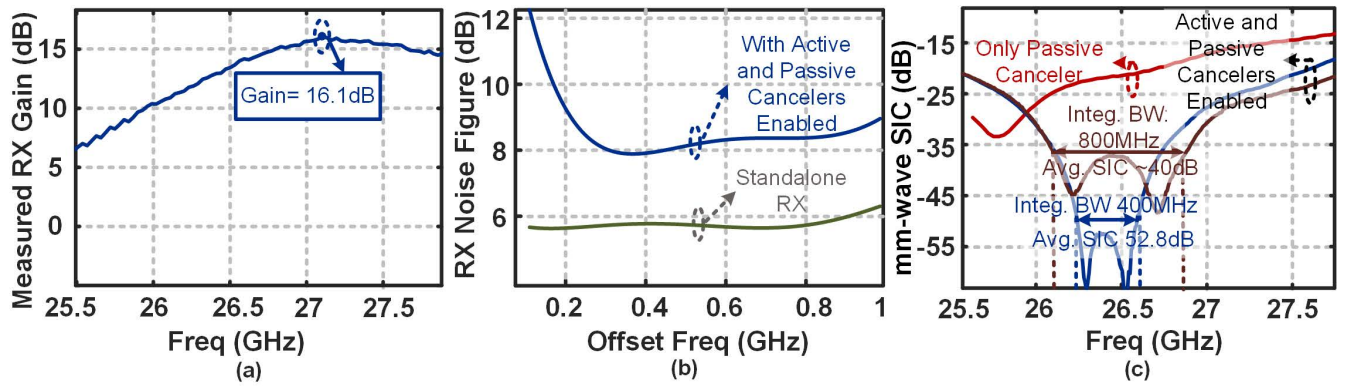


FIGURE 16. Measured (a) small-signal gain (b) noise figure (c) SIC with only passive and both passive and active cancelers 'ON'.

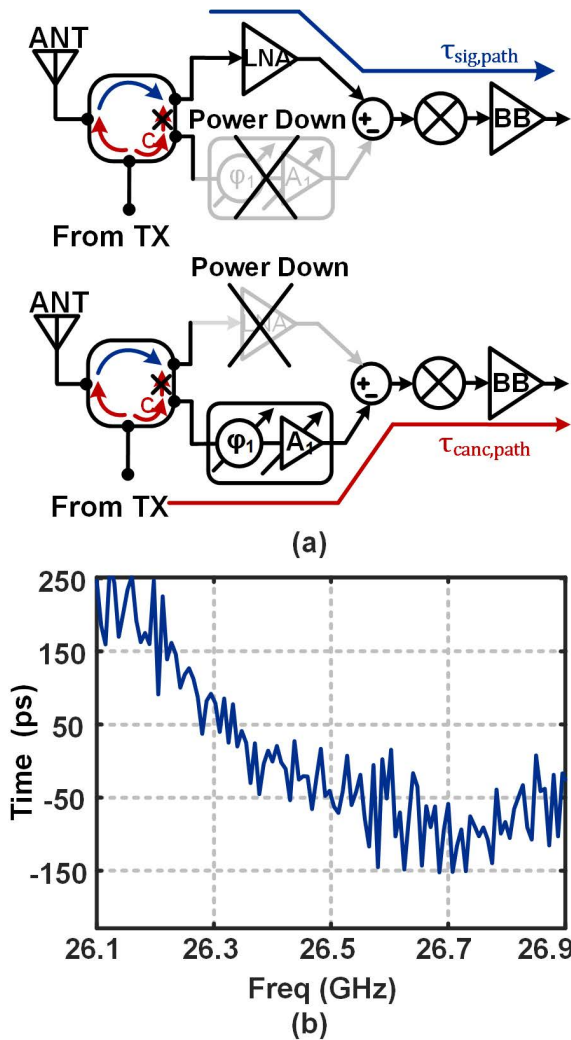


FIGURE 17. Setup for TX leakage through (a) 'main RX' (b) 'auxiliary RX' paths. (c) Difference in group delays between the leakage and cancellation paths.

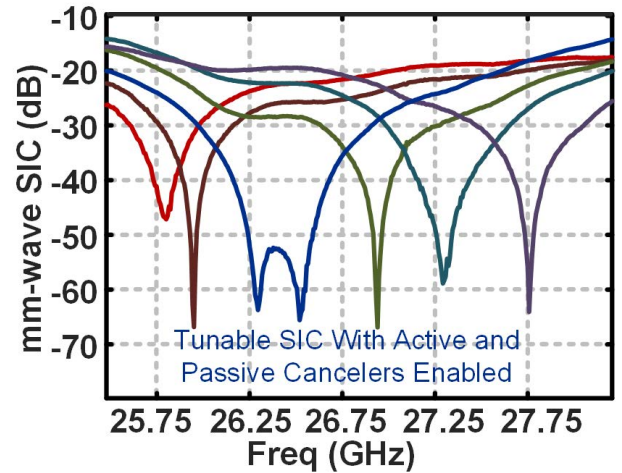


FIGURE 18. Measured SIC notch tunability with variation in on-chip phase shifter varactor and auxiliary LNA codes.

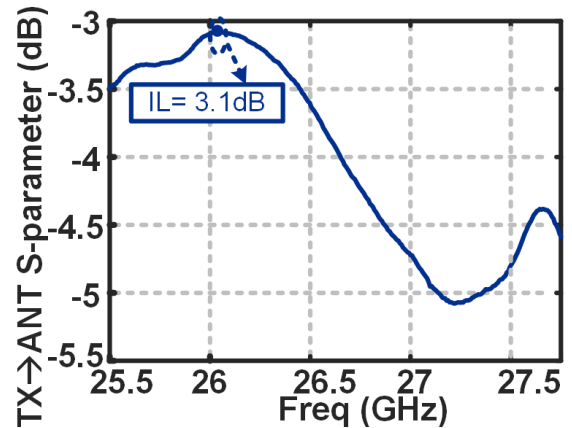


FIGURE 19. Measured TX to ANT port IL of proposed mm-wave FD circulator RX.

input power-matched stand-alone differential LNA architecture. The output of LNA is current summed with the

auxiliary-path LNA and resonated with an LC tank. Coarse-gain programmability in the auxiliary-path LNA (6 levels)

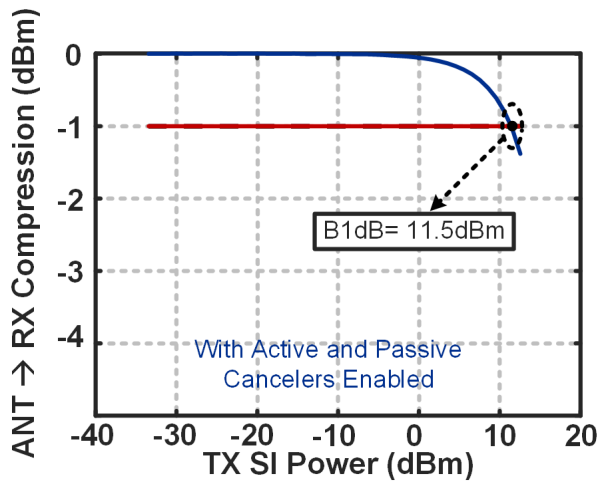


FIGURE 20. Measured normalized RX compression in the presence of a blocker.

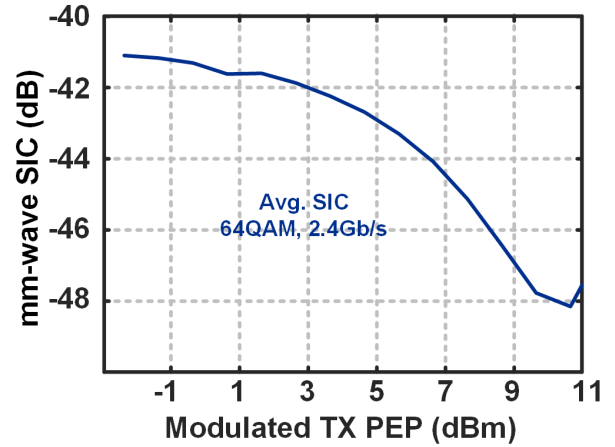


FIGURE 22. Measured SIC across 64-QAM modulated TX power applied to ANT port.

Notably, higher TX residue isolation between N_{THR2} and N_{CPL2} requires lower auxiliary path gain for active SI cancellation, which leads to lower degradation in noise figure of the RX when auxiliary and main paths are combined. Passive SIC in this design has been optimized to limit the simulated NF degradation due to presence of auxiliary path below 1.5 dB.

A pseudo-differential RTPS drives an input matched programmable auxiliary path LNA. Auxiliary LNA has been designed to always input-match to $50\ \Omega$ (single-ended) irrespective of the gain setting. To ensure such matching across all the gain settings, a current steering mechanism is provided Fig. 12. For instance, lower codes steer the excessive current to VDD (1.2V) supply, thus reducing the effective gm to the load. Input matching at auxiliary LNA ensures that the phase shifters witness a matched load at its isolated port. Range of programmability for the auxiliary path LNA is $0 - gm/2$, where gm is the transconductance of the main path LNA. RX LNA consumes 27 mW of power, and the auxiliary path consumes 13.8 mW of power.

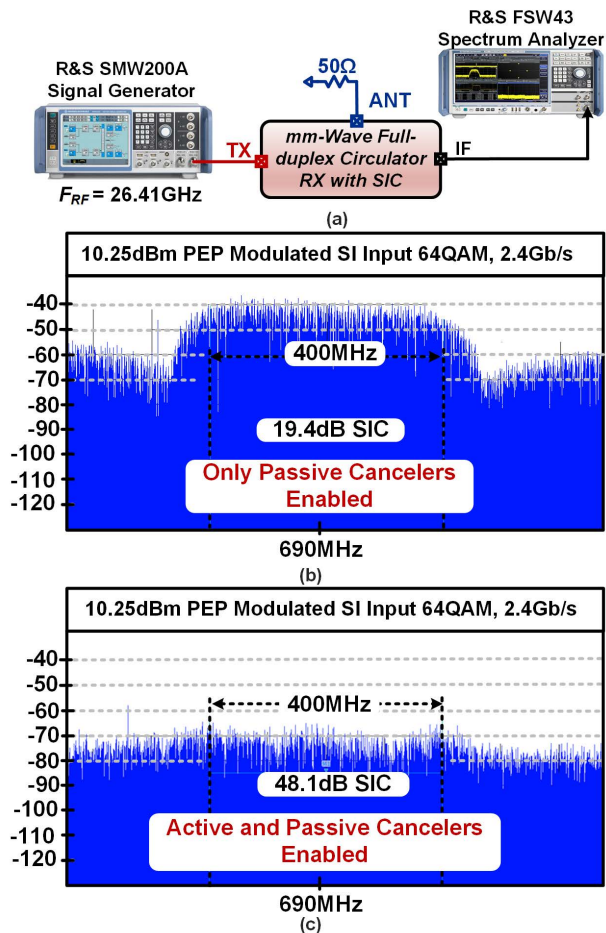


FIGURE 21. (a) Setup for connectorized large signal modulated TX leakage cancellation (b) SIC with only passive cancelers enabled (c) SIC with both passive and active cancelers enabled.

provides additional amplitude control for canceling leakage using the auxiliary path.

E. QUADRATURE PASSIVE MIXER AND LO DISTRIBUTION

The current combined output of the main path and auxiliary LNA is directly downconverted with 26 GHz clock driving the passive quadrature mixer, as shown in Fig. 7. Quadrature LO is generated from a single-ended clock using a lumped element 90° hybrid coupler. Furthermore, the single-ended quadrature signal is converted to differential using baluns. Finally, the LO is buffered through cascaded common source amplifier and gm-cell buffer. LO driver consumes 10.5 mW of power from 1.2 V supply.

F. BASEBAND AMPLIFIER

The passive mixer is loaded with a transconductance stage based on invertors with resistive feedback. Baseband amplifier drives a $100\ \Omega$ differential T-line load. Quadrature baseband amplifier consumes 50.4 mW power from 1.2 V supply.

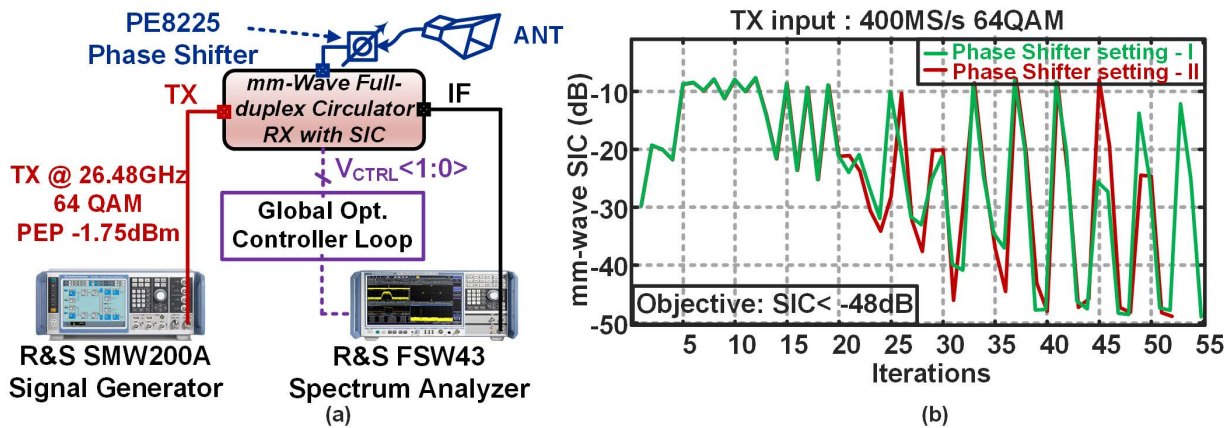


FIGURE 23. (a) Setup to demonstrate SIC response to varying EM environments where environment variation is emulated by a horn antenna and a phase shifter (b) SIC settings convergence achieving using global optimization loop with <55 iterations to meet < -48 dB SIC objective.

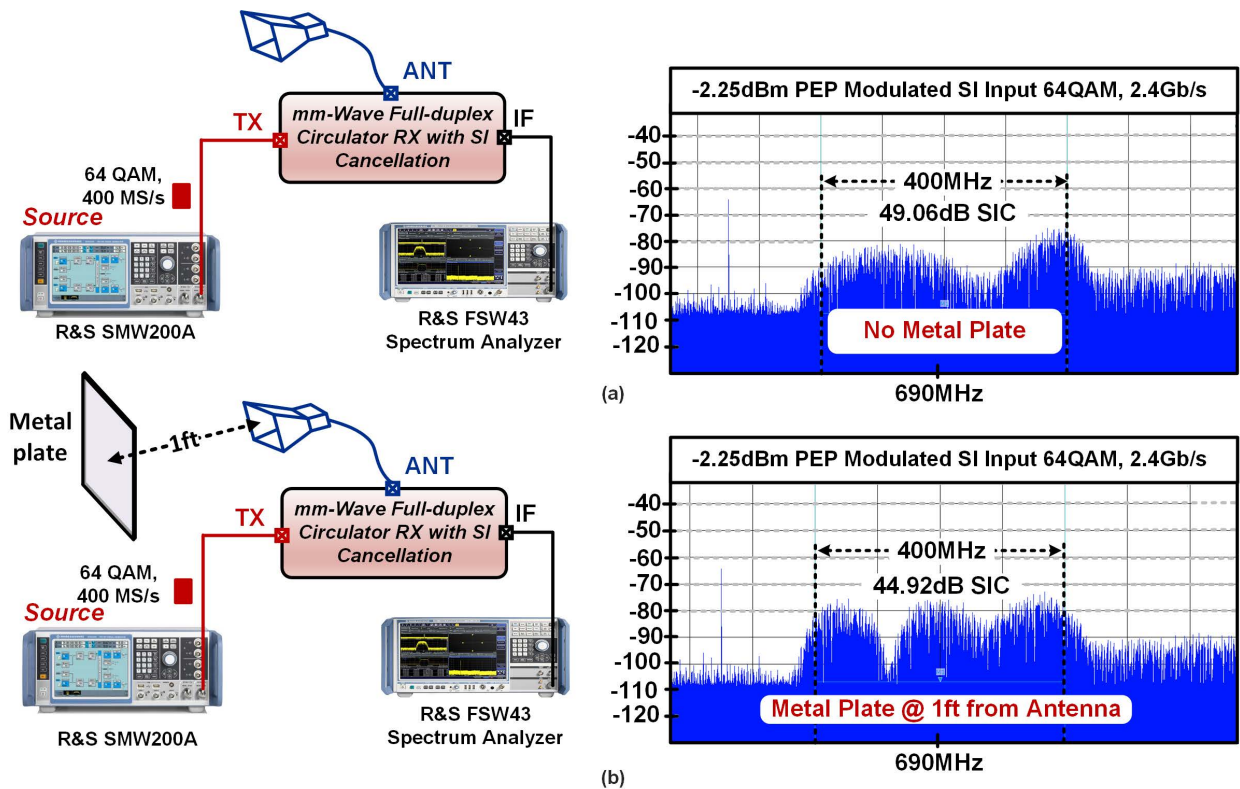


FIGURE 24. Measured TX SIC for modulated TX signal- (a) without the metal plate (b) with the metal plate at 1 ft from horn antenna.

IV. MEASUREMENT RESULTS

The prototype is fabricated in 45nm SOI CMOS process and the micro-photograph of IC is shown in Fig. 13. The active area of the IC is 4.54 mm² and the IC is flip-chip packaged onto a RO4350B three-layer printed circuit board for measurements. The measurement setup is shown in Fig. 14 for connectorized CW and modulated signal measurements.

The measured matching at the TX and ANT ports is shown in Fig. 15. Since the input matching is constrained by the

matching of the branch-line 90° coupler, HC1, the distributed implementation leads to wideband matching.

With respect to input at the ANT port, for operation as a receiver, the measured gain from ANT to IF is shown in Fig. 16(a). A peak RX Gain of ~16 dB is measured for the signal path. Corresponding NF is shown in Fig. 16(b) with a standalone NF of ~ of 6 dB. When the SIC path is enabled, the NF is degraded as discussed in Sec. III-D. The measured degradation of NF is 2.1 dB.

Fig. 16(c) shows measured integrated SIC for two cases; i) with only passive cancellation enabled where the auxiliary LNA output is not summed with the main path ii) with both passive and active cancellations enabled. The passive SIC from NTL at HC1 output and subsequent quadrature combining in HC2 is 22 dB at ~26.4 GHz. The phase and amplitude programmability in the auxiliary path enables active SIC and the settings can be optimized for notch depth or cancellation bandwidth. As shown in Fig. 16(c), the proposed architecture is configured to achieve an integrated SIC of ~53 dB over 400 MHz and 40 dB SIC over 800 MHz signal BW at mm-wave.

Wideband SIC is demonstrated with measurements shown in Fig. 17. Group delay is measured for, i) the P_{TX} leakage through the main path with auxiliary path powered down ii) leakage through the auxiliary path with the main path powered down. The difference in the group delays between the leakage and cancellation path is shown in Fig. 17. A relatively flat group delay difference of <250 ps demonstrates the wideband transfer function of the cancellation path.

The SIC path is tuned from 25.5 GHz to 28 GHz by varying the varactor bias of the RTPS and using the variable amplitude in the auxiliary path LNA. The tunability in the SIC is shown in Fig. 18 with both passive and active cancelers enabled, where the SIC null is shifted across frequency.

The TX to ANT IL is measured with the SIC enabled and the performance is shown in Fig. 19. TX to ANT IL is primarily due to T-line losses in distributed implementation of HC1 and finite reflection coefficient, $\Gamma_{R,TX}$. Measured results show the TX to ANT IL of 3.1 dB.

Fig. 20 shows the measured large-signal blocker 1 dB compression point for the RX with respect to input on the TX. For B1dB measurement, the P_{TX} is gradually increased from -10 dBm till ANT to IF witnesses 1 dB compression. Measurements of Fig. 20 demonstrates that power handling capability of wideband FD circulator RX is +11.5 dBm with respect to the TX port.

Connectorized SIC measurements with a modulated TX signal incident on the system are shown in Fig. 21(a). The ANT port is terminated with a 50 Ω , and a signal generator is used as a source for the TX port. A strong 10.25 dBm Peak Envelope Power (PEP) with PAPR of ~7 dB, modulated (64 QAM) TX signal at 2.4 Gb/s data rate and frequency of 26.41 GHz is applied, and SI suppression is measured for two cases; i) only passive cancellation enabled (Fig. 21(b)) ii) both passive and active cancellations enabled (Fig. 21(c)). Measurements show SIC of 48.1 dB, demonstrating 100x improvement over state-of-the-art IBFD receivers for large P_{TX} . Notably, large signal SIC performance of the proposed system is comparable to the small signal, demonstrating high power handling.

The robustness of SIC with respect to P_{TX} is demonstrated with Fig. 22 where the power of a modulated 64 QAM TX signal at 2.4 Gb/s is varied and the SIC is measured across different power settings. Notably, RTPS and VGA codes are optimized for highest cancellation around +11 dBm P_{TX} , and

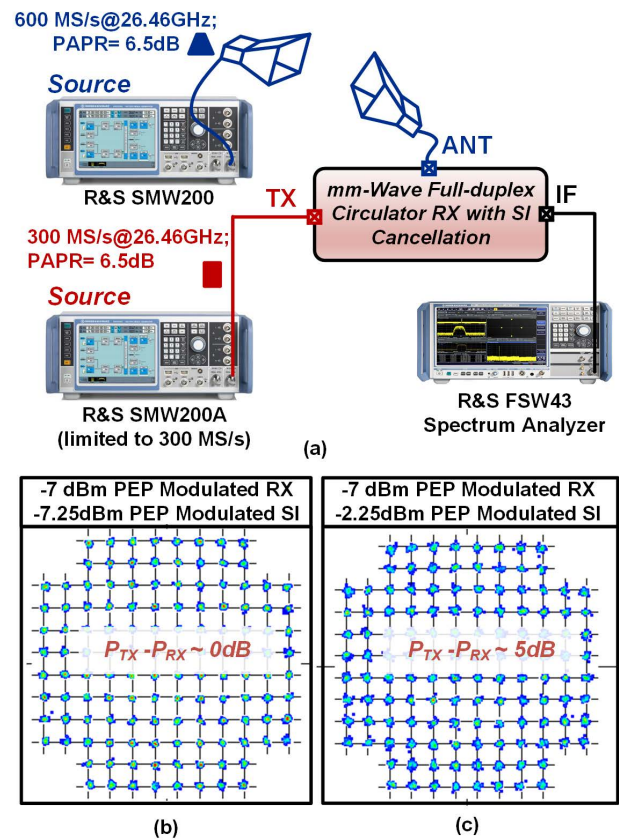


FIGURE 25. (a) Setup for Over-the-air(OTA) measurements with modulated TX and RX signals incident on ANT port (b) Measured EVM performance for modulated RX and TX signals with $P_{TX} - P_{RX} \sim 0$ (c) $P_{TX} - P_{RX} \sim 5$ dB.

are not changed during power sweep. Low variation for a sweep around high P_{TX} demonstrates the robustness of SIC settings to power changes.

SIC performance is also characterized in varying EM environments. Fig. 23(a) shows the setup to measure SIC with a horn antenna attached to the ANT port. In the absence of a mm-wave impedance tuner, variable EM environment is emulated by an external tunable phase shifter and variable attenuator in series with the horn antenna. A global optimization loop is used to find optimum canceler gain and phase coefficients by measuring the TX leakage power and dynamically varying the on-chip RTPS varactor controls. The optimization loop converges to settings that achieve desired objective function of 48-dB integrated SIC across 400 MS/s (64QAM) in <55 cycles as shown in Fig. 23(b) for two phase shifter settings, with and without attenuation of 1 dB in the path. This suggests that environment variations can be compensate in ms time frames.

Robustness against antenna impedance variations is also demonstrated by attaching a Horn antenna to the ANT port and measuring the SIC ‘with’ and ‘without’ the presence of a metal plate. Modulated TX port is excited with a -2.25 dBm PEP 64 QAM at 2.4 Gb/s at 26.41 GHz as shown in Fig. 24

TABLE 1. Comparison with state-of-the-art.

Architecture	Shared ANT interface ‘without RX’				‘Separate ANT interface’ with RX				Shared ANT interface with RX
[Reference]	[38]	[39]	[33]	[34]	[14]	[28]	[21]	[40]	This work
Technology	180 nm SOI	180 nm CMOS	45 nm RFSOI	45 nm RFSOI	65 nm CMOS	65 nm CMOS	40 nm CMOS	65 nm CMOS	45 nm RFSOI
Freq. (GHz)	1.9-2.2	24	22.7-27.3	50-56.8	0.8-1.4	0.15-3.5	1.7-2.2	28/37/39	25.5-27.75
TX-ANT	>-3.7	-5.7	-3.3	-3.6:1.2V	NA	NA	NA	NA	-3.1
ANT-RX	>-3.9	-5.7	-3.2	-3.1	27-42	24	20-36	16.1/10.9/8.3	16.1
NF (dB)	NR	7.6	3.3	3.2	4.8	4-6 (HD)	-4	6.2/7/7.9	5.8
Excess NF due to SIC (dB)	N/A	3.5	N/A	N/A	0.9-1.2 /1.1-1.5	6.3	1.55	NR	2.1
Isolation dB/Hz: small signal	>50 dB: 300 MHz	20 dB: 380 MHz	18.5 dB [£] : 6 GHz	40 dB: 1.3 GHz	20 dB: 15/25 MHz	27 dB: 16.25 MHz	50 dB: 42 MHz	26 dB: 500 MHz	~53/40 dB [#] : 400/800 MHz
Isolation dB/Hz: >10dBm TX Power	>50dB: CW	N/A	17.5dB: NR	22dB: NR	N/A	N/A	N/A	N/A	~48.1dB [#] :400MS/s (64QAM 2.4Gb/s)
Power Handling (dBm)	27	NR	>21.5 [£]	+20 [£]	>-8	>+1.5	+3	NR	+11.6
Power (mW)	N/A: RX, 0*: Canc.	N/A: RX, 7.2: Canc.	N/A: RX, 78.4: Canc.	N/A: RX, 41(1.2V): Canc.	63-69: RX, 44-91: Canc.	23-56 [®]	22: RX, 11.5: Canc	37.6: RX, NR: Canc	88: RX, 23.5: Canc
Chip Area (mm ²)	1.75	0.72	2.16	1.72	4.8	2	3.5 ^β	0.48	4.54
EVM with SIC	NR	NR	NR	NR	NR	NR	NR	RX and TX (-16dBm, 1.6Gb/s):	TX [£] (2.1Gb/s,-7.25dBm): 128QAM, RX-EVM ^Γ 3.3%
								64QAM, RX-EVM ~4.4%	TX [£] (2.1Gb/s,-2.25dBm): 128QAM, RX-EVM ^Γ 4.2%

*Passive ANT interface [£]Limited by test setup [®]Total including LO tree, ^βIncludes TX and Integrated PLL, ^ΓMeasured at RX(4.2 Gb/s,-7 dBm), [#]Measured at 26.25 GHz.

and measurements show degradation of only about ~4 dB with metal plate 1 ft from the horn antenna.

Setup and measured results to demonstrate and characterize mm-wave IBFD circulator RX performance for over-the-air (OTA) link is shown in Fig. 25(a)-(c). Two horn antennas are used to excite the ANT port of DUT wirelessly with a desired modulated RX signal at 128 QAM, 600MS/s as shown in Fig. 25(a). Simultaneously, TX signal with 128 QAM and symbol rate of 300 MS/s (limited by instrument) is applied. RX constellation is plotted, and EVM is measured for two cases; i) $P_{TX} - P_{RX} \approx 0$ dB and ii) $P_{TX} - P_{RX} \approx 5$ dB. EVM is shown to be 3.3%/4.2% for the two cases respectively in Fig. 25. EVM of 3.3% demonstrates the high power handling and feasibility of the implemented system for full-duplex communication applications such as IAB relays and repeaters.

Table 1, compares the proposed architecture with recently published state-of-the-art. This work is the first fully integrated shared antenna interface based IBFD circulator RX at mm-wave. The presented architecture supports high integrated SIC over 400 MHz instantaneous bandwidth for >10 dBm modulated TX signal at 2.4 Gbps. Significant improvement (>100x) in SIC performance at mm-wave frequencies for high P_{TX} is measured. Additionally, modulated

large signal measurements demonstrate the robustness of the IBFD circulator RX.

V. CONCLUSION

A 26-GHz in-band full-duplex circulator RX with SIC employing shared ANT interface with ‘passive’ followed by ‘active’ cancelers is presented. The feasibility of IBFD circulator RX for mm-wave relays and repeaters is demonstrated through connectorized and wireless measurements. The proposed mm-wave IBFD circulator mitigates the challenge of TX to RX self-interference at high TX powers by suppressing TX leakage at mm-wave frequencies. Wide cancellation bandwidth and low group delay are critical for millimeter wave 5G applications. This system demonstrates programmable SIC bandwidth and integrated TX leakage magnitude. SIC of ~53 dB over 400 MHz and ~40 dB over 800 MHz while maintaining a TX to ANT IL ~3.1 dB is measured. Wireless measurements with modulated RX in the presence of strong modulated TX and varying VSWR demonstrate robustness of the system.

VI. ACKNOWLEDGMENT

The authors acknowledge the support of Dr. Tim Hancock (DARPA), John Bowne (Rohde & Schwarz), and

Radu Fetcu (Rohde & Schwarz). Dr. Yao Liu and members of High-Speed Integrated Circuits (HSIC) Laboratory, Oregon State University, provided support with equipment and technical inputs.

REFERENCES

- [1] W. Roh, J. Seol, J. Park, B. Lee, and J. Lee, "Millimeter-wave beamforming as an enabling technology for 5G cellular communications: Theoretical feasibility and prototype results," *IEEE Commun. Mag.*, vol. 52, no. 2, pp. 106–113, Feb. 2014.
- [2] K. Networks, "Rethinking 5G microcell backhaul to deliver superior customer experienceskumu networks," Kumu Netw., Sunnyvale, CA, USA, Tech. Rep., 2015. [Online]. Available: <https://kumunetworks.com/wp-content/uploads/2020/04/Full-Duplex-Integrated-Access-Backhaul-for-5G-Kumu-Networks-White-Paper-V1.0.pdf>
- [3] S. Sun, T. A. Thomas, T. S. Rappaport, H. Nguyen, I. Z. Kovacs, and I. Rodriguez, "Path loss, shadow fading, and line-of-sight probability models for 5G urban macro-cellular scenarios," in *Proc. IEEE GLOBECOM*, Dec. 2015, pp. 1–7.
- [4] L. Zhang, M. Xiao, G. Wu, M. Alam, Y.-C. Liang, and S. Li, "A survey of advanced techniques for spectrum sharing in 5G networks," *IEEE Wireless Commun.*, vol. 24, no. 5, pp. 44–51, Oct. 2017.
- [5] O. Teyeb, A. Muhammad, G. Mildh, E. Dahlman, F. Barac, and B. Makki, "Integrated access backhauled networks," in *Proc. IEEE 90th Veh. Technol. Conf. (VTC-Fall)*, Sep. 2019, pp. 1–5.
- [6] F. Boccardi, R. W. Heath, A. Lozano, T. L. Marzetta, and P. Popovski, "Five disruptive technology directions for 5G," *IEEE Commun. Mag.*, vol. 52, no. 2, pp. 74–80, Feb. 2014.
- [7] T. Rappaport, S. Sun, R. Mayzus, and H. Zhao, "Millimeter wave mobile communications for 5G cellular: It will work!" *IEEE Access*, vol. 1, pp. 335–349, 2013.
- [8] P. Commware, "Holographic beam forming and phased arrays," in *Proc. Commware*, 2019, pp. 1–7.
- [9] R. Taori and A. Sridharan, "Point-to-multipoint in-band mmwave backhaul for 5G networks," *IEEE Commun. Mag.*, vol. 53, no. 1, pp. 195–201, Jan. 2015.
- [10] M. Shafi, A. F. Molisch, P. J. Smith, T. Haustein, P. Zhu, P. De Silva, F. Tufvesson, A. Benjebbour, and G. Wunder, "5G: A tutorial overview of standards, trials, challenges, deployment, and practice," *IEEE J. Sel. Areas Commun.*, vol. 35, no. 6, pp. 1201–1221, Jun. 2017.
- [11] S. Hong, J. Brand, J. I. Choi, M. Jain, J. Mehlman, S. Katti, and P. Levis, "Applications of self-interference cancellation in 5G and beyond," *IEEE Commun. Mag.*, vol. 52, no. 2, pp. 114–121, Feb. 2014.
- [12] D. Bharadia and S. Katti, "FastForward: Fast and constructive full duplex relays," *SIGCOMM Comput. Commun. Rev.*, vol. 44, no. 4, pp. 199–210, Aug. 2014.
- [13] M. Hashemi, M. Coldrey, M. Johansson, and S. Petersson, "Integrated access and backhaul in fixed wireless access systems," in *Proc. 86th Veh. Tech. Conf.*, Sep. 2017, pp. 1–5.
- [14] J. Zhou, T. Chuang, T. Dinc, and H. Krishnaswamy, "Receiver with >20 MHz bandwidth self-interference cancellation suitable for FDD, co-existence and full-duplex applications," in *IEEE ISSCC Dig. Tech. Papers*, Oct. 2015, pp. 1–3.
- [15] A. Sabharwal, P. Schniter, D. Guo, D. W. Bliss, S. Rangarajan, and R. Wichman, "In-band full-duplex wireless: Challenges and opportunities," *IEEE J. Sel. Areas Commun.*, vol. 32, no. 9, pp. 1637–1652, Sep. 2014.
- [16] T. Chi, J. S. Park, S. Li, and H. Wang, "A millimeter-wave polarization-division-duplex transceiver front-end with an on-chip multifeed self-interference-canceling antenna and an all-passive reconfigurable canceller," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3628–3639, Dec. 2018.
- [17] D. Yang, H. Yuksel, and A. Molnar, "A wideband highly integrated and widely tunable transceiver for in-band full-duplex communication," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1189–1202, May 2015.
- [18] K. Chu, M. Katanbaf, T. Zhang, C. Su, and J. C. Rudell, "A broadband and deep-TX self-interference cancellation technique for full-duplex and frequency-domain-duplex transceiver applications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 170–172.
- [19] S. Jain, A. Agrawal, M. Johnson, and A. Natarajan, "A 0.55-to-0.9 GHz 2.7 dB NF full-duplex hybrid-coupler circulator with 56MHz 40dB TX SI suppression," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 400–402.
- [20] N. Reiskarimian, J. Zhou, and H. Krishnaswamy, "A CMOS passive LPTV nonmagnetic circulator and its application in a full-duplex receiver," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1358–1372, May 2017.
- [21] T. Zhang, C. Su, A. Najafi, and J. C. Rudell, "Wideband dual-injection path self-interference cancellation architecture for full-duplex transceivers," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1563–1576, Jun. 2018.
- [22] J. Zhou, N. Reiskarimian, and H. Krishnaswamy, "Receiver with integrated magnetic-free N-path-filter-based non-reciprocal circulator and baseband self-interference cancellation for full-duplex wireless," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2016, pp. 178–180.
- [23] A. Nagulu, A. Alu, and H. Krishnaswamy, "Fully-integrated non-magnetic 180 nm SOI circulator with > 1W P1dB, > + 50 dBm IIP3 and high isolation across 1.85 VSWR," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2018, pp. 104–107.
- [24] N. Reiskarimian, M. B. Dastjerdi, J. Zhou, and H. Krishnaswamy, "Analysis and design of commutation-based circulator-receivers for integrated full-duplex wireless," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2190–2201, Aug. 2018.
- [25] M. B. Dastjerdi, S. Jain, N. Reiskarimian, A. Natarajan, and H. Krishnaswamy, "28.6 full-duplex 2x2 MIMO circulator-receiver with high TX power handling exploiting MIMO RF and shared-delay baseband self-interference cancellation," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 448–450.
- [26] B. van Liempd, B. Hershberg, B. Debaillie, P. Wambacq, and J. Craninckx, "An electrical-balance duplexer for in-band full-duplex with < -85 dBm in-band distortion at +10 dBm TX-power," in *Proc. 41st Eur. Solid-State Circuits Conf.*, Sep. 2015, pp. 176–179.
- [27] B. Hershberg, B. van Liempd, X. Zhang, P. Wambacq, and J. Craninckx, "A dual-frequency 0.7-to-1 GHz balance network for electrical balance duplexers," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2016, pp. 356–357.
- [28] D. J. van den Broek, E. A. M. Klumperink, and B. Nauta, "A self-interference-cancelling receiver for in-band full-duplex wireless with low distortion under cancellation of strong TX leakage," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.
- [29] B. van Liempd, A. Visweswaran, S. Ariumi, S. Hitomi, P. Wambacq, and J. Craninckx, "Adaptive RF front-ends using electrical-balance duplexers and tuned saw resonators," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 11, pp. 4621–4628, Nov. 2017.
- [30] G. Qi, B. van Liempd, P.-I. Mak, R. P. Martins, and J. Craninckx, "A SAW-less tunable RF front end for FDD and IBFD combining an electrical-balance duplexer and a switched-LC N-Path LNA," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1431–1442, May 2018.
- [31] Y. Liu and A. Natarajan, "A 60 GHz polarization-duplex TX/RX front-end with dual-pol antenna-IC co-integration in SiGe BiCMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 127–130.
- [32] T. Dinc, A. Chakrabarti, and H. Krishnaswamy, "A 60 GHz CMOS full-duplex transceiver and link with polarization-based antenna and RF cancellation," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1125–1140, May 2016.
- [33] T. Dinc and H. Krishnaswamy, "17.2 a 28GHz magnetic-free non-reciprocal passive CMOS circulator based on spatio-temporal conductance modulation," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 294–295.
- [34] A. Nagulu and H. Krishnaswamy, "28.5 non-magnetic 60 GHz SOI CMOS circulator based on loss/dispersion-engineered switched bandpass filters," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 446–448.
- [35] R. Garg, S. Jain, P. Dania, and A. Natarajan, "14.3 A 26 GHz full-duplex circulator receiver with 53 dB/400 MHz(40 dB/800 MHz) self-interference cancellation for mm-wave repeaters," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2021, pp. 222–224.
- [36] *ADS Momentum*, Keysight, Santa Rosa, CA, USA, 2015.
- [37] R. Garg and A. S. Natarajan, "A 28-GHz low-power phased-array receiver front-end with 360° RTPS phase shift range," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 11, pp. 4703–4714, Nov. 2017.
- [38] B. van Liempd, B. Hershberg, S. Ariumi, K. Raczkowski, K.-F. Bink, and U. Karthaus, "A +70-dBm IIP3 electrical-balance duplexer for highly integrated tunable front-ends," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4274–4286, Dec. 2016.
- [39] J.-F. Chang, J.-C. Kao, Y.-H. Lin, and H. Wang, "Design and analysis of 24-GHz active isolator and quasi-circulator," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 8, pp. 2638–2649, Aug. 2015.
- [40] S. Mondal and J. Paramesh, "Power-efficient design techniques for mm-wave hybrid/digital FDD/Full-duplex MIMO transceivers," *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2011–2026, Aug. 2020.



ROBIN GARG (Member, IEEE) received the B.Tech. degree in electrical engineering from the Indian Institute of Technology Madras, India, in 2010, and the M.S. and Ph.D. degrees in electrical engineering and computer science from Oregon State University (OSU), Corvallis, USA, in 2016 and 2021, respectively.

From 2010 to 2014, he joined as an RF Design Engineer at Texas Instruments India Pvt. Ltd., Bengaluru, India, where he worked on wireless connectivity solutions. In 2016, he joined Cypress Semiconductors Pvt. Ltd., Lynwood, USA. Since 2021, he has been working as a Staff Design Engineer at MediaTek USA Inc. His research interests include integrated circuits and systems design for wireless RF/mm-wave transceivers. He is currently serving as an Affiliate Member for the IEEE MTT-S Technical Committee on Microwave and Millimeter-Wave Integrated Circuits. He is an Active Member of the IEEE Solid-Circuits Society (IEEE-SSCS) for the past five years and served as the Chair for the SSCS OSU Student Chapter. He received the Outstanding Student Designer Award from Analog Devices Inc., for excellence in IC design, in 2020. He was a recipient of the Best Student Paper Award (second place) at IEEE RFIC, in 2020. He also received a prestigious 2020–2021 Predoctoral Achievement Award from the IEEE Solid-State Circuits Society. Since 2017, he has been serving as a reviewer for IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, IEEE ACCESS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, and IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS.



SANKET JAIN (Member, IEEE) received the B.E. degree (Hons.) in electronics and instrumentation from the Birla Institute of Technology and Science, Pilani, India, in 2009, the M.Sc. degree in electrical engineering from the Swiss Federal Institute of Technology, Lausanne, Switzerland, in 2013, and the Ph.D. degree from Oregon State University, in September 2019, where his research focused on RF and mm-wave transceiver design.

From 2013 to 2014, he worked as a Scientific Collaborator at the Institute of Microengineering, Neuchatel, Switzerland. He was awarded the Swiss Government Scholarship from Swiss Embassy, EPFL (2011–2013); the International Scholarship from KU Leuven, Belgium, in 2012; and the Rickert Engineering Fellowship at Oregon State University, in 2014. In 2018, he was awarded the Analog Devices Outstanding Student Designer Award. He serves as a reviewer for IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, and IEEE JOURNAL OF SOLID-STATE CIRCUITS.



ARUN S. NATARAJAN (Member, IEEE) received the B.Tech. degree from IIT Madras, Chennai, India, in 2001, and the M.S. and Ph.D. degrees from the California Institute of Technology, Pasadena, CA, USA, in 2003 and 2007, respectively, all in electrical engineering.

From 2007 to 2012, he was a Research Staff Member with IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, where he worked on millimeter-wave (mm-wave) phased arrays for multi-Gb/s data links and airborne radar and on self-healing circuits for increased yield in sub-micrometer process technologies. In 2012, he joined Oregon State University, Corvallis, OR, USA, where he is currently an Associate Professor with the School of EECS. His research interests include RF, mm-wave, and sub-mm-wave integrated circuits and systems for high-speed wireless communication and imaging. He was a recipient of the National Talent Search Scholarship from the Government of India, from 1995 to 2000, the Caltech Atwood Fellowship, in 2001, the IBM Research Fellowship, in 2005, the 2011 Pat Goldberg Memorial Award for the Best Paper in Computer Science, Electrical Engineering, and Mathematics published by IBM Research, the CDADIC Best Faculty Project Awards, in 2014 and 2016, the NSF CAREER Award, in 2016, the Oregon State University Engelbrecht Young Faculty Award, in 2016, and the DARPA Young Faculty Award, in 2017. He has served as a Distinguished Lecturer for the IEEE SSCS and on the TPC of the IEEE Compound Semiconductors IC Symposium (CSICS). He also serves on the Technical Program Committee for the IEEE International Solid-State Circuits Conference (ISSCC) and the IEEE Radio-Frequency Integrated Circuits Conference (RFIC). He is also an Associate Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. He has served as an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and a Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS.

• • •