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Design and Comparative Study of Voltage Regulation-Based 2-Tap Flexible Feed-Forward Equalizer for Voltage-Mode Transmitters

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ABSTRACT Herein, the analog-based, 2-tap feed-forward equalization (FFE) voltage-mode transmitter using dual supply/ground voltage regulation is presented. In an FFE data modulator, the data are divided into transition and non-transition segments, and are transmitted to the main- and post-tap drivers. By using dual voltage regulation, flexible FFE strength adjustment is possible without process dependency, and the short-current path is eliminated, thus improving the overall energy efficiency. Furthermore, this structure with independent impedance calibration loops has good on-resistance and return loss characteristics, thereby securing signal integrity. In addition, by regulating the supply/ground voltages, the output swing and common-mode voltage can be adjusted independently. Therefore, our transmitter can serve multiple standards and channel environments with a single design. To verify the effectiveness of our method, we designed a prototype of the source-synchronous transmitter in a 65 nm CMOS process, and its performance was compared with that of a conventional FFE design. The simulation results show that the proposed design has better on-resistance, return loss, and FFE controllability, and it has an energy efficiency of 2.23 pJ/bit at 20 Gb/s.

INDEX TERMS Voltage-mode driver, feed-forward equalization, impedance calibration, serial link, return loss, on-resistance.

I. INTRODUCTION

With the advent of the data-centric era [1], [2], many emerging technologies such as virtual reality, cloud services, high-performance computing, and autonomous vehicles are rapidly growing by using machine or deep learning to process meaningful information. These technologies also attempted to extract key attributes from massive data [3]. Because these recent trends demand the extension of the input/output (I/O) bandwidth, electrical links are expending extensive efforts to develop high-bandwidth, high-robustness, and more energy-efficient technologies [4].

One way to achieve these demands is to increase the data rate per pin with improved energy efficiency. However, the frequency-dependent insertion loss of the channel limits the increasing data rate per pin; therefore, equalization techniques are required [5]. Because the applications and environments of recent electrical links are more diversified, their channels have varied insertion losses at the Nyquist frequency in different applications or even in the same application [6]. Therefore, it is important to design a transmitter that uses feed-forward equalization (FFE), in which the tap coefficients can be flexibly adjusted to cope with different channel conditions.

FFE in the voltage-domain, such as de-emphasis or pre-emphasis, is extensively used in transmitters owing to the simplicity of its design and testing. When the FFE is used in a current-mode driver [7], [8] or a low-voltage differential signaling driver [6], tap coefficients can be usually controlled by the bias current, achieving high resolution. However, the

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FFE linearity can deteriorate owing to the MOS transistor-based nonlinear current source; the FFE range is limited owing to the saturation operating margin. In addition, this type of driver has worse energy efficiency than a voltage-mode driver. Implementing the FFE in the voltage-mode driver can alleviate these issues [9]–[12]. However, in the voltage-mode driver, the output driver segmentation used to implement the equalization limits the FFE resolution, causes routing congestion, and increases the pre-driver complexity [13]. Therefore, it is difficult to apply these voltage-mode designs [9]–[12] to applications with various channel environments with a single design. That is, the design methodology or process node should be modified depending on the application.

In this paper, we present a voltage-mode transmitter with a flexible 2-tap FFE adjustment using dual supply/ground regulation. The transmitted data are divided into transition and non-transition parts in an FFE data modulator. The transition data are passed to a main-tap driver with a main-tap VDD/VSS regulator, and the non-transition data are passed to a post-tap driver with a post-tap VDD/VSS regulator. Our design solves the aforementioned issues of the existing designs as follows: (1) the overall power consumption is reduced by removing the short current path on FFE operations, and (2) by using separate impedance calibration loops for the main- and post-tap driver based on considerations of the drain-source voltage level (V_{ds}) change, the output impedance matches the channel impedance well, even for non-transition data transmission cases. Thus, our design affords better on-resistance and return loss characteristics, thereby improving signal integrity. Additionally, (3) our proposed design can finely adjust the FFE strength by regulating the VDD/VSS voltages, and (4) output characteristics, such as output voltage swing and common-mode voltage, can be independently controlled with the supply/ground voltage regulation. That is, a transmitter with a flexible FFE strength adjustment and independent control of the output characteristics can serve multiple standards and channel environments.

The remainder of this paper is organized as follows: in Section II, we describe the voltage-mode FFE using dual supply/ground voltage regulation. In Section III, we introduce an overall transmitter architecture to verify the proposed method. Section IV presents the simulation results and comparative studies with a conventional structure to highlight the advantages of the proposed structure. Finally, in Section V, we outline conclusions.

II. FEED-FORWARD EQUALIZATION USING DUAL SUPPLY/GROUND VOLTAGE REGULATION

A. RELATED WORKS

In transmitter designs, a 2-tap FFE can be incorporated into the current- or voltage-mode driver. Figure 1 shows the conventional 2-tap FFE implementation of the current-mode driver [7], wherein the FFE coefficients are adjusted by controlling the ratio of the tail currents, I_{main} and I_{post},

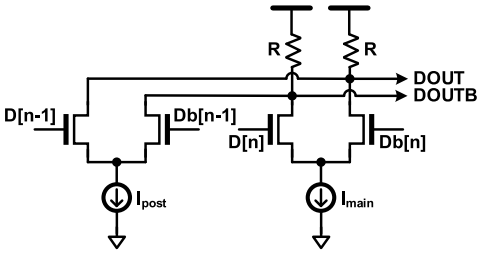


FIGURE 1. Conventional 2-tap feed-forward equalization (FFE) design of current-mode driver [7].

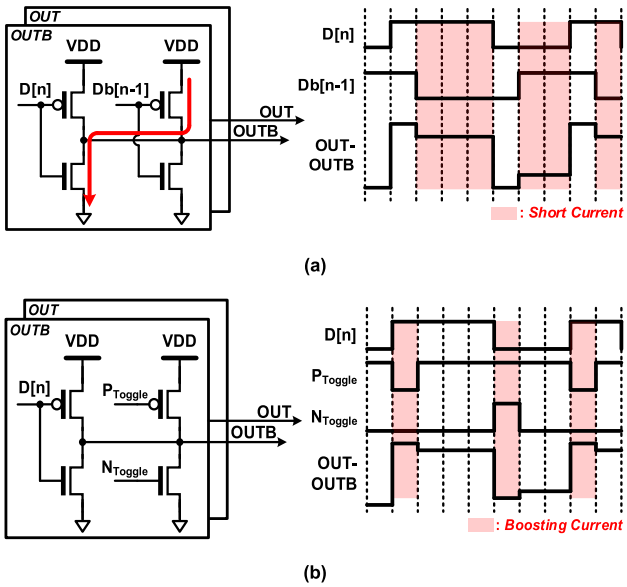


FIGURE 2. (a) Conventional [15] and (b) toggling serialization-based FFE designs [16] in voltage-mode driver.

assigned to the main- and post-tap drivers, respectively; this allows for the resolution to be fine-tuned. Because the transistors in the current source must operate in the saturation region wherein the transistor's resistance is large, the value of the passive resistor, R, determines the output on-resistance; thus, the channel impedance matching scheme is simple to implement in this transmitter. However, this type of implementation has some drawbacks: the static current consumption occurs in all the data transmissions. Because its output signal should refer either to the VDD or VSS [14], adjusting the common-mode voltage affects the output swing.

Figure 2 shows several previous FFE implementations of the voltage-mode driver [15], [16]. In the conventional FFE implementation [15], the data, D[n], and the 1-unit interval (UI) delayed inversion data, Db[n-1], are used, making the short current path from VDD to VSS during transmission of the non-transition data (Figure 2(a)); this considerably increases the overall power consumption. The FFE which uses a toggling serialization [16], as shown in Figure 2(b), can implement a pre-emphasis and remove the short current path. However, it needs a boosting current to implement FFE, which does not improve the overall current

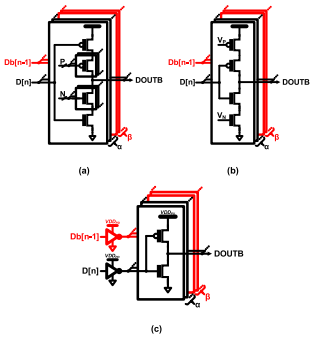


FIGURE 3. On-resistance adjustment in 2-tap FFE designs by (a) digital selection [17], [18], by controlling (b) gate-source voltage [19], and (c) supply regulation [20], [21]. In these circuit diagrams, only half of the circuit that outputs the DOUTB signal is shown.

consumption. Furthermore, V_{ds} changes during the non-transition data transmission affect the amount of boosting current.

In voltage-mode drivers with 2-tap FFE, the on-resistance, which is the output resistance when the output driver is turned on, can be adjusted by controlling the number of transistors (Figure 3(a)) [17], [18], gate-source voltage (Figure 3(b)) [19], or supply voltage of the pre-driver and its output driver (Figure 3(c)) [20], [21]. These voltage-mode drivers require the segmentation of the output driver to implement the FFE. The implementation and the FFE strength adjustment are simple; however, the FFE resolution and control range depend on the total number of segments. A large number of segments can increase the FFE resolution, resulting in nonuniform FFE resolutions, routing congestion, substantial pre-driver current, and large areas. Similar to the case of the current-mode design, the output swing depends on either the VDD or VSS; thus, it is also difficult to adjust the common-mode voltage and output swing independently.

B. PROPOSED FEED-FORWARD EQUALIZER DESIGN USING DUAL SUPPLY/GROUND VOLTAGE REGULATION

To alleviate the aforementioned issues in previous designs, a voltage-mode driver with a 2-tap FFE is proposed using dual supply/ground voltage regulation, as shown in Figure 4. From the serializer, the full-rate data signal, DIN[n], and its 1-UI delayed data signal, DIN[n-1], are transmitted to a single-to-differential (S-to-D) converter, in which the differential data signals, D[n], Db[n], D[n-1], and Db[n-1], are generated. By using these differential signals, an FFE data modulator generates four modulated data signals, namely, D_{main}, Db_{main}, D_{post}, and Db_{post}, used for our 2-tap FFE using dual supply/ground regulation. Figure 5 shows the timing diagram of the FFE data modulator operation and the differential output signal of the transmitter using these modulated data signals. D_{main} and Db_{main} signals represent the transition data from 0 to 1 and from 1 to 0, of the differential output signal, and the D_{post} and Db_{post} signals represent the non-transition data 0 and non-transition data 1, of the differential output signal. In other words, by dividing the original data into transition and non-transition data, the main and post-tap drivers can be respectively operated; this does not create a short current path.

Upon this transmitter power on, an impedance calibration block finds the selection codes, Z_n and Z_p, to match the channel impedance, and these codes are transmitted to a data selector. The data selector determines which driver leg turns on by these codes, and sends the selected modulated data signals, P_{main}, P_{post}, N_{main}, and N_{post}, to the corresponding output driver; P_{main} and P_{post} data signals take the necessary form to invert the modulated data to drive the PMOS transistors.

VDD and VSS regulators supply regulated supply/ground voltages, VDD_{main}, VDD_{post}, VSS_{main}, and VSS_{post}, in each main- and post-tap driver, and the output driver's output voltage swing, common-mode voltage, and FFE strength can be adjusted independently by controlling their regulated supply/ground voltages. Compared with the previous FFE adjustment methods, this method facilitates easier selection of the FFE resolution and range targets during the design process.

III. OVERALL ARCHITECTURE OF THE VOLTAGE-MODE TRANSMITTER

To verify our proposed FFE method, the prototype was designed by integrating it into a source-synchronous transmitter, as shown in Figure 6. The transmitter adopts a half-rate clocking architecture and has one data path, one clock path, two VDD/VSS regulators with 3–5 pF on-chip decoupling MOSFET capacitors (MOSCAPs) for the main- and post-tap drivers, and impedance calibration loops. Large off-chip decoupling capacitors for each regulated supply/ground voltages are also used to absorb the switching noise. A clock source transmits the CLKIN signal to each data and clock path.

A. DATA TRANSMITTER

A pseudo-random binary sequence generator (PRBS Gen.) generates 40-bit parallel PRBS data signals by receiving a CLK_{dig} signal, which is obtained by dividing the frequency of the CLKIN signal by 20 at a 40:1 serializer. The 40:1 serializer performs the parallel-to-serial conversion, producing the full-rate data signal, DIN[n]. The 1-UI delayed data signal, DIN[n-1], is generated using the latch; these DIN[n] and the DIN[n-1] signals are used to implement the 2-tap FFE. They are then transmitted to an FFE controller that includes the S-to-D converter, FFE data modulator, and data selector, as shown in Figure 4. Finally, the differential signals, DOUT and DOUTB, are output through the main- and post-tap drivers.

The signal paths of the modulated FFE data in the main- and post-tap drivers are designed to match the path delay between them to prevent glitch noise at the output. Nonetheless, process, voltage, and temperature (PVT) variations can cause path delay mismatch. To check the variation of the path delay, we performed the best, typical, and worst-case

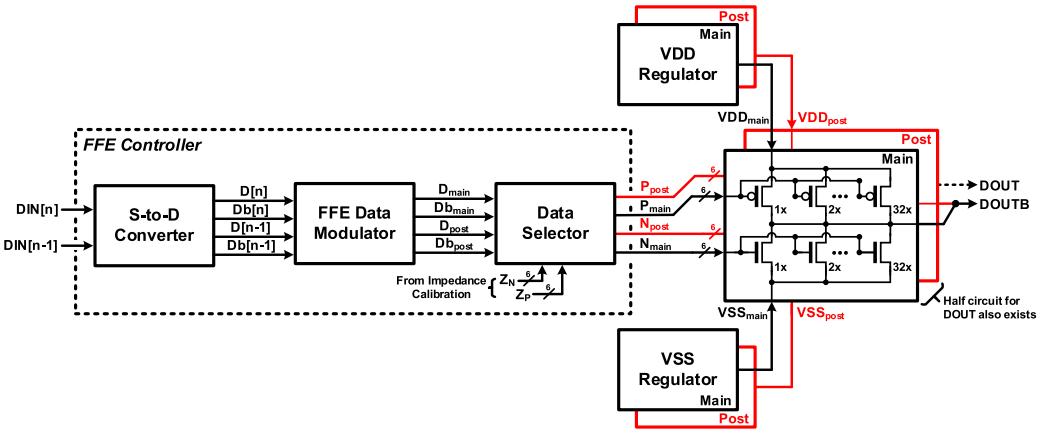


FIGURE 4. Proposed 2-tap FFE implementation using supply/ground voltage regulation, of voltage-mode output driver.

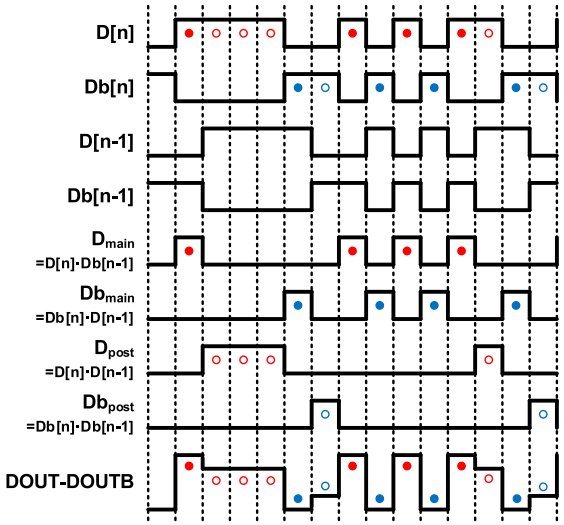


FIGURE 5. Timing diagram of FFE data modulator. In this diagram, the full-colored circle indicates the transition data, and the blank circle represents the non-transition data.

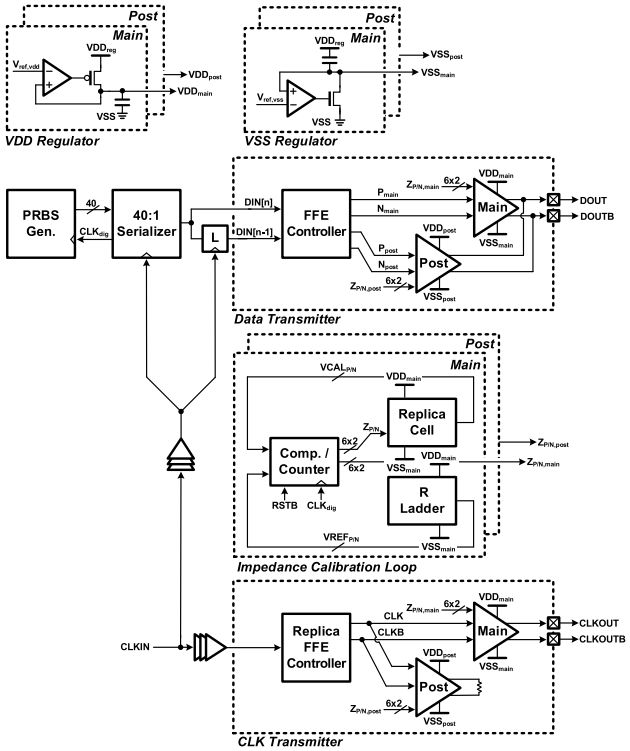


FIGURE 6. Overall architecture of the source-synchronous transmitter used to verify the FFE using dual supply/ground regulation. The FFE controller includes the S-to-D converter, the FFE data modulator, and the data selector in Figure 4.

post-layout simulations; the path delay mismatch ranged from −3.6 to 2.4 ps. The high-frequency component of the glitch noise is less than the driver's output bandwidth owing to hundreds of fF C_{IO} value; thus, the glitch is filtered out, as shown in Figure 7.

B. DUAL SUPPLY/GROUND VOLTAGE REGULATOR

In the proposed architecture, the output voltage swing, common-mode voltage, and FFE strength are independently controlled by the VDD_{main}, VDD_{post}, VSS_{main}, and VSS_{post} of the output drivers. The VDD/VSS regulator adjusts the supply/ground voltages. In this prototype, the VDD and VSS control range is from 0.6 V to 0.8 V and from 0.2 V to 0.4 V, respectively. As shown in Figure 8, there are two configurations which are used for the implementation of the on-chip VDD regulator: (1) use of a small on-chip MOSCAP and a large off-chip capacitor (Figure 8(a)), and (2) use of a small on-chip MOSCAP and a load current compensation circuit (Figure 8(b)) [12]. One of them can be selected depending on the design priority, such as the on-chip or off-chip area overhead and power overhead. The on-chip regulator with the small on-chip MOSCAP and large off-chip capacitor can reduce the on-chip area overhead, but it occupies the off-chip PCB area owing to the large off-chip capacitor. A small on-chip MOSCAP with a load current compensation circuit can reduce the on- and off-chip areas. However, this can increase the overall power consumption

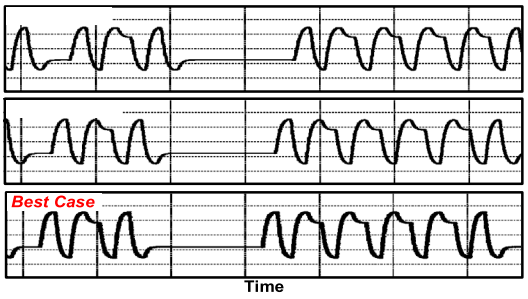


FIGURE 7. Output waveforms of the best, typical, and worst-case post-layout simulations; there is no glitch issue at the output.

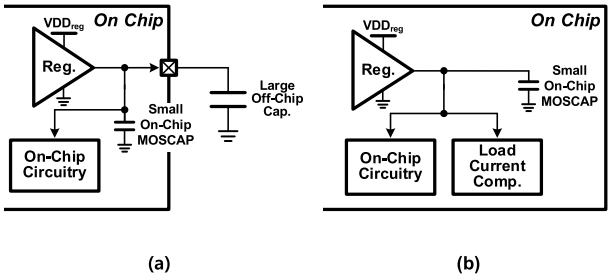


FIGURE 8. Two VDD regulator configurations using (a) a small on-chip MOSFET capacitor (MOSCAP) and a large off-chip capacitor and (b) a small on-chip MOSCAP and a load current compensation circuit [12].

owing to the compensated load current, and there can be a fluctuation of regulated supply/ground voltages due to the delay variation of the signal that drives the load current compensation circuit.

Figure 9 shows the simulation results of the regulated supply/ground voltages and load currents of the two configurations. The target VDD_{main}, VSS_{main}, VDD_{post}, and VSS_{post} are 0.8 V, 0.2 V, 0.65 V, and 0.35 V, respectively. The first configuration in Figure 8(a) uses an on-chip 3 pF MOSCAP and an 80 pF off-chip capacitor in each supply/ground voltage, while the second configuration in Figure 8(b) uses the on-chip 13 pF MOSCAP. Our simulation verified that the voltage regulator using a small on-chip MOSCAP and a large off-chip capacitor is associated with a smaller current consumption and voltage fluctuation. Increasing the on-chip MOSCAP or compensation current can reduce the supply/ground voltage fluctuations; however, it causes a large on-chip area and power overhead. Therefore, in this prototype, the on-chip regulator adopts the first configuration using the small on-chip MOSCAP and the large off-chip capacitor to reduce the on-chip area and power overhead. Although there is a minor supply/ground fluctuation during the on-switching of the main- and post-tap drivers, as shown in Figure 9(a), signal integrity can be secured by differential signaling and a larger off-chip capacitor.

To verify the power supply rejection ratio (PSRR) characteristics, we set up and performed the simulation, in which the 3 pF on-chip MOSCAP was used in each regulated voltage node. In addition, we used 30 nF off-chip capacitors. The

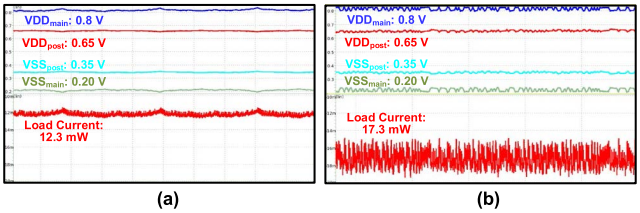


FIGURE 9. Regulated supply/ground voltages and load current of VDD/VSS regulator in two distinct configurations: (a) using a small on-chip MOSCAP and a large off-chip capacitor and (b) using a small on-chip MOSCAP and a load current compensation circuit [12].

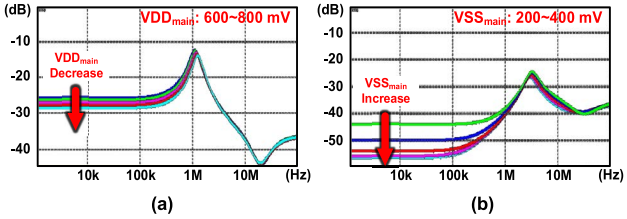


FIGURE 10. Power supply rejection ratio (PSRR) simulation results in the (a) VDD and (b) VSS regulators.

PSRR simulation results of the regulated VDD from 0.6 to 0.8 V and the regulated VSS from 0.2 to 0.4 V are shown in Figure 10(a) and (b), respectively.

C. CLOCK TRANSMITTER

The source synchronous architecture should have the same jitter profile between the data and the clock. Therefore, a clock transmitter in the clock path is designed to have the same architecture as the data transmitter to match the latency with the data path. A clock signal has one frequency component. Thus, FFE is not required. Therefore, the post-tap driver in the clock transmitter is powered off, and the replica circuit of the FFE controller passes the clock signal through.

D. IMPEDANCE CALIBRATION LOOP

The output on-resistance should be matched with the channel impedance because the impedance mismatch causes signal reflection and worsens signal integrity. Figure 11 shows a block diagram of the impedance calibration loop of the proposed transmitter. It consists of four blocks that calibrate the on-resistances of the main- and post-tap output drivers independently. Each main- and post-tap impedance calibration loop operates in the same VDD/VSS domains as the main- and post-tap drivers; this makes the on-resistances of the non-transition and transition data match the channel impedance, thus improving signal integrity. The selection code, $Z_{P/N}$, adjusts the on-resistance, thus achieving the output voltage, $VCAL_{P/N}$, by resistive division. This output voltage is compared with the reference voltage, $VREF_{P/N}$, in the comparator, and the STOP signal is output when the $VCAL_{P/N}$ level reaches the $VREF_{P/N}$ level. The counter operation ends when the STOP signal is asserted. Subsequently, the $Z_{P/N}$ codes are

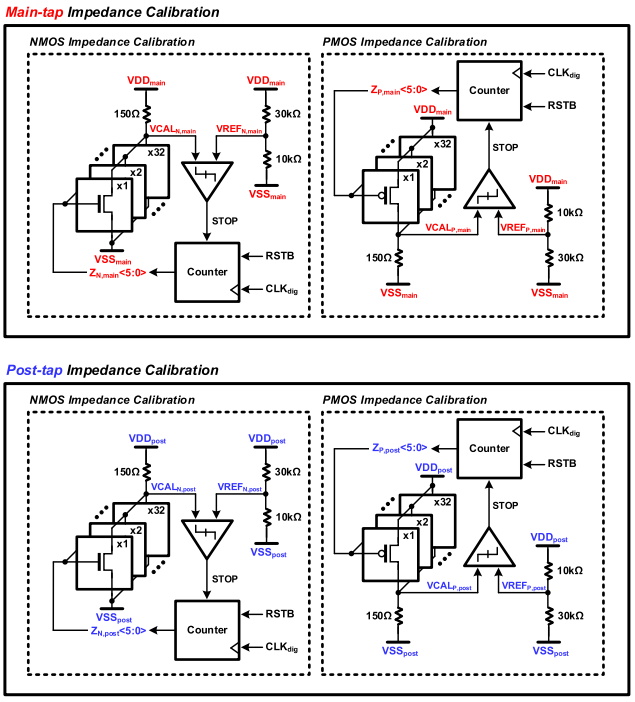


FIGURE 11. Block diagram of the main- and post-tap impedance calibration loops.

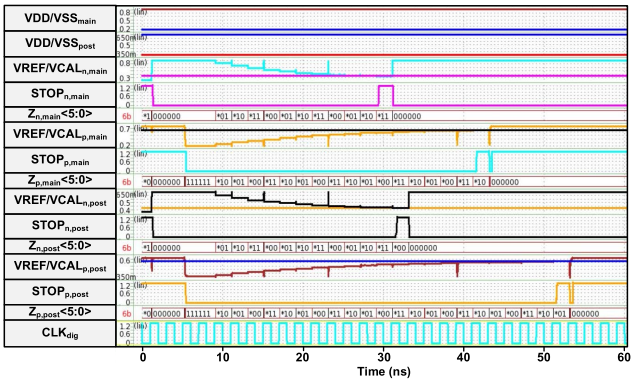
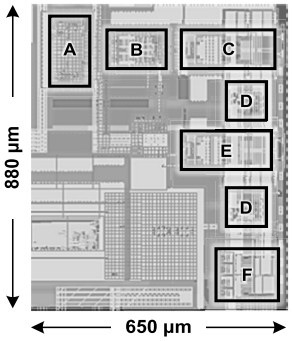


FIGURE 12. Simulated operation waveform of the impedance calibration loop.

transmitted to each transmitter, and the impedance calibration loop is powered down.

Figure 12 shows its simulated operation waveform when VDD_{main}, VSS_{main}, VDD_{post}, and VSS_{post} are 0.8 V, 0.2 V, 0.65 V, and 0.35 V, respectively. The CLK_{dig} frequency is 500 MHz. Each impedance calibration loop independently performed the aforementioned operations. This calibration was first performed after the chip was powered on to match the channel impedance. It can also be operated between data transfers to cope with voltage and temperature (VT) variations. Because this foreground impedance calibration loop does not operate during data transmission, it does not affect considerably the average power consumption of the overall operation.



	Block Description
A	PRBS Gen.
B	40:1 Serializer
C	Data Transmitter
D	VDD/VSS Regulator
E	CLK Transmitter
F	Impedance Cal. Loop

FIGURE 13. Layout of the prototype and its block description.

IV. SIMULATION RESULTS AND COMPARATIVE STUDIES

We designed a prototype of the source-synchronous transmitter in a 65 nm CMOS process. Figure 13 shows the layout of the prototype and its block description. For the comparative study, we implemented a conventional 2-tap FFE circuit using the same process, as shown in Figure 14. A total of 20 output driver segments were used, and each segment had a 1 kΩ on-resistance, which resulted in an output on-resistance of 50 Ω. In the conventional design, the FFE coefficient, α, can be controlled by adjusting the number of driver segments; for example, if the FFE coefficient, α, is equal to two, the numbers of main- and post-tap drivers are 18 and 2, respectively.

A. CURRENT CONSUMPTION

Because most of the power in the transmitter is consumed in the output driver, we simulated and compared the average current consumption of the output driver between the conventional and proposed designs, as shown in Figure 15, to verify the effectiveness. The PRBS7 data pattern was used, and the differential 100 Ω termination and 100 fF capacitors were connected to the driver's differential outputs. When the FFE strength is 4.44 dB, the average current consumption of the driver in our FFE design is 4 mA, whereas that of the driver in the conventional FFE design is 6.62 mA; therefore, the current consumption is reduced by 39.6%.

B. DEPENDENCY BETWEEN VOLTAGE SWING AND COMMON-MODE VOLTAGE

In the conventional FFE design with differential termination, assuming that the driver impedance is matched with that of the channel, the voltage swing, V_{SW}, and common-mode voltage, V_{CM}, are determined by adjusting the supply voltage as follows:

$$V_{SW} = \frac{3}{4} \cdot VDD - \frac{1}{4} \cdot VDD = \frac{1}{2} \cdot VDD \quad (1)$$

$$V_{CM} = \frac{1}{2} \cdot (\frac{3}{4} \cdot VDD + \frac{1}{4} \cdot VDD) = \frac{1}{2} \cdot VDD \quad (2)$$

Because the adjustment of the supply voltage VDD has the same effect on both the voltage swing and the common-mode voltage, the conventional design could not adjust the

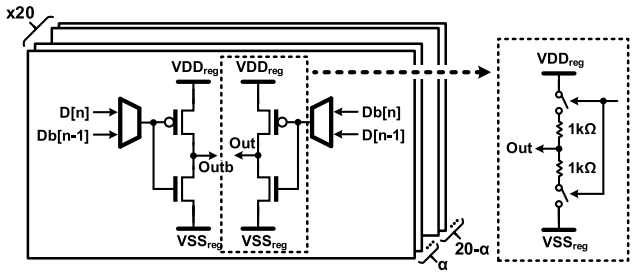


FIGURE 14. Conventional 2-tap FFE circuit diagram for comparison with our proposed FFE.

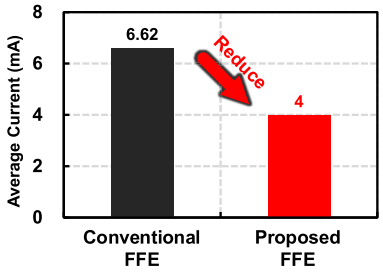


FIGURE 15. Simulated average current consumption of output driver in conventional and proposed FFE implementations when all FFE strengths are 4.44 dB.

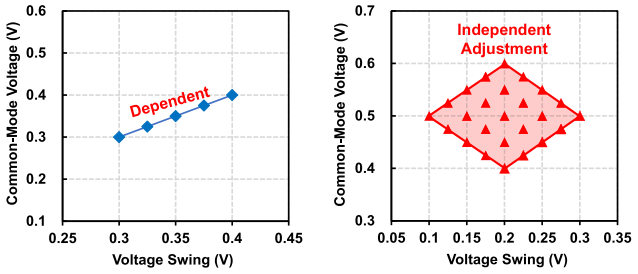


FIGURE 16. Relationship between the common-mode voltage and voltage swing in the (a) conventional and (b) proposed transmitters.

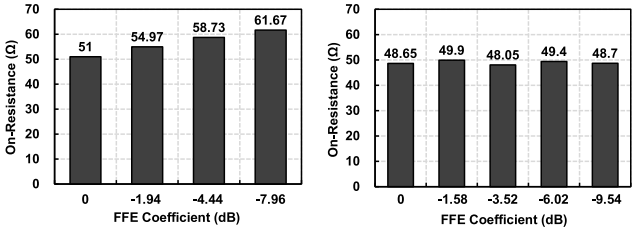


FIGURE 17. Simulated worst-case on-resistance of the (a) conventional and (b) proposed FFE designs.

voltage swing and the common-mode voltage independently, as shown in Figure 16(a). In this figure, the control range of VDD is from 0.6 V to 0.8 V with 0.05 V resolution. The proposed FFE design can adjust the voltage swing and output common-mode voltage by regulating both the supply and ground voltages as follows:

$$\begin{aligned} V_{SW} &= \left\{\frac{3}{4}\cdot(VDD_{main}-VSS_{main})+VSS_{main}\right\} \\ &\quad -\left\{\frac{1}{4}\cdot(VDD_{main}-VSS_{main})+VSS_{main}\right\} \\ &= \frac{1}{2}VDD_{main}-\frac{1}{2}VSS_{main} \qquad (3) \\ V_{CM} &= \frac{1}{2}VDD_{main}+\frac{1}{2}VSS_{main} \qquad (4) \end{aligned}$$

This can achieve independent adjustment of the voltage swing and common-mode voltage by regulating the VDD_{main} and VSS_{main}, respectively. Figure 16(b) shows the independent relationship between the voltage swing and the common-mode voltage. The control ranges of VDD_{main} and VSS_{main} are from 0.6 V to 0.8 V and from 0.2 V to 0.4 V, respectively, with 0.05 V resolution.

C. ON-RESISTANCE

The on-resistance determines the voltage swing and impedance matching characteristic. Therefore, the on-resistance of the output driver must be calibrated to have a resistance of 50 Ω. Its on-resistance depends on the V_{ds} as follows:

$$R_{on} \propto 1/V_{ds} \qquad (5)$$

In the conventional FFE design, the on-resistance is calibrated based on the output voltage level of the transition data (main-tap voltage level). Thus, the on-resistance of the non-transition data transmission deviates from 50 Ω owing to the V_{ds} change [22]. Figure 17(a) shows the worst-case on-resistance of the conventional FFE design. As shown, the worst-case on-resistance occurs when non-transition data are transmitted. The on-resistance deviation causes variations in the FFE coefficients; thus, the equalization performance is degraded. This phenomenon is discussed in detail in Section IV.E. Because the proposed scheme calibrates the on-resistance in each main- and post-tap driver, the on-resistance value during transition and non-transition data transmissions remain around 50 Ω, as shown in Figure 17(b), thus improving signal integrity.

Figure 18 shows the simulated average on-resistances of the proposed transmitter in three corner cases: TTTT, SSSS, and FFFF. At each FFE coefficient, the on-resistances of the PMOS and NMOS, $R_{on,p}$ and $R_{on,n}$, remain almost equal to 50 Ω, thus making the target output voltage swing correct and matching with the channel impedance.

D. RETURN LOSS

The return loss (S_{11}) is an important parameter when designing high-speed transmitters [23]. This parameter is given by

$$S_{11} = 20\cdot log_{10}|r| \qquad (6)$$

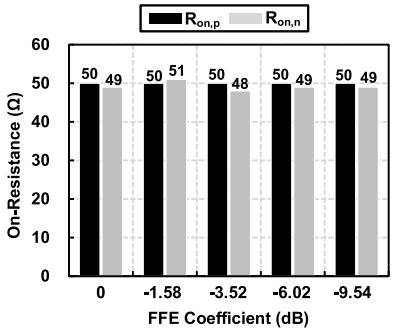


FIGURE 18. Simulated average PMOS and NMOS on-resistances, $R_{on,p}$ and $R_{on,n}$, of the proposed transmitter in three corner cases: TTTT, SSSS, and FFFF.

where r is the output reflection factor, which is given by

$$r = \frac{Z_{TX} - Z_{CH}}{Z_{TX} + Z_{CH}}. \tag{7}$$

Our channel model for the experiment has a characteristic impedance, Z_{CH}, equal to 50 Ω. The output impedance of the transmitter, Z_{TX}, is composed of the MOS transistor resistance of the output driver, parasitic capacitance, packaging, and electrostatic discharge diode (ESD). In the return loss parameter, the high-frequency component indicates the capacitive discontinuities caused by parasitic capacitance, packaging, and ESD [23]. In our simulation setup, packaging and ESD were not included.

The impedance calibration loop determines the on-resistance or the large-signal (DC) resistance. However, the small-signal (AC) resistance can deviate from the DC resistance owing to V_{ds} variation during the transmission operation [12]. Therefore, AC resistance affects the low-frequency characteristic of the return loss. When FFE is used, the return loss characteristics at low frequencies will be affected adversely depending on how much the on-resistance deviates from 50 Ω during non-transition data transmission.

To verify this, the differential-mode return losses of the conventional and proposed transmitters were simulated, as shown in Figure 19. These results were divided into transition and non-transition data return losses. The transition data are the main-tap data, and the non-transition data refer to the post-tap data [6]. The conventional transmitter with a 2-tap FFE calibrates the impedance based on the voltage level of the main-tap data. Therefore, V_{ds} variation occurs on non-transition data transmission, leading to the AC resistance deviation. As the FFE coefficient increases, V_{ds} increases, thereby deteriorating the return loss (Figure 19(a)).

The proposed transmitter using a 2-tap FFE can calibrate each main- and post-tap on-resistance based on consideration of V_{ds} changes. Therefore, the return loss of the non-transition data does not deteriorate; instead, it improves because the AC resistance deviation is small owing to the small V_{ds} range under the regulated supply/ground voltage, as shown in Figure 19(b) [12]. Therefore, the proposed FFE

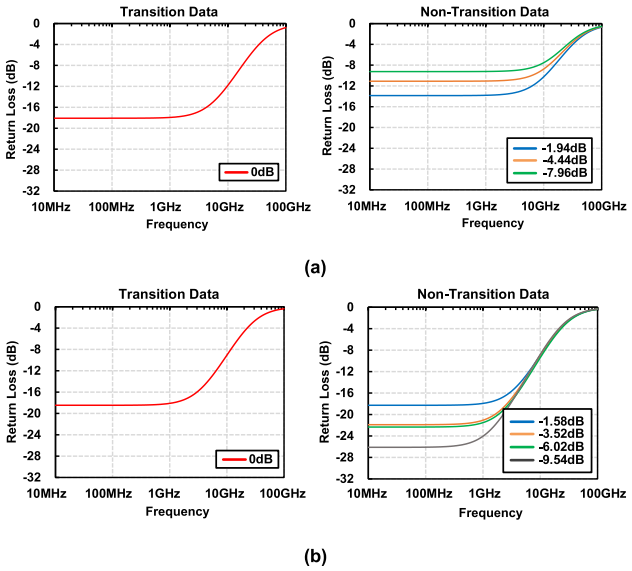


FIGURE 19. Simulated differential-mode return losses of transition and non-transition data in (a) conventional and (b) proposed transmitters according to FFE coefficients.

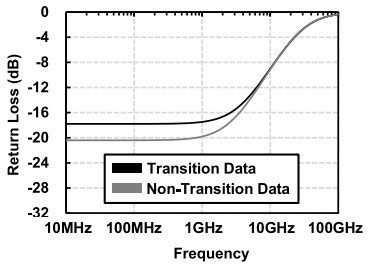


FIGURE 20. Simulated average differential-mode return loss of the proposed transmitter in three corner cases, namely, TTTT, SSSS, and FFFF.

can have a better output signal quality compared with the conventional FFE structure.

Figure 20 shows the simulated average differential-mode return loss of the proposed method in three corner cases, namely, TTTT, SSSS, and FFFF. The differential output voltage swing of the transition data was 0.6 V, and that of the non-transition data was 0.4 V. This shows that the proposed transmitter has good return-loss characteristics on both transition and non-transition data transmission, thus securing signal integrity.

E. FFE STRENGTH AND OUTPUT VOLTAGE LEVEL

One of the advantages of the proposed transmitter is flexible FFE strength adjustment. Figure 21 shows the output high and low voltage levels of the conventional and proposed transmitters according to the FFE strength when VDD is 0.8 V and VSS is 0.2 V. For the conventional transmitter in Figure 14, the FFE strength can be controlled by adjusting the number of drivers allocated to the main and post-tap out of 20 driver segments; thus, discrete control is only possible. To achieve a finer adjustment of the FFE strength,

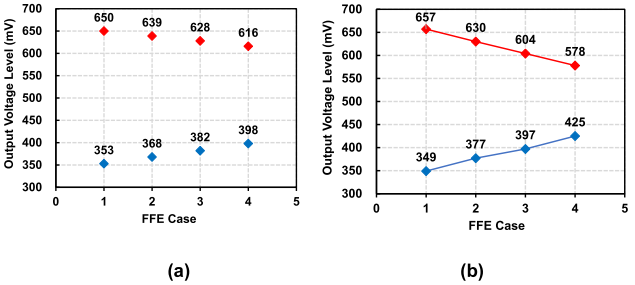


FIGURE 21. Output high and low voltage levels of the (a) conventional and (b) proposed transmitters according to the FFE strength.

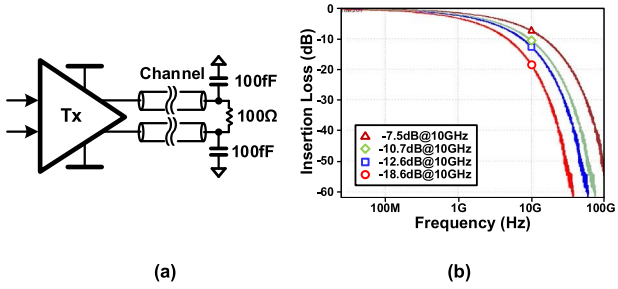


FIGURE 22. (a) Simulation setup used to measure the eye diagram, and (b) insertion loss plots for four channel environments.

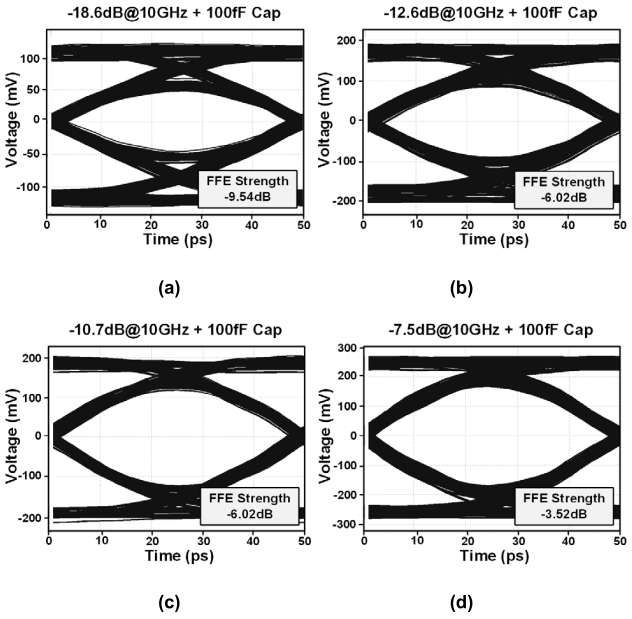


FIGURE 23. Simulated differential eye diagrams for a variety of channel insertion losses with 100 fF capacitor using a PRBS7 data pattern at 20 Gb/s: (a) −18.6 dB@10 GHz, (b) −12.6 dB@10 GHz, (c) −10.7 dB@10 GHz, and (d) −7.5 dB@10 GHz. The differential output voltage swing is 0.6 V. Each FFE strength is also displayed in the eye diagram.

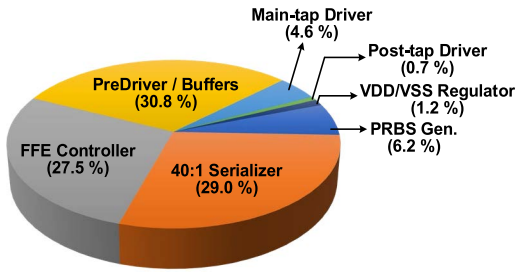


FIGURE 24. Power breakdown of data transmitter at 20 Gb/s when voltage swing of 0.3 V and FFE of −6.02 dB are used.

the number of segments should be increased, but it is limited by the process and the design based on the consideration of PVT variations. That is, because the minimum size in one output driver segment cannot be changed owing to the process dependency, the segmentation number is limited. Thus, it is difficult to achieve a fine FFE resolution. In addition, because the on-resistance is determined based on the main-tap voltage level, as the FFE strengthens, the on-resistance deviates from the optimum point owing to V_{ds} variation, as shown in Figure 17(a) in which the average differential nonlinearity (DNL) is 0.25 least sequence bit (LSB).

As shown in Figure 21(b), the FFE strength in the proposed transmitter can be controlled linearly owing to the constant on-resistance. The average DNL is 0.05 LSB. This result shows only four cases for comparison, but it can be adjusted more finely owing to its analog controllability. Thus, this graph is plotted using lines rather than discrete points to indicate that fine-tuning is possible.

F. EYE DIAGRAM

Figure 22(a) shows the simulation setup used to measure the eye diagram. Our prototype transmitter is connected to a differential 100 Ω termination and 100 fF capacitors after the channel. The insertion losses for the four channel environments used in this simulation are shown in Figure 22(b).

Figure 23 shows the simulated differential eye diagrams for various channel environments shown in Figure 22(b). The PRBS7 data pattern was used, the differential output voltage swing was 0.6 V, and the data rate was 20 Gb/s. These results show that our transmitter can cope with various channel environments. Therefore, the proposed flexible FFE adjustment scheme can be adopted for a more diverse channel environment with a single structure and can be used together with the independent voltage swing and common-mode voltage adjustment to accommodate a variety of standards [8], [14].

G. POWER BREAKDOWN

Figure 24 shows a power breakdown of the data transmitter at 20 Gb/s when a voltage swing of 0.3 V and FFE of −6.02 dB are used. Its total power consumption is 44.70 mW. The largest power consumption blocks are the 40:1 serializer, FFE controller, and predriver and buffers. The main- and post-tap drivers only account for 4.6 % and 0.7 %, respectively, of the overall power consumption owing to the use of the proposed FFE method.

TABLE 1. Design summary and comparison with other recent transmitter designs using feed-forward equalization.

	This Work	[6]	[8]	[10]	[12]	[16]
Process	65 nm CMOS	28 nm CMOS	16 nm FinFET	65 nm CMOS	16 nm CMOS	65 nm CMOS
Supply Voltage	1.2 V	1.05 V	0.9/0.9/1.2 V	1.5/1.1 V	-	1 V
Maximum Data Rate	20 Gb/s	3.2 Gb/s	16.3 Gb/s	32 Gb/s	32.75 Gb/s	8 Gb/s
Driver Type	Voltage-Mode	LVDS	Current-Mode	Voltage-Mode	Voltage-Mode	Voltage-Mode
Equalization	2-tap FFE	2-tap FFE	3-tap FFE	2-tap FFE	3-tap FFE	2-tap FFE
Independently Controllable of Output Characteristics?	Yes	Yes	No	No	Yes	No
Voltage Swing Range [a]	0.10–0.30 V	0.11–0.54 V	N/A	0.2–0.65 V	0.13–0.45 V	0.05–0.15 V
Common-mode Voltage Range	0.40–0.60 V	0.29–0.61 V	N/A	N/A	N/A	N/A
FFE Strength Adjustment	Voltage Regulation	Driver Segmentation	Driver Segmentation	Driver Segmentation	Driver Segmentation	Boosting Current
FFE Strength Controllable finely and linearly?	Yes	No	No	No	No	No
Impedance Matching with Non-Transition Data	Yes	Yes	Yes	No	No	Yes
Energy Efficiency (Voltage Swing, FFE Strength)	2.23 pJ/bit [b] @20 Gb/s (0.30 V, -6.02 dB)	3.90 pJ/bit @3.2 Gb/s (0.54 V, N/A)	2.96 pJ/bit @16.3 Gb/s (N/A, N/A)	2.74 pJ/bit @32 Gb/s (N/A , N/A)	3.69 pJ/bit @32.75 Gb/s (N/A, N/A)	0.33 pJ/bit @8 Gb/s (0.08 V, -6.0dB)

[a] Single-ended voltage swing

[b] Energy efficiency of data transmitter based on post-layout simulation result

H. COMPARISON WITH OTHER DESIGNS USING FFE

Our design is summarized and compared with other recent transmitters using FFE in Table 1. With a single design, our transmitter can independently and finely control the output voltage swing, common-mode voltage, and FFE strength. Furthermore, the dual supply/ground voltage regulation makes impedance matching with non-transition data as well as transition data. This proposed design has an energy efficiency of 2.23 pJ/bit at 20 Gb/s, when the voltage swing of 0.3 V and the FFE of −6.02 dB is used.

A low-voltage differential signaling (LVDS) driver with coupled-bias common-mode feedback [6] can independently adjust the output characteristics and match the impedance during non-transition data transmission. However, it is difficult to control the FFE strength finely and linearly due to the driver segmentation method, and its current-mode LVDS scheme consumes large power. A voltage-mode driver with 2-tap FFE using boosting current [16] can have good impedance matching characteristics even when non-transition data are transmitted; however, this voltage-mode structure cannot achieve independent controllability of output characteristics with a single design, and V_{ds} variation changes the boosting current, thus making the linear FFE control difficult.

V. CONCLUSION

We present a 2-tap FFE voltage-mode transmitter using dual supply/ground voltage regulation. This analog-based FFE structure can achieve flexible FFE adjustment with impedance matching of both transition and non-transition data transmissions, thus achieving good on-resistance and return loss characteristics. In addition, the short current path is removed, thereby reducing the overall power consumption. With dual supply/ground voltage regulation, the output characteristics, such as the output swing and common-mode voltage can be adjusted independently. In other words, the proposed architecture can be used in multiple standards and channel environments.

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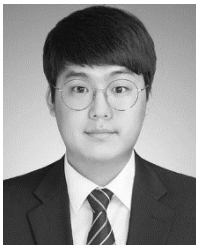

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