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Performance Improvement of Dual-Buck Inverter With Mitigating Reverse Recovery Characteristics and Supporting Reactive Power

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ABSTRACT This paper proposes a three-level dual-buck inverter (DBI) that reduces reverse recovery current and compensates reactive power. To reduce the reverse recovery problem of main switching diodes in the DBI, the auxiliary circuit consisting of diodes and coupled inductors is adapted. The auxiliary circuit enables zero-current turn-off of the diodes. The coupled inductor design is also conducted considering not only for unity power factor (PF) but also non-unity PF operations. By utilizing the auxiliary circuit, the reverse recovery and the shoot-through problems in silicon devices can be significantly mitigated so that the efficiency and the reliability of the DBI are much improved. Meanwhile, the pulse-width modulation scheme is also proposed to supply reactive power with the DBI which is a unidirectional inverter. In the proposed modulation method, the duty offset is simply added according to the required PF and the operating region of the DBI. By doing so, traditional current control concepts for bidirectional inverters can be directly applied to the DBI without any modification. By utilizing the proposed techniques, the reliability, efficiency, and utilization of the DBI can be significantly improved. The experimental results with a 3 kVA DBI prototype demonstrate the effectiveness of the proposed DBI.

INDEX TERMS DC-AC power conversion, inductors, modulation, photovoltaic power systems, pulse width modulation, reactive power.

I. INTRODUCTION

As the penetration of the distributed generation (DG) into the distribution networks continues to increase, the DGs are required to participate in the grid stability control [1]–[15]. One of the requirements is the low voltage ride through [1]–[5]. In case of a grid fault, the DGs should be connected to the grid for the specified voltage and time, and then inject the reactive power to support the grid. Another important role is the point of common coupling (PCC) voltage regulation [6]–[15]. The DGs lead bidirectional power flow in the distribution networks. This power flow and the line impedance cause the voltage rise or drop at PCC of each DGs. Thus, the active and reactive powers of the DGs should be adjusted to compensate the PCC voltage fluctuation. In photovoltaic (PV) systems, inverters with a unidirectional power transfer characteristic such as H5, highly efficient and reliable inverter concept (HERIC) and dual-buck inverter (DBI) have been widely applied because of their high efficiency and low leakage current [16]–[31]. However, the reactive power control with the unidirectional topologies is relatively limited, because their switching pattern and modulation scheme are somewhat different with traditional inverters.

To overcome these constraints, it has been studied that the inverters with the unidirectional characteristics provide a reactive power. In [16], the principle of reactive power generation of PV inverters was analyzed, and it was found that freewheeling paths are required in the negative power direction. A modulation scheme that provides the freewheeling paths for reactive power generation has also been proposed. This has been applied and verified only with H5 and HERIC. A high efficiency transformerless PV inverter is proposed in [17], and a modulation technique for this inverter to supply reactive power is presented in [18]. The switching legs of this inverter consist of metal oxide semiconductor field effect transistors (MOSFETs) and diodes as DBIs. This inverter

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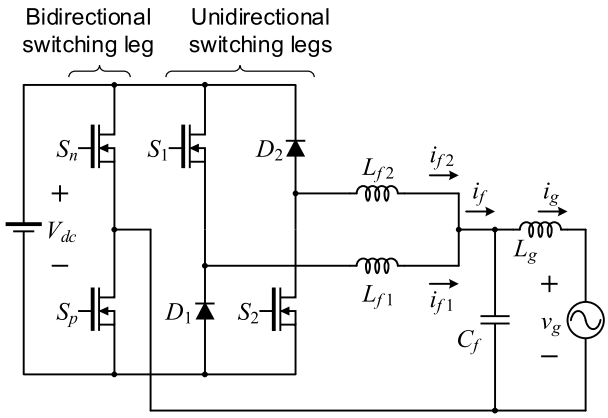

FIGURE 1. Traditional three-level DBI.

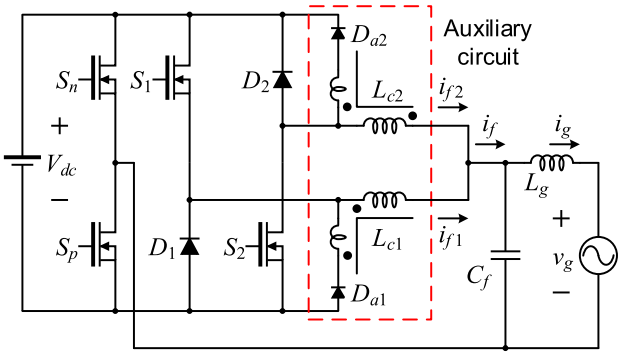

FIGURE 2. Three-level DBI with the proposed auxiliary circuits.

accomplishes high efficiency, high reliability, and reactive power generation, but requires many switching devices.

The DBIs also have been studied to work under non-unity power factor (PF) conditions. There are various dual-buck structures [19]–[36]. A half-bridge DBI (HBDBI) for energy storage system (ESS) with a capability of bidirectional power flow was proposed in [19]. However, an input voltage of the HBDBI has to be at least twice an output voltage, resulting in high voltage stress on components of the system [20]. In [21], the DBI can generate reactive power, but it is constructed in cascade. A DBI was modified to use single filter inductor in [22]. Although operation mode is analyzed for reactive power generation, there are no results for non-unity PF operation.

A three-level DBI shown in Fig. 1 is proposed in [23]–[26]. The DBI consists of a bidirectional switching leg and two unidirectional switching legs. Since the bidirectional switching leg operates at the grid frequency, switching losses and a shoot-through phenomenon from this leg can be inherently removed. The switching losses from the unidirectional switching legs are also low, because only one switch is driven at a high switching frequency for the half cycle of the grid voltage [23]. Moreover, the three-level DBI restrains the leakage current, which is caused by the parasitic capacitance between the PV panel and the ground of the grid [22]–[25]. In [26], the three-level DBI with a bidirectional power conversion capability was presented. However, the operation in non-unity PF condition has not been verified.

In dual-buck topologies, a body diode of MOSFET does not conduct current. So, there is no reverse recovery issues of the body diode [28]–[34]. However, a diode in a switching leg still has the reverse recovery problems, which reduce the reliability. To improve the reliability, silicon carbide (SiC) Schottky diodes are employed in [18], [23]. By using SiC devices, the reverse recovery issues can be easily avoided, and high efficiency can be also achieved. In industrial applications, however, the use of silicon (Si) devices is still preferred due to the high cost of SiC devices [37].

With Si devices, auxiliary circuits are adapted to reduce the reverse recovery problem. In order for synchronous converters to achieve zero voltage switching (ZVS), employing auxiliary circuits has been proposed in [38], [39]. To achieve ZVS turn-on, they require a switching leg that allows current to flow in bidirectional. Therefore, they cannot be directly applied to the DBIs which have unidirectional switching legs. Buck and boost converters with an auxiliary circuit are introduced in [40], [41], respectively. The turn-off rates of diodes are regulated by an auxiliary coupled inductor so that the reverse recovery problems are mitigated. In a similar way, a bridgeless boost rectifier and a dual-paralleled-buck inverter that reduced the reverse recovery problems were presented in [42], [43]. They consist of unidirectional switching legs similar to the DBI, and the design of the auxiliary coupled inductor to reduce the reverse recovery current is introduced. However, in [42], the current ripple was defined as the same as the conventional converters, which may result a difficulty in design process. In addition, all analyses in [42], [43] were performed only for unity PF operation.

This paper proposes two engineering techniques to improve the reliability, the efficiency, and the usability of single-phase DBIs. First, the auxiliary circuit consists of a diode with a coupled inductor is adapted to mitigate the reverse recovery problem of a main switching leg in the DBI. By doing so, passive snubber circuits can be removed, and faster switching of the active device is achievable as well as improving the efficiency of the DBI. Second, the modified pulse-width-modulation (PWM) strategy for the DBI is suggested to provide the capability of reactive power supply to the utility grid. By using the proposed PWM method, both leading and lagging PF operations are easily implemented so that utilization rate of the DBI can be enhanced.

This paper is organized as follows. Section II provides an analysis of the proposed DBI. In Section III, the design of the coupled inductor is described. The experimental results are presented in Section IV to verify the effectiveness of the proposed inverter.

II. PROPOSED DUAL-BUCK INVERTER

Fig. 2 shows the three-level DBI employing the proposed auxiliary circuit configuration which consists of two auxiliary diodes and two coupled inductors, L_{c1} and L_{c2}, for positive

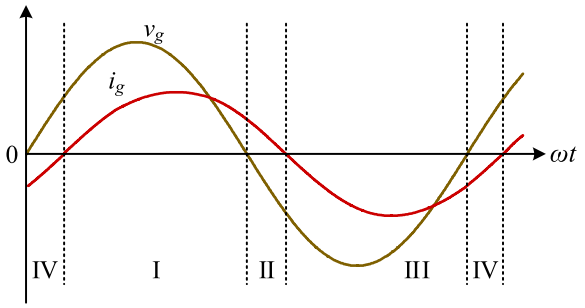

FIGURE 3. Definition of the operating region under different polarities of v_g and i_g.

TABLE 1. Definition of operating region.

Operating Region	Polarity	
	v_g	i_g
I	positive	positive
II	negative	positive
III	negative	negative
IV	positive	negative

and negative grid voltage cycles. Here, the filter inductors L_{f1} and L_{f2} in traditional three-level DBI shown in Fig. 1 are replaced with L_{c1} and L_{c2}. The main role of the auxiliary circuits is to smooth out the slope of turn off current in the main switching diodes D_1 and D_2 so that the reverse recovery problem can be lessened. It should be noticed that the proposed auxiliary circuit can be easily adapted to any types of DBI structure regardless of the three-level DBI configuration which is dealt in this paper. Like the traditional three-level DBI, the bidirectional switching leg with S_p and S_n is synchronized to the fundamental frequency of the utility grid while the unidirectional legs are switched at the high switching frequency.

Fig. 3 defines the operating region of the proposed inverter. By referring Fig. 3, Table 1 summarizes the relationship between the operating region and the polarities of the grid voltage v_g and the grid-side current i_g. According to the operating region, the analysis of the current conduction path is different, and it will be detailed in later sections. It should be noticed that regions I and III appear when the inverter is at the unity PF operation while regions II and IV turn up under non-unity PF operation which is not the case in traditional DBIs.

A. OPERATING MODE ANALYSIS WITH THE AUXILIARY CIRCUIT

Figs. 4 and 5 represent the equivalent circuit of the proposed DBI and the switching waveforms during one switching period in regions I and II where the polarity of i_g is positive. In Fig. 4, the equivalent expression of L_{c1} in Fig. 2 is represented by the primary self-inductance L_p, the

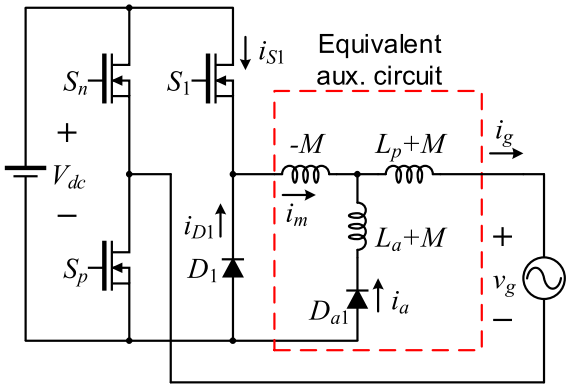

FIGURE 4. Equivalent circuit of the proposed inverter in region I and II.

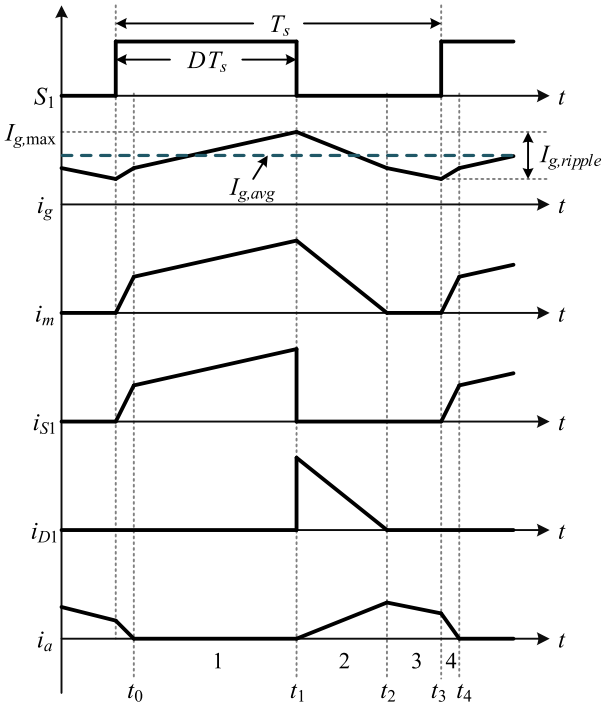

FIGURE 5. Switching waveforms in region I and II.

secondary self-inductance L_a, and the mutual inductance M considering the dot convention [38]. To simplify the analysis, the filter capacitor C_f and the grid-side inductor L_g are neglected, and the charging and discharging transients of the output capacitance in the switching devices are not considered.

The operation modes in region I where S_p is turned on are shown in Fig. 6. By referring Figs. 5 and 6, the operation mode analysis is conducted as follows.

Mode 1 (*Interval* 1): At t_0, S_1 is already turned on, and D_1 and D_{a1} are turned off. The output current i_g and the current path through the mutual inductance i_m increase up to $I_{g,\max}$. At this condition, the slope of i_g is obtained as follows:

$$\frac{di_g}{dt} = \frac{di_m}{dt} = \frac{V_{dc} - v_g}{L_p} \tag{1}$$

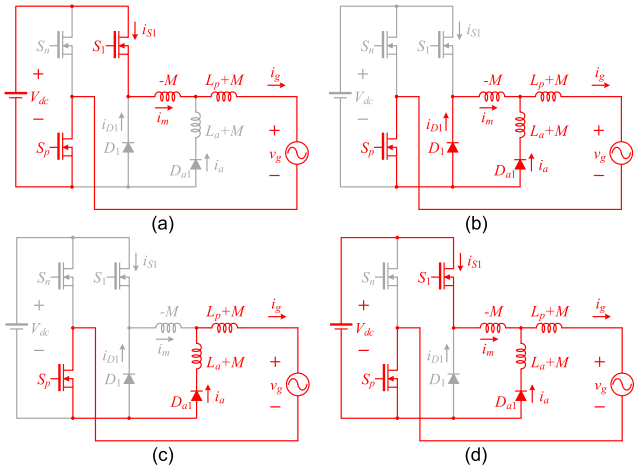

FIGURE 6. Operation modes in region I. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

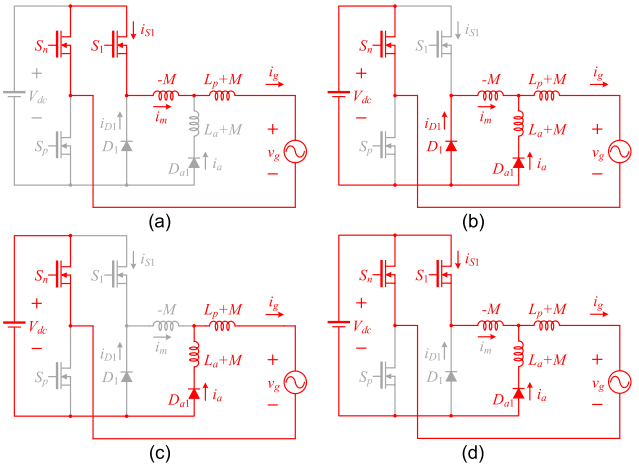

FIGURE 7. Operation modes in region II. (a) Mode 5. (b) Mode 6. (c) Mode 7. (d) Mode 8.

Mode 2 (*Interval* 2): When S_1 is turned off, i_g flows through D_1 and D_{a1}. Here, i_g is represented as:

$$i_g = i_m + i_a \tag{2}$$

where

$$i_m = i_{D1} \tag{3}$$

Since S_1 is turned off, i_m decreases from $I_{g,\max}$ until zero. According to (3), i_{D1} becomes zero at t_2, so that D_1 is turned off at the zero current condition so that no reverse recovery current is built up. Meanwhile, the auxiliary path current i_a takes i_g, and it flows via D_{a1}. By considering the coupled inductor effect, the current equations of i_g, i_m, and i_a are derived as:

$$\frac{di_g}{dt} = \frac{-L_a v_g}{L_p L_a - M^2} \tag{4}$$

$$\frac{di_m}{dt} = \frac{-\left(L_a + M\right) v_g}{L_p L_a - M^2} \tag{5}$$

$$\frac{di_a}{dt} = \frac{M v_g}{L_p L_a - M^2} \tag{6}$$

Mode 3 (*Interval* 3): This interval starts when i_m reaches zero. At this interval, i_g is the same as i_a, and continuously decreases with the slope derived as in (7) until S_1 is turned on.

$$\frac{di_g}{dt} = \frac{di_a}{dt} = \frac{-v_g}{L_p + L_a + 2M} \tag{7}$$

Due to the increased equivalent inductance, the slope is less steep than previous interval as can be seen in Fig. 5.

Mode 4 (*Interval* 4): At t_4, as S_1 is turned on, i_m increases from zero through S_1, and i_a decreases. This interval keeps going until i_a fully reaches zero, and D_{a1} is also under zero current turn off condition. The slopes of individual inductor currents are written as:

$$\frac{di_g}{dt} = \frac{\left(L_a + M\right) V_{dc} - L_a v_g}{L_p L_a - M^2} \tag{8}$$

$$\frac{di_m}{dt} = \frac{\left(L_p + L_a + 2M\right) V_{dc} - \left(L_a + M\right) v_g}{L_p L_a - M^2} \tag{9}$$

$$\frac{di_a}{dt} = \frac{-(L_p + M) V_{dc} + M v_g}{L_p L_a - M^2} \tag{10}$$

For region II which turns up when a reactive power is injected, the operation modes are described in Fig. 7. As similar to the analysis taken in region I, the equations for the inductor currents can be obtained according to the operation modes as follows.

Mode 5 (*Interval* 1):

$$\frac{di_g}{dt} = \frac{di_m}{dt} = -\frac{v_g}{L_p} \tag{11}$$

Mode 6 (*Interval* 2):

$$\frac{di_g}{dt} = \frac{-L_a \left(V_{dc} + v_g\right)}{L_p L_a - M^2} \tag{12}$$

$$\frac{di_m}{dt} = -\frac{\left(L_a + M\right) \left(V_{dc} + v_g\right)}{L_p L_a - M^2} \tag{13}$$

$$\frac{di_a}{dt} = \frac{M \left(V_{dc} + v_g\right)}{L_p L_a - M^2} \tag{14}$$

Mode 7 (*Interval* 3):

$$\frac{di_g}{dt} = \frac{di_a}{dt} = -\frac{V_{dc} + v_g}{L_p + L_a + 2M} \tag{15}$$

Mode 8 (*Interval* 4):

$$\frac{di_g}{dt} = \frac{M V_{dc} - L_a v_g}{L_p L_a - M^2} \tag{16}$$

$$\frac{di_m}{dt} = \frac{\left(L_p + M\right) V_{dc} - \left(L_a + M\right) v_g}{L_p L_a - M^2} \tag{17}$$

$$\frac{di_a}{dt} = \frac{-L_p V_{dc} + M v_g}{L_p L_a - M^2} \tag{18}$$

The same analysis can be also made for regions III and IV where i_g is negative, but it is omitted in this paper. From the mode analysis above, it is found that each interval has two

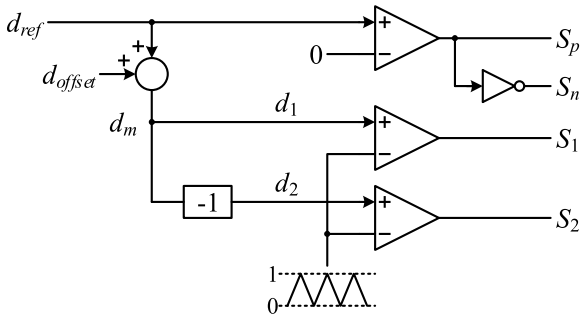

FIGURE 8. Proposed modulation method using d_{offset}.

TABLE 2. Determination of d_{offset} according to polarity.

Polarity		d_{offset}
d_{ref}	i_{ref}	
positive	positive	0
negative	positive	1
negative	negative	0
positive	negative	-1

individual current equations in regions I and II, respectively, e.g., (1) and (11). In these equations in the same interval, the inductance coefficients are the same, but the applied voltages and the polarity are different. Due to this dissimilarity, the ZCS turn off may not be fully guaranteed in regions II and IV, and this will be described in Section III.

B. MODULATION STRATEGY FOR NON-UNITY PF OPERATION

For non-unity PF operation where the inverter injects a reactive power into the utility grid, the inverter should be capable of operation under both buck and boost modes [16]. In regions I and III in Fig. 3 where both v_g and i_g are positive, the DBI operates in buck mode, and the relationship among the duty cycle D, v_g, and V_{dc} is written as (19).

$$D = \frac{|v_g|}{V_{dc}} \tag{19}$$

In regions II and IV, the output power is negative, because the polarities of v_g and i_g are opposite. At this condition, the inverter works in boost mode, and D in regions II and IV is derived as below:

$$D = 1 - \frac{|v_g|}{V_{dc}} \tag{20}$$

In order for the inverter to operate under non-unity PF, the duty cycle must be generated for each mode, which requires a nonlinear duty reference. However, the nonlinear duty reference includes very high order harmonics, which are above the bandwidth of typical current controllers such as a proportional-integral (PI) or a proportional-resonant

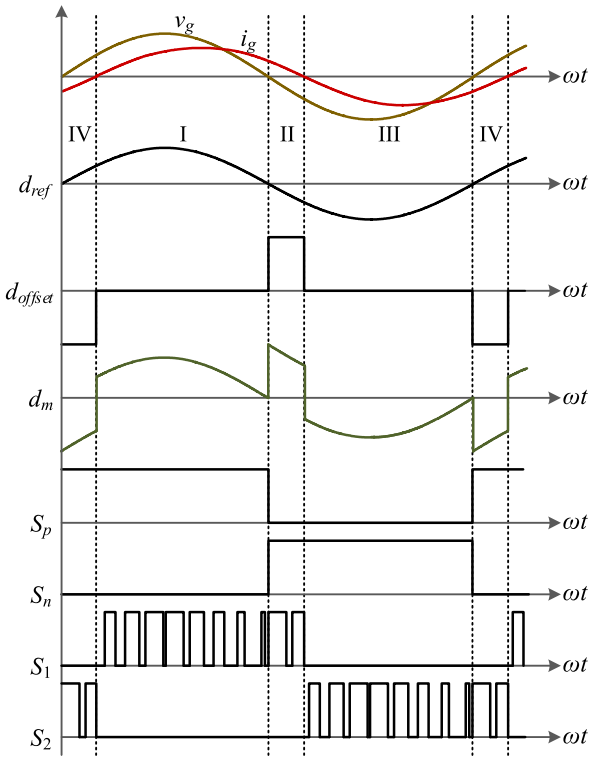

FIGURE 9. Waveforms of the DBI with the proposed modulation method.

(PR) controller. It causes the output current distortion under non-unity PF condition.

In this paper, a modulation method is proposed to enable that the DBI is operated under non-unity PF condition while a sinusoidal duty reference is generated. Therefore, the inverter current can be regulated with general controller. The proposed modulator is depicted in Fig. 8. The duty reference d_{ref} is generated by the current controller. The switches of the bidirectional switching leg are operated according to the polarity of the sinusoidal d_{ref} regardless of the operating mode. A duty offset d_{offset} is determined by the polarity of d_{ref} and a current reference i_{ref} as shown in Table 2. A modified duty reference d_m is generated by combining d_{ref} and d_{offset}. The duty references for S_1 and S_2 are d_1 and d_2, respectively. When the DBI is operated as shown in Fig. 3, the waveforms of d_{ref}, d_{offset}, d_m and switching patterns are illustrated in Fig. 9.

III. DESIGN OF THE COUPLED INDUCTOR

The main role of the auxiliary circuits is to alleviate the reverse recovery problems. For positive i_g, the slope of i_{D1} is regulated by parameters of L_{c1}. Thus, L_{c1} should be designed to reduce the reverse recovery current of D_1. This consideration also applies for D_2 and L_{c2} when i_g is negative, so L_{c1} and L_{c2} are designed equally as L_c. In order to reduce the reverse recovery current of D_1, i_{D1} must reach zero while S_1 is turned off. This means that the slopes of i_m in interval 2 meet the following criteria:

$$\left| \frac{-(L_a + M)\, v_g}{L_p L_a - M^2} \right| (1 - D)\, T_s \geq I_{g,\max} \tag{21}$$

$$\left|-\frac{(L_a+M)\left(V_{dc}+v_g\right)}{L_pL_a-M^2}\right|(1-D)\,T_s \geq I_{g,\max} \tag{22}$$

where (21) is for mode 2 in region I, and (22) is for mode 6 in region II. If the current controller regulates $I_{g,avg}$ in Fig. 5 which is the average value of i_g during a switching period to accurately track i_{ref}, $I_{g,\max}$ can be assumed as below:

$$I_{g,\max} \approx i_{ref} + \frac{I_{g,ripple}}{2} \tag{23}$$

If the slope of i_m in mode 2 has a minimum value that satisfies (21) and (22), mode 3 does not exist. Then, based on (4) and (12), the output current ripple $I_{g,ripple}$ for each mode is obtained as follows:

$$I_{g,ripple} = \left|\frac{-L_a v_g}{L_pL_a-M^2}\right|(1-D)\,T_s \tag{24}$$

$$I_{g,ripple} = \left|\frac{-L_a\left(V_{dc}+v_g\right)}{L_pL_a-M^2}\right|(1-D)\,T_s \tag{25}$$

By substituting (19), (20) and (23)-(25) into (21) and (22) for each mode, the condition for reducing the reverse recovery current is expressed as follows:

$$\frac{(L_a+M)\left(V_{dc}-|v_g|\right)|v_g|}{\left(L_pL_a-M^2\right)f_{sw}V_{dc}} \geq i_{ref} + \frac{L_a\left(V_{dc}-|v_g|\right)|v_g|}{2\left(L_pL_a-M^2\right)f_{sw}V_{dc}} \tag{26}$$

where the switching frequency f_{sw} is:

$$f_{sw} = \frac{1}{T_s} \tag{27}$$

For selecting L_a, (26) is rearranged as below:

$$L_a \leq \frac{2f_{sw}M^2V_{dc}i_{ref} + 2M\left(V_{dc}-|v_g|\right)|v_g|}{2f_{sw}L_pV_{dc}i_{ref} - \left(V_{dc}-|v_g|\right)|v_g|} = L_{a,\max} \tag{28}$$

This criterion is valid except when i_{ref} meets the following condition.

$$i_{ref} \leq \frac{\left(V_{dc}-|v_g|\right)|v_g|}{2f_{sw}L_pV_{dc}} \tag{29}$$

To verify when i_{ref} satisfies (29), (26) is expressed as follows:

$$\frac{L_pL_a+2L_pM}{L_pL_a-M^2} \times \frac{\left(V_{dc}-|v_g|\right)|v_g|}{2f_{sw}L_pV_{dc}} \geq i_{ref} \tag{30}$$

Hence, (29) is a sufficient condition for (30). The criterion in (28) determines the maximum value of L_a. The parameters in (26) except L_p, L_a and M are determined regardless of the auxiliary circuit. Based on (21)-(23), the required slope of i_m increases with i_{ref}, so that the design of L_c is performed under maximum output power condition.

The minimum value of L_a is determined by the coupling coefficient k that cannot be greater than 1. The relationship among L_p, L_a, M, and k is defined as follows:

$$M = k\sqrt{L_pL_a} \tag{31}$$

Based on (28), L_a should satisfy the following condition.

$$L_a \geq \frac{M^2}{L_p} = L_{a,\min} \tag{32}$$

If L_a is within the boundary of (28) and (32), the reverse recovery current of D_1 is removed. However, there are additional considerations for the use of the auxiliary circuits. First, L_p and M are assumed to be fixed. Substituting (31) into (24) and (25), $I_{g,ripple}$ is expressed as follows:

$$I_{g,ripple} = \frac{1}{1-k^2} \times \frac{\left(V_{dc}-|v_g|\right)|v_g|}{L_pf_{sw}V_{dc}} \tag{33}$$

If k is 1, $I_{g,ripple}$ is the same as in the traditional inverter. Based on (31) and (33), $I_{g,ripple}$ increases as L_a decreases. The increase in $I_{g,ripple}$ causes an increase in losses and the current stress of switching devices. The small L_a can also lead to the reverse recovery problem on the auxiliary diodes. As L_a becomes smaller, the magnitude of (10) and (18) becomes larger. Even if D_{a1} is turned off with zero current, the reverse recovery current may occur due to the steep current slope. Therefore, L_a should be selected as large as possible. Fig. 10 shows the maximum value of L_a for various L_p and M in unity PF operation with parameters in Table 3. Under unity PF condition, $L_{a,\max}$ always has the smallest value at 90 deg, independent of L_p and M. Accordingly, $L_{a,\max}$ at 90 deg is satisfies (28) for all phases and is the largest value that can be selected.

Next, to determine L_p and M, it is assumed that L_a is chosen as $L_{a,\max}$ at 90 deg. Since L_a is satisfied with (28), the reverse recovery issue of the main diodes does not need to be considered. Therefore, L_p and M should be selected in a way that reduces the slope of i_a in mode 4 and $I_{g,ripple}$. When the phase of i_g is 90 deg under unity PF operation, the magnitude of (10) and $I_{g,ripple}$ are illustrated in Figs. 11 and 12, respectively. As shown in Figs. 11 and 12, if L_p is increased, and M is decreased to reduce $I_{g,ripple}$, the slope of i_a will be steep. On the other hand, smoothing the slope increases $I_{g,ripple}$. Thus, for an appropriate compromise, L_p and M are selected as values near the knee-point in each graph.

Finally, the operation under non-unity PF condition is verified. Fig. 13 shows $L_{a,\max}$ for various PF where L_p is 1 mH and M is 0.3 mH. The values for the condition in (29) are not marked. As shown in Fig. 13, under non-unity PF operation, L_a is required as $L_{a,\min}$ at zero voltage. In accordance with (33), this causes severe $I_{g,ripple}$. Therefore, L_a should be determined based on unity PF operation, and then the reverse recovery current in narrow ranges under non-unity PF operation will be allowed.

IV. EXPERIMENTAL RESULTS

For the experimental verification, the 3 kVA DBI prototype implemented with the proposed techniques was built and tested. Fig. 14 shows the photograph of the prototype. The designed L_c consists of one coupled inductor and an additional inductor for reinforcing the insufficient secondary leakage inductance. In the experiment, a resistor is connected

TABLE 3. Parameters of DBI and utility grid.

Parameter	Value
Maximum output power, S_{max}	3 kVA
Grid voltage, v_g	220 V
DC-link voltage, V_{dc}	380 V
DC-link capacitor, C_{dc}	2600 µF
Grid frequency, f_g	60 Hz
Switching frequency, f_{sw}	30 kHz

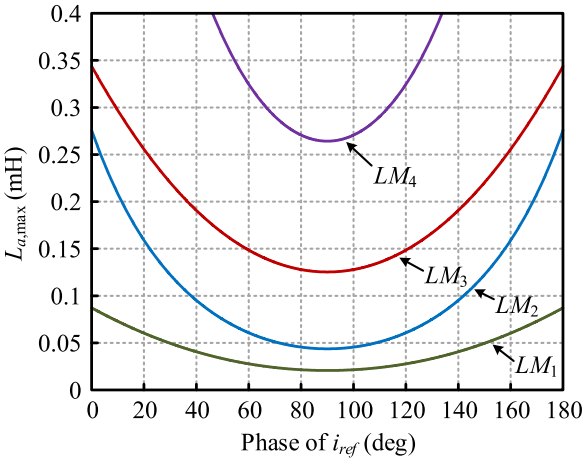

FIGURE 10. The maximum value of L_a for different L_p and M ($LM_1 : L_p$ = 1 mH & M = 0.1 mH, $LM_2 : L_p$ = 0.5 mH & M = 0.1 mH, $LM_3 : L_p$ = 1 mH & M = 0.3 mH, and $LM_4 : L_p$ = 0.5 mH & M = 0.3 mH).

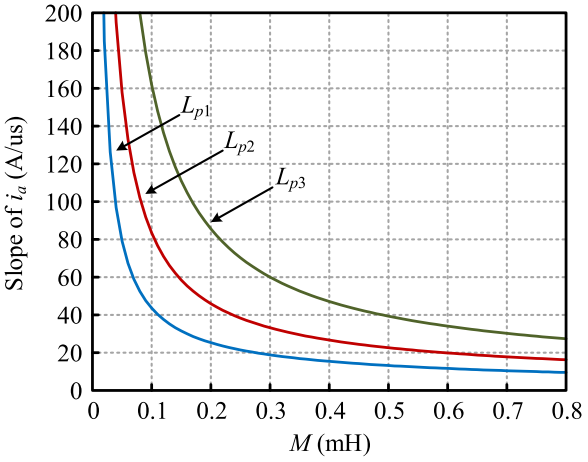

FIGURE 11. The slope of i_a for different L_p (L_{p1} = 0.5 mH, L_{p2} = 1 mH, and L_{p3} = 2 mH).

in series to the filter capacitor for passive damping. For the power stage implementation of the DBI, IPZ60R040C7 CoolMOS^{TM} from Infineon and DSEI30-10 fast recovery diode from IXYS were employed. The control algorithm including the proposed reactive power support function was implemented with TMS320F28335 digital signal controller from Texas instruments. The waveforms of grid voltage and the output current are measured with a voltage differential probe HVD3106A and current probe from LeCroy.

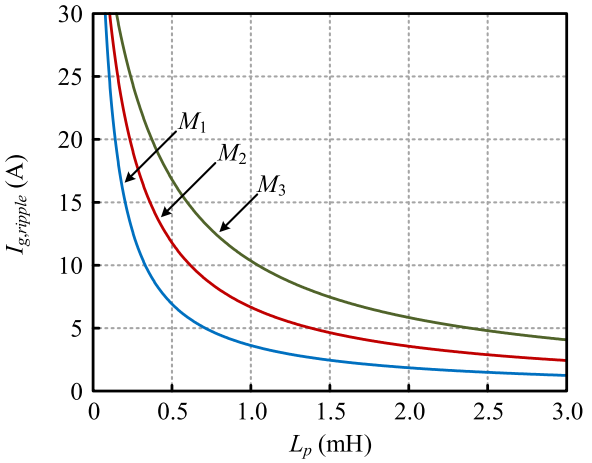

FIGURE 12. The output current ripple for different M (M_1 = 0.1 mH, M_2 = 0.3 mH, and M_3 = 0.6 mH).

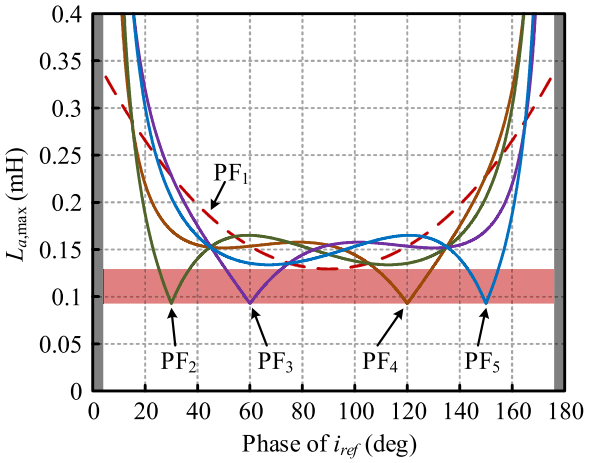

FIGURE 13. The maximum value of L_a for different power factor (PF_1 = 1.0, PF_2 = 0.87 leading, PF_3 = 0.5 leading, PF_4 = 0.5 lagging, and PF_5 = 0.87 lagging).

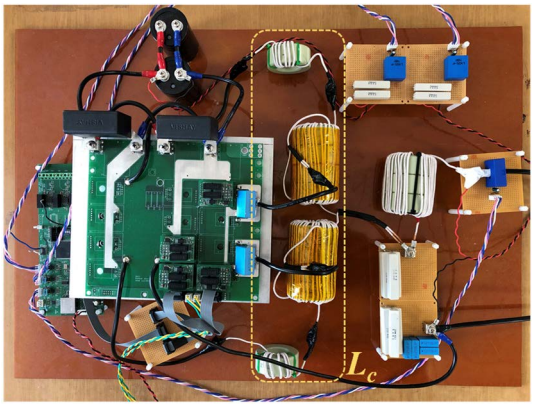

FIGURE 14. 3 kVA DBI prototype.

The switching waveforms are measured with Rogowski current probe CWTMini50HF from PEM, and the variables inside the controller are monitored using digital-to-analog

TABLE 4. Parameters of coupled inductor and output filter.

Parameter	Value
Coupled inductor primary self-inductance, L_p	0.97 mH
Coupled inductor secondary self-inductance, L_a	0.12 mH
Coupled inductor mutual inductance, M	0.3 mH
Filter capacitor, C_f	330 nF
Damping resistor, R_d	3.33 Ω
Grid-side inductor, L_g	0.85 mH

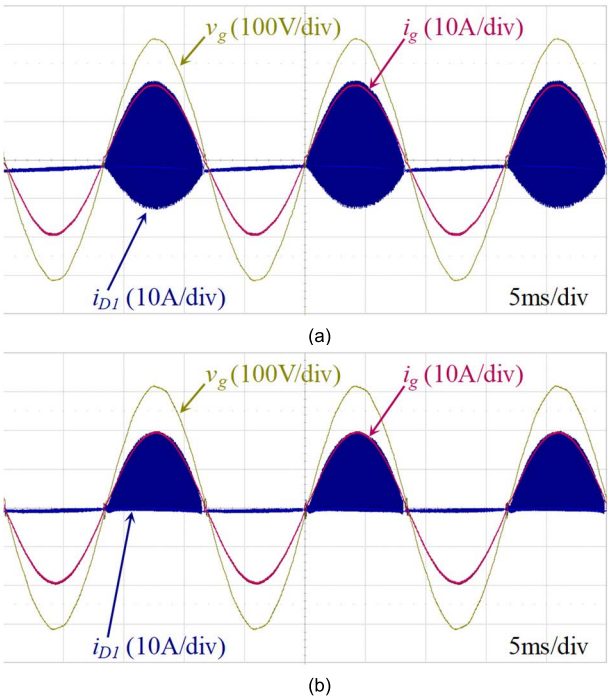

FIGURE 15. Waveforms of 3 kW unity PF operating. (a) Without the auxiliary circuits. (b) With the auxiliary circuits.

converter (DAC) on the digital control board. The parameters of the designed L_c and the output filter are summarized in Table 4. The experiment was carried out comparing the proposed DBI with the traditional DBI. The prototype can be operated as either the proposed DBI or the traditional DBI depending on whether the secondary side of L_c is connected to the auxiliary diodes. When the prototype works as the traditional DBI, L_c is the same as the filter inductor in Fig.1 with the value of L_p.

Fig. 15 show the experimental results under 3 kW unity PF operating. Regardless of the auxiliary circuits, i_g is regulated equally. However, i_{D1} without the auxiliary circuits in Fig. 15(a) has the reverse recovery current. This is detailed in Fig. 16. In the figure, almost 20 A of reverse recovery current which is about the same amount of the conducting current is occurred at every turn-off instant. Apparently, it is supposed that the unidirectional switching legs in the DBI are undergoing shoot-through phenomenon. The switching waveforms with the proposed auxiliary circuit are shown in Fig. 17. Since D_1 is turned off with zero current, and i_{Da1} reaches zero with

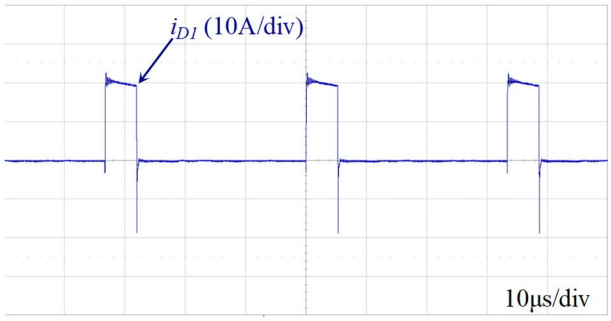

FIGURE 16. Switching waveform with the traditional DBI at peak of i_g.

FIGURE 17. Switching waveforms with the proposed DBI. (a) At peak of i_g. (b) At 0.5 of duty cycle.

a moderate slope, the reverse recovery current does not occur. As shown in Fig. 17, mode 3 appears shorter at peak of i_g than at 0.5 of the duty cycles. This is because the coupled inductors are designed for maximum output current conditions. These results are very well matched with the analyses taken in sections II and III. Fig. 18 verifies that the proposed inverter also mitigates the reverse recovery problems under different power ratings.

To verify the operation of the DBI under non-unity PF, the experimental results for each modulation techniques are compared. Figs. 19 and 20 illustrate the results of 1.5 kVA conditions with the conventional and the proposed modulation methods, respectively. In Fig. 19, d_{ref} which is produced by the controller is directly applied. As can be seen in the figure, i_g is distorted at this condition, because the switching operation of the DBI during freewheeling intervals for the reactive power supply is not adequately handled. On the other

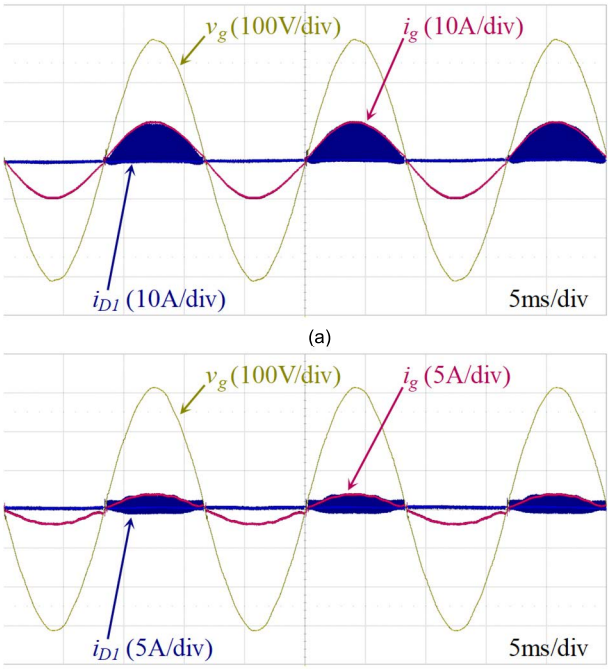

FIGURE 18. Waveforms of unity PF operation with the proposed inverter. (a) 50% of the rated output power. (b) 10% of the rated output power.

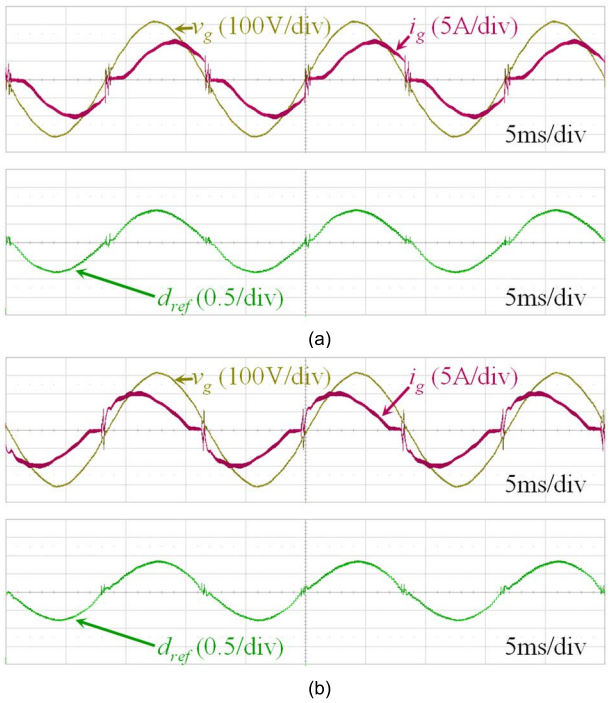

FIGURE 19. Waveforms of 1.5 kVA operation with the conventional modulation method. (a) 30 deg lagging PF. (b) 30 deg leading PF.

hand, the proposed modulation method converts d_{ref} to d_m depending on the buck and boost modes. Accordingly, i_g is well regulated as a sinusoidal shape, as shown in Fig. 20. Although it is not shown in the figure, it is supposed that d_{ref} should be sinusoidal, and the duty commanding from the current controller is not artificially altered.

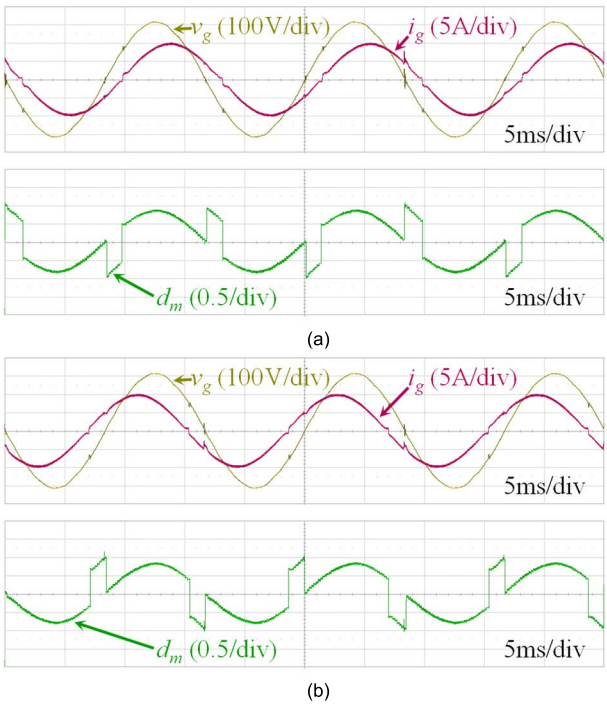

FIGURE 20. Waveforms of 1.5 kVA operation with the proposed modulation method. (a) 30 deg lagging PF. (b) 30 deg leading PF.

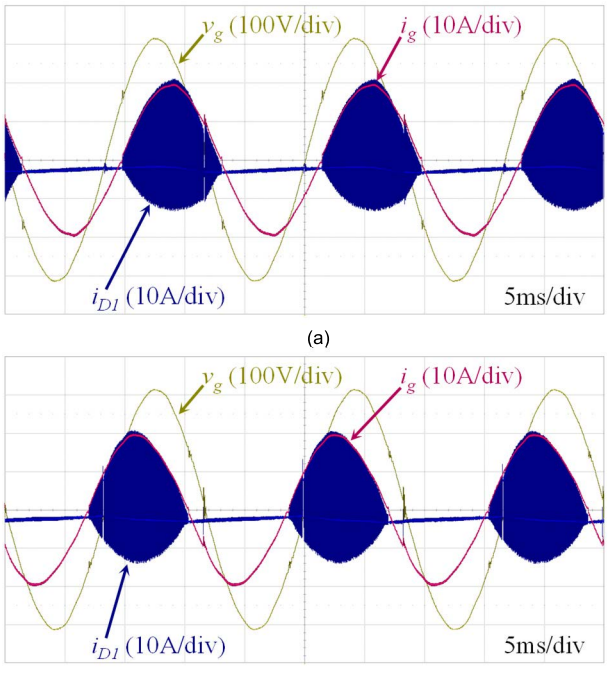

FIGURE 21. Waveforms of 3 kVA operation without the auxiliary circuits. (a) 30 deg lagging PF. (b) 30 deg leading PF.

Figs. 21 and 22 show the difference in reverse recovery current of D_1 without and with the auxiliary circuits under non-unity PF conditions. As shown in Fig. 22, with the auxiliary circuits, the reverse recovery current is mitigated except near zero crossing points of v_g. Although it seems

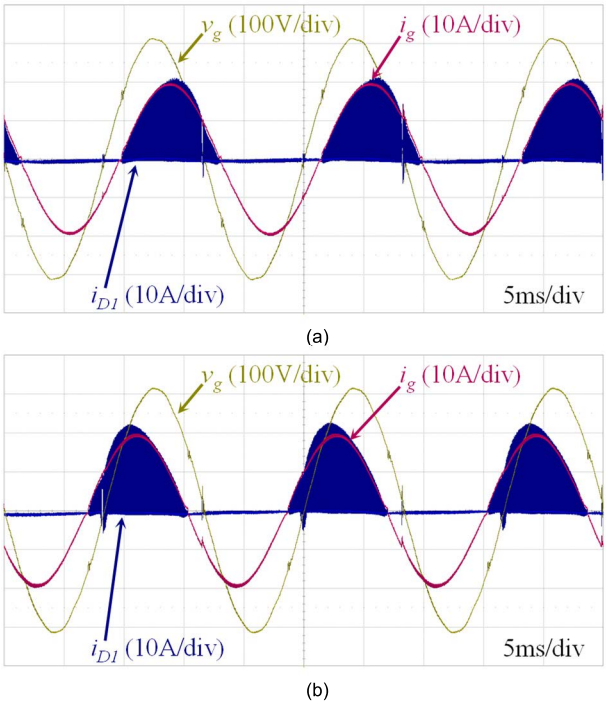

FIGURE 22. Waveforms of 3 kVA operation with the auxiliary circuits. (a) 30 deg lagging PF. (b) 30 deg leading PF.

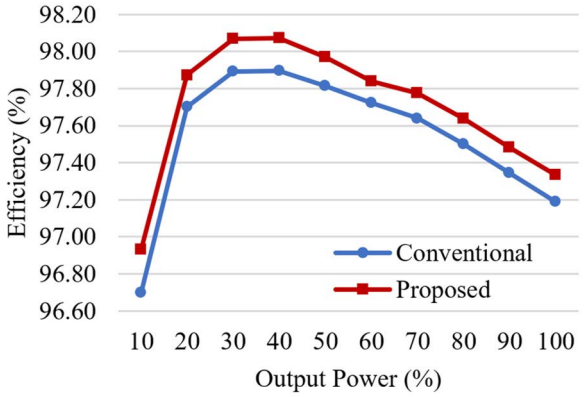

FIGURE 23. Efficiency measurement results.

that the proposed inverter has the reverse recovery issue at the zero crossing points of vg under non-unity PF operation, this is trivial and negligible compared to that of the traditional DBI as shown in Fig. 21. In fact, this little reverse recovery issue at non-unity PF operation was discussed in section II and III. Fig. 23 compares the efficiency measurement results of the conventional and the proposed DBI at unity PF. The efficiency was measured using WT 1800 from YOKOGAWA. For all output power conditions, the efficiency of the proposed DBI is higher than of the conventional DBI. The maximum efficiency of the proposed DBI was measured by 98.07% compared to 97.89% for the conventional DBI. From this result, it is supposed that the reduced reverse recovery losses are greater than the additional losses caused by the auxiliary circuit.

V. CONCLUSION

In this paper, two techniques were proposed and verified for DBIs to alleviate the reverse recovery problem and to implement reactive power supporting. The proposed auxiliary circuit for the DBI allows the diodes to be turned off at zero current, thereby reducing the reverse recovery losses and shoot-through phenomenon. The operational principle of the auxiliary circuit was explained in detail, and the design criterions were discussed in depth. On the other hand, with the proposed PWM scheme, the reactive power could be simply generated by the unidirectional DBI without a nonlinear duty commanding from the current controller. Accordingly, the DBI can actively participate in the grid stability control without the current distortion. The proposed techniques have been validated by the experimental results obtained with the 3 kVA DBI prototype. Through the results, it has been shown that the proposed DBI supports reactive power with a traditional current controller and maintains high efficiency and reliability by mitigating the reverse recovery and shoot-through problems even though Si devices are employed. In sum, it is expected that the proposed techniques can be easily applied to traditional grid-connected DBIs.

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