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A New Single-Source Nine-Level Quadruple Boost Inverter (NQBI) for PV Application

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ABSTRACT Multi-level inverters (MLIs) with switched capacitors are becoming popular due to their utilization in AC high-voltage applications as well as in the field of renewable energy. To achieve the required magnitude of output voltage, the switched capacitor (SC) technique employs a lesser number of DC sources in accordance with the voltage across the capacitor. Designing an efficient high-gain MLI with fewer sources and switches needs a rigorous effort. This paper introduces a prototype of a nine-level quadruple boost inverter (NQBI) topology powered by one solar photo-voltaic source using fewer capacitors, switches, and diodes when compared to the other SC-MLIs topology. The suggested NQB inverter produces nine levels of voltage in its output by efficiently balancing the voltages of the two capacitors. The various SC-MLIs are compared in order to highlight the benefits and drawbacks of the proposed nine-level quadruple boost inverter (NQBI) topology. To validate the efficacy of the proposed solar photovoltaic based NQBI without grid connection, detailed experimental results are presented in a laboratory setting under various test conditions.

INDEX TERMS NQBI, reduced switch count, switched capacitor inverter, SPWM technique.

I. INTRODUCTION

Multi-level inverters (MLIs) are the most popular means for voltage conversion from DC to AC power, and are used in fuel cell and photo-voltaic (PV) based sustainable or renewable energy systems (RES). The core advantages of MLIs include, higher voltage output with minimal switch stress voltage, lowered dv/dt, and a better output voltage harmonic profile. Over the last few decades, the three most common forms of MLIs have been proposed: the flying capacitor (FC) topology, the diode clamped neutral point clamped (NPC) topology, and the cascaded H-bridge (CHB) topology. In order to maintain the voltage balance of capacitors, external hardware circuits and complex control algorithms are needed in the case of the FC-MLI and NPC-MLI topologies. In CHB-MLI, a large number of DC sources are employed, which results in a higher number of output voltage levels. While implementing the MLI with RES, voltage boosting is expected to achieve the higher output voltage. A dc-dc boost converter or transformer is required to achieve the desired higher output voltage. These components results in complex, large, and costly inverter systems [1]–[5]. Multilevel inverters based on the SC principle have been identified as a recent advancement to address the aforementioned shortcomings [6]–[18].

The SC-MLIs boost the input voltage along with an increased number of output voltage levels. In [6], a single isolated DC source was proposed without the need for an H-bridge. The individual switches in [6] are subjected to less voltage stress, but as the voltage level rises, the number of capacitors and power electronics switches also increases.

The SC-MLI topologies proposed in [7], [8] have inherent capacitor voltage balancing and boosting abilities and are suggested for renewable energy conversion due to low voltage stress. Though both topologies has same number output voltage levels and switch count, [7] uses one additional capacitor than [8] to develop better voltage boost.

A nine-level H-bridge based switched capacitor inverter and its three-phase application is also explored in [17]. The inverter topology has self capacitor voltage balance capacity but lacks the boosting ability. Three nine-level SC-based inverters with a single source topology have been suggested in [9], [10], [18], in which capacitor voltage balance is performed without complicated circuits or auxiliary power. On the other hand, the voltage multiplication factor for them

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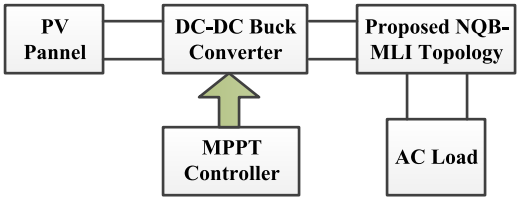

FIGURE 1. Schematic diagram of proposed inverter based off-grid PV system with AC loads.

is two. The converter with a voltage multiplication factor of four is suggested in [11]. This topology uses fewer power electronics switches, but the number of capacitors and diodes is more. In [12], the SC-MLI uses a single isolated DC source for a quadruple boost in the output voltage, but the topology requires more switching devices. Several topologies having a wide range of higher voltage applications are mentioned in [13]–[16]; however, they require more components to produce a (9-L) output voltage. The cost of inverter topology and losses increases with an increase in the number of components. This work proposes a nine-level quadruple boost inverter (NQBI) topology to resolve the shortcomings of the traditional topologies established in previous research. The significant benefits of the proposed topology are mentioned below:

- In the NQBI topology, the amplitude of the output voltage can be attained up to four times the voltage magnitude of the DC source.
- The NQBI topology has self-voltage balancing capability. Hence, no extra hardware circuits are required to control the capacitor voltage.
- The NQBI topology can be connected with a load having a standard range of power factor.
- The NQB inverter is designed with a significantly reduced component count.

The structure of this paper is as follows: In Section II, the design and operation of the proposed inverter are discussed. Section III compares the performance of the proposed topology with the other states of SC-MLI. The experimental results are presented in Section IV. Section V gives the conclusion of the paper.

II. PROPOSED NQBI TOPOLOGY BASED PV SYSTEM

The proposed system using NQBI for an off-grid solar photovoltaic application is shown in FIGURE 1. The DC-DC buck converter is connected to the PV output, and the maximum power point tracking (MPPT) method is implemented to obtain the maximum output power. The suggested NQBI configuration is depicted in FIGURE 2. The proposed MLI can produce a 9-L output voltage with a quadruple boost in the output voltage and requires only ten power electronics switches.

This inverter topology has a level-generating part, which can provide four voltage levels by quadruple boosting and employing two capacitors, C_1 and C_2 with a voltage rating of V_{dc} and $2V_{dc}$, respectively, as seen in Figure 2. The switches

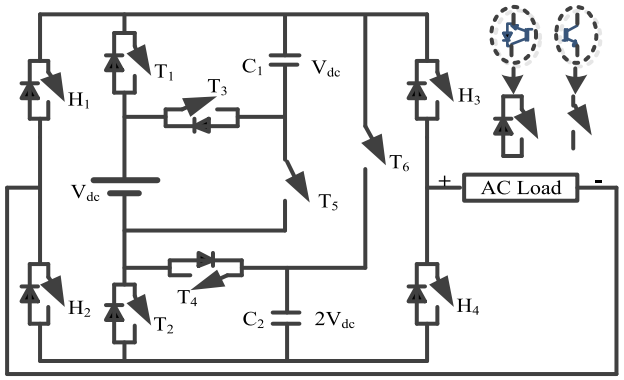

FIGURE 2. Proposed NQBI topology.

TABLE 1. The switching states,output voltage and state of capacitors of the proposed NQBI.

T_1	T_2	T_3	T_4	T_5	T_6	H_1	H_2	H_3	H_4	$V_o(xV_{dc})$	C_1	C_2
0	0	1	1	0	0	0	1	1	0	4	D	D
1	0	0	1	1	0	0	1	1	0	3	C	D
0	1	1	0	0	1	0	1	1	0	2	D	C
1	1	0	0	1	0	0	1	1	0	1	C	-
1	0	0	0	1	0	1	0	1	0	Zero	C	-
1	0	0	0	1	0	0	1	0	1			
1	1	0	0	1	0	1	0	0	1	-1	C	-
0	1	1	0	0	1	1	0	0	1	-2	D	C
1	0	0	1	1	0	1	0	0	1	-3	C	D
0	0	1	1	0	0	1	0	0	1	-4	D	D

Where: 0/1 = OFF/ON switch, '-' = capacitor constant voltage, D/C = discharging/charging of capacitor.

T_5 and T_6 are configured as reverse blocking switches to prevent the unnecessary discharge of the capacitors C_1 and C_2. The alternating polarity can be generated by the polarity generating part composed of four switches H_1, H_2, H_3 and H_4. Table1 shows the possible switching states and modes of capacitors to achieve the nine-level AC output voltage.

A. ANALYSIS OF SELF VOLTAGE BALANCE AND CAPACITANCE OF C_1 AND C_2

The proposed NQBI has self voltage balancing ability as it implements serial-parallel linking technique for charging and discharging of capacitors C_1 and C_2. The capacitor C_1 gets connected to DC source and charged upto V_{dc} when T_1 and T_5 are simultaneously in on-state during ± 0, $\pm V_{dc}$ and $\pm 3V_{dc}$ output voltage level as shown in TABLE 1. The capacitor C_1 is connected in series with DC source and the capacitor C_2 gets connected in parallel when T_2, T_3 and T_6 are in ON state. The capacitor C_1 discharges while capacitor C_2 charges upto $2V_{dc}$ during $\pm V_{dc}$ output voltage level. Both capacitors (C_1 & C_2) and DC source are connected in series when T_2, T_4 are simultaneously turned on and $\pm 4V_{dc}$ voltage level is attained. FIGURE 3 displays the charging and discharging patterns of C_1 and C_2 for one cycle of output voltage. The capacitor voltage of C_1 and C_2 starts to reduce from the nominal value under discharging mode of operation. The overall capacitance value C_1 and C_2 needed for an appropriate ripple of voltages (ΔV), peak load current ($I_{o,\,peak}$), frequency of output voltage and corresponding maximum discharge time

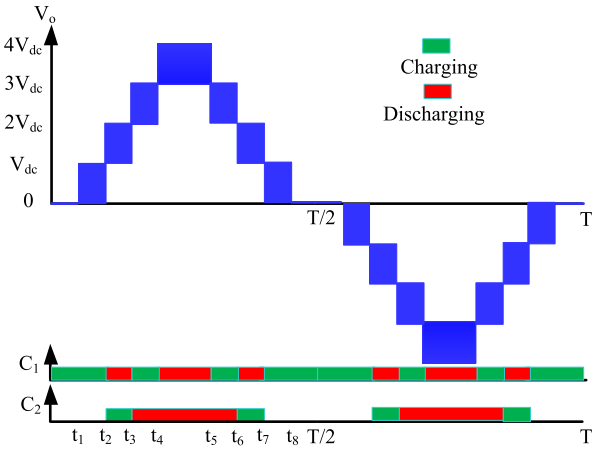

FIGURE 3. Output voltage and charging pattern of capacitors.

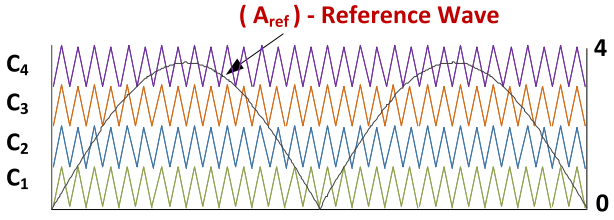

FIGURE 4. LS-PWM modulation technique.

of ΔT_1 and ΔT_2 are as follows:

$$\left.\begin{aligned} C_1 &= \frac{I_{o,peak}}{\pi \times f \times \Delta V} \times \Delta T_1 \\ C_2 &= \frac{I_{o,peak}}{\pi \times f \times \Delta V} \times \Delta T_2 \end{aligned}\right\} \quad (1)$$

where $\Delta T_1 = t_5 - t_4$ is the interval of the voltage level $4V_{dc}$ and $\Delta T_2 = t_6 - t_3$ is the interval of the voltage level of ($3V_{dc}$ and $4V_{dc}$) [11].

B. PULSED-WIDTH MODULATION TECHNIQUE

The NQBI is being controlled with sinusoidal pulse-width modulation, in which a sinusoidal reference signal (v_{ref}) of required amplitude (v_m) is simultaneously compared with eight level-shifted carrier waves of equal amplitude (A_C) as depicted in FIGURE 4. The generated gate-pulses for the proposed NQBI is shown in the FIGURE 5. The magnitude of the reference signal varies according to the modulation index to obtain the desired magnitude of output voltage. The modulation index is expressed as follows:

$$M_i = \frac{v_m}{4A_C}. \quad (2)$$

C. POWER LOSS ANALYSIS OF THE PROPOSED NQBI TOPOLOGY

The losses in the inverter occur due to the existing non-idealities in the inverter components. Three types of major losses occurring in the proposed NQBI are switching losses (P_{sw}), conduction losses (P_c) and ripple losses (P_{ripple}) considered. Hence, total power loss (P_{loss}) occurring in the NQBI is

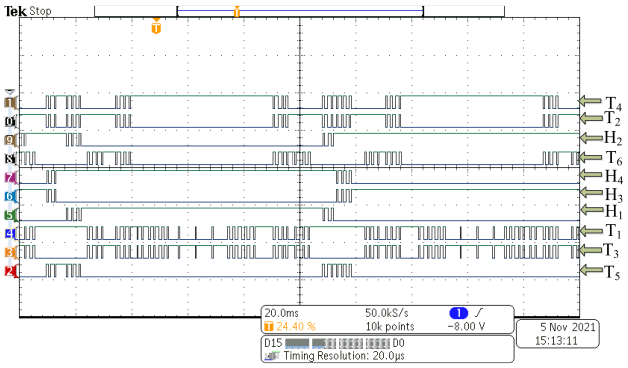

FIGURE 5. Gate-pulses for the proposed nine-level inverter.

$$P_{loss} = P_c + P_{sw} + P_{ripple} \quad (3)$$

During each switching transition, the voltage and current overlap due to intrinsic delays in the switching of IGBT, which leads to switching loss. It can be expressed as:

$$P_{sw} = \sum_{\text{switches}} \sum_{\text{within } 1/f_o} \left(\frac{V_{on} \times I_{on} \times T_{on}}{6} + \frac{V_{off} \times I_{off} \times T_{off}}{6} \right) \times f_{sw} \quad (4)$$

where, V_{on} is the voltage across the IGBT in the pre-ON state. The current that flows through the power switch after it has been turned on is referred to as I_{on}. T_{on} is the time span during which the ON state is in transition. The voltage across the power switch, the current that runs through a power switch before the transition to the OFF state, and the transition duration of the OFF state are V_{off}, I_{off}, and T_{off} respectively. The switching frequency and the frequency of the fundamental output voltage are denoted by f_0 and f_{fsw} respectively.

Conduction losses are power losses that occur as a result of the internal resistance provided by the switch while the switch is in the conduction mode, and can be expressed as

$$P_c = \sum_{\text{all switches}} I_{switch}^2 \times R_{on} \quad (5)$$

In which I_{switch} is the amount of current that flows through a switch with an internal resistance of R_{on}.

The ripple losses caused by the charging and discharging of the capacitors are also a significant component in the overall power loss of the SC-MLI. It is possible to lose power when the parallel capacitor connected to the DC source is charged. The charging current flows through the capacitor and, as a result of a difference between the input source and the capacitor voltage, the ripple voltage ΔV_C results, which causes the power loss. The ripple power loss of a capacitor can be computed using the following formula:

$$P_{ripple} = \sum_{\text{all capacitors}} C \times \Delta V_C^2 \times f_{sw} \quad (6)$$

TABLE 2. Proposed NQBI topology of power loss profile.

Power loss of	P_{sw}	P_{con}	P_{loss}
H_1 (W)	0.015	0.62	0.635
H_2 (W)	0.015	0.61	0.625
H_3 (W)	0.0044	0.602	0.6064
H_4 (W)	0.0044	0.603	0.6074
T_1 (W)	0.047	1.11	1.157
T_2 (W)	0.113	1.56	1.674
T_3 (W)	0.136	1.56	1.696
T_4 (W)	0.05	0.75	0.8
T_5 (W)	0.074	0.55	0.624
T_6 (W)	0.076	0.45	0.526
C_1 (W)	1.11		
C_2 (W)	3.44		
$P_{Total\ loss}$ (W)	13.5		
Output power (W)	500		
Efficiency (%)	97.3		

The component-wise power loss for the proposed inverter at an output power of 0.5 kW has been listed in Table 2. The proposed NQB inverter exhibits 97.3 efficiency at 0.5kW output power.

III. COMPARATIVE ANALYSIS

The voltage boosting capability of the proposed topology, along with nine voltage levels at the output terminal, makes it a suitable candidate for injecting high power quality into the load/grid.

A comparison is carried out with the other MLI topologies that can produce quadruple voltage at their terminals, and the result is shown in the TABLE 3. As evident from the table, topologies suggested in [11] and [15] requires fewer active switches, but the number of diodes is greater than the proposed NQBI topology. Furthermore, the proposed topology has two capacitors of V_{dc} and $2V_{dc}$ rating for quadruple voltage increase, while the topology of [11] requires two capacitors of $2V_{dc}$ rating and one capacitor of V_{dc} rating. Having a greater number of capacitors in an MLI leads to an increase in cost and difficulty managing charging and discharging. The topology suggested in [12] requires two capacitors but at the expense of twelve active switches, as against ten active switches required in the proposed inverter.

Another important benchmark for comparison of SC topologies is the number of conducting power electronic components in the loading of capacitors, i.e. the N_{SC}. In order to accommodate the charge current of the capacitor, equipment in the charging loop must be of greater current rating. The proposed topology would need only four devices with higher current ratings. Topologies proposed in [6], [9], [11]–[16] requires more devices in the loading loop, resulting in higher costs and losses as compared to the proposed topology in this paper. The total number of power electronic devices conducting (TCD) at each voltage level is also considered for comparison. Furthermore, from TABLE 3, it can be inferred that during the inverter's operation of the proposed NQBI, a minimum number of conduction devices is required at any stage compared to other state-of-the-art topologies. The total average standing voltage per unit (TSV_{pu}) of the proposed inverter is greater than that of other MLIs, except for [15]. The proposed NQBI's cost function (CF) can be defined as:

$$CF = N_{sw} + N_c\left(1 \times N_{C\_V_{dc}} + 2 \times N_{C\_2V_{dc}}\right) + N_{sc} + N_d + \alpha * \mathrm{TSV_{pu}} + \beta * \mathrm{TCD_{avg}} \quad (7)$$

where weight coefficients of TSV_{pu} and TCD_{avg} are α and β respectively. The CF is regulated by the expense of the power electronic switches, capacitors, and gate driver circuits.

TABLE 3 enlist CF of various typologies for different values of weight coefficient α and β. The CF value of the proposed NQB-MLI is found to be less than that of other MLIs. Different topologies are modelled in PLECS programme with specification: $V_{dc} = 30V$, $C = 4700\mu$F and carrier frequency=5kHz. FIGURE 6 shows the efficiency of different topologies with various loading conditions. The maximum efficiency of the suggested topology is 98.2 %, as evident from FIGURE 6. Moreover, because of the lower component count of lower voltage ratings and lesser conduction losses, the performance of the suggested NQB-MLI is found to be better than all other topologies.

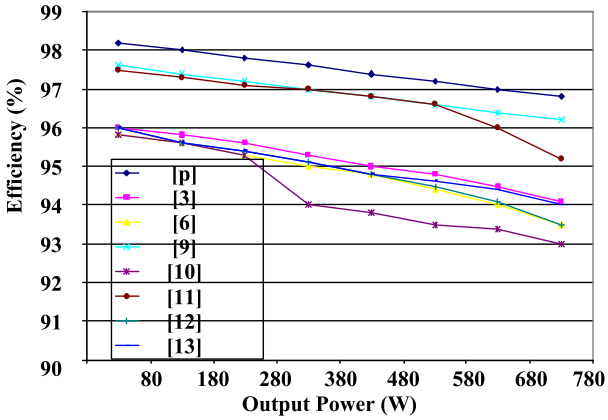

FIGURE 6. Calculated efficiency comparison of proposed nine-level inverter with existing inverter topologies.

IV. HARDWARE IMPLEMENTATION AND RESULTS ANALYSIS

A laboratory prototype of the proposed NQBI-based standalone solar PV system was developed to validate its operations as shown in FIGURE 7.

The specifications of the components utilised to design the proposed NQBI are listed in TABLE 4. The detailed specifications of the solar panel considered as a source are represented in TABLE 5. The technical details of the DC-DC constant voltage constant current MPPT converter utilized for the realization of the proposed system are shown in TABLE 6.

The R-C based circuit is designed to introduce a dead time of 0.002 ms between the switches in the same leg to avoid the resulting shoot-through current through them.

The switching pulse generated at unity modulation index (MI) under level shifted PWM is fed to the respective switches of NQBI and corresponding voltage and current

TABLE 3. Comparison of various topologies with the proposed NQB-MLI topology.

Topology	N_{sw}	N_{gd}	N_d	N_{com}	N_c	V_C		N_{sc}	$TSV_{p.u.}$	TCD					CF (with value of α and β)				G
						V_{dc}	$2V_{dc}$			$\pm1^{st}$	$\pm2^{nd}$	$\pm3^{rd}$	$\pm4^{th}$	TCD_{avg}	0.5, 0.5	1.0, 1.0	1.5, 0.5	0.5, 1.5	
[6]	17	17	0	17	3	3	0	9	5.5	8	8	8	8	8	35.75	42.5	41.25	43.75	4
[11]	8	8	3	11	3	1	2	6	5.75	5	5	5	5	5	27.375	32.75	33.125	32.375	4
[12]	12	12	0	12	2	1	1	6	5.25	6	7	6	6.5	6.5	26.875	32.75	32.125	33.375	4
[13]	17	17	5	22	4	4	0	12	5.5	10	9.5	8.5	8.5	9	45.25	52.5	50.75	54.25	4
[14]	13	13	0	13	3	3	0	6	6.25	8	7	6	5	6.5	28.375	34.75	34.625	34.875	4
[15]	8	8	6	14	3	3	0	6	8	8	4	5	5	5.5	29.75	36.5	37.75	35.25	4
[16]	10	10	3	13	3	3	0	6	6.25	8	5	5	5	5.75	28	34	34.25	33.75	4
[9]	10	10	1	11	2	2	0	3	5.75	5	5	5	4	4.75	21.25	26.5	29.37	28.87	2
[17]	8	8	2	10	3	3	0	3	5	5	4	6	5	5	29.5	42	49.5	34.5	2
[18]	10	10	1	11	2	1	1	3	5.55	5	4	5	5	4.75	20.25	25.50	28.37	27.87	2
Proposed NQBI	**10**	**10**	**0**	**10**	**2**	**1**	**1**	**3**	**6.25**	**5**	**5**	**5**	**4**	**4.75**	**20.25**	**25.50**	**28.37**	**27.87**	**4**

N_{sw}=Quantity of power electronics switches, N_{gd}=Quantity of gate driver circuits, N_d=Quantity of additional diodes, N_{com}=Sum of N_{sw} and N_d, N_c=Quantity of capacitor, V_C = Capacitor voltage rating, N_{sc} = Quantity of devices conducting in charging capacitors, $TSV_{p.u.}$ = Total standing voltage in per unit, G= Gain, and TCD = Total conducting device.

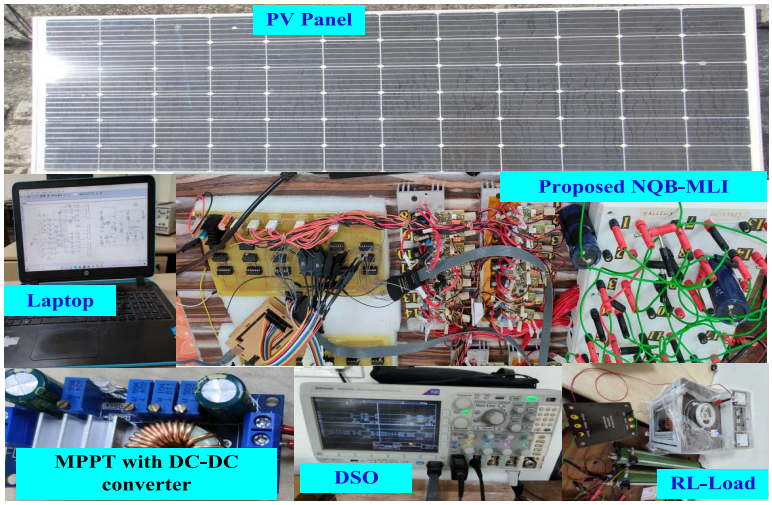

FIGURE 7. Experimental prototype of the proposed NQBI topology.

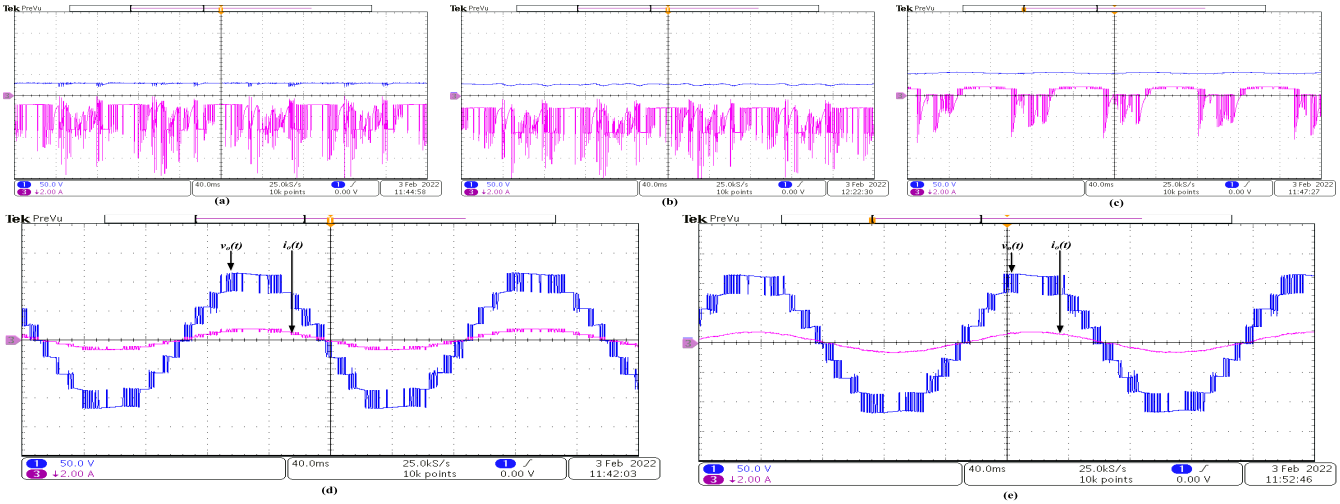

FIGURE 8. Experimental waveforms at modulation index 1 (a) Output vol the DC-DC converter, (b) capacitor voltage V_{C1}, (c) capacitor voltage V_{C2} (d)output voltage and current at $Z_L = 160\Omega$ and (e) output voltage and current at $Z_L = 160\Omega + 200\ mH$.

waveform of the DC/DC converter, switched capacitors (C_1 and C_2) and the output of inverter are presented in FIGURE 8. The output of the DC-DC converter acting as the DC source for the proposed NQBI is 30 V. It is observed from FIGURE 8 that the voltage across capacitor C_1 (V_{C1}) matches the voltage of the DC source, while the voltage across capacitor C_2 (V_{C2})

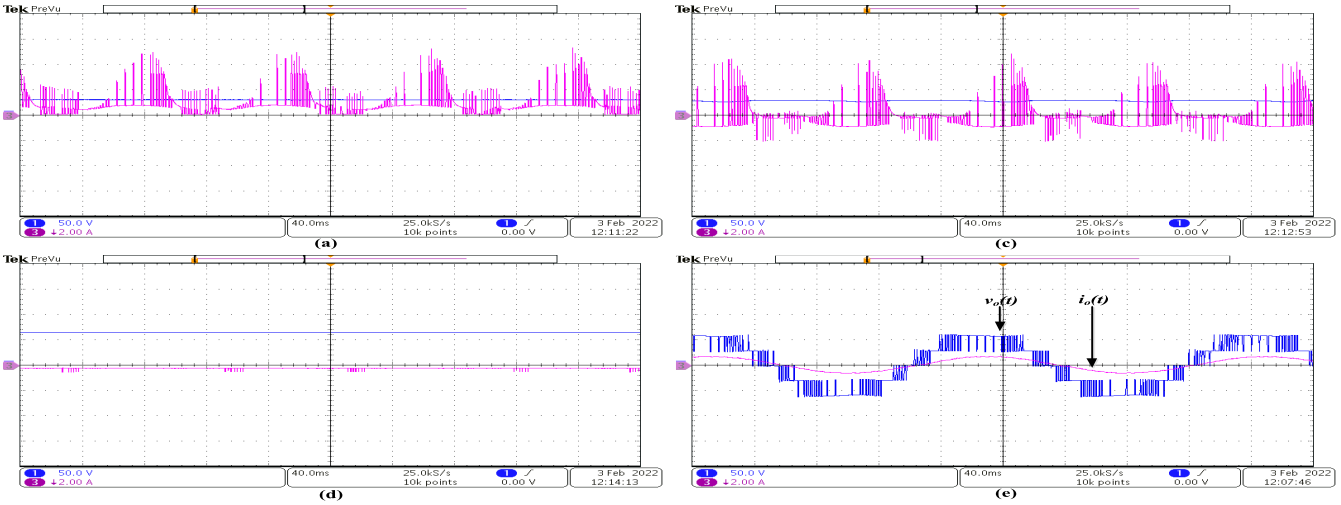

FIGURE 9. Experimental waveforms at modulation index 0.5 (a) Output vol the DC-DC converter, (b) capacitor voltage V_{C1}, (c) capacitor voltage V_{C2} (d) output voltage and current at $Z_L = 80\Omega + 200\ mH$.

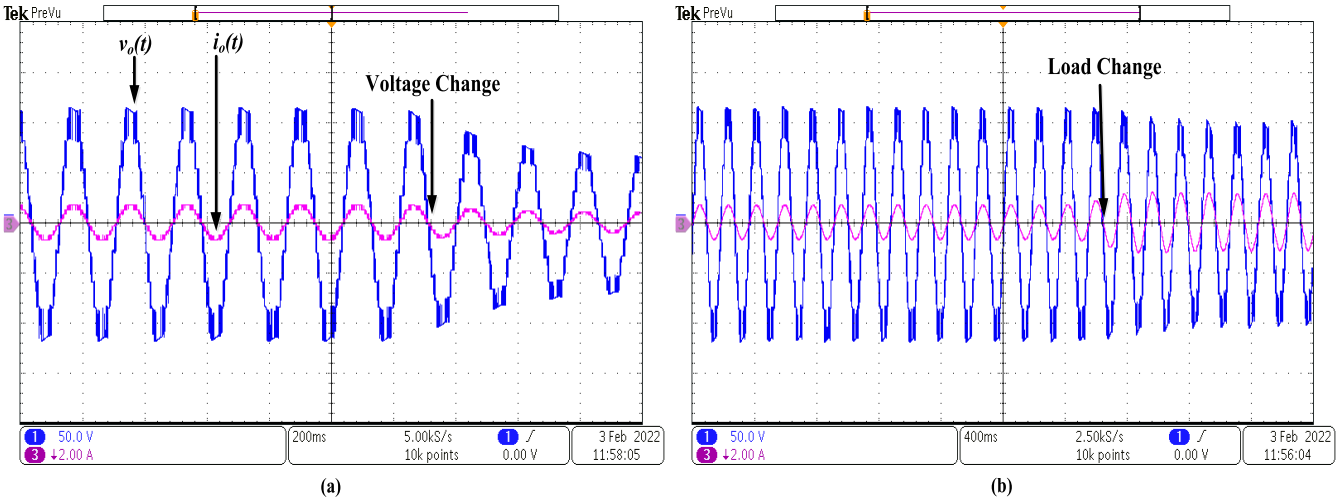

FIGURE 10. Experimental waveforms of (a) output voltage and current Output under voltage variation of DC -DC converter from 30V to 18V and (b) output voltage and current under load variation from $Z_{L1} = 160\Omega + 200\ mH$ to $Z_{L2} = 80\Omega + 200\ mH$.

TABLE 4. Detailed specifications for the design of NQBI topology.

IGBT Switches	CT60AM 18F IGBT
Controller	Arduino mega 2560
Optocoupler	TLP250
C_1 and C_2	1000μF and 2000μF
Resistive load	0-160 Ω
Inductive load	0-200 mH
Carrier frequency	5KHz
Reference frequency	50Hz
dead time	0.002ms

TABLE 5. Specification for the solar panel.

Output Power	375 Watts
Panel Technology	Mono Crystalline
voltage at max power	39.00 volts
current at max power	9.62 amps
open circuit voltage	44.50 volts
short circuit current	9.90 amps

holds twice the voltage across C_1. The capacitor voltage for both switched capacitors C_1 and C_1 is seen to be balanced. The output voltage ($v_o(t)$) and current ($i_o(t)$) waveform for resistive load ($Z_L = 80\Omega$) is shown in FIGURE 8 (d). It is observed that the $v_o(t)$ waveform has nine levels and $i_o(t)$ is in phase with $v_o(t)$. Moreover, the output voltage ($v_o(t)$) waveform and current ($i_o(t)$) waveform for resistive-inductive load ($Z_L = 80\Omega + 200\ mH$) is shown in FIGURE 8 (e). It is observed that the current $i_o(t)$ lags behind the voltage $v_o(t)$ by some phase-angle.

To further verify the operation of proposed NQB inverter at lower modulation index (say 0.5), the voltage and current waveform of the DC/DC converter, switched capacitors (C_1 and C_2) and the output of inverter is obtained and represented in FIGURE 9. The voltage and current waveform of the

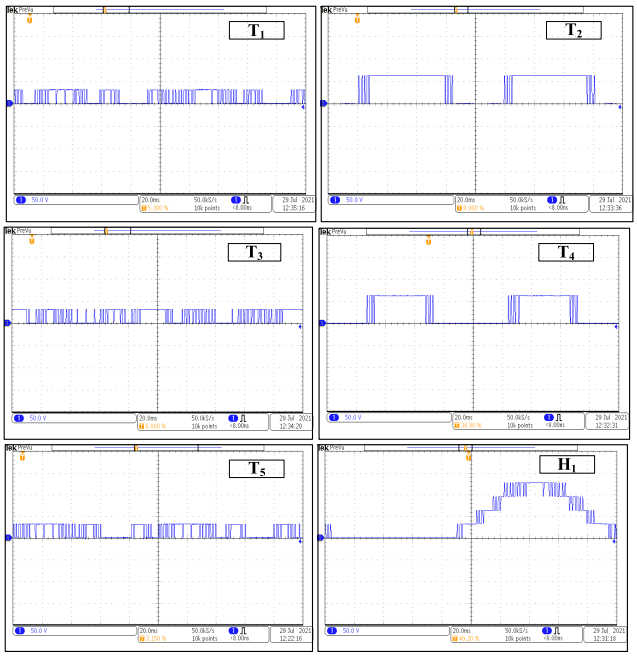

FIGURE 11. Blocking voltages across switches.

TABLE 6. Technical specification of DC-DC constant voltage constant current MPPT controller.

Input voltage	6-36V
MPPT voltage setting range	6-36V
Output current range	0.05-5A
Operating temperature	-40 to 85 degree
Operating frequency	180 KHz
Conversion efficiency	up to 95%
Short circuit protection	Yes
Over temperature protection	Yes

capacitors show that only C_1 is engaged actively. The reduced output voltage ($v_o(t)$) with five levels and respecive current ($i_o(t)$) waveform for resistive-inductive load ($Z_L = 80\Omega + 200mH$) is shown in FIGURE 9 (d).

FIGURE 10 illustrates the inverter output waveforms for dynamic source and load conditions at unity modulation index. FIGURE 10(a) shows the voltage ($v_o(t)$) and current ($i_o(t)$) waveform when the resistive-inductive load is changing from $Z_{L1} = 160\Omega + 200\,mH$ to $Z_{L2} = 80\Omega + 200\,mH$. It is observed that the magnitude of load current increases as the impedance decreases. The phase difference between $v_o(t)$ and $i_o(t)$ also varies accordingly. In addition to that FIGURE 10 (b) shows the output voltage ($v_o(t)$) and current ($i_o(t)$) waveforms for resistive load ($Z_1 = 160\Omega$) when the input DC voltage is varied from 30 volts to 18 volts corresponding to the variation in irradiates. The voltage appearing across the switches of the NQBI are shown in FIGURE 11. The maximum blocking voltage across switches T_1, T_2, T_3, T_4, T_5 are 30V, 60V, 30V, 60V and 30V respectively. The maximum blocking voltage across all four switches H_1, H_2, H_3 and H_4 are 120 V as they are operating as polarity-generating parts.

It is evident from the experimental results that the operation of the proposed NQBI-based PV system is effective and reliable. The output of the NQB inverter is found to be stable under a variety of operating conditions, including changes in load type and load impedance.voltage across both capacitors is also balanced to provide a nine-level output voltage under load variation without any capacitor voltage balancing technique.

V. CONCLUSION

A reduced-switch, nine-level, switched-capacitor-based quadruple boost inverter topology is proposed in this paper. The NQBI is suggested for PV applications by using a solar PV panel as the only source. Though the inverter topology employs two capacitors of unequal voltage rating, the capacitor voltage equilibrium is established without employing an additional voltage balancing strategy. The comparative study shows that the proposed nine-level inverter topology has several advantages over other popular nine-level switched-capacitor inverter topologies, such as performance, total component count, and manufacturing cost. Finally, the results from the experiments show that the proposed NQB inverter-based PV system can work.

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