Performance Analysis of Multi-Carrier PWM and Space Vector Modulation Techniques for Five-Phase Three-Level Neutral Point Clamped Inverter

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ABSTRACT In industries, the demand for multi-phase Multi-Level Inverters (MLIs) increases as they have reduced switching loss, Common Mode Voltage (CMV) and voltage stress across switches. The Multi-Carrier PWM (MCPWM) and Space Vector Modulation (SVM) techniques are predominantly used for controlling the inverter. This paper discusses various PWM techniques like PD, POD, APOD, IC, PSC, VFC PWM and SVM (OFV and SVM with Zero CMV) for 5-phase NPC 3L Inverter. Each PWM techniques gives better results in voltage THD/ dc-link balancing/ CMV. The SVM is significant for obtaining better performances in all these aspects. The Optimized Five Vector (OFV) which has 113 vectors is preferred than normal SVM as it has inequality relationship between 5-phase voltages. Though, OFV gives better results in terms of higher output voltage and lower NPF, the CMV is not eliminated. To eliminate CMV, 51 vectors that generates Zero CMV is selected to drive the inverter where output voltage and NPF is also improved. However, due to the presence of x-y components the distortion is present. The vectors are further reduced to 31 where the x-y components are neglected to reduce the distortion is proposed in this paper. The performance of the inverter drive is enhanced by applying proposed SVM with 31 vectors. The NPF, CMV and losses are calculated for all PWM techniques, also the THD performances of an inverter is found for various techniques. The simulation is carried out for all PWM techniques and the results are verified by experimental results.

INDEX TERMS Multi-carrier pulse width modulation, 5-phase multilevel inverter, neutral point clamped inverter, space vector modulation, common mode voltage, total harmonic distortion.

ABBREVIATION

3L	3 Level.
APOD PWM	Alternate Phase Opposition and Disposition PWM.
CMV	Common Mode Voltage.
DC	Direct Current.
FPGA	Field Programmable Gate Array.
IC PWM	Interleaved Carrier PWM.
LS PWM	Level Shifting PWM.
MCPWM	Multi carrier Pulse Width Modulation.
MLI	Multi-Level Inverter.
NPC	Neutral Point Clamped.
NPF	Neutral Point Fluctuation.
OFV	Optimized Five Vectors.
PD PWM	Phase Disposition PWM.
POD PWM	Phase Opposition and Disposition PWM.
PSC PWM	Phase Shifting Carrier PWM.
PWM	Pulse Width Modulation.
RMS	Root Mean Square.
SVD	Space Vector Diagram.
SVM	Space Vector Modulation.
THD	Total Harmonic Distortion.
VFC PWM	Variable Frequency Carrier PWM.

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I. INTRODUCTION

The MLIs have gained more attraction for controlling motor drives with high voltage and current ratings [1]. The MLIs

are most commonly categorized into Neutral-Point Clamped Inverter (NPC), Flying Capacitor Inverter and Cascaded H-Bridge Inverter [2]–[5]. Among these three types, NPC draws the industry attraction due to small electromagnetic interference and increased efficiency. NPC inverters mathematical calculations and operational limitations are reviewed in [6]. Though NPC is well established in MV high power application, it has certain challenges like power quality improvement, rejection of Common Mode Voltage (CMV) and DC-Link Capacitor balancing [7]. Several strategies have been taken into consideration to improve power quality, CMV and reduction of Total Harmonic Distortion (THD) [8]–[10]. The inverter drive is controlled by providing PWM strategies which are categorized as Multi-carrier PWM, Selective Harmonic Elimination PWM [11] and Space Vector Modulation [12].

In MCPWM, PWM is generated by changing the level and phase of carrier signals. The level-shifted PWM like Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternate Phase Opposition Disposition (APOD) are discussed in [13]–[15]. In phase-shifting carrier PWM (PSC PWM), the power loss in the semiconductor switches is equally distributed [16]–[18]. The Interleaved Carrier (IC) PWM techniques is discussed in [19], [20]. An investigation is done for level-shifted PWM, phase-shifted PWM and IC PWM in [21], [22] which proposes that the PD PWM technique gives a better THD profile among phase-shifted and level-shifted PWM techniques. The current harmonics and current per phase are high in 3-phase motors. This issue can be reduced by using the 5-phase motors [23] and the torque ripple frequency is also increased which is given as $2n\pm1$, where n is the number of phases [24].

The 5-phase motors are preferred in high-power applications like air crafts, locomotive tractions, hybrid and electric vehicles, etc., [25]. The PWM control techniques for 5-phase inverters are discussed in various papers over the past decades. The PD PWM technique is applied in [26] where the voltage balancing is also done. The harmonic distortion factor for 5-phase PWM techniques is compared among PD, POD, APOD and PS PWM where the POD technique provides the highest harmonic distortion factor [27]. Various PWM techniques are compared for 5-phase Open-End Winding topology [28]. The PD technique offers a better THD profile compared to other PWM techniques. Several research studies have compared PWM techniques in a 5-phase inverter [29]–[32]. In this paper, various MCPWM is discussed along with IC PWM and Variable Frequency Carrier (VFC) PWM technique for 5-phase load that can generate Three Level (3L) output.

The research SVM techniques for 5-phase inverter is majorly done for two-level inverters [33], [34] and the control techniques of 5-phase two-level inverters [35], [36]. SVM techniques for 5-phase 3L NPC are discussed in this paper, where 243 vectors are available [37], [38]. However, only 113 vectors are utilized to produce desired voltage at d-q sub-space and maintain zero average voltage

at x-y sub-space which is named as Optimized Five Vector [39], [40]. Many control strategies like Model Predictive Control, Direct Torque Control, Field Oriented Control has been discussed in [41]–[43]. The CMV responsible for bearing current can be eliminated by selecting 51 vectors that generate zero CMV [44]. The voltage distortion is further reduced by reducing the switching vectors to 31 by neglecting the x-y components which is proposed in this paper. The voltage THD is less in this technique and the NPF is very low which balances the dc-link capacitor voltages of the NPC MLI. The 5-phase 3L NPC MLI with 31 vector SVM can be implemented in motor applications in the industries as well as in Electric Vehicles.

As the 5-phase inverter is getting more attention in the industries, a comparative study for various MCPWM and SVM techniques for 5-phase loads is done in this paper. The proposed 31 vector SVM technique is also analysed and it is found that this technique provides better performance than other PWM techniques. The section II is explained about structure, CMV, NPF and loss calculations of 5-phase NPC-MLI. In section III, various PWM and SVM strategies are discussed. The section IV comprises of simulation results for MCPWM and SVM techniques of 5-phase 3L NPC MLI. The experimentation is done and their results are presented in section V and followed by a conclusion in section VI.

II. 5-PHASE NPC-MLI
The multi-phase drive has advantages over the traditional 3-phase drive. The multi-phase drive has higher reliability, reduced harmonic current losses and current per phase, less noise, fault tolerance and efficiency are improved. The 3L NPC-MLI for 5-phase load is displayed in Fig.1.
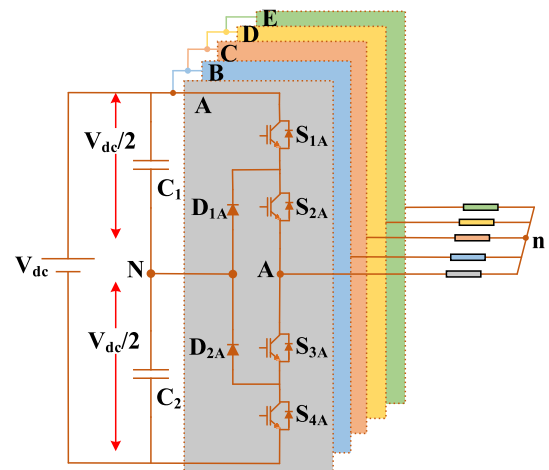

FIGURE 1. 3L NPC inverter for a 5-phase load.

The five legs of inverter are shared by two dc-link capacitors (C_1 and C_2) with a common dc source V_{dc}. This topology consists of twenty semiconductor switching devices (S_{1A}-S_{4E}) and ten clamping diodes (D_{1A}-D_{2E}). In phase-A, the Switches S_{1A} and S_{3A} are complement to each other, similarly, the switches S_{2A} and S_{4A} are complement to each
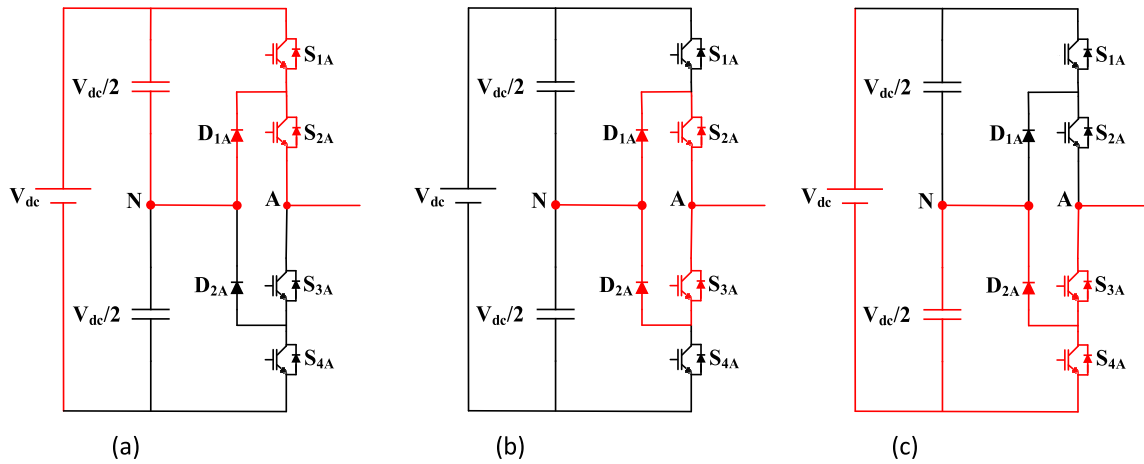
FIGURE 2. Modes of Operation for output voltage (a) Vdc/2, (b) 0, (c) -Vdc/2.

other. Likewise, each phase contains two complementary pairs of switches. The voltage stress of switches is limited to $V_{dc}/2$ through neutral point and dc-link capacitor. The voltage levels generated by switching configuration are $+V_{dc}/2$, 0 and $-V_{dc}/2$.

The switching table for phase A of 5-phase 3L NPC MLI is given in Table 1. The remaining phases will have a similar switching table. When the above two switches S_{1A} and S_{2A} are ON, then output will be $+V_{dc}/2$. When the bottom two switches S_{3A} and S_{4A} are turned ON, then output will be $-V_{dc}/2$. The output will be Zero when switches S_{1A} and S_{4A} are in ON condition. The modes of operation for 3L NPC inverter are shown in Fig. 2.

TABLE 1. Switching table for phase A of 5-phase 3L NPC MLI.

S_{1A}	S_{2A}	S_{3A}	S_{4A}	Output Voltage	Switching state
1	1	0	0	$+V_{dc}/2$	p
0	1	1	0	0	o
0	0	1	1	$-V_{dc}/2$	n

A. NEUTRAL POINT FLUCTUATION

In NPC-MLI, two dc-link capacitors are used in parallel to dc voltage source (V_{dc}). The voltage across both capacitors should be equal ($V_{dc}/2$). Still, the dc-link voltages are not balanced owing to the unequal commutation of the switches and injection of third harmonic current in neutral point. This variation of voltages at a neutral point is called Neutral Point Fluctuation.

The NPF is calculated by using the formula given below

$$NPF = \frac{\frac{V_{dc}}{2} - V_{c2}}{\frac{V_{dc}}{2}} * 100 \qquad (1)$$

where V_{c2} is the voltage across C_2 capacitor and V_{dc} is the input voltage. The 3L NPC inverter has 4 operating areas during the change of switching states. The flow of Neutral

Point Current is shown in Fig. 3 and the commutation loop in Fig. 4.

The dc-link capacitor voltage is maintained by the redundant vectors. If the dc-link voltage at the upper capacitor increases, the vector which produces low dc-link voltage is applied. Meanwhile, if the dc-link voltage at the upper capacitor is decreased, then the vector that produce high dc-link voltage is applied at the same magnitude. Likewise the dc-link capacitor voltage is balanced in SVM techniques.

B. COMMON MODE VOLTAGE

The average sum of instant voltage is called common-mode voltage (CMV). It is also known as the voltage between the neutral point of load and the inverter's ground. CMV for the 5-phase inverter is given as

$$CMV = \frac{V_{an} + V_{bn} + V_{cn} + V_{dn} + V_{en}}{5} \qquad (2)$$

where V_{an}, V_{bn}, V_{cn}, V_{dn} and V_{en} are the voltage between phase and neutral of load.

The high frequency model for 5-phase load is shown in Fig. 5 (a) where R is the resistance of stator winding per phase, L is self-inductance and C_w is a capacitance between neutral of star-connected winding and phase winding of stator, C_g is a stray capacitance between the neutral point of stator winding and ground potential. The voltage and current equations of each phase in the high-frequency model are given in Table 2. The common-mode current of the inverter will be flowing through stray capacitance C_g and calculated from Eqn. 3.

$$i_g = i_a + i_b + i_c + i_d + i_e = 5i_o = C_g \frac{dv_g}{dt} \qquad (3)$$

The common-mode model for 5-phase load is presented in Fig. 5 (b) in which l_o, R_o and C_{wo} are the zero-sequence component of L, R and C respectively. The differential mode model is presented in Fig. 5 (c) in which l_q, R_q and C_{wq} are the q-axis component of L, R and C respectively, while the d-axis model will be same as the q-axis model.
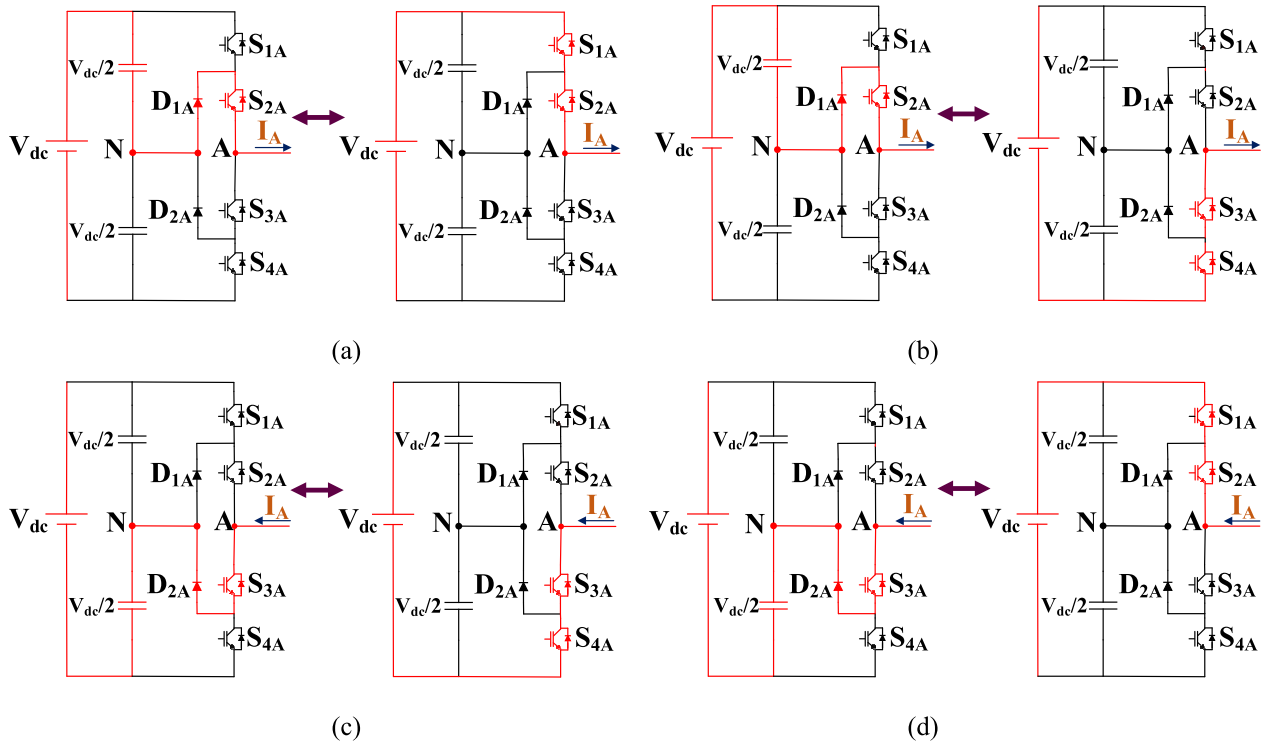
FIGURE 3. Neutral point current paths for (a) Operating Area 1, (b) Operating Area 2, (c) Operating Area 3, (d) Operating Area 4.
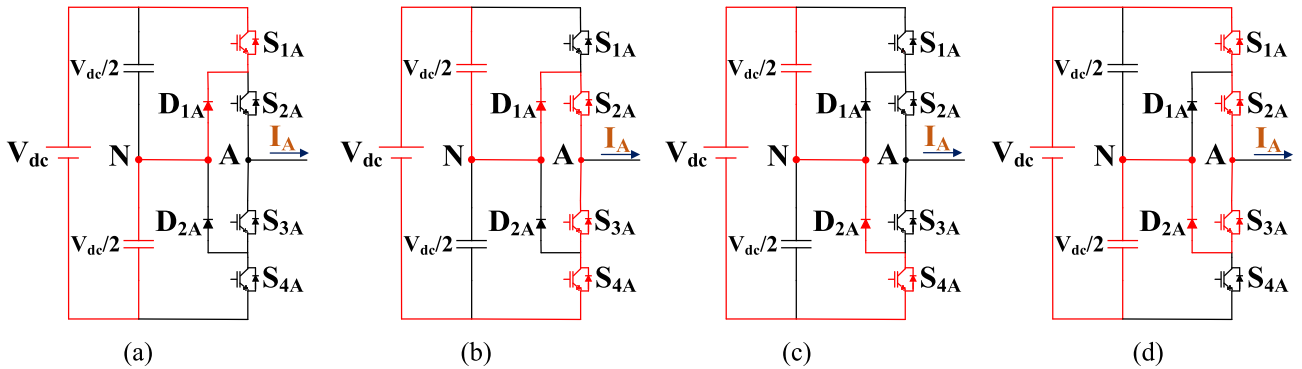

FIGURE 4. Commutation loop for (a) Operating Area 1, (b) Operating Area 2, (c) Operating Area 3, (d) Operating Area 4.

The admittance transfer function for the common-mode model (Y_o) is described as in Eqn. 4 which can be derived from Fig.5 (c) and for the differential mode model ($Y_q = Y_d$) is derived from Eqn. 5.

$$Y_o = \frac{i_o}{v_o} = \frac{s C_g L_o C_{wo}\left[s^2 + s\frac{R_o}{L_o} + \frac{1}{L_o C_{wo}}\right]}{L_o\left(C_g + 5C_{wo}\right)\left[s^2 + s\frac{R_o}{L_o} + \frac{5}{L_o(C_g+5C_{wo})}\right]} \quad (4)$$

$$Y_d = Y_q = \frac{i_q}{v_q} = \frac{C_{wq}\left[s^2 + s\frac{R_q(f)}{L_q} + \frac{1}{L_q C_{wq}}\right]}{L_q\left[s + \frac{R_q(f)}{L_q}\right]} \quad (5)$$

C. LOSSES CALCULATION

In an inverter, the power electronic switches are turned ON and OFF, leading to an increase in junction temperature. This increase in temperature is due to switching and conduction loss of switching devices. Thus, the switching loss and conduction loss are considered for loss calculation [45], [46].

1) CONDUCTION LOSSES

When the switch is turned ON, the voltage drop across collector and emitter terminal (V_{CE}) is multiplied by current will result in conduction losses. When the switch is turned OFF, conduction loss is neglected as the leakage current is very small. The conduction loss across switch and diode in phase A is given in Eqn. 6 and Eqn. 7.

$$P_S = V_{CE,S}I_{avg,S} + r_S I_{rms,S}^2 \quad (6)$$
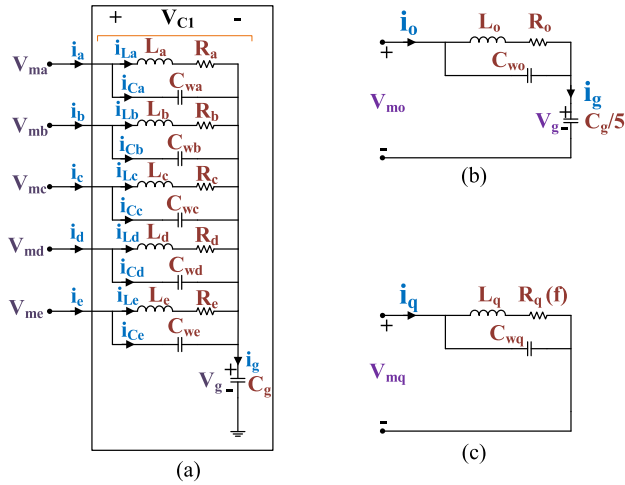
$$P_D = V_D I_{avg,D} + r_D I_{rms,D}^2 \quad (7)$$

FIGURE 5. (a) High frequency model of a 5-phase inverter motor drive, (b) Common mode model, (c) Differential mode model.

TABLE 2. Voltage and current equations of high-frequency model.

	Voltage Equations	Current Equations
Phase A	$V_{ma} = V_{C1} + V_g = L\dfrac{di_{L1}}{dt} + Ri_{L1} + v_g$	$i_a = i_{L1} + C_w\dfrac{dv_{C1}}{dt}$
Phase B	$V_{mb} = V_{C2} + V_g = L\dfrac{di_{L2}}{dt} + Ri_{L2} + v_g$	$i_b = i_{L2} + C_w\dfrac{dv_{C2}}{dt}$
Phase C	$V_{mc} = V_{C3} + V_g = L\dfrac{di_{L3}}{dt} + Ri_{L3} + v_g$	$i_c = i_{L3} + C_w\dfrac{dv_{C3}}{dt}$
Phase D	$V_{md} = V_{C4} + V_g = L\dfrac{di_{L4}}{dt} + Ri_{L4} + v_g$	$i_d = i_{L4} + C_w\dfrac{dv_{C4}}{dt}$
Phase E	$V_{me} = V_{C5} + V_g = L\dfrac{di_{L5}}{dt} + Ri_{L5} + v_g$	$i_e = i_{L5} + C_w\dfrac{dv_{C5}}{dt}$

The average current, RMS current and conduction loss for switch S$_{1A}$ are given in Eqn. 8, 9 and 10. The conduction loss for switch S$_{4A}$ is same as in S$_{1A}$.

$$I_{avg,S1} = I_{avg,S4} = \frac{MI_{CM}}{4\pi}[\sin\emptyset + (\pi - \emptyset)\cos\emptyset] \quad (8)$$

$$I_{rms,S1}^2 = I_{rms,S4}^2 = \frac{MI_{CM}^2}{6\pi}\left[1 + 2\cos\emptyset + \cos^2\emptyset\right] \quad (9)$$

$$P_{con,S1} = P_{con,S4} = \frac{MI_{CM}}{12\pi}\left\{3V_{CE,S1}[\sin\emptyset + (\pi - \emptyset)\cos\emptyset]\right.$$
$$\left. + 2r_{S1}I_{CM}[1 + \cos\emptyset]^2\right\} \quad (10)$$

The average current, RMS current and conduction loss for switch S$_{2A}$ are given in Eqn. 11, 12 and 13. The conduction loss for switch S$_{3A}$ is same as in S$_{2A}$.

$$I_{avg,S2} = I_{avg,S3} = \frac{I_{CM}}{\pi} + \frac{MI_{CM}}{4\pi}[(2\emptyset - \pi)\cos\emptyset - 2\sin\emptyset] \quad (11)$$

$$I_{rms,S2}^2 = I_{rms,S3}^2 = \frac{I_{CM}^2}{4} - \frac{MI_{CM}^2}{3\pi}\left[1 + \cos^2\emptyset\right] \quad (12)$$

$$P_{con,S2} = P_{con,S3} = \frac{I_{CM}}{12\pi}\left\{V_{CE,S2}[12 + 3M(\emptyset\cos\emptyset - \sin\emptyset)]\right.$$
$$\left. + r_{S1}I_{CM}\left[3\pi - 2M(1 + \cos\emptyset)^2\right]\right\} \quad (13)$$

The average current, RMS current and conduction loss for diodes (D) which is parallel to the switches S$_{1A}$, S$_{2A}$, S$_{3A}$ and S$_{4A}$ are given in Eqn. 14, 15 and 16. The conduction loss for the diodes parallel to switches are equal.

$$I_{avg,D} = \frac{MI_{CM}}{4\pi}[\sin\emptyset - \emptyset\cos\emptyset] \quad (14)$$

$$I_{rms,D}^2 = \frac{MI_{CM}^2}{6\pi}\left[1 - 2\cos\emptyset + \cos^2\emptyset\right] \quad (15)$$

$$P_{con,D} = \frac{MI_{CM}}{12\pi}\left\{3V_{D1}[\sin\emptyset - \emptyset\cos\emptyset]\right.$$
$$\left. + 2r_{D1}I_{CM}[1 - \cos\emptyset]^2\right\} \quad (16)$$

The average current, RMS current and conduction loss for diodes D$_{1A}$ and D$_{2A}$ are given in Eqn. 17, 18 and 19. The conduction loss for diode D$_{1A}$ is same as in D$_{2A}$.

$$I_{avg,D1A} = I_{avg,D2A} = \frac{I_{CM}}{\pi} + \frac{MI_{CM}}{4\pi}$$
$$\times [(2\emptyset - \pi)\cos\emptyset - 2\sin\emptyset] \quad (17)$$

$$I_{rms,D1A}^2 = I_{rms,D2A}^2 = \frac{I_{CM}^2}{4} - \frac{MI_{CM}^2}{3\pi}\left[1 + \cos^2\emptyset\right] \quad (18)$$

$$P_{con,D1A} = P_{con,D2A} = \frac{I_{CM}}{12\pi}\left\{V_{D2}[12 + 3M(\emptyset\cos\emptyset - \sin\emptyset)]\right.$$
$$\left. + r_{D1}I_{CM}\left[3\pi - 2M(1 + \cos\emptyset)^2\right]\right\} \quad (19)$$

2) SWITCHING LOSSES

The current will start rising during the turn-on period even before voltage drops to forward voltage drop. Likewise, the voltage will start rising during the turn-off period even before the current reduces to forward leakage current. The losses occur during turn-on and turn-off time is called as switching loss and it is expressed as

$$P_{swloss} = \frac{P_{swon} + P_{swoff}}{2} \quad (20)$$

The switching losses can be minimized by selecting proper PWM techniques which has less switching loss. The switching loss at switches S$_{1A}$, S$_{2A}$, S$_{3A}$ and S$_{4A}$ and the diodes D$_{1A}$, D$_{2A}$, D$_{3A}$ and D$_{4A}$ is given in Eqn. 21-24.

$$P_{sw,S1} = P_{sw,S4} = f_s\frac{V_{CE}}{V_{CEN}}\frac{B_{oT}}{2\pi}$$
$$\times \begin{bmatrix} I_{CM}(1 + \cos\emptyset) \\ + \dfrac{C_{oT}}{4\pi}I_{CM}^2(\cos\emptyset\sin\emptyset + (\pi - \emptyset)) \end{bmatrix} \quad (21)$$

$$P_{sw,S2} = P_{sw,S3} = f_s\frac{V_{CE}}{V_{CEN}}\begin{bmatrix} \dfrac{B_{oT}}{2\pi}I_{CM}(1 - \cos\emptyset) \\ + \dfrac{C_{oT}}{4\pi}I_{CM}^2(\emptyset - \cos\emptyset\sin\emptyset) \end{bmatrix} \quad (22)$$

$$P_{sw,D} = f_s\frac{V_{CE}}{V_{CEN}}$$
$$\times \begin{bmatrix} \dfrac{A_{oD}}{2\pi}\emptyset + \dfrac{B_{oD}}{2\pi}I_{CM}(1 - \cos\emptyset) \\ + \dfrac{C_{oD}}{4\pi}I_{CM}^2(\emptyset - \cos\emptyset\sin\emptyset) \end{bmatrix} \quad (23)$$

$$P_{sw,D1A} = P_{sw,D2A} = f_s \frac{V_{CE}}{V_{CEN}}$$

$$\times \left[\begin{array}{l} \dfrac{A_{oD}}{2\pi}(\pi - \emptyset) + \dfrac{B_{oD}}{2\pi} I_{CM}(1 + \cos \emptyset) \\ + \dfrac{C_{oD}}{4\pi} I_{CM}^2 (\cos \emptyset \sin \emptyset (\pi - \emptyset)) \end{array} \right] \quad (24)$$

III. PWM STRATEGIES FOR MULTILEVEL CONVERTERS

In Multi-level converter applications, many PWM strategies like MCPWM and SVM are available. The MCPWM scheme is usually classified into Level Shifting (LS) PWM, PSC PWM and VFC PWM. The LS PWM techniques are further classified into PD, POD and APOD PWM. The carrier signal required for MCPWM is n-1 carrier, where n is number of levels in line voltage. IC PWM method is also considered with other MCPWM techniques. The SVM schemes for generating 3L output are also considered here. The output voltage and THD performances are studied for different PWM techniques.

A. PHASE DISPOSITION (PD) PWM

In the PD PWM technique, the amplitude and frequency of all carrier signals are same, however, all carriers are displaced to different positions. The arrangements of reference and carrier signals for a 3L inverter are shown in Fig. 6 (a). In this technique, high-frequency carrier signals also can be used. The expression for modulation index and frequency ratio is given as

$$M_a = \frac{A_m}{(m-1).A_c} \quad (25)$$

$$M_f = \frac{f_c}{f_m} \quad (26)$$

where A_c and A_m are the amplitude of carrier and modulating signal respectively, meanwhile f_c and the f_m are the frequencies of carrier and modulating signal respectively.

B. PHASE OPPOSITION DISPOSITION (POD) PWM

In POD PWM technique also, amplitude and frequency of all carrier signals are maintained constant. However, the phase angles of carrier signals below and above zero reference are shifted by 180°. The arrangement of carrier signals shown in Fig. 6 (b) is for 3L inverter. This method is a combination of phase opposition and phase disposition methods. The carriers above zero reference generate positive levels, while the carriers below zero reference produce negative levels. The zero level is generated without the help of carrier signals.

C. ALTERNATIVE PHASE OPPOSITION DISPOSITION (APOD) PWM

All the carrier signals have same amplitude and frequency in APOD PWM technique however the phase angle of alternate carriers is shifted by 180° as shown in Fig. 6 (c), which is shown for 3L inverter. The carriers above and below zero reference are used to produce positive levels and negative levels. The voltage stress is reduced to some extent with this technique. It can be noted that POD and the APOD techniques
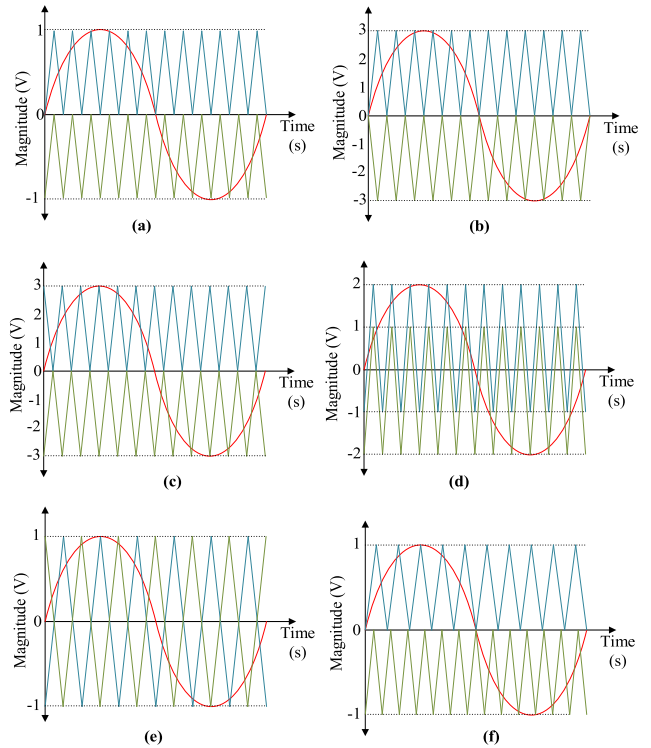

FIGURE 6. Reference and Carrier signal arrangement of 3L NPC inverter for (a) PD, (b) POD, (c) APOD, (d) IC, (e) PSC, (f) VFC PWM techniques.

will give similar results for 3L inverters, while they are different for higher-level inverters. If the level is higher than three, then POD and APOD give different outputs in which the APOD technique provides better THD performances.

D. INTERLEAVED CARRIER (IC) PWM

In IC PWM, the amplitude and frequency of all carrier signals are the same. On the other hand, they will overlap each other. Some parts of the upper carrier will be overlapped with the lower carrier signal and vice versa. This technique will improve the output voltage and reduce THD. The positive and negative levels will be generated using upper and lower carriers. The carrier and reference signal arrangements for 3L IC PWM technique are shown in the Fig. 6 (d).

E. PHASE SHIFTING CARRIER (PSC) PWM

In the PSC PWM technique, all carrier signals' levels are the same; however, the phase of every carrier signal is moved by certain degrees that result in a stepped output waveform. The amplitude and frequency of the carrier signal are identical for all carriers. The phase-shifting degree is based on the number of carriers used. The carrier and reference signal arrangements of 3L PSC PWM are shown in Fig. 6 (e).

F. VARIABLE FREQUENCY CARRIER (VFC) PWM

In the VFC PWM technique, all carriers will not have same frequency. Some of the carriers will have different frequencies. The carrier and reference signal arrangements of 3L
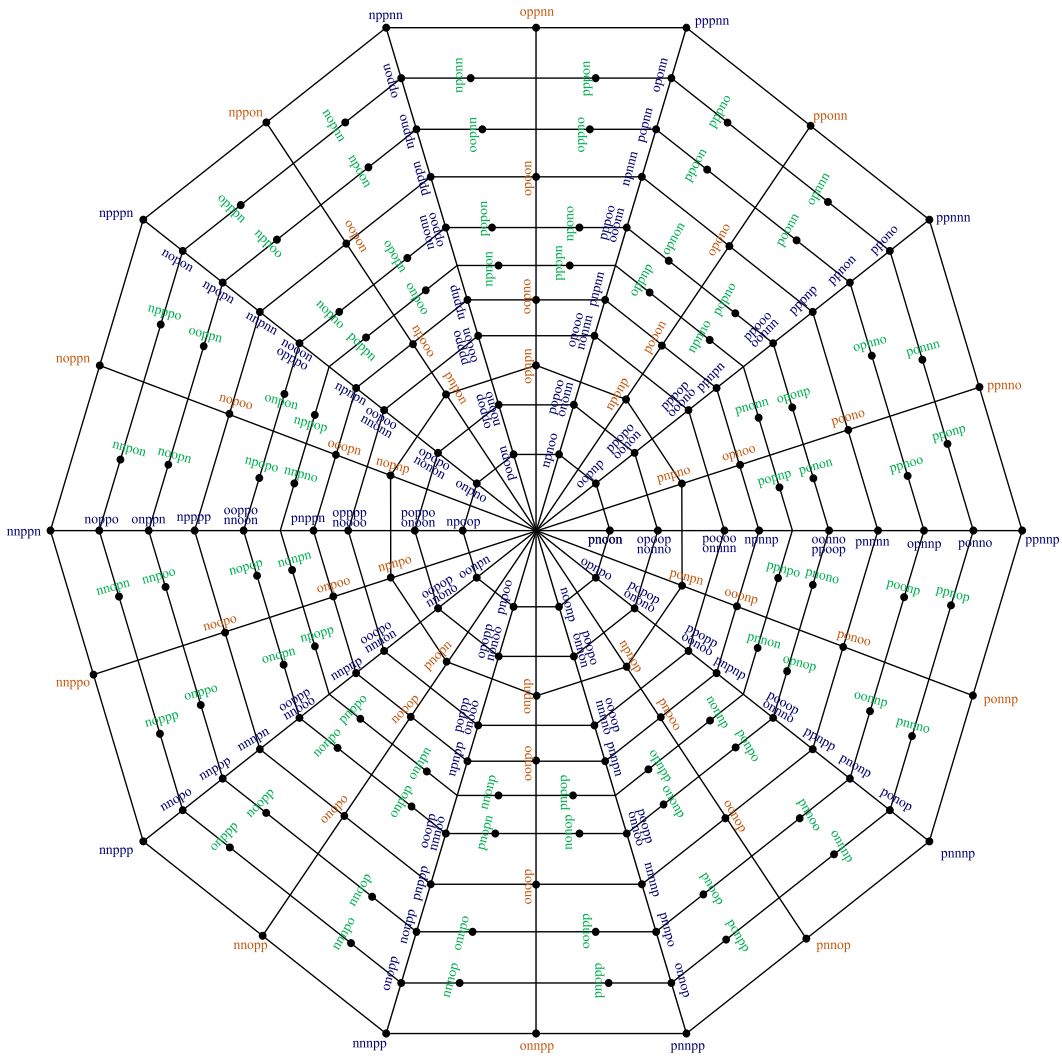
FIGURE 7. d-q space vector diagram for 5 phase NPC MLI.

TABLE 3. Magnitude of vertex and Non-vertex vectors.

Vertex Vector									
d-q space	$0.647V_{dc}$	$0.524V_{dc}$	$0.447V_{dc}$	$0.4V_{dc}$	$0.324V_{dc}$	$0.247V_{dc}$	$0.2V_{dc}$	$0.124V_{dc}$	$0.076V_{dc}$
x-y space	$0.076V_{dc}$	$0.124V_{dc}$	$0.2V_{dc}$	$0.247V_{dc}$	$0.324V_{dc}$	$0.4V_{dc}$	$0.447V_{dc}$	$0.524V_{dc}$	$0.647V_{dc}$
Non-Vertex Vector									
d-q space	$0.615V_{dc}$			$0.380V_{dc}$			$0.235V_{dc}$		$0.145V_{dc}$
x-y space	$0.145V_{dc}$			$0.235V_{dc}$			$0.380V_{dc}$		$0.615V_{dc}$

VFC PWM are shown in Fig. 6 (f). The carriers above zero level generate positive levels and the carriers below zero level generates negative levels.

G. SPACE VECTOR MODULATION (SVM)

In 5-phase 3L NPC MLI, the possibilities of switching states are $3^5 = 243$. Out of these switching vectors, 3 are zero vectors and the remaining 240 are active vectors. Two vector spaces are available for the 5-phase system, namely d-q space

and x-y space. The space vector voltages V_{dq} and V_{xy} are calculated from Eqn. 27 and Eqn. 28, by knowing the values of 5-phase pole voltages (V_{an}, V_{bn}, V_{cn}, V_{dn} and V_{en}) from switching states.

$$V_{dq} = \frac{2}{5}\left(V_{an} + \delta V_{bn} + \delta^2 V_{cn} + \delta^3 V_{dn} + \delta^4 V_{en}\right) \quad (27)$$

$$V_{xy} = \frac{2}{5}\left(V_{an} + \delta V_{cn} + \delta^2 V_{en} + \delta^3 V_{bn} + \delta^4 V_{dn}\right) \quad (28)$$

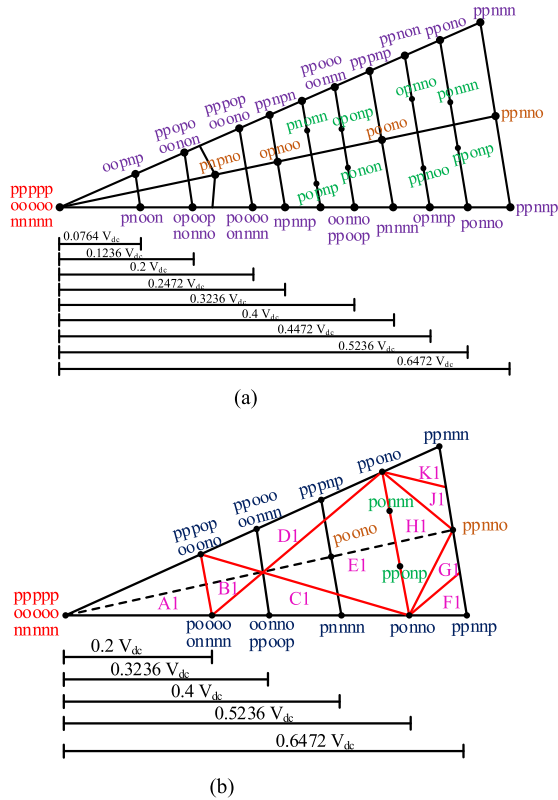where $\delta = e^{j\frac{2\pi}{5}}$

(a)

(b)

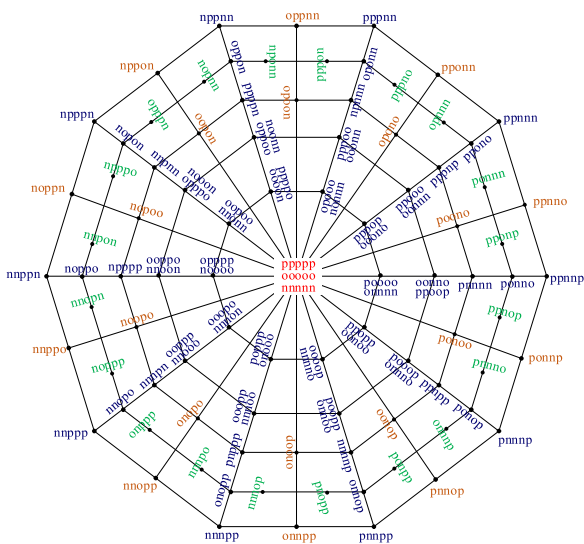**FIGURE 8.** Sector I representation of (a) general 3L SVM, (b) OFV SVM.

FIGURE 9. Optimized Five Vector diagram for 5-phase NPC MLI in d-q frame.

TABLE 4. Potential switching sequences of OFV in sector I.

Sub Region	Switching Sequence
1 (A1)	oonno-ooono-ooooo-poooo-ppooo-ppoop
2 (B1)	oonno-ooono-poono-poooo-ppooo-ppoop
3 (C1)	oonno-ponno-poono-poooo-ppooo-ppoop
4 (D1)	oonno-ponno-poono-ppono-ppooo-ppoop
5 (E1)	oonno-ooono-poono-ppono-ppooo-ppoop
6 (F1)	oonno-ponno-ppnno-ppnnp-pponp-ppoop
7 (G1)	oonno-ponno-ppnno-ppono-pponp-ppoop
8 (H1)	oonno-ponno-ppnno-ppono-ppooo-ppoop
9 (J1)	oonnn-ponnn-poono-ppnno-ppono-ppoop
10 (K1)	oonnn-ponno-ppnnn-ppnno-ppono-ppoop
11	oonno-ponno-poono-ppono-pponp-ppoop
12	oonnn-ponno-poono-ppono-ppono-ppooo
13	onnnn-oonnn-ponnn-ponno-poono-poooo
14	oonno-ooono-poono-ppono-pponp-ppoop
15	onnnn-pnnnn-ponnn-ponno-poono-poooo
16	ooono-poono-ppono-pponp-pppnp-pppop

TABLE 5. Vectors of 5-phase 3L inverter with zero CMV.

Vector number	Switching Vectors	Vector number	Switching Vectors	Vector number	Switching Vectors
V0	ooooo	V17	nooop	V34	nppon
V1	pnpno	V18	oonpo	V35	noppn
V2	nponp	V19	pnooo	V36	nnppo
V3	opnpn	V20	ooonp	V37	nnopp
V4	pnpno	V21	poono	V38	onnpp
V5	nopnp	V22	opono	V39	pnnop
V6	npnpo	V23	opoon	V40	ponnp
V7	pnopn	V24	oopon	V41	opnnp
V8	onpnp	V25	nopoo	V42	ppnon
V9	npnop	V26	noopo	V43	popnn
V10	ponpn	V27	onopo	V44	nppno
V11	opnoo	V28	onoop	V45	npopn
V12	pooon	V29	oonop	V46	onppn
V13	oopno	V30	ponoo	V47	nnpop
V14	npooo	V31	ppnno	V48	nonpp
V15	ooopn	V32	pponn	V49	pnnpo
V16	onpoo	V33	oppnn	V50	pnonp

where S_a, S_b, S_c, S_d and S_e (+1, 0 or -1) are the switching states of a, b, c, d and e phases.

The space vector diagram for d-q space model is shown in Fig. 7. The space vector has ten sectors each separated by 36° from one another. There are two vertices in 5-phase SVM, one is the Vertex vector whose angle is ($\theta = 0°$, 36°, 72°, so on) and the other is a non-vertex vector whose angle is ($\theta = 18°$, 54°, 90° so on). From the space vector diagram, it can be noticed that 120 vectors are present in vertex vector

The phase voltage across stator winding can be given as

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \\ V_{dn} \\ V_{en} \end{bmatrix} = \frac{1}{5}\frac{V_{dc}}{2} \begin{bmatrix} 4 & -1 & -1 & -1 & -1 \\ -1 & 4 & -1 & -1 & -1 \\ -1 & -1 & 4 & -1 & -1 \\ -1 & -1 & -1 & 4 & -1 \\ -1 & -1 & -1 & -1 & 4 \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \\ S_d \\ S_e \end{bmatrix} \quad (29)$$
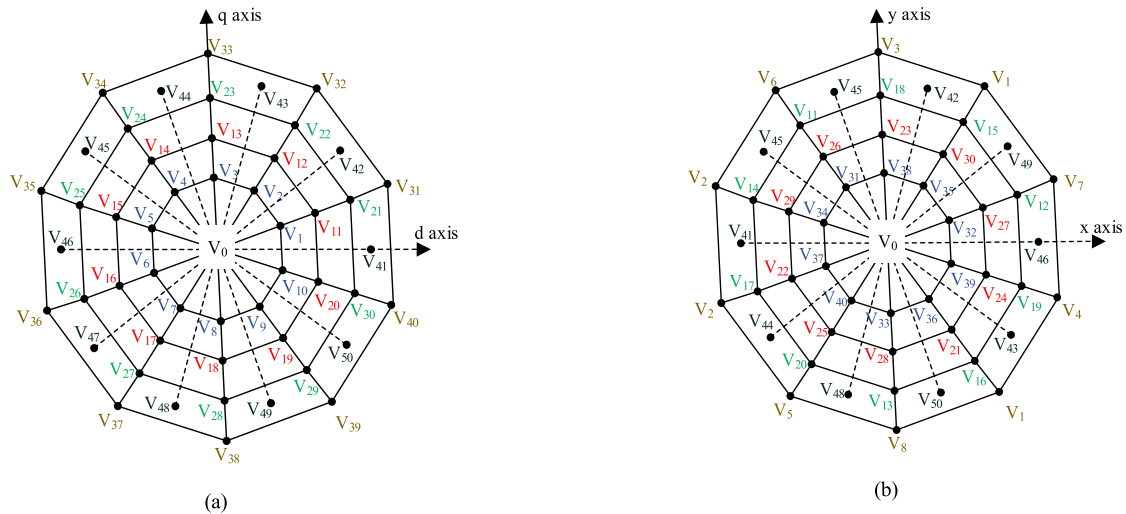
FIGURE 10. SVM with 51 vectors for producing zero CMV of (a) d-q sub-space (b) x-y sub-space.
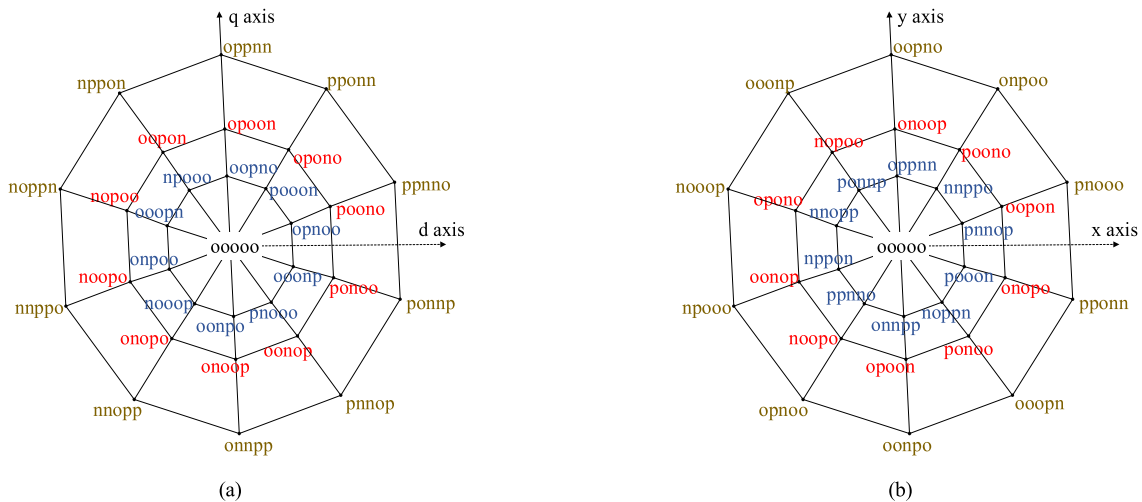

FIGURE 11. SVM with 31 vectors for producing zero CMV of (a) d-q sub-space (b) x-y sub-space.

out of which 60 vectors are redundant, while 40 vectors are available in non-vertex vector and 80 vectors will be placed in between vertex and non-vertex with the remaining three vectors are zero vectors placed at the origin. The magnitude of vertex and non-vertex vectors is given in table 3. It can be noticed that when d-q space has highest magnitude, x-y space has lowest magnitude and vice versa.

The volt-sec equation of the resultant vector is given as

$$T_s\overrightarrow{V_{dqref}} = T_o\overrightarrow{V_o} + T_1\overrightarrow{V_1} + T_2\overrightarrow{V_2} + T_3\overrightarrow{V_3} + T_4\overrightarrow{V_4} \quad (30)$$

$$T_s\overrightarrow{V_{xyref}} = T_oV_o + T_1\overrightarrow{V_1} + T_2\overrightarrow{V_2} + T_3\overrightarrow{V_3} + T_4\overrightarrow{V_4} = 0 \quad (31)$$

$$T_s = T_o + T_1 + T_2 + T_3 + T_4 \quad (32)$$

where, T_o, T_1, T_2, T_3 and T_4 are the dwell time of switching vectors $\overrightarrow{V_o}$, $\overrightarrow{V_1}$, $\overrightarrow{V_2}$, $\overrightarrow{V_3}$ and $\overrightarrow{V_4}$ of selected switching sequence, T_s is the switching period, $\overrightarrow{V_{dqref}}$ and $\overrightarrow{V_{xyref}}$ are the reference output voltage in d-q and x-y space. The matrix form of dwell

time is given in Eqn. 33.

$$\begin{bmatrix} T_0 \\ T_1 \\ T_2 \\ T_3 \\ T_4 \end{bmatrix} = \begin{bmatrix} V_{d0} & V_{d1} & V_{d2} & V_{d3} & V_{d4} \\ V_{q0} & V_{q1} & V_{q2} & V_{q3} & V_{q4} \\ V_{x0} & V_{x1} & V_{x2} & V_{x3} & V_{x4} \\ V_{y0} & V_{y1} & V_{y2} & V_{y3} & V_{y4} \\ 1 & 1 & 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} V_d \\ V_q \\ V_x \\ V_y \\ T_s \end{bmatrix} \quad (33)$$

1) OPTIMIZED FIVE VECTOR SVM

The general 3L SVM which has 243 vectors are not used because of the inequality relationship between 5-phase voltages. Thus, vectors are reduced to 113 vectors to produce desired voltage reference at d-q subspace and maintain zero-average voltage at x-y subspace. These vectors are called OFV. The sector I representation of SVM and OFV SVM for 5-phase 3L is shown in Fig. 8 (a) and Fig. 8 (b). The balancing of DC-link capacitor voltage in unbalanced condition is taken care by redundant vectors available in SVM. The OFV has
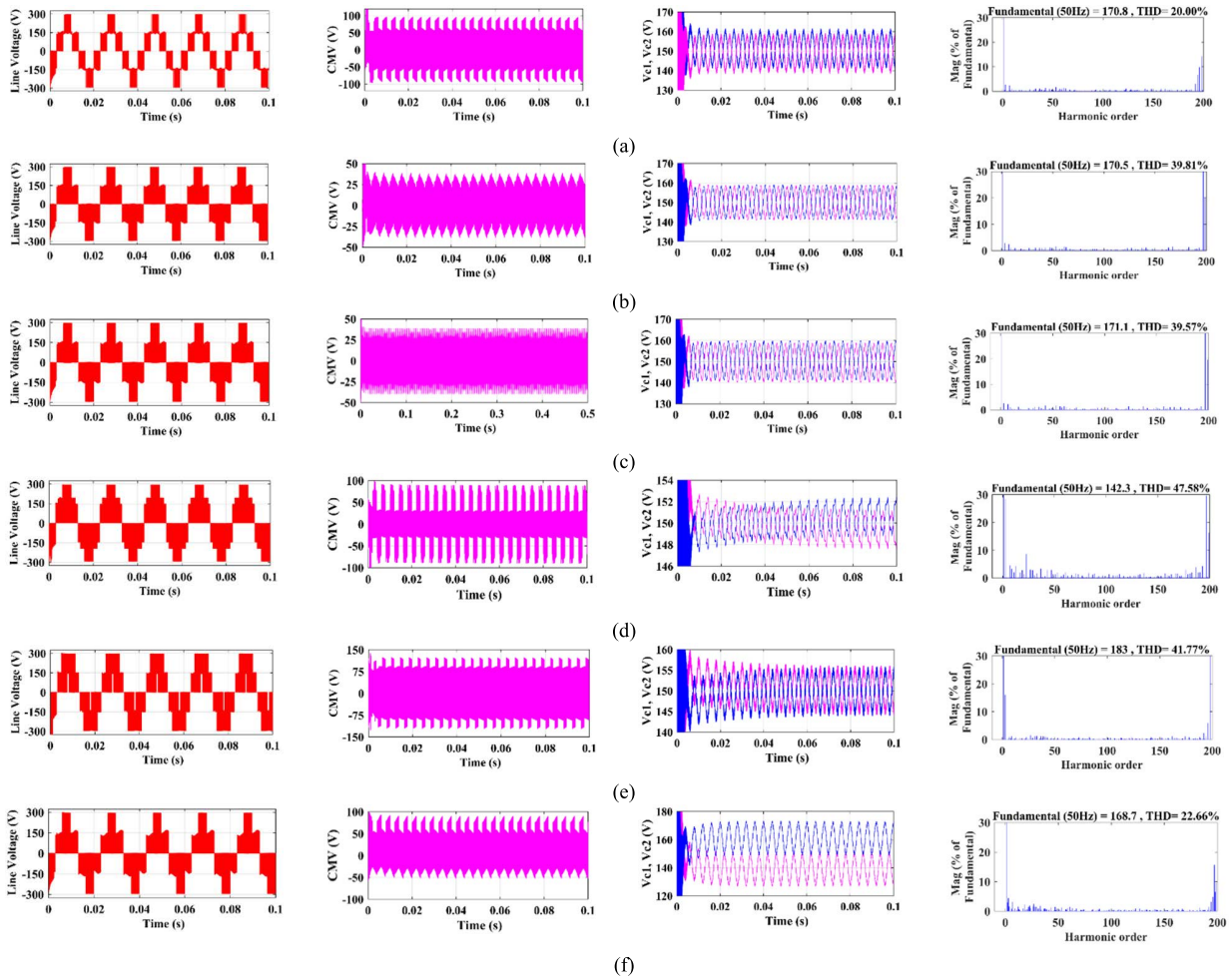
FIGURE 12. Simulation results - Line voltage, THD, CMV, DC link capacitor voltages for (a) PD, (b) POD, (c) APOD, (d) PSC, (e) IC, (f) VFC.

21 vectors in sector I compared to general 3L SVM which has 39 vectors. The magnitudes of vectors in OFV SVM are $0.2V_{dc}$, $0.324V_{dc}$, $0.4V_{dc}$, $0.524V_{dc}$ and $0.647V_{dc}$. The potential switching sequences based on OFV have been listed in Table 4. The sub-region 1 to 10 will produce desired voltage reference in d-q sub-space by removing the x-y sub-space vectors whose regions are shown in Fig. 8 (b). The switching sequences 11 to 16 are unable to nullify x-y sub-space vectors. Thus, the switching sequences at region A1 to K1 are only employed in OFV SVM. The SVM of OFV for 5-phase 3L NPC MLI at d-q subspace is shown in Fig. 9.

The sub-region 1 to 10 will produce desired voltage reference in d-q sub-space by removing the x-y sub-space vectors whose regions are shown in Fig. 8 (b). The switching sequences 11 to 16 are unable to nullify x-y sub-space vectors. Thus, the switching sequences at region A1 to K1 are only employed in OFV SVM. The SVM of OFV for 5-phase 3L NPC MLI at d-q subspace is shown in Fig. 9.

2) SVM WITH ZERO CMV
To eliminate CMV in a 5-phase inverter, the SVM for 3L is developed with 51 selected vectors with zero CMV which is listed in Table. 5. The SVM diagram is shown in Fig. 10 (a) and 10 (b) are for d-q plane and x-y plane which produce zero CMV at the output. The voltage resulting from 51 vectors will have distortion due to the availability of x-y components. By neglecting the vectors in x-y components, the distortion is further reduced as shown in Fig. 11 (a) and Fig. 11 (b). In this combination, 30 active vectors are available while one vector is zero vector. All the active vectors in this condition are present in a non-vertex vector with the magnitude of $0.235V_{dc}$, $0.380V_{dc}$ and $0.615V_{dc}$.

IV. SIMULATION RESULTS
The performance of 5-phase 3L NPC is investigated for various MCPWM schemes with MATLAB/ Simulink. A 300V DC supply is given with a 100μF capacitor and 10 kHz switching frequency. The RL load is considered with R = 10Ω and L = 2mH. The output voltage and THD waveform for different PWM schemes with a modulation index of 1 ($M_i = 1$) are shown in Fig. 12. The Third Harmonic Injection (THI) is done for all MC PWM techniques and their performances are also studied. The line voltage, CMV, DC link voltages and voltage THD of PD is shown in Fig. 12 (a),
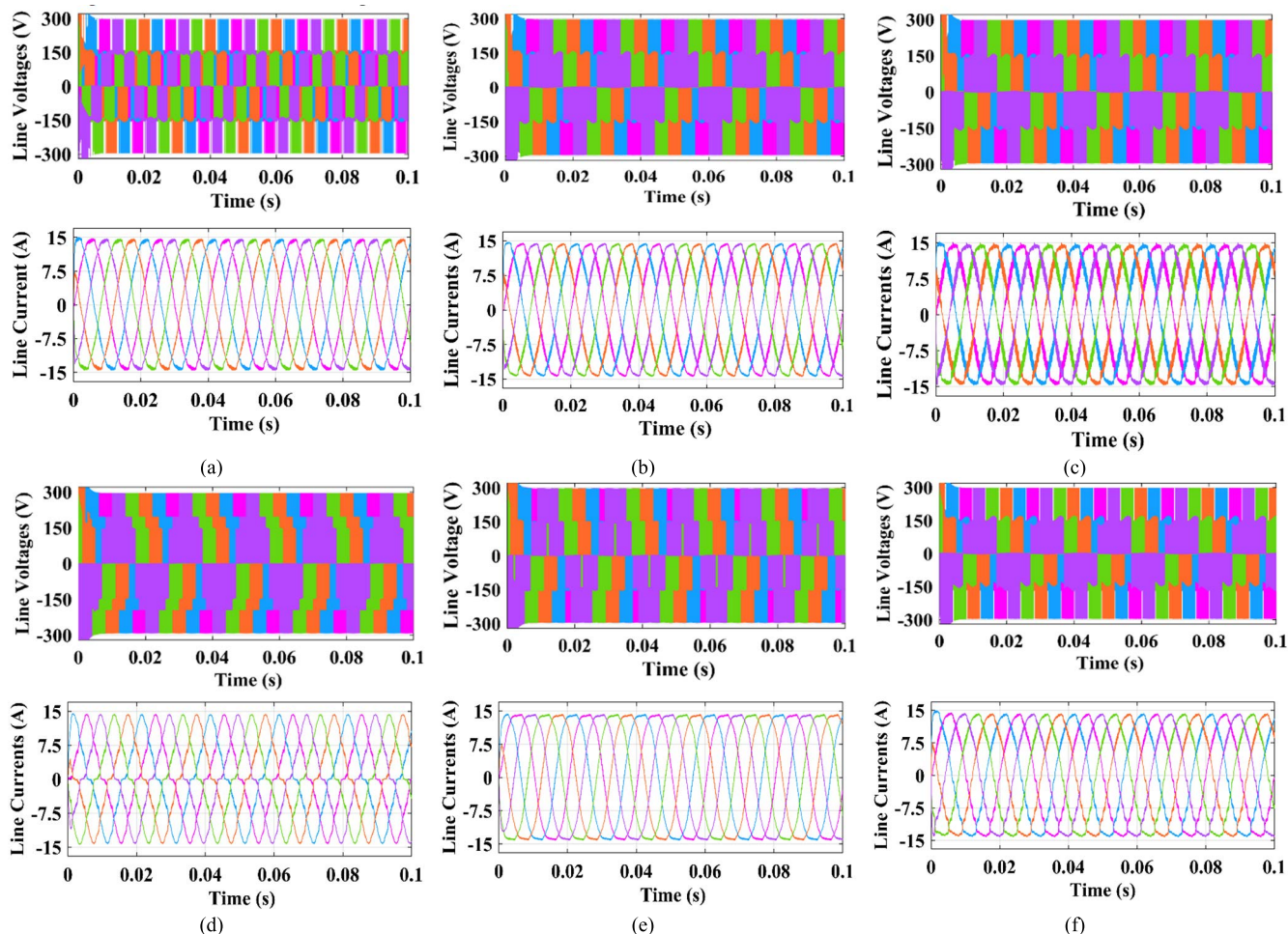
FIGURE 13. Simulation results: Line voltages and Line currents of 5-phase loads for (a) PD, (b) POD, (c) APOD, (d) PSC, (e) IC, (f) VFC.

where quarter symmetry of the output voltage is maintained in this technique. The voltage is read as 170.80V, while CMV is high in this condition. The NPF is at considerable range as V_{C1} and V_{C2} is obtained in the range of 140 V to 160V. The results of POD technique are shown in Fig. 12 (b), output voltage is maintained similar to PD technique whereas CMV is reduced to 39V and THD is increased to 39.81%. In APOD technique, all output results will be similar to POD technique as both techniques are equivalent in 3L PWM generation. The results of APOD technique is shown in Fig. 12(c).

The phase of the carrier signal is varied by keeping the amplitude and frequency unchanged. The voltage level drop in this technique while CMV and THD is increased as shown in Fig. 12(d), however NPF is very low in PSC PWM. The performances of IC and VFC PWM techniques are displayed in Fig. 12 (e) and Fig. 12 (f). The output voltage is increased in IC PWM whereas CMV is very high with voltage THD also reads more. The VFC PWM technique reduces the voltage THD level to match with PD PWM technique, however NPF touches the highest value among other PWM techniques which increases the dc-link balancing issue.

The line voltages and line currents of all 5-phases are observed as shown in Fig.13 (a) to Fig. 13 (f). The line voltages are symmetrical through all 5-phase while applying normal MCPWM techniques as the reference signals are sinusoidal. The line currents are obtained as 15A for all types of PWM techniques. As RL load is used for the simulation, the line current is of sinusoidal shape with each phase is varied by 72°. The line currents at PSC PWM technique is not fully sinusoidal as all the carrier signals at equal amplitude as shown in Fig. 13 (d). In VFC PWM techniques, the current is not pure sinusoidal as the frequency of the carrier signals are different as in Fig. 13 (f).

The 3rd harmonic is injected in all types of MC PWM; the line voltage, THD, CMV and DC link voltage for PD Third Harmonic Injection (THI) is shown in Fig. 14 (a). The output voltage drops a little compared to normal PO PWM technique whereas NPF is increased by the injection of third harmonic content to the carrier signal. The results of POD THI and APOD THI are given in Fig. 14 (b) and Fig. 14 (c). The output voltage, CMV, DC link voltage and voltage THD is similar in both conditions for 3L inverter. The performance
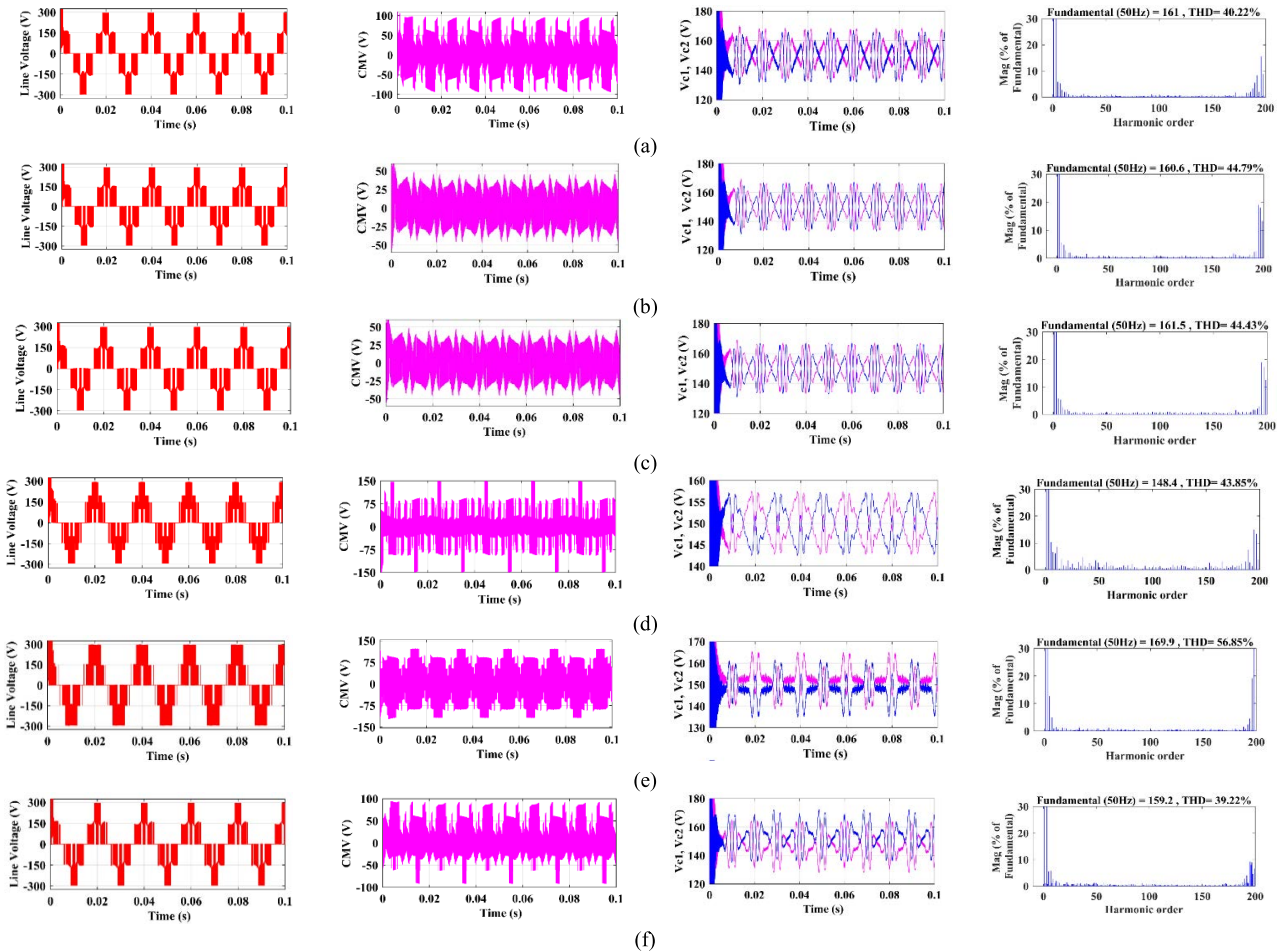
FIGURE 14. Simulation results - Line voltage, THD, CMV, DC link capacitor voltages for (a) PD THI, (b) POD THI, (c) APOD THI, (d) PSC THI, (e) IC THI, (f) VFC THI.

of PSC THI like line voltage, voltage THD, CMV and DC link voltage is obtained as in Fig. 14 (d). The THD is reduced after few orders and it is increased again near to the 200th order. Though NPF is less, CMV is high in this technique. The output of NPC inverter when applied with IC THI and VFC THI are shown in Fig. 14 (e) and Fig. 14 (f). The output voltage of IC THI PWM technique is higher (169.90V) than other THI technique whereas voltage THD and CMV is higher in this technique. The results of VFC THI reads the output voltage as 159.20V with THD is better among other THI techniques while NPF is high in this types as the frequency of each carrier signal is different.

The line voltages and line currents of all 5-phase for THI PWM types are shown in Fig. 15 (a) to 15 (f). The output voltages are unsymmetrical in all phase due to the injection of the third harmonic content in the reference signals. The distortion of output voltage is very high in PSC THI technique. The output current is non-sinusoidal as it is noticed from the current waveforms. Similar to output voltage, the output current is also unsymmetrical. Owing to the presence of third harmonic content, the phase angle various in each phase that

leads to the unsymmetrical waveform. The output voltage and current of PD THI technique is shown in Fig. 15 (a), while the results of POD THI and APOD THI techniques are shown in Fig. 15 (b) and Fig. 15 (c) respectively. As mentioned earlier, the results of POD THI and APOD THI will be similar to each other. The line voltage and line current of all 5-phases for PSC THI PWM is shown in Fig. 15 (d) and it is noticed that the distortion of voltage and current is high in this condition. Meanwhile, the results of IC THI PWM technique is shown in Fig. 15 (e) and the output waveforms of VFC THI techniques are shown in Fig. 15 (f). From the results, it can be observed that, PWM with THI degrade the performance of the inverter when compared to the PWM technique where sinusoidal reference signal is implemented. However, the reference vector detection takes more time in MCPWM as they generate analog control signal.

The simulation for SVM techniques is also done using MATLAB Simulink. The results of OFV SVM are shown in Fig. 16 (a) where the THD (27.31%) and CMV (40V) performances are better compared with MC PWM techniques. The NPF is reduced by applying OFV SVM technique. The
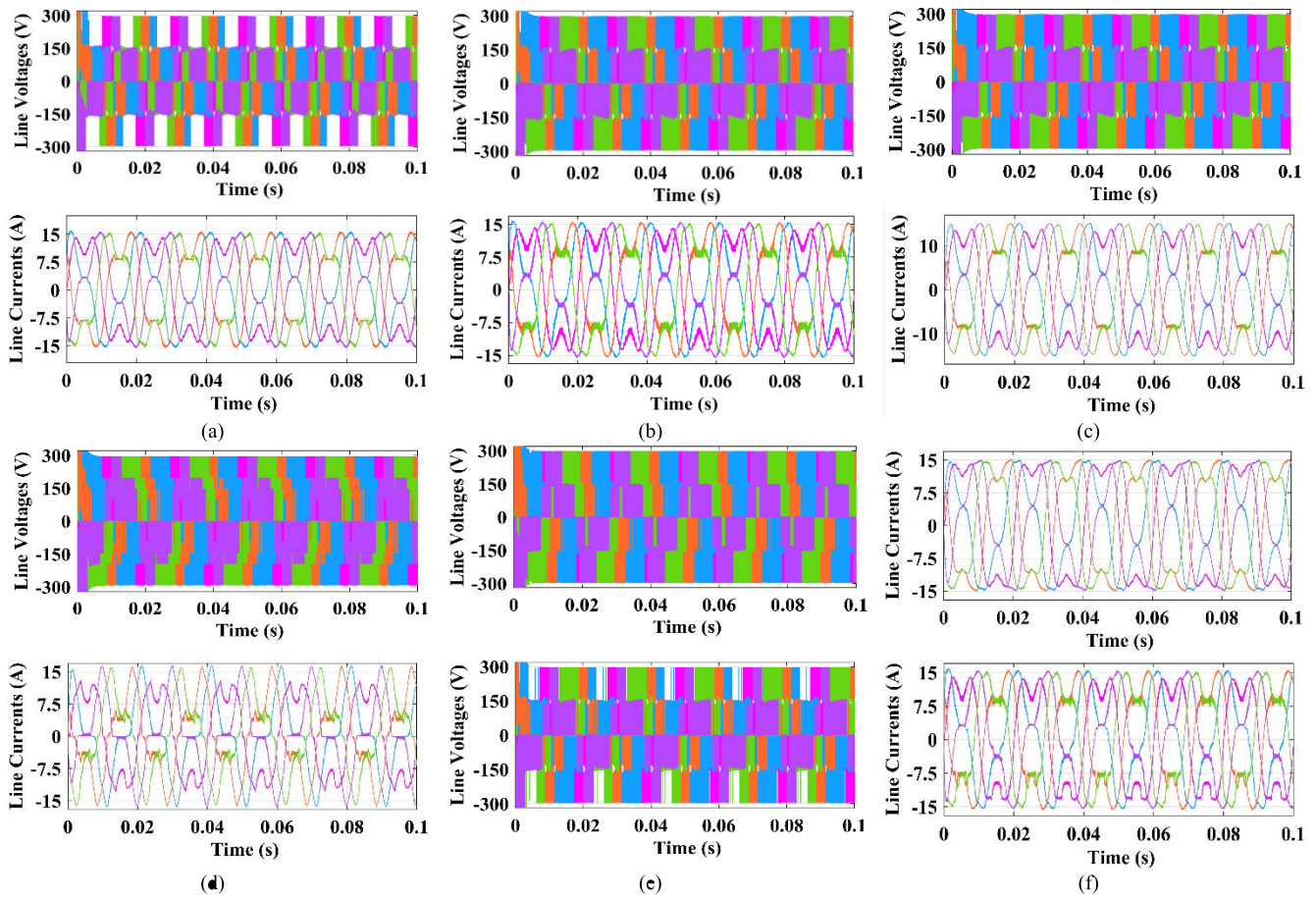
FIGURE 15. Simulation results: Line voltages and Line currents of 5-phase loads for (a) PD THI, (b) POD THI, (c) APOD THI, (d) PSC THI, (e) IC THI, (f) VFC THI.
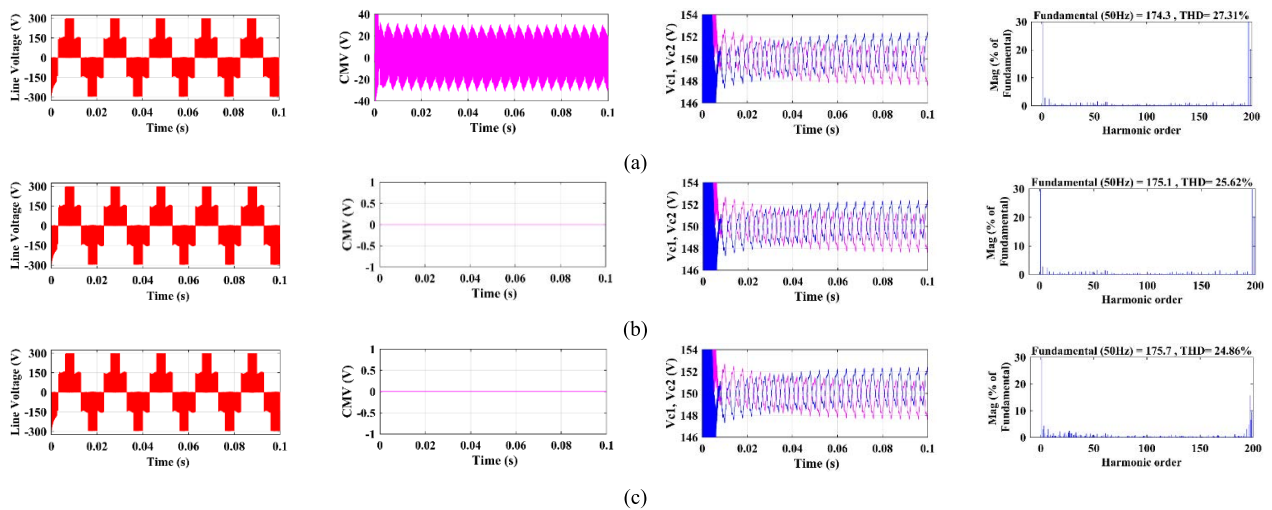

FIGURE 16. Line voltage, THD, CMV, DC link capacitor voltages of (a) OFV SVM, (b) 51 vectors, (c) 31 vectors.

CMV resulting in the inverter is responsible for the flow of bearing current in motors. Thus, the elimination of CMV is very important to improve the performances of the inverter drives. The CMV is eliminated by selecting 51 vectors which

generates Zero CMV and its results are shown in Fig. 16 (b). It is noted that the CMV is Zero in this SVM technique, with voltage THD is obtained as 25.62% and NPF as 1.33%. The output performance are increased as the switching states
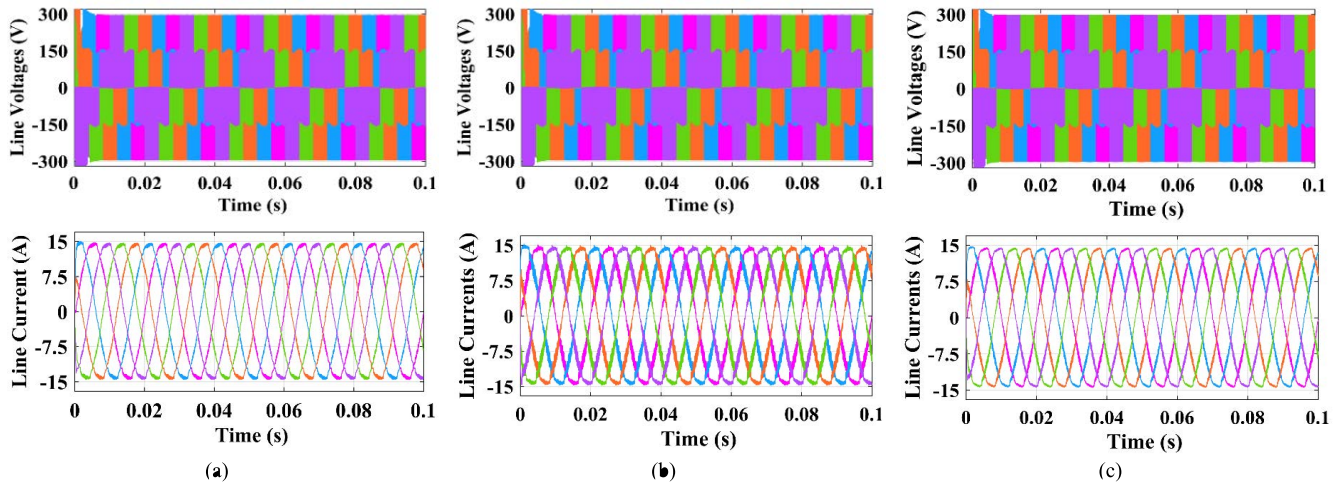
FIGURE 17. Simulation results: Line voltages and Line currents of 5-phase loads for (a) OFV, (b) 51 Vectors, (c) 31 vectors.

are reduced in this type. The switching vectors are further reduced to 31 which reduces the ripples with output voltage, THD, CMV and DC link voltages are shown in Fig. 16 (c). The CMV is Zero and the voltage THD is obtained as 24.86%. The NPF is also less in this type and it is calculated as 1.44%. It can be noticed that in 51 vectors and 31 vectors types of SVM, the CMV is completely eliminated.

The results of line voltage and line currents at all 5-phases are shown in Fig. 17. The line current is read as 15 A in SVM techniques. It is also observed that the output waveforms are symmetrical with 72° phase shift. The line voltage and current for OFV is shown in Fig. 17 (a). The vector are reduced to 51 vectors which can generate Zero CMV is selected and the corresponding voltage and current waveforms are obtained as in Fig. 17 (b). Though it eliminates the CMV, the ripples are present in the current which is noticed form the output waveform. This distortion can be reduced by further reducing the vectors to 31 in which the x- components are neglected. The respective 5-phase voltage and current waveforms of 31 vector SVM is shown in Fig. 17 (c).

In terms of control complexities, the controlling is easy when MCPWM techniques are implemented. However, the performance of the inverter is less when compared to SVM techniques. In SVM techniques, the control complexity is high as the vectors available is more (113 vectors) which leads to long waiting time for the selection of vector. The tracing of reference vector is difficult as many triangles are available in the SVM. To overcome this complexity issue, the 31 vector SVM technique is proposed where the complexity is reduced as the number of vectors are less and also the CMV is eliminated as the vectors which generates zero CMV is selected. The voltage THD and NPF is less in the proposed 31 vector SVM which increases the efficiency of the inverter. The different PWM techniques are analysed and the pros and cons of each technique is listed in table 6.

The simulation is carried out for different modulation indices (M_i = 1, 0.9, 0.8, …, 0.1). The inverter output

TABLE 6. Pros and Cons of different PWM techniques.

PWM Technique	Pros	Cons
PD	THD is Low	CMV is High
POD	CMV is Low	THD is High
APOD	CMV is Low	THD is High
PSC	NPF is low	Output Voltage is low CMV is High THD is High
IC	Output Voltage is high	CMV is High THD is High
VFC	THD is Low	CMV is High NPF is High
PD THI	THD is Low	CMV is High
POD THI	CMV is Low	THD is High
APOD THI	CMV is Low	THD is High
PSC THI	NPF is low	Output Voltage is low CMV is High THD is High
IC THI	Output Voltage is high	CMV is High THD is High
VFC THI	THD is Low	CMV is High NPF is High
OFV	THD, CMV and NPF are low	CMV is present
51 Vector SVM	THD, CMV and NPF are low	Ripples are present
Proposed 31 Vector SVM	THD, CMV and NPF are low	-

voltage is almost identical for all PWM techniques, however THD performance is the one to be noticed among these techniques. The PD and VFC provide better THD performances 20.33% and 22.66%, respectively, compared to other PWM techniques. When the modulation index is reduced, the output line voltage is considerably reduced for all PWM techniques. If the modulation index is 0.5 or less, then the output voltage will be of 2L instead of 3L.

The inverter output line voltage, THD%, CMV and NPF% obtained from various PWM schemes at different modulation

TABLE 7. Simulation results of line voltage and THD for various PWM techniques.

| PWM	Output	Mi = 1	0.9	0.8	0.7	0.6	0.5	0.4	0.3	0.2	0.1
PD	V	170.80	153.60	136.00	118.40	100.90	83.36	65.52	47.60	29.25	9.97
	THD %	20.00	21.17	22.05	23.54	33.60	42.84	52.03	59.27	63.66	66.49
	CMV	95.00	94.00	94.00	94.10	92.50	92.00	91.00	92.00	90.50	90.00
	NPF%	8.30	6.38	5.63	6.01	4.17	3.45	2.74	2.39	1.69	0.33
POD	V	170.50	153.50	135.90	118.20	100.80	83.30	65.58	47.52	29.33	9.95
	THD %	39.81	44.28	50.64	59.30	69.14	78.79	88.28	98.53	110.27	150.88
	CMV	39.00	37.50	36.50	35.50	34.00	33.50	32.00	31.50	30.50	30.20
	NPF%	6.38	5.63	4.90	4.17	3.09	2.74	1.69	1.01	0.67	0.13
APOD	V	171.10	153.60	136.10	118.60	100.80	83.38	65.43	47.66	29.17	9.98
	THD %	39.57	43.95	50.71	59.13	68.93	78.76	88.78	98.29	109.59	150.35
	CMV	38.80	37.70	36.50	35.60	34.40	33.60	32.50	31.50	30.80	30.00
	NPF%	7.14	5.49	4.53	3.95	2.95	2.46	1.63	1.08	0.50	0.07
PSC	V	142.30	128.90	90.27	80.09	61.81	36.33	10.05	9.02	6.86	3.55
	THD %	47.58	60.41	74.38	84.89	142.52	158.87	224.84	496.52	728.22	832.16
	CMV	89.00	91.00	90.20	90.70	90.40	90.10	90.20	90.20	30.50	30.50
	NPF%	1.69	2.04	0.67	0.87	0.40	0.13	0.17	0.17	0.03	0.03
IC	V	183.00	174.30	160.50	143.90	133.70	111.80	90.19	70.96	40.38	18.73
	THD %	41.77	41.27	38.36	36.59	36.91	32.06	32.56	26.01	31.31	65.45
	CMV	123.00	111.00	125.00	128.50	138.50	146.00	145.00	154.50	150.50	149.90
	NPF%	4.17	11.94	6.08	9.09	12.36	4.53	7.14	3.81	0.67	0.47
VFC	V	168.70	155.30	133.60	120.30	98.07	85.48	61.91	49.73	23.19	12.30
	THD %	22.66	26.15	26.25	36.43	36.10	53.61	46.23	76.54	65.92	108.24
	CMV	90.00	101.00	85.00	103.50	89.00	108.00	67.00	123.00	30.00	170.00
	NPF%	18.11	14.50	20.48	19.05	25.52	26.05	42.18	58.73	68.00	90.00
PD THI	V	161.00	151.90	137.90	121.20	103.30	85.74	69.82	51.60	32.39	14.52
	THD %	40.22	38.96	41.94	45.00	47.33	54.30	62.21	71.00	76.79	100.78
	CMV	96.00	93.00	95.00	93.00	93.00	91.00	92.00	91.50	91..8	90.50
	NPF%	12.00	12.00	7.33	4.67	4.67	4.33	3.00	2.00	3.00	1.00
POD THI	V	160.60	152.30	138.10	121.60	103.30	85.84	69.88	51.62	32.37	14.56
	THD %	44.79	46.99	52.96	60.96	69.31	80.03	88.63	99.55	110.76	135.88
	CMV	46.00	45.50	39.00	35.00	35.50	33.00	33.00	31.50	33.50	31.50
	NPF%	11.33	11.00	6.20	3.60	3.67	2.67	2.27	1.07	2.67	0.73
APOD THI	V	161.50	151.60	137.80	120.90	103.20	85.64	69.72	51.54	32.39	14.48
	THD %	44.43	46.32	53.64	61.24	69.11	79.98	88.79	99.98	111.20	135.58
	CMV	36.60	36.70	34.10	33.80	33.00	33.60	37.50	33.50	39.20	35.50
	NPF%	4.47	4.53	2.93	2.67	2.00	3.00	5.20	2.67	6.20	3.60
PSC THI	V	148.40	134.90	110.90	86.87	57.19	42.22	22.52	8.48	5.02	2.66
	THD %	43.85	49.39	60.16	82.38	108.66	138.32	218.61	480.88	712.16	805.49
	CMV	151.50	149.50	150.50	150.00	151.00	153.00	136.00	138.00	150.00	30.10
	NPF%	4.93	4.53	2.53	1.87	1.67	2.53	0.93	0.60	0.27	0.07
IC THI	V	169.90	163.00	155.10	141.30	128.50	109.10	91.66	70.65	47.88	24.65
	THD %	56.85	54.47	54.34	53.26	52.21	51.74	45.92	45.39	38.97	61.17
	CMV	122.00	155.00	147.60	155.00	157.00	153.50	157.00	156.20	152.60	151.00
	NPF%	10.00	10.00	4.80	4.67	6.00	4.20	5.67	5.07	3.07	0.87
VFC THI	V	159.20	153.00	138.40	122.70	103.00	87.30	67.54	52.10	30.20	14.86
	THD %	39.22	37.52	39.29	44.94	46.43	56.46	63.51	64.45	83.21	113.71
	CMV	92.50	97.00	95.70	95.00	88.00	94.50	99.00	90.00	93.50	117.00
	NPF%	14.67	9.33	10.47	6.33	11.00	5.33	10.33	9.67	3.67	29.33
OFV SVM	V	174.30	155.70	138.19	121.35	104.72	88.46	69.91	51.27	33.67	12.25
	THD %	27.31	28.86	30.42	35.26	38.55	45.81	54.68	61.26	66.23	69.48
	CMV	32.20	31.80	31.80	31.50	31.40	31.00	30.80	30.40	30.20	30.10
	NPF%	1.44	1.33	1.33	1.20	1.07	1.00	0.80	0.67	0.53	0.53
51 Vector SVM	V	175.10	156.12	138.98	122.20	105.43	89.11	71.02	51.95	34.38	12.86
	THD %	25.62	26.74	28.25	32.43	34.68	43.39	53.42	60.82	65.46	68.21
	CMV	0	0	0	0	0	0	0	0	0	0
	NPF%	1.44	1.33	1.20	1.13	1.07	1.00	0.80	0.67	0.53	0.53
31 Vector SVM	V	175.70	156.96	139.62	12.85	106.02	90.22	71.76	52.48	35.12	13.62
	THD %	24.86	26.02	27.45	31.05	33.18	42.54	52.75	60.14	64.83	67.48
	CMV	0	0	0	0	0	0	0	0	0	0
	NPF%	1.44	1.33	1.20	1.07	1.00	0.87	0.80	0.60	0.53	0.47
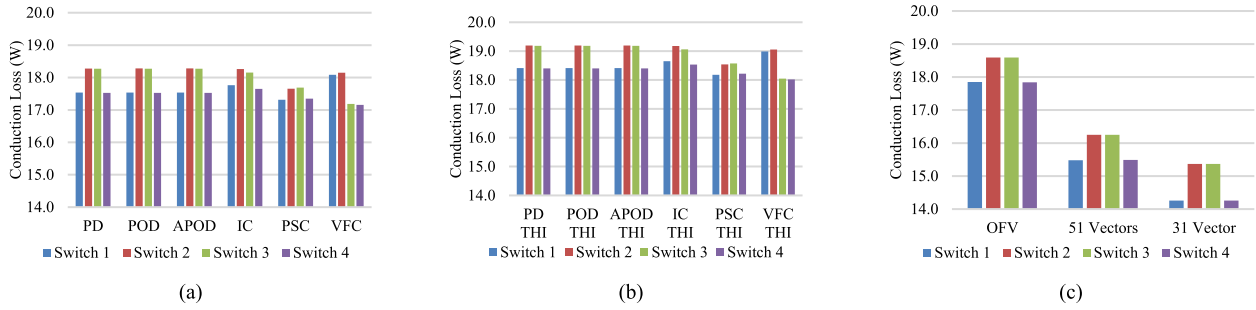
FIGURE 18. Conduction loss of Phase A for (a) Normal MC PWM techniques (b) MC THI PWM Techniques, (c) SVM techniques.
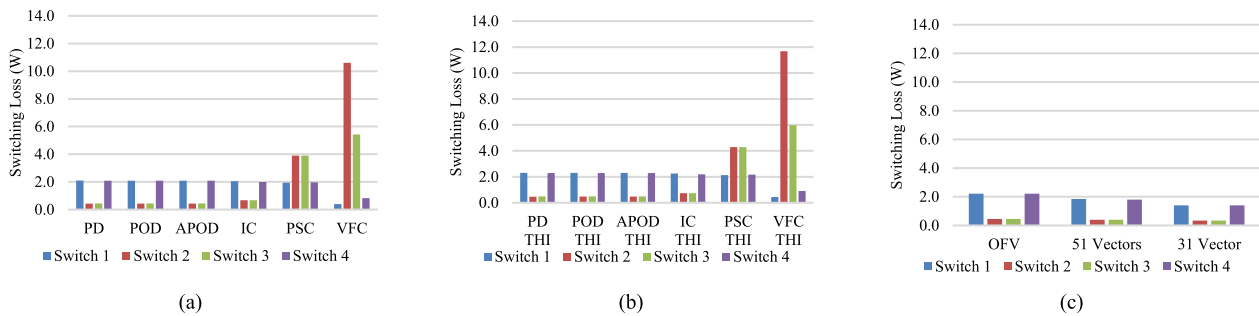

FIGURE 19. Switching loss of Phase A for (a) Normal MC PWM techniques (b) MC THI PWM techniques, (c) SVM techniques.
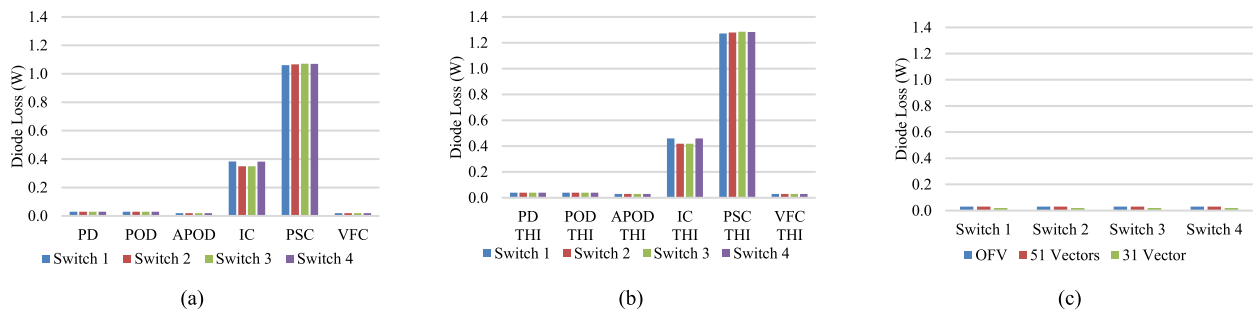

FIGURE 20. Diode loss of phase A for (a) Normal MC PWM techniques (b) MC THI PWM techniques, (c) SVM techniques.
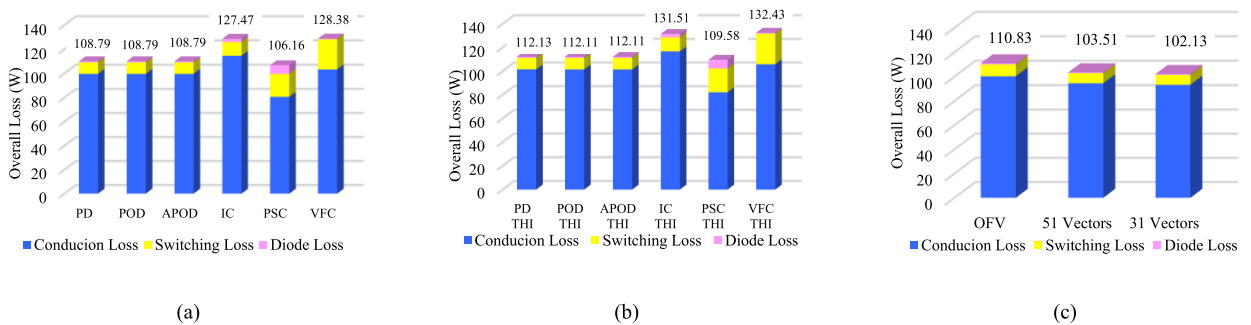

FIGURE 21. Average overall loss of Phase A for (a) Normal MC PWM techniques (b) MC THI PWM techniques, (c) SVM techniques.

indices are listed in Table 7. The NPF% is measured for different PWM techniques across dc-link capacitors. From the table it is noted that the IC PWM technique has least fluctuation in capacitor voltages while the VFC PWM technique has highest fluctuation among the discussed PWM. The NPF for all PWM technique is in acceptance range. The CMV for various PWM
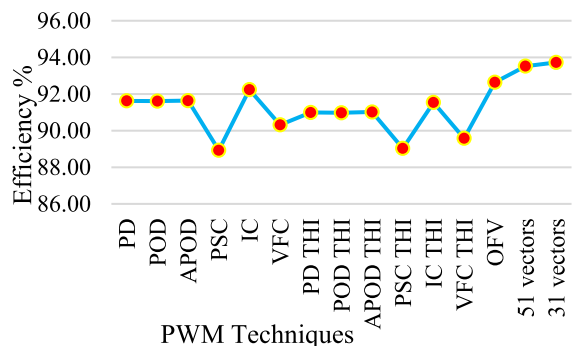
FIGURE 22. Efficiency of NPC MLI for different PWM techniques.

Techniques are also listed and it is found that CMV is less for POD and APOD techniques while it is high in IC PWM technique.

The results from the table shows that PD and VFC PWM techniques provide better THD performance, while NPF is high. The NPF is less in PSC PWM techniques when compared to other MC PWM techniques while the CMV is less in POD and APOD PWM techniques. The MCPWM fails to satisfy all the aspects as it can able to provide better results in one or two output parameters only. This can be overcome by applying SVM techniques to the inverter where all output parameters are improved. The results of SVM techniques are better when compared to MC PWM techniques, also the CMV is eliminated in both 51 vectors and 31 vectors SVM. However, the voltage ripple and THD is less in 31 vector SVM.

The losses of power switching devices are obtained through PLECS software. The conduction loss of each switch in phase A is shown in Fig. 18, while the switching loss across four switches is shown in Fig.19 with their diode loss in Fig. 20. The average overall loss for switches in phase A is shown in Fig. 21. The losses in other phases will be identical to the losses obtained in phase A. Thus, phase A is represented in the following figures. It can be noticed that the conduction loss is high in middle switches (S_2 and S_3) as it is conducted for a longer period of time than S_1 and S_4. In VFC PWM, the conduction loss is high in S_1 and S_2 as the frequency is less in top carrier while the conduction loss is less in S_3 and S_4 as shown in Fig. 18 (a).

The conduction loss and switching loss is slightly higher when THI is done and it is noticed in Fig. 18 and Fig. 19.
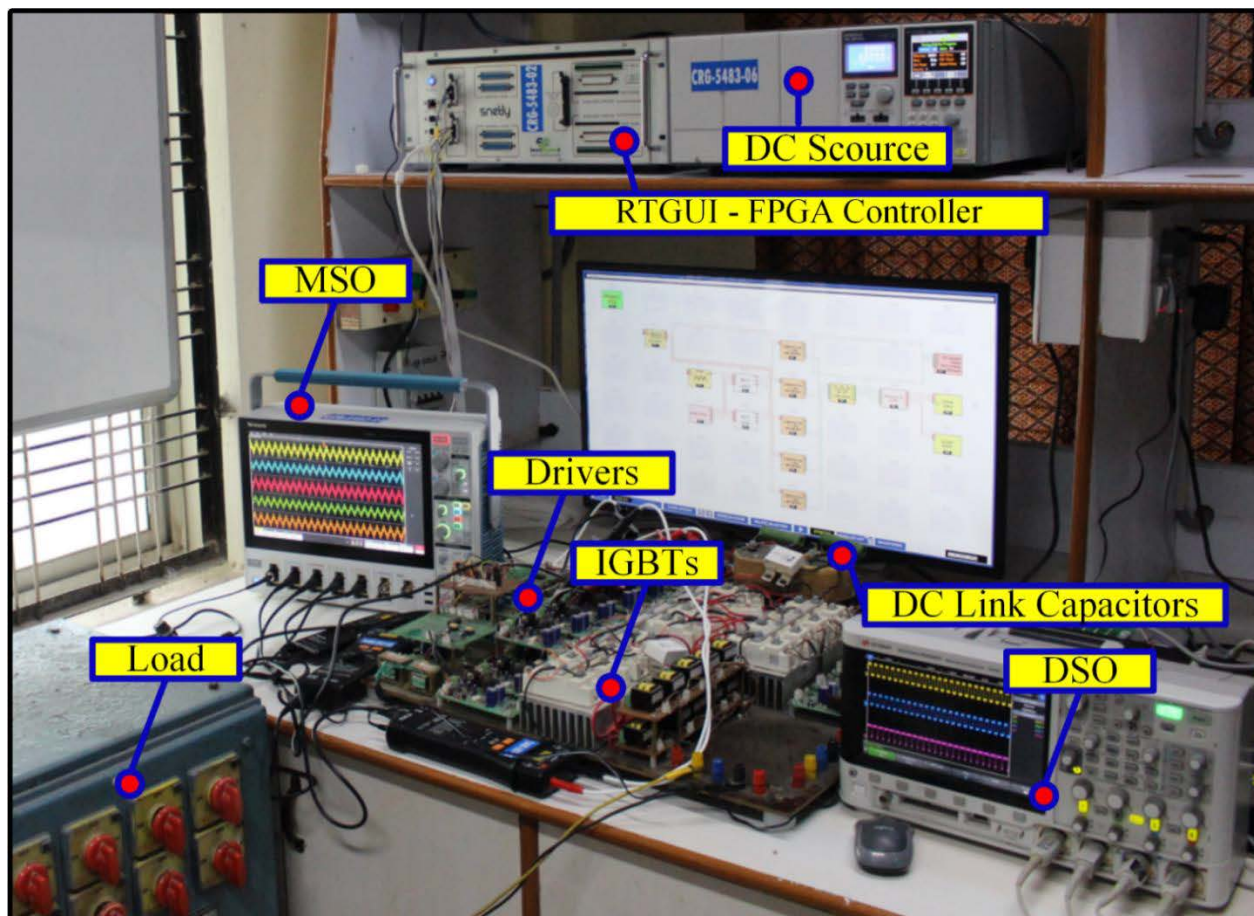

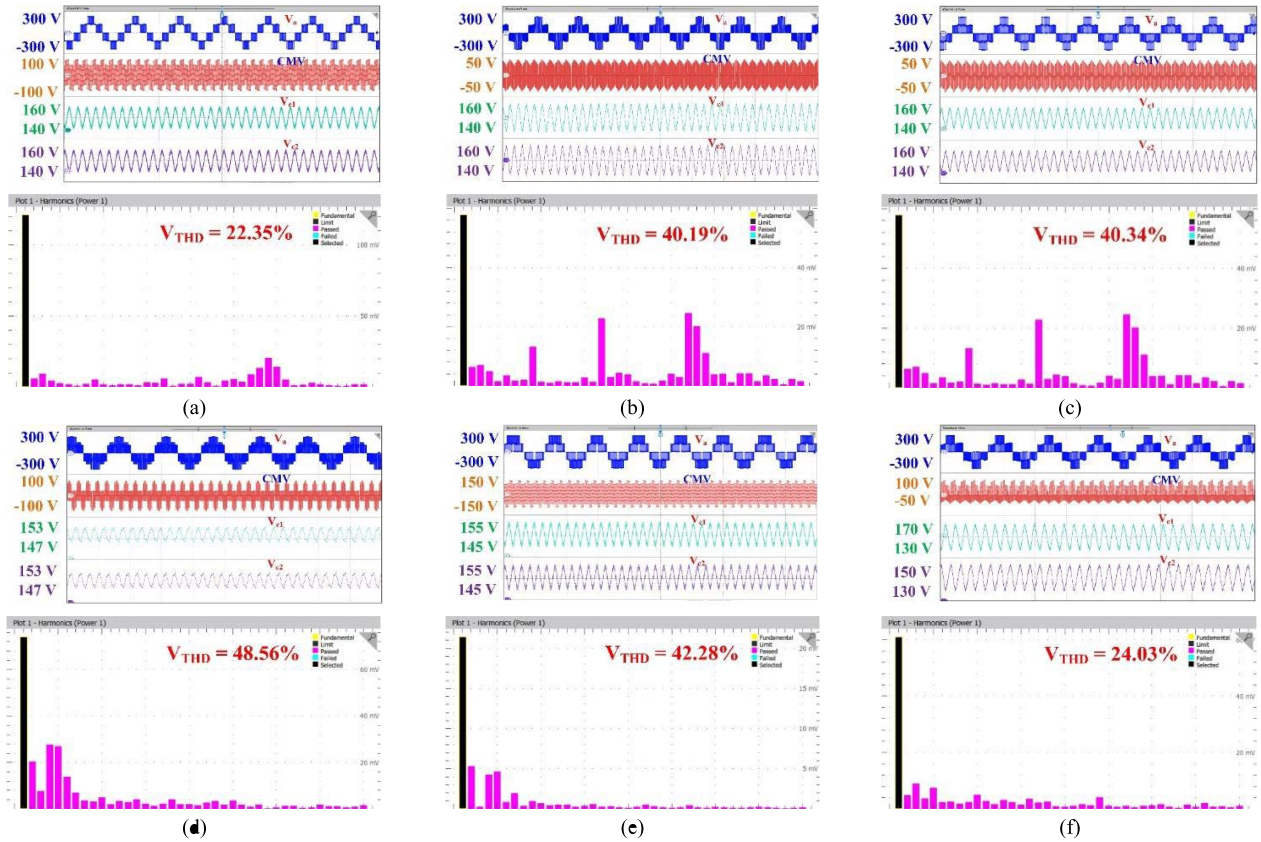**FIGURE 23.** Experimental Setup of 5-phase NPC MLI.

FIGURE 24. Experimentation results - Line voltage, CMV, DC link voltages and THD for (a) PD, (b) POD, (c) APOD, (d) PSC, (e) IC, (f) VFC.

TABLE 8. Experimental results of line voltage and THD for various PWM techniques.

PWM	Output	M_i = 1	0.6	0.3	PWM	M_i = 1	0.6	0.3	PWM	M_i = 1	0.6	0.3
PD	V	167.43	99.88	46.19	POD	167.15	99.53	46.71	APOD	167.43	99.62	46.83
	THD %	22.35	35.86	63.22		40.19	73.25	102.33		40.34	72.49	101.82
	CMV	97.00	95.00	93.50		40.00	35.00	32.00		40.00	35.00	32.00
	NPF%	8.67	4.33	2.67		6.67	3.50	1.33		6.67	3.33	1.00
PSC	V	141.45	60.75	8.63	IC	173.21	138.26	72.64	VFC	172.05	96.85	48.22
	THD %	48.56	145.24	508.31		42.28	38.47	27.35		24.03	37.35	77.62
	CMV	90.00	92.00	92.00		125.00	140.00	155.00		92.00	93.00	125.00
	NPF%	2.00	0.67	0.33		3.33	13.67	4.27		16.67	28.33	62.00
PD THI	V	159.93	101.68	50.16	POD THI	158.78	98.62	46.41	APOD THI	158.78	98.75	46.68
	THD %	41.74	49.05	72.27		46.81	71.28	101.31		46.67	70.98	101.24
	CMV	98.00	94.00	92.00		48.00	37.00	33.00		39.00	35.00	34.00
	NPF%	14.00	5.33	2.67		13.33	4.28	1.67		13.33	2.53	1.87
PSC THI	V	146.07	56.28	7.96	IC THI	166.28	126.37	69.48	VFC THI	158.75	101.35	49.18
	THD %	46.39	110.34	486.24		59.25	53.18	46.42		40.93	47.24	67.82
	CMV	152.00	150.00	140.00		125.00	156.00	158.00		95.00	93.00	90.00
	NPF%	4.33	2.17	0.97		9.33	6.33	5.67		13.33	11.67	10.00
OFV SVM	V	173.21	102.18	50.43	51 Vector SVM	173.78	104.29	53.46	31 Vector SVM	173.78	105.72	54.38
	THD %	29.45	40.57	63.81		26.75	38.43	62.18		25.15	38.69	61.57
	CMV	35.00	33.00	31.00		0	0	0		0	0	0
	NPF%	1.33	1.27	0.80		1.33	1.00	0.67		1.33	0.87	0.53

This is due to the variation in pulses as third harmonic content is included with normal reference signals. The diode loss is very low in all PWM techniques except PSC PWM as shown in Fig.20, the increase in diode loss is due to continuous conduction in all switches. The average total loss is high in IC, VFC, IC THI and VFC THI PWM techniques.
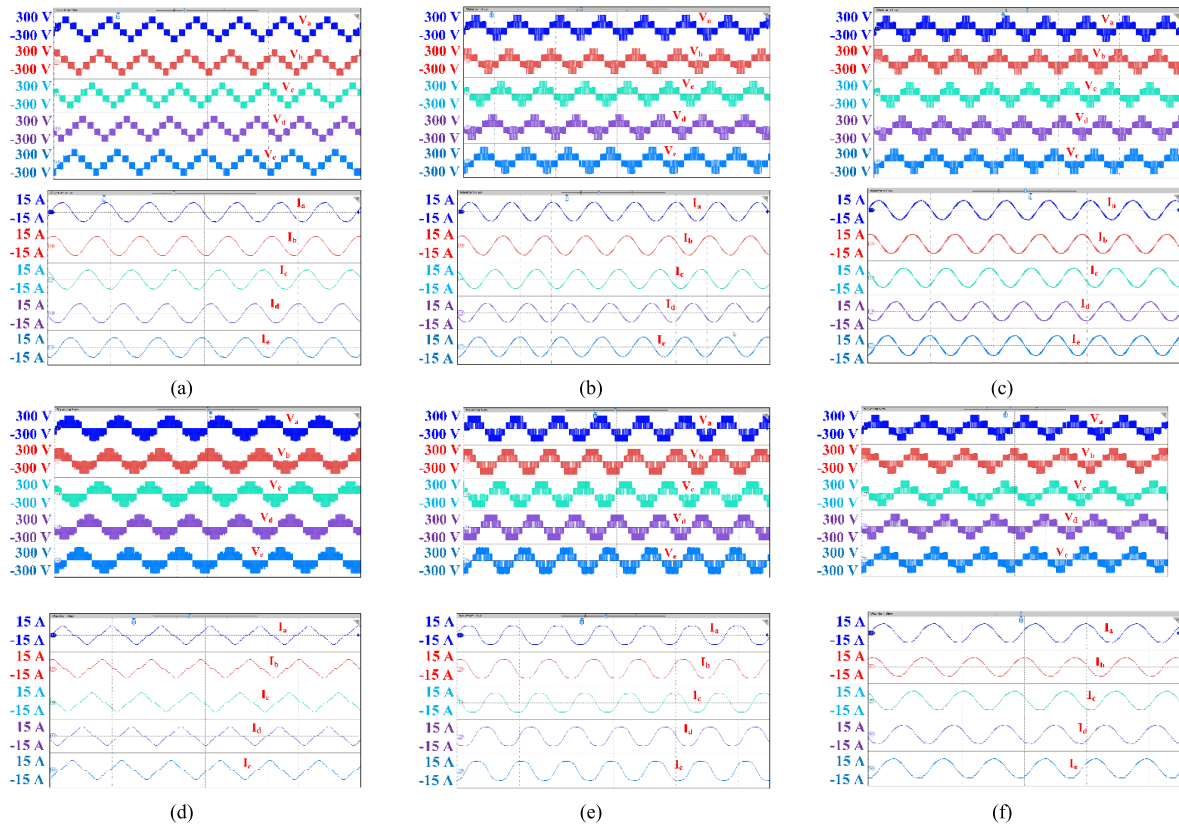
FIGURE 25. Experimentation results – Line voltages and Line currents of 5-phase for (a) PD, (b) POD, (c) APOD, (d) PSC, (e) IC, (f) VFC.
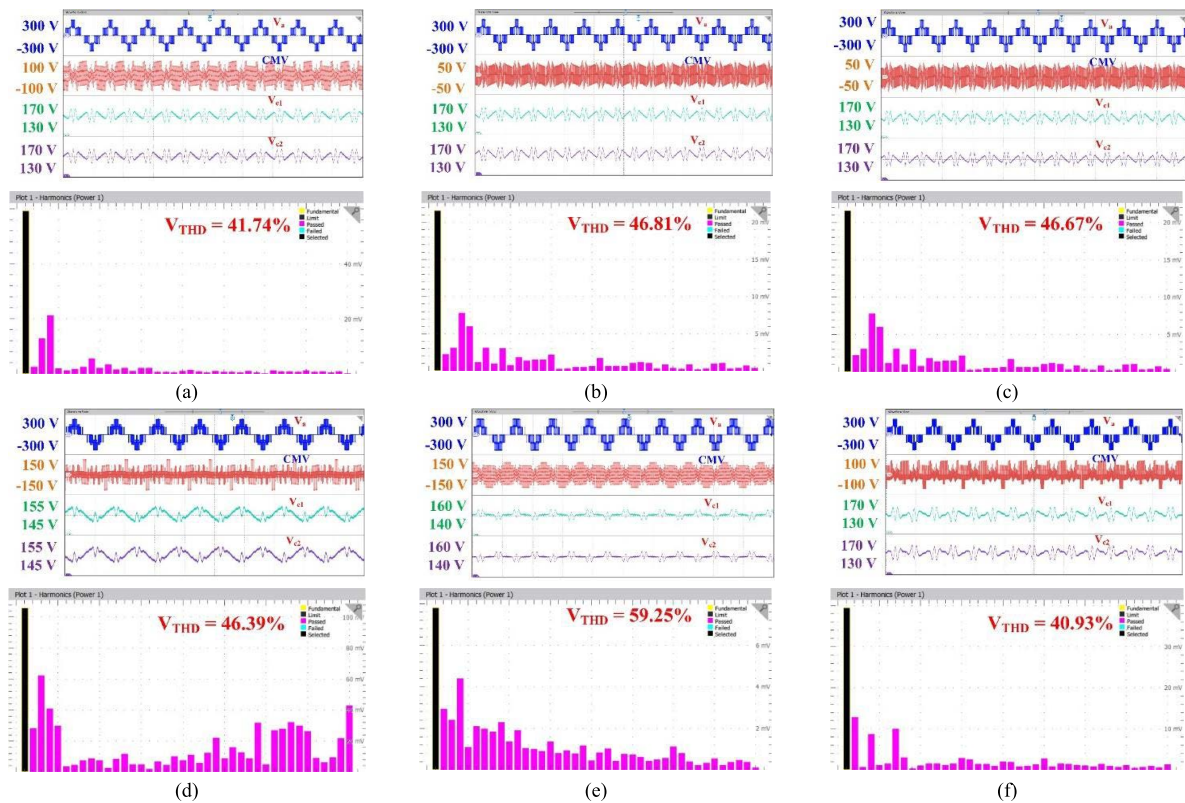

FIGURE 26. Experimentation results - Line voltage, CMV, DC link voltages and THD for (a) PD THI, (b) POD THI, (c) APOD THI, (d) PSC THI, (e) IC THI, (f) VFC THI.
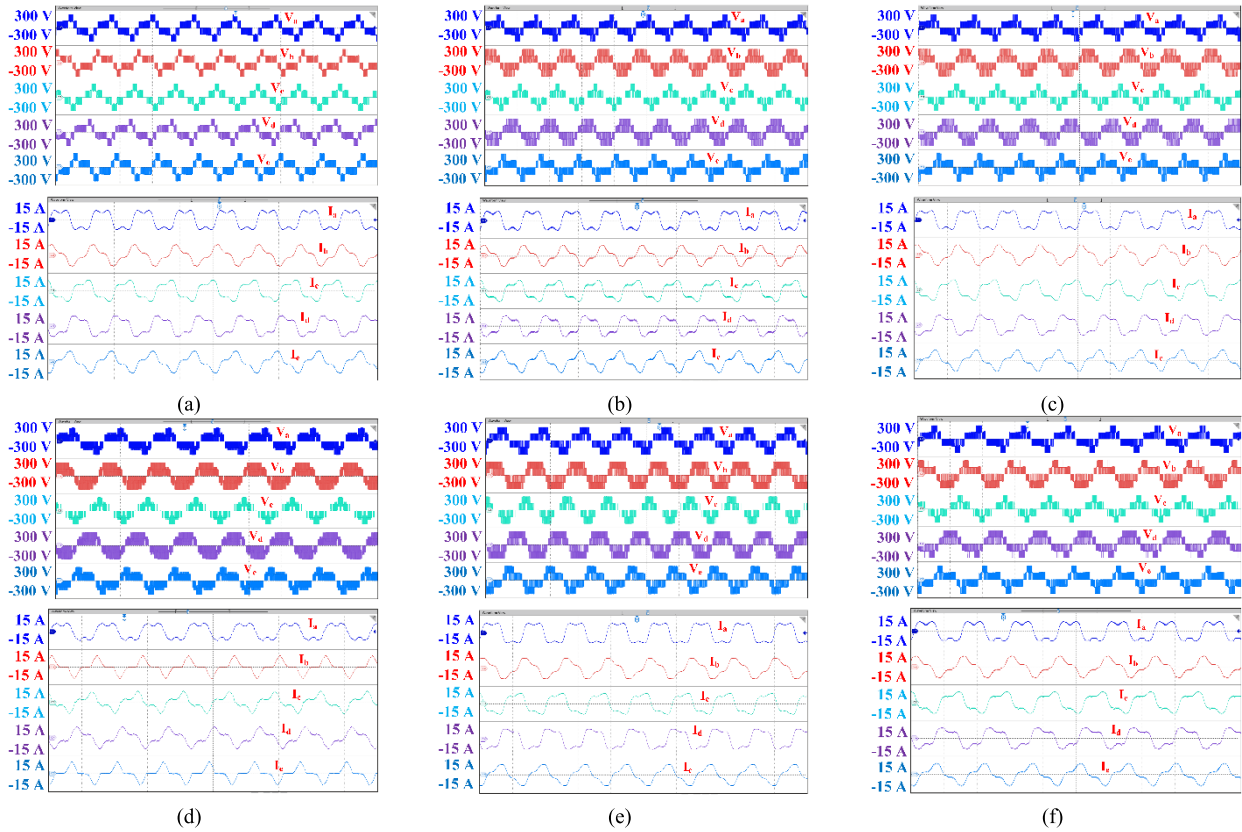
FIGURE 27. Experimentation results - Line voltages and Line currents of 5-phase for (a) PD THI, (b) POD THI, (c) APOD THI, (d) PSC THI, (e) IC THI, (f) VFC THI.

The overall loss is less in other techniques, whereas the loss is even reduced in OFV SVM techniques as it given digital pulse to the switches. The losses are even further reduced in 51 vector and 31 vector type of SVM. This reduction is due to the usage of less number of switching states.

The efficiency of the inverter is calculated as

$$\text{Efficiency,} \quad \eta = \frac{P_{out}}{P_{out} + P_{loss}} * 100\% \qquad (34)$$

where $P_{loss} = P_{con} + P_{sw}$, P_{con} is the conduction loss of semiconductor switches and diodes, while P_{sw} is switching loss of semiconductor switches and diodes in the inverter. The efficiency of inverter is calculated for different PWM techniques for the modulation index is 1 and shown in Fig.22.

From the results, it is observed that the performances of NPC inverter is better when applying SVM techniques. The efficiency is noted high with the proposed 31 vectors SVM among other PWM techniques. Thus the proposed SVM technique can be implemented to the inverter drives where the efficiency is improved.

V. EXPERIMENTAL RESULTS

The experimentation for 5-phase NPC MLI is done by using RL load with R = 10Ω and L = 2mH. IGBT - SKM100GM12T4 switches are used to develop the 5-phase NPC MLI. The pulse for inverter is generated by RTGUI - FPGA controller. The DC link voltage is considered 300V with the capacitor rated as 100μF. The experimental setup for 5-phase 3L NPC inverter is developed as shown in Fig. 23. The THD analysis of the experimentation is done by TEKTRONIX MSO 046. The 5-phase NPC MLI is applied with PD, POD, APOD, IC, PSC, VFC, PD THI, POD THI, APOD THI, IC THI, PSC THI, VFC THI, OFV SVM, 51 vector SVM, and proposed 31 vector SVM techniques and the corresponding line voltage, line current, CMV, dc-link voltage and THD results are obtained.

The experiment is carried out by providing PD PWM techniques and the output voltage, CMV, dc-link voltage and THD is obtained as shown in Fig. 24 (a). The NPF is read as 6.67% and voltage THD is 22.35%. In POD PWM technique, CMV is reduced to 50V with NPF is same as previous condition while voltage THD is higher (40.19%) as shown in Fig. 24 (b). The results of APOD technique is similar to POD technique in 3L inverter as shown in Fig. 24 (c). The NPF is read as 2% in PSC PWM technique, while THD is 48.56% as shown in Fig. 24 (d). In IC PWM, NPF is read as 3.33% while, CMV and voltage THD is high as 150V and 42.28% which is displayed in Fig. 24 (e). In VFC PWM technique, though voltage THD is less, CMV and NPF is high as shown in Fig. 24 (f).
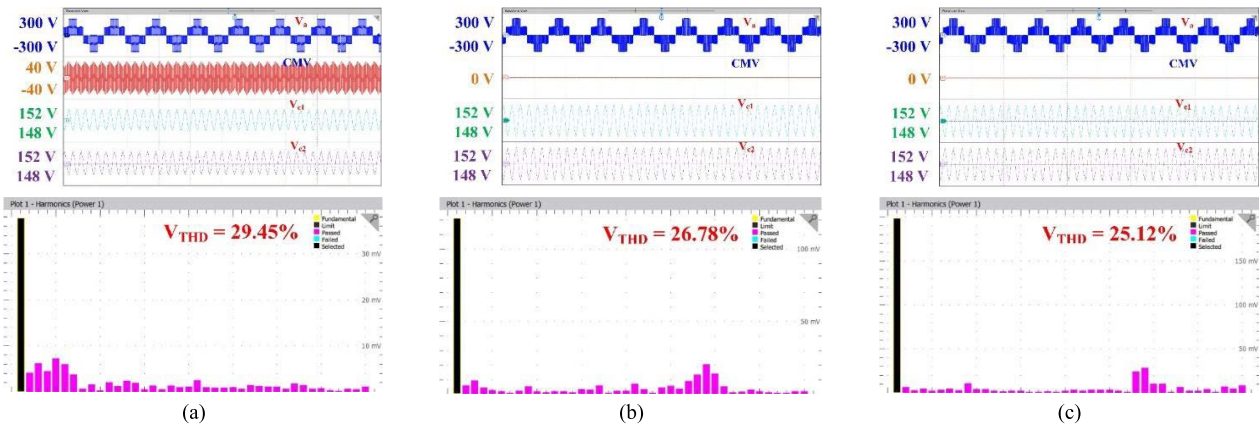
FIGURE 28. Experimentation results - Line voltage, CMV, DC link voltages and THD for (a) OFV SVM, (b) 51 vector SVM, (c) 31 vector SVM.
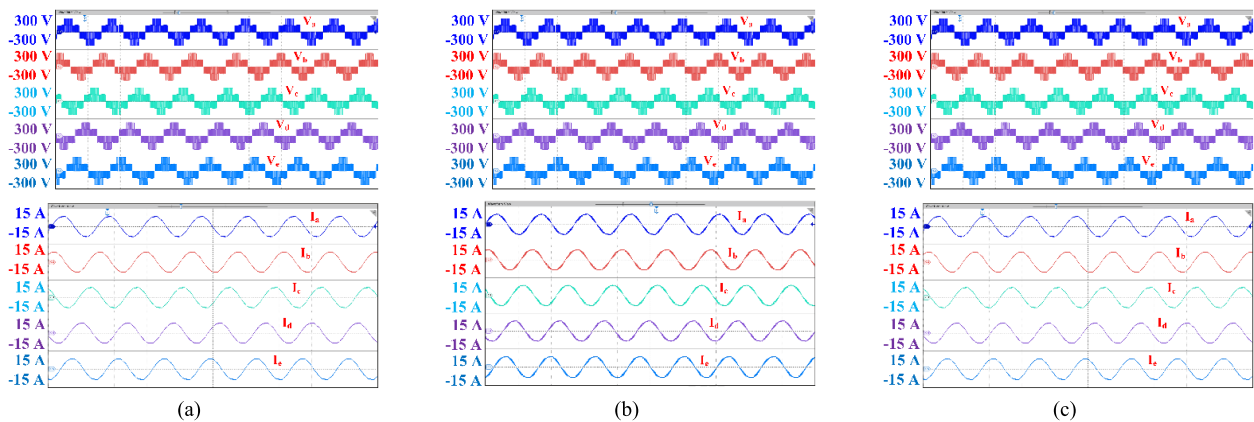

FIGURE 29. Experimentation results - Line voltages and Line currents of 5-phase for (a) OFV SVM, (b) 51 vector SVM, (c) 31 vector SVM.

The line voltage and line current of all phases with normal MCPWM techniques are shown in Fig. 25. The voltage and current waveform shows that each phase is shifted by 72° to each other. The line voltage across each phase is read as 300V while the current obtained is about 15A. As the reference signal is sinusoidal the output voltages and currents in all 5-phases are symmetrical to each other. The output current in PSC PWM is slightly deviated from pure sinusoidal as all the carrier signals reaches zero at the same time.

The third harmonic signal is injected to the sinusoidal reference signal and the experiment is conducted for 5-phase 3L NPC inverter. The output voltage, CMV, dc-link voltage and voltage THD for PD THI PWM technique is shown in Fig. 26 (a). The NPF and voltage THD is high when THI is done on comparing with sinusoidal PWM. The results of POD THI and APOD THI are similar to each other, CMV and the NPF in these techniques are obtained as 50V and 13.33% respectively which is shown in Fig. 26 (b) and Fig. 26 (c). Though CMV less in this type, the NPF and voltage THD remain high. The PSC THI technique reads CMV as 150V, NPF is 3.33% and voltage THD is 46.39% as shown in

Fig. 26 (d). The CMV for IC THI is obtained also high as 150V with NPF as 6.67% and voltage THD as 59.25% as displayed in Fig. 26 (e). The CMV of VFC THI technique is obtained as 100V with NPF is read as 13.33% and the voltage THD in this technique is 40.93% which is lower among THI PWM types as shown in Fig. 26 (f).

The line voltage and line current for all 5-phase has been measured by injecting the third harmonic content to the reference signal and it is shown in Fig. 27. The results shows that the waveforms are not uniform in all phases, as it varies due to the presence of third harmonic content. Thus the line currents in all phases does not follow sinusoidal path instead it gives distorted waveform. Due to this unsymmetrical output, the PWM technique with THI is not preferred for driving the motors as the performance and efficiency is reduced in this techniques.

The SVM is preferred in many places as it overcomes the issues faced in MCPWM techniques. The SVM in 5-phase 3L NPC inverter consists of 243 vectors. To avoid the inequality relationship among 5-phase OFV is preferred. The vectors are further reduced to 51-vectors and 31-vectors to eliminate the CMV and the simulation is carried out for these SVM

types. The output voltage, CMV, DC link voltage and THD of OFV are shown in Fig. 28 (a). The CMV is obtained around 40V while the voltage THD is measured as 29.45%. The result of NPC MLI when 51 vectors are applied where the CMV is eliminated as shown in Fig. 28 (b) while the performance of NPC MLI for proposed 31 vectors is shown in Fig. 28 (c). The voltage THD of 51 vectors and 31 vectors are obtained as 26.78% and 25.12% respectively. The results of SVM indicate that its performance is better than MCPWM techniques. The CMV is also eliminated in 51 vectors and 31 vectors SVM while THD is lower in later technique. The DC-link capacitor voltage is very close to balancing voltage, which means NPF is very low in SVM techniques. This shows that the SVM techniques with reduced switching states provide better results such as zero CMV, reduced NPF and lower voltage THD.

The experimentation results of all 5-phases for OFV, 51-vector SVM and 31-vector SVM techniques are shown in Fig. 29. The line voltage and line current of one phase are symmetrical to other phases with the delay of 72° to each other. The output current follows the sinusoidal path as RL load is applied to the inverter. The performance of the inverter is increased when SVM with reduced switching states are applied.

The experimentation is done by applying different modulation indices (M_i = 1, 0.6 and 0.3) and corresponding results are listed in Table. 8. The results obtained show that the SVM technique gives better performances in all parameters as obtained in simulation. The PWM techniques for the 5-phase NPC inverter discussed in this paper can be applied in motor driving applications in the industries. The SVM with a reduced number of switching states provides better performance with zero CMV to the inverter. The leakage current is reduced by eliminating the CMV from the inverter.

The results of different PWM and SVM technique are compared by plotting the graph in Fig. 30 and Fig. 31. The results of NPC inverter when modulation index is considered as 1 for the above graph which shows that the output voltage is high in the proposed SVM with 31 vector and the CMV is eliminated
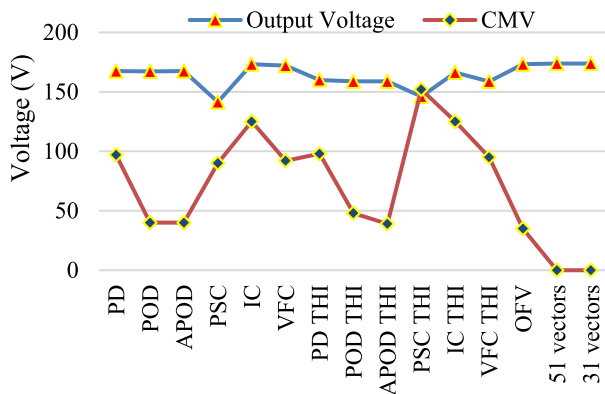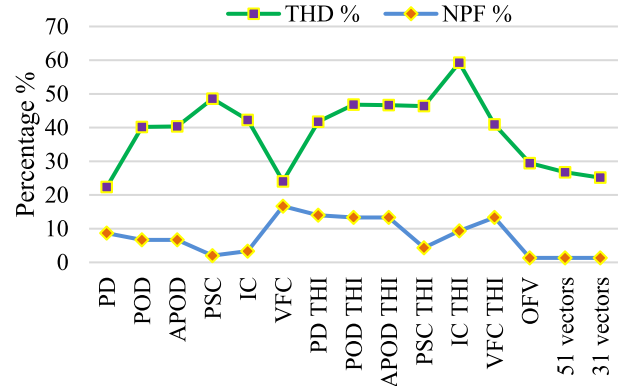

FIGURE 31. THD % and NPF % of all PWM techniques.

and read as 0V. Furthermore, the THD % and NPF % is less in this type compared to the other PWM techniques. Thus, the proposed SVM with 31 vectors offers better results which can be applicable for the motor applications in the industries as well as in Electric Vehicles.

VI. CONCLUSION

The output performances of 5-phase NPC inverter is analyzed with various PWM and SVM techniques. The MCPWM techniques like PD, POD, APOD, PSC, IC and VFC along with its THI types are implemented for 5-phase 3L NPC inverter. The harmonic content and NPF is better in PD technique, however the CMV is high, while in POD technique CMV and NPF is reduced nevertheless the THD is increased. Similar results are obtained for APOD technique as it is equivalent to POD technique in case of 3L inverter. Though NPF is very less in PSC, it fails in other aspects. In IC PWM technique, the output voltage is higher than any other technique besides reduction in NPF, however THD and CMV is at their peak. The VFC PWM technique provides better output voltage and THD performance, nevertheless the CMV and NPF is high in this condition. The THI PWM techniques has the same advantages as their normal PWM techniques however, the presence of third harmonic content in reference signal results in deviation of phase angle across each phase output. Thus the performance of the inverter is reduced in THI techniques. Based on the analysis of various MCPWM techniques, it is noted that each techniques gives better result in any one or two parameter; however it fails in remaining parameters. This concern is resolved when the SVM is implemented for NPC inverter. The OFV with 113 vector is executed to avoid inequality relationship. Though OFV type of SVM delivers good performance in all aspects like increased output voltage, lower THD and NPF, the CMV is still present in the inverter. To eliminate the CMV, 51 vectors that produce zero CMV is selected and implemented to 5-phase inverter. This eliminates the CMV furthermore improving the THD performance. However, due to the presence of x-y component the ripples are created in the output. To reduce the ripples, SVM with 31 vectors is proposed in this paper which gives

FIGURE 30. Output voltage and CMV of all PWM techniques.

lower NPF and better THD % along with high output voltage. Thus the proposed SVM with 31 vectors provides better efficiency when compared to other PWM techniques and also the computational complexity is less as the number of switching state is less.

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