IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received February 23, 2022, accepted March 20, 2022, date of publication March 23, 2022, date of current version March 31, 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3161658

Design and Experimentation of a Single-Phase PLL With Novel OSG Method

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This work was supported in part by ENEA Agenzia nazionale per le nuove tecnologie, l'energia e lo sviluppo economico sostenibile under Project RdS/PTR2020/055.

ABSTRACT Different phase-locked loop algorithms applied to three-phase grid voltages implement a closed control loop based on the Park transform to obtain the grid voltage instantaneous phase and frequency. When a single-phase grid voltage must be processed, one of the inputs of the Park transform is generated by a block that, starting from the available voltage, computes an additional signal with the same frequency of the grid voltage and ideally orthogonal to it. This paper introduces a novel method for the orthogonal signal generation and gives a detailed analysis of its functioning. Then, after sizing the control loop of the phase-locked loop, the paper considers different aspects relevant to implementation of the presented orthogonal signal generation and of the phase-locked loop on a digital signal controller, such as the finite numerical resolution, the memory usage and the computation time. Finally, the paper checks the comprehensive performance of the orthogonal signal generation and phase-locked loop pair by experimental tests and compares the obtained results with those available in the literature.

INDEX TERMS Orthogonal signal generation, phase-locked-loop, phase and frequency estimation.

I. INTRODUCTION

The phase-locked loop (PLL) algorithms are used in several applications where the instantaneous phase and /or frequency of a given signal must be estimated in real-time, with short delay with respect to their variations and with good resilience against noise or harmonics superimposed to the processed signal.

Regardless of their different structures and properties, all the PLLs have three elemental stages [1]. The first one is the phase detector (PD), in charge of generating the error signal between the real and the estimated phase. It is followed by the loop filter (LF), which is often a proportional-integral controller aimed to reduce the phase error to zero. The last stage is a voltage-controlled oscillator (VCO), which generates at its output an alternate signal that is synchronized to the signal applied at the PLL input.

A typical application of the PLL is the interfacing of a front-end inverter with a three-phase grid. In this case, the instantaneous phase of the grid voltages must be known to properly manage the active and reactive power exchange between the grid and the inverter. Power control is often based on the instantaneous power theory [2] that expresses the grid voltages by means of space vectors in the α, β or in the d,q reference frames, the first one obtained by applying the Clarke transform to the grid voltages and the second one worked out by a subsequent Park transform. In this context, a common solution is to base the PD on the Park transform, exploiting the property by which if the phase angle used for the transform is equal to the instantaneous phase of the α, β grid voltage space vector, the q component of the d,q grid voltage space vector is equal to zero. These PLLs are denoted as synchronous reference frame-PLL (SRF-PLL) [3].

The same approach cannot be adopted straightforwardly when interfacing with a single-phase grid because the Clarke transform, which supplies the two orthogonal signals v_α and v_β to the Park transform, can be applied only to three-phase systems. To face this limitation, two main classes of PD have been developed [4].

The power-based PLLs have a product-type PD, which introduces a second harmonic component in the phase error. To mitigate this disturbance several advanced power-based PLLs have been designed. The PLL based on a low pass filter (LPF) [5] requires an LPF with a low cutoff frequency to remove the second-order harmonic, thus slowing their transient response. In [6] a notch filter replaces the LPF;

The associate editor coordinating the review of this manuscript and approving it for publication was Poki Chen.

in this case the notch bandwidth strongly affects the PLL behavior: a narrow bandwidth gives fast responses but is weak against grid frequency variations, on the other hand, a large bandwidth is more robust but slows down the transient response. In [7] the second harmonic is removed by a compensation algorithm that uses both the estimated phase and the generated d,q components of the grid voltage space vector. An alternative approach makes use of an in-loop moving average filter [8]. This last solution is used also in the orthogonal signal generation (OSG) based PLLs [9].

The OSG-PLLs operate as the SRF-PLLs but are endowed with an additional stage uphill the PD that performs the OSG to obtain from the single-phase grid voltage a fictitious orthogonal signal to be used as the second member of the v_α, v_β pair processed by the Park transform [10], [11]. The simplest OSG method consists of delaying of one quarter of the period the signal obtained transducing the grid voltage, other approaches relies on the use of the inverse-Park transform [11], of the Hilbert transform [12], or of discrete-time filters with complex coefficients [13]. The OSG based on the second-order generalized integrator (SOGI) PLL [14], [15], in addition, providing a filtered orthogonal signal for the β-axis, contributes to reducing the harmonic content of the α-axis component. Several different solutions based on SOGI have been successively developed [16], [17]. In [18] an approach similar to that of the power-based PLL is used to perform the OSG. In this case, despite the use of a notch filter, the generated signals track accurately the grid voltage waveform.

A common feature of the OSG-PLLs is that the Park transform is applied to the pair of signals v_α, v_β, where v_α is ideally in phase with the grid voltage and v_β is orthogonal to it. This paper presents a different approach by which one of the outputs of the OSG leads the grid voltage of $\pi/4$ and the other lags it of the same phase. A similar proposal can be found in [19], but there, differently from the design procedure described in Section III, the sensitivity to the grid frequency variations of the filters that generate the v_α, v_β pair is not minimized; moreover, a more complex architecture is considered, with additional blocks inserted uphill and downhill the filters themselves.

The objectives of the paper can be summarized as:

- Presentation of a novel OSG method that reacts to the variation of the grid frequency in a way somehow complementary to that of the SOGI. (Section III).
- Design of the LF and the complete control loop of the PLL in the continuous-time domain and its subsequent discretization (Sections IV and V).
- Implementation of the OSG-PLL pair in the firmware of a digital signal controller (DSC) facing the issues arising from the finite resolution of the CPU, from the limited amount of available memory, and from the need of minimizing the computation time (Section VI).
- Experimentation of the PLL based on the presented OSG method in real operative conditions (Section VII) and discussion of its performance in comparison with those of other OSG-PLL pairs found in the literature (Section VIII).

Section II briefly reviews some of the existing OSG methods with particular attention to the SOGI to make an easier comparison with the proposed OSG method. Conclusions are reported in Section IX.

II. ORTHOGONAL SIGNAL GENERATION

The different digital OSG methods reviewed in the literature share the characteristic of generating the orthogonal signals v_α and v_β, with v_β lagging v_α, processing the signal v_g obtained by transduction and acquisition of the single-phase grid voltage. A second common feature of most of the OSG methods is that the signal v_α is, or should be, in phase with v_g so that the output of the PLL, which actually estimates the phase of v_α, ideally gives the phase of the grid voltage.

The simplest way to perform the OSG consists in setting $v_\alpha = v_g$ and in taking as samples of v_β the samples of v_g acquired one-quarter of the period before. This entails that operating at the nominal grid angular frequency $\omega_{g,N}$, the number of samples of v_g to be stored for the implementation of the OSG is given by (1).

$$N_{s,N} = \frac{\pi}{2}\frac{1}{\omega_{g,N}}\frac{1}{T_s}. \tag{1}$$

If the sampling period T_s is equal to 100μs [4], from (1) it derives that $N_{s,N} = 50$. If the grid angular frequency ω_g changes, N_s must be adjusted dynamically to maintain the required phase lag between v_α and v_β. Being that ω_g is not known, this adjustment is based on the estimate $\omega_{g,e}$ of ω_g, computed by the PLL itself. This method has the disadvantage that any variation occurring on v_g affects instantaneously the signal v_α but can be detected on v_β only after a quarter of the grid period, thus introducing an asymmetry on the signals processed by the PD and a delay in its response. Moreover, the grid frequency is inherently a continuous quantity whereas the delay between the signals v_α and v_β, being a multiple of T_s, takes only discrete values, hence the orthogonality between v_α and v_β is not assured unless both N_s and T_s are adjusted according to $\omega_{g,e}$.

In the derivative OSG method, v_g corresponds to v_β and the latter one is derived to work out v_α. Consequently, the phase estimated by the PLL is $\pi/2$ ahead with respect to that of v_g. Even if this offset can be easily compensated, the drawback of this method is that the derivation amplifies the harmonics of v_g thus affecting the accuracy of the estimate. The insertion of an LPF in series to the derivative block would attenuate the effects of the harmonics but will also reduce the phase lead of v_α with respect to v_β of an amount that varies with the actual grid frequency. An alternative solution consists in considering v_α equal to v_g and in obtaining v_β from it by integration. This approach solves the problem related to the harmonics of v_g, but is sensitive to its offset, if any. Insertion of a high pass filter would nullify the problem of the offset but at the expense of the accuracy of the orthogonality between v_α and v_β.

Another OSG method uses a block that implements the inverse-Park transform to work out v_β processing the grid phase estimate $\theta_{g,e}$ and the d,q component of v_g. Being the latter ones not available, their estimated values obtained by the direct Park transform that constitutes the PD of the PLL are used. In order to avoid algebraic loops in the OSG-PLL pair, the v_d and v_q signals generated by the PD are processed by two LPFs before entering the inverse-Park transform [10]. The LPFs introduce a delay in the system response. Moreover, like in the case of the delay-based OSG method, any sudden variation of v_g, and hence of v_α, is not immediately reported in v_β causing a dissymmetry in the processing of the v_α, v_β pair.

A different approach to OSG exploits the property by which the Hilbert transform of a sinusoidal signal is equal to the signal itself delayed of $\pi/2$ [9], [17]–[20]. The Hilbert transform is non-causal, but it can be approximated by a finite impulse response filter applied to the samples of v_g. This filter offers inherently a band-pass behavior that helps in reducing the effects of offset and distortion of v_g. Unfortunately, it is difficult to design a stable filter [4] and, as can be seen in [10], it has a satisfactory low-frequency gain only if its order is rather high so that at least 100 samples of v_g should be processed at every sampling time.

The SOGI method operates by means of two filters S_α and S_β that process v_g to generate v_α and v_β, respectively [11]. The continuous-time transfer function (TF) of the two filters are

$$S_\alpha(s) \triangleq \frac{V_\alpha(s)}{V_g(s)} = \frac{K_e\omega_{g,N}s}{s^2 + K_e\omega_{g,N}s + \omega_{g,N}^2}$$
$$S_\beta(s) \triangleq \frac{V_\beta(s)}{V_g(s)} = \frac{K_e\omega_{g,N}^2}{s^2 + K_e\omega_{g,N}s + \omega_{g,N}^2}, \quad (2)$$

where K_e is the filter gain. The Bode diagrams of $S_\alpha(j\omega_g)$ and $S_\beta(j\omega_g)$, obtained with $K_e = \sqrt{2}$, are reported in Fig. 1, using the red solid line and the blue dashed line, respectively.

The magnitude diagrams show that both the TFs attenuate the high-frequency components of v_g, and that $S_\alpha(s)$ is effective also in reducing its offset. The gains of the two TFs are equal to 1 at $\omega_g = \omega_{g,N}$, but if $\omega_g > \omega_{g,N}$ it results $|S_\beta(j\omega_g)| < |S_\alpha(j\omega_g)| < 1$ and if $\omega_g < \omega_{g,N}$ it is $|S_\alpha(j\omega_g)| < 1 < |S_\beta(j\omega_g)|$. The two signals v_α and v_β are always mutually orthogonal, but v_α leads or lags v_g when $\omega_g < \omega_{g,N}$ or $\omega_g > \omega_{g,N}$, respectively. Given that the PLL actually estimates the phase of v_α and not that of v_g, these non-idealities introduce oscillations and inaccuracy in the PLL output whenever $\omega_g \neq \omega_{g,N}$. This problem is usually solved by adjusting in real-time the coefficients of the filters in order to define (2) in terms of $\omega_{g,e}$ instead of $\omega_{g,N}$ [21]. In some papers the filter gain K_e is adjusted as well [22], in others, the authors propose to adjust the filters coefficients using an estimate of ω_g obtained by proper algorithms that operate independently from the PLL, such as in [23], where delayed samples of v_g are processed to work out ω_g, or in [24] and [25] that exploit the Teager energy operator to obtain ω_g.

These considerations highlight that even if usually the PLL is designed to compute $\theta_{g,e}$, nevertheless the use of an SRF-PLL requires to generate also $\omega_{g,e}$ to adjust the parameters of the OSG. This characteristic does not entail the implementation of a more complex PLL scheme because, as it will be shown in Section IV, the PLL inherently generates $\omega_{g,e}$ to obtain $\theta_{g,e}$.

Despite the adjustment of the coefficients, the behavior of $S_\alpha(s)$ and $S_\beta(s)$ is different at angular frequencies higher or lower than ω_g. In the first case, the harmonics of v_g are subjected to different attenuation and this difference becomes larger and larger as the frequency of the harmonics increase; in the second case, $S_\alpha(s)$ effectively attenuate any sub-harmonic and offset added to v_g whereas $S_\beta(s)$ leaves them nearly unchanged. This asymmetry in the OSG affects negatively the performance of the PLL. Reference [26] reports a proposal to get rid of this asymmetry by further processing of v_β aimed to obtain a signal in phase to v_g and with lower harmonic content. In [27] a higher-order SOGI is presented that both enforces the symmetry of the OSG and enhances its high- and low-frequency rejection capability. Higher-order SOGI is taken as reference in [27], working out the coefficients of a simpler, lower-order TF that approximates closely its transient response.

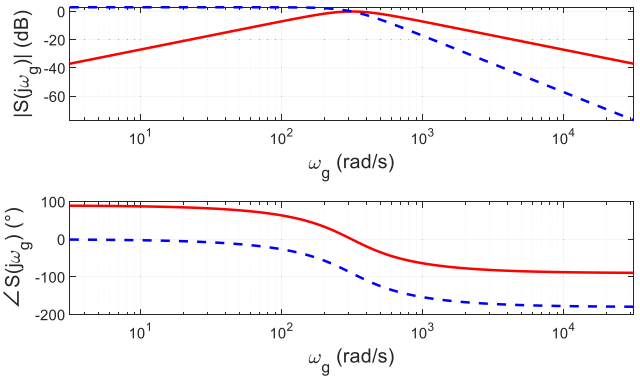

FIGURE 1. Bode diagrams of $S_\alpha(j\omega_g)$ (red solid line) and of $S_\beta(j\omega_g)$ (blue dashed line).

III. TWO ORTHOGONAL SIGNALs GENERATION

The OSG method proposed in this paper is denoted as "two orthogonal signals generation" (TOSsG) because two signals are actually generated using the two on-purpose designed filters F_{ld} and F_{lg}. The first one generates the signal v_{ld} that leads v_g by $\pi/4$ and the second generates v_{lg}, which lags v_g by the same phase angle. The two signals are mutually orthogonal and are used as input for the PD of the PLL.

The first requirement for F_{ld} is to give a phase lead of $\pi/4$ at the angular frequency $\omega_{g,N}$. The sensitivity of the phase lead with respect to variations of ω_g is minimized by nullifying the derivative of the filter phase with respect to it at $\omega_g = \omega_{g,N}$, i.e. by imposing to have the maximum phase advance of the filter at $\omega_g = \omega_{g,N}$.

The second requirement for the filter is to have unitary gain at $\omega_g = \omega_{g,N}$ so that v_{ld} and v_{lg} have the same amplitude at the nominal frequency. Both the requirements can be fulfilled by a filter having TF

$$F_{ld}(s) = G_{ld}\frac{1+s\tau_{z,ld}}{1+s\tau_{p,ld}} \tag{3}$$

In order to size the gain and the time constants of (3), it is convenient to start from the condition concerning the achievement of the maximum phase advance at $\omega_g = \omega_{g,N}$. This condition is expressed by the relation

$$\left.\frac{d\left(arctg(\omega_g\tau_{z,ld})\right)}{d\omega_g} - \frac{d\left(arctg(\omega_g\tau_{p,ld})\right)}{d\omega_g}\right|_{\omega_g=\omega_{g,N}} = 0 \tag{4}$$

From (4) and considering that

$$\frac{d\left(arctg(\omega\tau)\right)}{d\omega} = \tau\frac{1}{1+\omega^2\tau^2} \tag{5}$$

(6) is derived

$$\omega_{g,N}^2 = \frac{1}{\tau_{p,ld}\tau_{z,ld}} \tag{6}$$

If (6) holds, at $\omega_g = \omega_{g,N}$ the complex quantity $F_{ld}(j\omega_g)$ can be written in the form

$$F_{ld}\left(j\omega_{g,N}\right) = \frac{G_{ld}}{1+\frac{\tau_{p,ld}}{\tau_{z,ld}}}\left(2+j\frac{\tau_{z,ld}-\tau_{p,ld}}{\sqrt{\tau_{z,ld}\tau_{p,ld}}}\right). \tag{7}$$

Having a phase advance of $\pi/4$ at $\omega_g = \omega_{g,N}$ entails that the real and the imaginary parts of the term within the parentheses in (7) are both positive and equal. From this condition and from (6), a symmetrical system of equations is derived as

$$\begin{cases}\tau_{p,ld}\tau_{z,ld} = \frac{1}{\omega_{g,N}{}^2}\\ \tau_{p,ld}{}^2 + \tau_{z,ld}{}^2 - 6\tau_{p,ld}\tau_{z,ld} = 0.\end{cases} \tag{8}$$

Its solution gives the time constants of the F_{ld} filter

$$\tau_{z,ld} = \frac{\sqrt{2}+1}{\omega_{g,N}}\tau_{p,ld} = \frac{\sqrt{2}-1}{\omega_{g,N}}. \tag{9}$$

By substituting (9) in (3) and imposing the condition $|F_{ld}(j\omega_{g,N})| = 1$, the gain $G_{ld,N}$ is computed as

$$G_{ld,N} = \sqrt{\frac{1+\omega_{g,N}^2\tau_{p,ld}^2}{1+\omega_{g,N}^2\tau_{z,ld}^2}} = \sqrt{2}-1. \tag{10}$$

The lag filter F_{lg} is designed following the same procedure but imposing a negative value to the imaginary part of the term within parentheses in (7). The time constants and the gain of F_{lg} result

$$\tau_{z,lg} = \tau_{p,ld}\tau_{p,lg} = \tau_{z,ld}G_{lg,N} = \frac{1}{G_{ld,N}}. \tag{11}$$

The Bode diagrams of $F_{ld}(j\omega_g)$ and $F_{lg}(j\omega_g)$ are drawn in Fig. 2 using the red solid line and the blue dashed line, respectively.

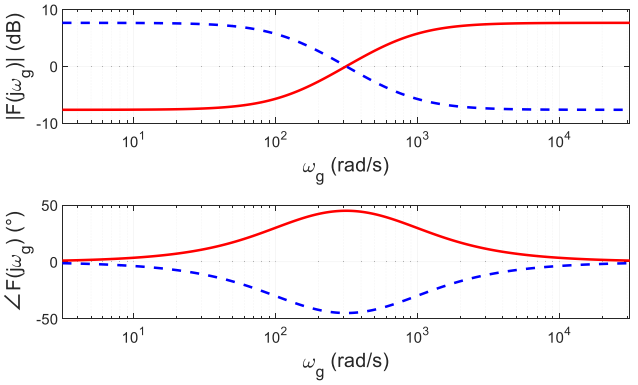

FIGURE 2. Bode diagrams of $F_{ld}(j\omega_g)$ (red solid line) and of $F_{lg}(j\omega_g)$ (blue dashed line).

Analysis of the phase diagrams confirms that the maximum phase deviation appears at $\omega_g = \omega_{g,N}$ and is equal to $\pi/4$ for $F_{ld}(j\omega_g)$ and to $-\pi/4$ for $F_{lg}(j\omega_g)$. The signals v_{ld} and v_{lg} are orthogonal only when $\omega_g = \omega_{g,N}$; nevertheless, because of condition (6), the difference of their relative phase with respect to $\pi/2$ is minimized around $\omega_g = \omega_{g,N}$ and the same happens with the variation of the phase existing between v_{ld} and v_g so that it can be expected that the phase estimate supplied by a PLL based on TOSsG will be less sensitive to variations of ω_g than that of a PLL based on SOGI.

The amplitude diagrams show that at $\omega_g = \omega_{g,N}$ both the gains of the filters are unitary, as required, and that, in the logarithmic scales, the gains vary about linearly as ω_g deviates from $\omega_{g,N}$. In this occurrence, the two gains are no more equal but, differently the SOGI method, the maximum difference between them is lower than 20 dB in both the high and low- frequency ranges. The consequent difference in the amplitudes of v_{ld} and v_{lg} leads to oscillations in $\theta_{g,e}$ and $\omega_{g,e}$. Like the SOGI method, the TOSsG exploits $\omega_{g,e}$ to adjust the amplitudes of v_{ld} and v_{lg} by multiplying the outputs of the filters by the tuning coefficients

$$T_{ld}\left(\omega_{g,e}\right) = \frac{1}{G_{ld,N}}\sqrt{\frac{1+\omega_{g,e}^2\tau_{p,ld}^2}{1+\omega_{g,e}^2\tau_{z,ld}^2}}$$
$$T_{lg}\left(\omega_{g,e}\right) = \frac{1}{T_{ld}\left(\omega_{g,e}\right)}, \tag{12}$$

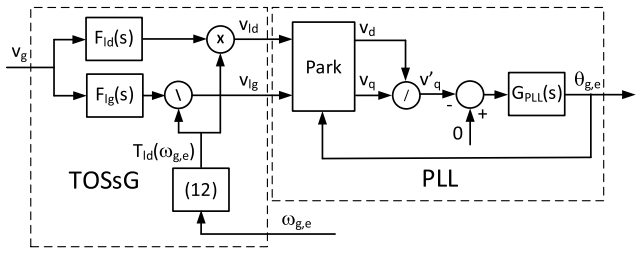

FIGURE 3. Block diagram of the TOSsG and of the PLL architecture.

derived from (10). A similar approach applied to the SOGI can be found [17], where the amplitude of v_β, i.e. the gain of $S_\beta(j\omega)$ is adjusted according to $\omega_{g,e}$.

It is worth to highlight that, following from (9)-(11), the parameters of $\tau_{z,ld}$, $\tau_{p,ld}$, $\tau_{z,lg}$, $\tau_{p,lg}$, depend only on $\omega_{g,N}$ and that $G_{ld,N}$ and $G_{lg,N}$ are constant. Consequently, the filters do not need to be redesigned in different implementation of the TOSsG that operate with the same nominal grid frequency.

IV. PLL DESIGN AND SIZING

The complete architecture of the OSG-PLL pair is shown in Fig. 3. In the hypotheses of having a purely sinusoidal v_g signal, as in (13),

$$v_g(t) = V_g \cos(\omega_g t). \tag{13}$$

and that ω_g is not much different from $\omega_{g,N}$, in steady-state the outputs of the filters F_{ld} and F_{lg}, respectively multiplied and divided by the tuning coefficients given by (12), are

$$\begin{aligned} v_{ld}(t) &= |F_{ld}(j\omega_g)|\, T_{ld}(\omega_{g,e})\, V_g \cos\left(\omega_g t + \frac{\pi}{4}\right) \\ &\cong V_g \cos\left(\omega_g t + \frac{\pi}{4}\right) \\ v_{lg}(t) &= \frac{|F_{lg}(j\omega_g)|}{T_{ld}(\omega_{g,e})} V_g \cos\left(\omega_g t - \frac{\pi}{4}\right) \\ &\cong V_g \cos\left(\omega_g t - \frac{\pi}{4}\right). \end{aligned} \tag{14}$$

The Park transform uses the estimated phase angle $\theta_{g,e}$ to process v_{ld} and v_{lg} according to

$$\begin{aligned} v_d(t) &\cong V_g \cos\left(\theta_g + \frac{\pi}{4}\right)\cos\theta_{g,e} + V_g \sin\left(\theta_g + \frac{\pi}{4}\right)\sin\theta_{g,e} \\ v_q(t) &\cong -V_g \cos\left(\theta_g + \frac{\pi}{4}\right)\sin\theta_{g,e} + V_g \sin\left(\theta_g + \frac{\pi}{4}\right)\cos\theta_{g,e}, \end{aligned} \tag{15}$$

obtained denoting with θ_g the grid voltage instantaneous phase $\omega_g t$ and exploiting the equality $\cos(\theta_g - \pi/4) = \sin(\theta_g + \pi/4)$.

Using the expressions of cos(·) and sin(·) of the difference between two angles, in the hypothesis that the error between $\theta_{g,e}$ and the actual phase of v_{ld} is small, (15) can be approximated by

$$\begin{aligned} v_d(t) &\cong V_g \cos\left[\left(\theta_g + \frac{\pi}{4}\right) - \theta_{g,e}\right] \cong V_g \\ v_q(t) &\cong V_g \sin\left[\left(\theta_g + \frac{\pi}{4}\right) - \theta_{g,e}\right] \cong V_g \left[\left(\theta_g + \frac{\pi}{4}\right) - \theta_{g,e}\right] \end{aligned} \tag{16}$$

From (15) and (16) it derives that in the SRF-PLLs the Park transform operates both as VCO and as PD.

The amplitude V_g of v_g is proportional to that of the grid voltage and hence, from (16), variations of the latter one act as variations of the gain of the LF. This influence is avoided by dividing v_q by v_d that, in steady-state, is equal to V_g. During the transients, the division by v_d does not assure a constant gain of the LF and the stability of the PLL control loop must be verified in more general conditions, as it will be done in the next Subsection. The ratio v_q/v_d is denoted as v_q' in Fig. 3 and in the following figures. It supplies the LF and, from (16), is proportional to the difference between the grid voltage phase augmented of $\pi/4$ and the estimated angle $\theta_{g,e}$, thus demonstrating that with the TOSsG the PLL actually estimates the phase of v_{ld} rather than θ_g. Being the difference between the two phases known and constant, there is no difficulty in working out θ_g by subtracting $\pi/4$ from $\theta_{g,e}$. This last operation is not mentioned in the following discussion to simplify the figures and the equations. With the given definition of v_q', the control loop built around the LF can be redrawn as in Fig. 4, where $G_{PLL}(s)$ has been split into two blocks, according to (17)

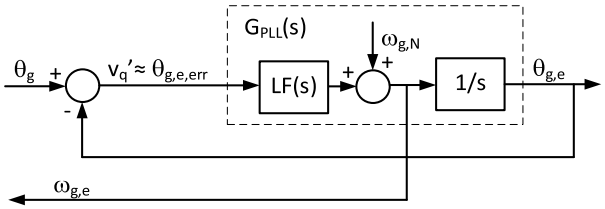

FIGURE 4. Block diagram of the PLL control loop of $\theta_{g,e}$.

$$G_{PLL}(s) = LF(s)\frac{1}{s}. \tag{17}$$

The phase angle θ_g has a ramp-like behavior and consequently $\theta_{g,e}$ can follow it accurately only if $G_{PLL}(s)$ is a type-2 system. From (17), this feature entails that LF(s) must have a pole in the origin.

The output of LF(s) is integrated to obtain $\theta_{g,e}$ and hence it must be equal to $\omega_{g,e}$. In order to speed up the transients of the control loop, a feedforward contribution equal to $\omega_{g,N}$ is usually added at the output of LF(s).

As explained in the previous Sections, the TOSsG processes $\omega_{g,e}$ to adjust the gains of the filters F_{ld} and F_{lg}, therefore the estimation of ω_g must be accurate and without disturbances. Given that neither F_{ld} nor F_{lg} effectively attenuates the high -frequency components of v_g, the filtering action of the pole in the origin of LF(s) is not sufficient to get rid of the oscillations of $\omega_{g,e}$ and must be enhanced with an additional pole. This modification and the presence of the integrator downhill LF(s) require an accurate design of LF(s) itself to ensure an adequate phase margin at the selected crossover angular frequency

A. DESIGN OF THE LOOP FILTER

According to the previous considerations, LF(s) is expressed as

$$LF(s) = K_{PLL}\frac{(1 + s\tau_{z,PLL})}{s(1 + s\tau_{p,PLL})}, \tag{18}$$

with the gain K_{PLL} and the time constants $\tau_{z,PLL}$ and $\tau_{p,PLL}$ defined according to the following analysis.

From (17) and (18), the open-loop transfer function of the PLL is

$$G_{PLL}(s) = K_{PLL}\frac{\left(1+s\tau_{z,PLL}\right)}{s^2\left(1+s\tau_{p,PLL}\right)}. \tag{19}$$

The presence of the second pole in the TF (18) gives an additional degree of freedom to design the PLL with respect to the conventional solutions. One of the degrees of freedom is used to optimize the ratio between the time constants $\tau_{z,PLL}$ and $\tau_{p,PLL}$ in order to fully exploit the effect of the zero-pole pair. To this end, their maximum phase advance is set in correspondence to the crossover angular frequency ω_{cr} of $G_{PLL}(s)$. This requirement is the same that led to (6) and is fulfilled if ω_{cr}, $\tau_{z,PLL}$ and $\tau_{p,PLL}$ satisfy the relation (20).

$$\omega_{cr}^2 = \frac{1}{\tau_{z,PLL}\tau_{p,PLL}}. \tag{20}$$

By definition, at $\omega = \omega_{cr}$ the magnitude of $G_{PLL}(j\omega)$ is equal to 1 so that it is

$$K_{PLL}^2\frac{\left(1+\omega_{cr}^2\tau_{z,PLL}^2\right)}{\omega_{cr}^4\left(1+\omega_{cr}^2\tau_{p,PLL}^2\right)} = 1. \tag{21}$$

After substituting (20) in (21), some manipulations lead to expression (22)

$$K_{PLL}^2\frac{\left(\frac{\tau_{p,PLL}+\tau_{z,PLL}}{\tau_{p,PLL}}\right)\tau_{z,PLL}^2\tau_{p,PLL}^2}{\left(\frac{\tau_{p,PLL}+\tau_{z,PLL}}{\tau_{z,PLL}}\right)} = 1. \tag{22}$$

Using again (20), it gives

$$K_{PLL} = \frac{\omega_{cr}}{\tau_{z,PLL}}, \tag{23}$$

which links K_{PLL} to the other parameters of LF(s).

It is worth to highlight that at this point of the LF design ω_{cr} has not yet been set and that it will be determined by imposing the conditions described in the following paragraphs. These conditions are derived from [21] and are enforced to use the same PLL control loop in comparing the TOSsG with the other OSG methods reviewed in that paper.

The closed-loop TF $W_{PLL}(s)$ from θ_g to $\theta_{g,e}$ is readily obtained from (19) and the diagram of Fig. 4. By considering (20) and (23), $W_{PLL}(s)$ is written in the form

$$W_{PLL}(s) = \frac{\frac{\omega_{cr}}{\tau_{z,PLL}}\left(1+s\tau_{z,PLL}\right)}{s^3\frac{1}{\omega_{cr}^2\tau_{z,PLL}}+s^2+s\omega_{cr}+\frac{\omega_{cr}}{\tau_{z,PLL}}} \tag{24}$$

TABLE 1. Requirements and design parameters of PLL control loop.

Requirements		Design parameters	
ξ_{PLL}	0.7	ω_{cr}	99.36 rad/s
ω_B	$2\pi\cdot100$ rad/s	$\tau_{z,PLL}$	24.15 ms
G_B	-25dB	$\tau_{p,PLL}$	4.193 ms
		K_{PLL}	4113

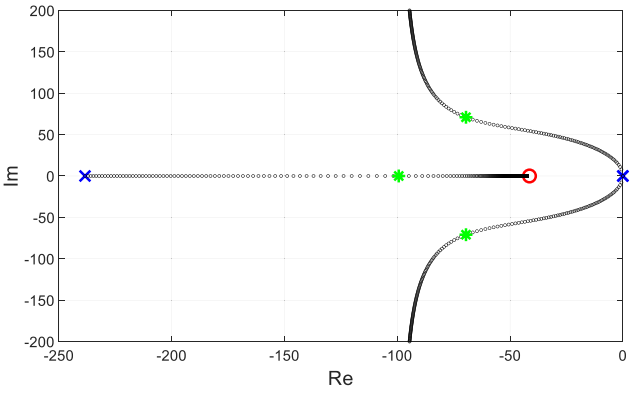

FIGURE 5. Root locus of the PLL control loop.

and then as

$$W_{PLL}(s) = \frac{\frac{\omega_{cr}}{\tau_{z,PLL}}\left(1+s\tau_{z,PLL}\right)}{(s+\omega_{cr})\left[s^2\frac{1}{\omega_{cr}^2\tau_{z,PLL}}+s\left(1-\frac{1}{\omega_{cr}\tau_{z,PLL}}\right)+\frac{1}{\tau_{z,PLL}}\right]}. \tag{25}$$

From (25) it is possible to work out the damping coefficient of the second-order term within the square brackets. It is given by

$$\xi_{PLL} = \frac{\omega_{cr}\tau_{z,PLL}-1}{2}. \tag{26}$$

This coefficient does not correspond to the actual damping coefficient of $W_{PLL}(s)$ because the derivative effect of the zero in $\tau_{z,PLL}$ causes an overshoot in the step response of $W_{PLL}(s)$ even if ξ_{PLL} is equal or even bigger than 1.

An effective filtering action of LF(s) is enforced by imposing that the magnitude of $G_{PLL}(j\omega_g)$ is less than 1 at angular frequencies higher than $\omega_{g,N}$. In particular, setting $G_{PLL}(j\omega_B) = G_B < 1$ at the angular frequency $\omega_B > \omega_{g,N}$ in rewriting (21) gives the relation

$$K_{PLL}^2\frac{\left(1+\omega_B^2\tau_{z,PLL}^2\right)}{\omega_B^4\left(1+\frac{\omega_B^2}{\omega_{cr}^2\tau_{z,PLL}^2}\right)} = G_B^2 \tag{27}$$

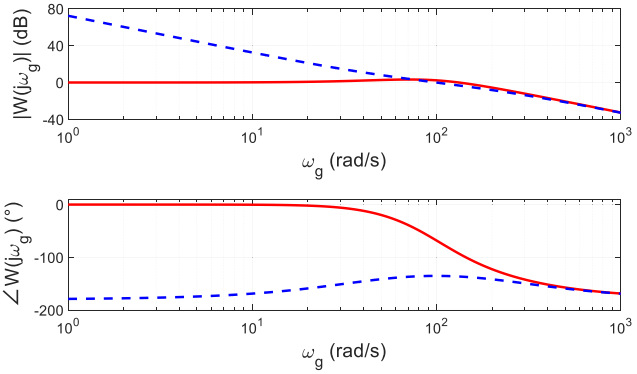

FIGURE 6. Bode diagrams of $G_{PLL}(j\omega_g)$ (blue dashed line) and $W_{PLL}(j\omega_g)$ (red solid line) with $\xi_{PLL} = 0.7$.

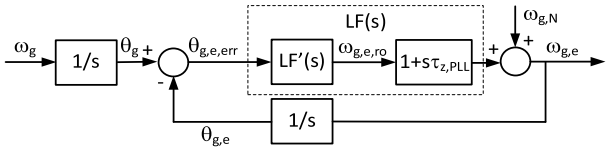

FIGURE 7. Block diagram of the PLL control loop of $\omega_{g,e}$ as derived from Fig. 4.

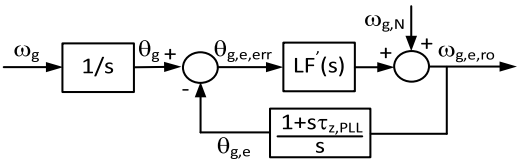

FIGURE 9. Block diagram of the PLL control loop of $\omega_{g,e,ro}$ with ZFBP.

and, after some manipulations that involve the use of (23) and (26), leads to the equation

$$\Omega_{cr}^3 + \Omega_{cr}^2\omega_B^2\left(2\xi_{PLL}-1\right)^2 - \Omega_{cr}G_B^2\omega_B^4\left(2\xi_{PLL}-1\right)^2 - \omega_B^6 G_B^2 = 0 \quad (28)$$

where $\Omega_{cr} \triangleq \omega_{cr}^2$.

Application of the Descartes rule of signs shows that (28) has always one positive solution so that it is possible to find ω_{cr} for any combination of ξ_{PLL}, ω_B, and G_B. Moreover, being (28) of degree three in the variable Ω_{cr}, it would be possible to express ω_{cr} analytically as a function of ξ_{PLL}, ω_B, and G_B. Once obtained ω_{cr}, by inversion of (26) and (20) and using (23), the design parameters of LF(s) are determined.

The requirements reported in the left column of Table 1 have been used in designing LF(s), obtaining numerically the design parameters listed in the right column.

Using the parameters of Table 1, the root locus of the PLL control loop results as reported in Fig. 5. It has three branches that originates from the poles of $G_{PLL}(s)$, represented by the blue crosses. One branch moves toward the zero of $G_{PLL}(s)$, represented by the red circle, whereas the other two are not limited. All the branches lie completely on the left half of the complex plane entailing that the PLL control loop is stable for any value of the loop gain. In particular, when the gain given by the v_d/v_q ratio is equal to one, the roots of $W_{PLL}(s)$ lie on the green stars. The correspondent Bode diagrams of $G_{PLL}(s)$ and $W_{PLL}(s)$ are reported in Fig. 6 with the blue dashed line and the red solid line, respectively. The plots show that the PLL control loop has a phase margin of about 80° and that it exhibits the low pass behavior required to attenuate the oscillations superimposed to the phase estimate due to not ideal waveform of the grid voltage.

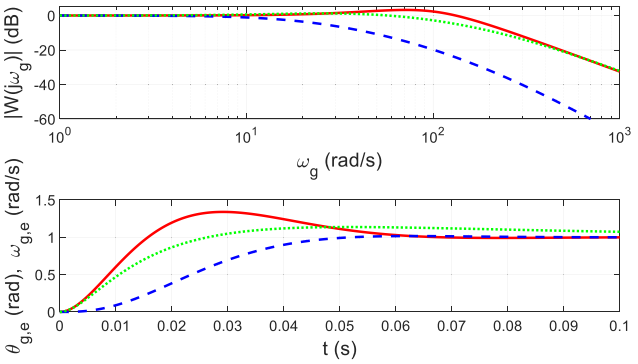

FIGURE 8. Bode diagrams (top) and step responses (bottom) of $W_{PLL}(j\omega_g)$ with $\xi_{PLL} = 0.7$ (red solid line), of $W_{PLL}(j\omega_g)$ with $\xi_{PLL} = 2$ (green dotted line) and of $W'_{PLL}(j\omega_g)$ with $\xi_{PLL} = 0.7$ (blue dashed line).

B. GENERATION OF THE ESTIMATED ANGULAR FREQUENCY

In order to analyze the performance of the PLL control loop in generating $\omega_{g,e}$, i.e. the estimate of the grid angular frequency, the block diagram shown in Fig. 4 is redrawn in the form of Fig. 7, considering $\omega_{g,e}$ as the output variable and moving the integrator in the feedback path. A second integrator is added at the input of the loop to use ω_g instead of θ_g as the input variable.

For reasons that will be explained in the following paragraphs, LF(s), defined in (18), has been split into two stages according to (29)

$$LF(s) = LF'(s)\left(1 + s\tau_{z,PLL}\right), \quad (29)$$

where

$$LF'(s) = K_{PLL}\frac{1}{s\left(1 + s\tau_{p,PLL}\right)}, \quad (30)$$

From the analysis of the diagram of Fig. 7, it comes that the TF from ω_g to $\omega_{g,e}$ is the same as the TF from θ_g to $\theta_{g,e}$, given by (24), and consequently its magnitude Bode diagram and step response are those reported by the red solid lines in Fig. 6. A magnification of the magnitude Bode diagram of $W_{PLL}(j\omega_g)$ is reported also in the upper half of Fig. 8 by the red solid line and the relevant step response is plotted in the lower half of the figure with the same line and color features. The magnitude of $W_{PLL}(j\omega_g)$ exhibits an overshoot higher than 3dB at $\omega_g \approx 74$ rad/s; it is reflected in the step response that has an overshoot of about 35%.

The overshoot in the step response of $W_{PLL}(j\omega_g)$ can be reduced by increasing the damping coefficient ξ_{PLL}. For example, the plots drawn with the green dotted lines in Fig. 8 have been obtained setting $\xi_{PLL} = 2$. Despite this large damping coefficient, the step response still has an overshoot higher than 13% and is far from reaching the steady-state within the time interval considered in the figure.

This behavior can be explained by hypothesizing that ω_g is subjected to a positive step. In the very first instants after the application of the step, $\theta_{g,e}$ lags θ_g so that the only way for $\theta_{g,e}$ to reach again θ_g is that for a while $\omega_{g,e}$ exceeds ω_g. This means that the step response of $\omega_{g,e}$ has an overshot and that this overshoot cannot be avoided, otherwise $\theta_{g,e}$ will never reach the correct value. The step response of $\theta_{g,e}$ is equal to that of $\omega_{g,e}$ and consequently it has an unavoidable overshoot as well.

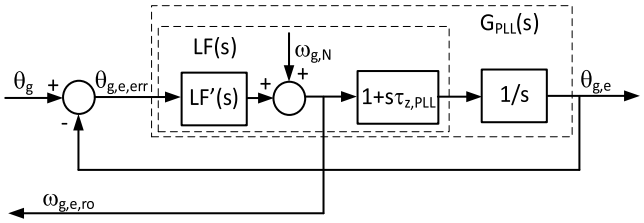

FIGURE 10. Comprehensive block diagram of the PLL control loop.

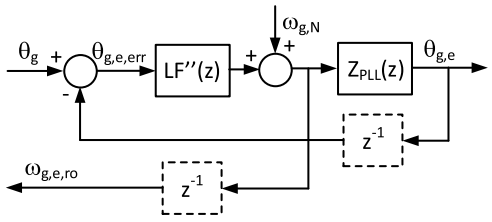

FIGURE 11. Block diagram of the discretized PLL control loop with ZFBP.

A solution to get rid of the overshoot in $\omega_{g,e}$, reported for example in [3], and here denoted as "zero in the feedback path" (ZFBP), consists in considering the output of LF'(s), denoted as $\omega_{g,e,ro}$, i.e. the estimate of the grid angular frequency with reduced overshoot, instead of $\omega_{g,e}$ as an estimate of the grid angular frequency. The block scheme representing the TF from ω_g to $\omega_{g,e,ro}$ is depicted in the diagram of Fig. 9, obtained from Fig. 7 by considering $\omega_{g,e,ro}$ as an output variable and moving the zero of LF(s) in the feedback path.

With ZFBP, the open-loop and the closed-loop TFs of the PLL are still given by (19) and (25), respectively, and consequently zeros, poles and stability of this loop are not affected by ZFBP. However, with ZFBP, the TF from ω_g to $\omega_{g,e,ro}$ changes from (24) to

$$W'_{PLL}(s) = \frac{\frac{\omega_{cr}}{\tau_{z,PLL}}}{s^3 \frac{1}{\omega_{cr}^2 \tau_{z,PLL}} + s^2 + s\omega_{cr} + \frac{\omega_{cr}}{\tau_{z,PLL}}}. \quad (31)$$

Clearly the denominator remains the same, but the derivative effect of the zero at the numerator disappears. Consequently, according to the blue dashed line plot in the Fig. 8, the low pass effect at high frequency is stronger. Indeed, the slope of the magnitude diagram increases from −40 dB/dec to −60 dB/dec, and the overshoot nearly disappears without increasing the time needed to reach the steady-state condition

Introducing the ZFBP approach, the comprehensive block diagram of the PLL control loop results as depicted in Fig. 10, obtained from Fig. 4 by decomposing LF(s) according to (29) and considering $\omega_{g,e,ro}$ as additional output variable used also as input for the computation of the tuning gains T_{ld} and T_{lg}.

V. TOSsG AND PLL DISCRETIZATON AND SIMULATION

The filters that implement the TOSsG and the PLL control loop must be discretized to be coded in the firmware of the DSC. The discretization of $F_{ld}(s)$ by Tustin's method leads to the following expression

$$F_{ld}(z) = G_{ld,N} \frac{\left(1 + \frac{2\tau_{z,ld}}{T_s}\right) + z^{-1}\left(1 - \frac{2\tau_{z,ld}}{T_s}\right)}{\left(1 + \frac{2\tau_{p,ld}}{T_s}\right) + z^{-1}\left(1 - \frac{2\tau_{p,ld}}{T_s}\right)}. \quad (32)$$

The expression of $F_{lg}(z)$ is the same as (32) provided that its coefficients are changed according to (11).

The discretized version of (30) is

$$LF'(z) = K_p \frac{T_s}{2} \times \frac{(1+z^{-1})^2}{\left(1 + \frac{2\tau_{p,PLL}}{T_s}\right) + z^{-1}\left(-\frac{4\tau_{p,PLL}}{T_s}\right) + z^{-2}\left(-1 + \frac{2\tau_{p,PLL}}{T_s}\right)}. \quad (33)$$

It can be decomposed in the cascade of two discrete TFs, as in

$$LF'(z) = \frac{(1+z^{-1})}{2} LF''(z), \quad (34)$$

with

$$LF''(z) = K_p T_s \times \frac{(1+z^{-1})}{\left(1 + \frac{2\tau_{p,PLL}}{T_s}\right) + z^{-1}\left(-\frac{4\tau_{p,PLL}}{T_s}\right) + z^{-2}\left(-1 + \frac{2\tau_{p,PLL}}{T_s}\right)} \quad (35)$$

From (34) it comes that actually the output of LF'(z) is the average value of two subsequent samples of the output of LF''(z). From this consideration, an attempt has been made to simplify the implementation of the PLL by neglecting the computation of the average value and coding LF''(z) instead of LF' (z) in the DSC firmware.

The discretization of $(1+s\tau_{z,PLL})/s$ gives

$$Z_{PLL}(z) = \frac{T_s}{2} \frac{\left(1 + \frac{2\tau_{z,PLL}}{T_s}\right) + z^{-1}\left(1 - \frac{2\tau_{z,PLL}}{T_s}\right)}{(1 - z^{-1})}. \quad (36)$$

Starting from Fig. 10 and substituting LF'(s) and $(1+s\tau_{z,PLL})/s$ with LF''(z) and $Z_{PLL}(z)$, respectively, the discrete-time block diagram of the PLL reported in Fig. 11 is obtained.

Analysis of Figs. 3, 10, and 11, and of (35) and (36) shows that there are direct feed-throughs from the output of $Z_{PLL}(z)$ to the input of $LF''_{PLL}(z)$ and from the output of $LF''_{PLL}(z)$ to its input through (12) and the Park transform. The direct feedthroughs cannot be implemented in the control firmware so that a one-step delay is inserted in each loop. This operation is represented in Fig. 11 by the z^{-1} symbols within the dashed boxes. Given the low cutoff frequency of the control loop, which is about 16 Hz in the considered case, and the sampling time of the discrete control system, which can be considered in the order of 100μs, the effects of the

TABLE 2. Simulation results.

	TOSsG (no-LUT)	TOSsG (s-LUT)	TOSsG (l-LUT)
$f_{g,e}$ Settling time (ms)	55.8	50.6	50.8
$f_{g,e,ro}$ Settling time (ms)	39.6	39.3	39.7
$f_{g,e}$ Overshoot (Hz)	1.0	0.9	0.9
$f_{g,e,ro}$ Overshoot (Hz)	0.07	0.03	0.06
$f_{g,e}$ Peak-to-Peak (mHz)	392	18.0	6.8
$f_{g,e,ro}$ Peak-to-Peak (mHz)	24	1.1	0.4
$\theta_{g,err}$ Max (°)	16.8	8.7	8.7
$\theta_{g,err}$ Steady-state (°)	0.0	0.0	0.0

delay blocks can be neglected and their insertion does not require to re-design LF(s).

The real-time computation of (12) to adjust the gains of the TOSsG filters is time-consuming for the DSC and hence the tuning coefficients $T_{ld}(\omega_{g,e})$ and $T_{lg}(\omega_{g,e})$ have been computed in advance from (9) and (12) for different values of $\omega_{g,e}$, and their samples have been stored in a look-up table (LUT). The output of the LUT is computed performing a linear interpolation between the two values corresponding to the LUT's entries immediately lower and higher than its actual input.

To test the sensitivity of TOSsG to the grid frequency variation, two LUTs have been filled considering the grid frequency f_g spanning the interval 45 Hz to 55 Hz: one large LUT with 101 entries, evenly spaced of 0.1 Hz, and a small LUT with only 3 entries set at 45 Hz, 50 Hz, and 55 Hz. The large LUT maintains the amplitude of the two orthogonal signals nearly equal to that of v_g in all the considered range of f_g; on the contrary, the small LUT satisfies exactly this condition only at the nominal and at the extreme frequencies and originates the maximum error at 47.5 Hz and 52.5 Hz.

The performance of the discrete time PLL has been at first checked by simulations developed in the Matlab-Simulink environment setting the sampling time to 100μs. In particular, the response of the PLL to step changes of f_g has been tested in three different conditions: disabling the TOSsG filter adjustment (no-LUT), enabling the real-time adjustment with the large LUT (l-LUT), and enabling the adjustment with the small LUT (s-LUT). The frequencies of 47.5 Hz and 52.5 Hz have been selected as the initial and the final values of the f_g step in order to check the performance of the small LUT in the worst conditions.

Table 2 reports the settling time of the frequency estimates $f_{g,e}$ and $f_{g,e,ro}$ within $f_g \cdot (1 \pm 0.005)$, their overshoot, and their steady-state peak-to-peak oscillation. In the last two rows of the table are shown the maximum and the steady-state value of the phase estimate error.

Analysis of the simulation results confirms that the PLL based on TOSsG operates correctly and, in the considered range of frequency, successes in estimating accurately the phase of v_g even when the filters are not tuned. On the contrary, tuning of the filters is necessary to reduce the oscillations on the estimated frequency but it can be performed using the small LUT. Finally, the ZFBP solution exerts an effective action in reducing the oscillations amplitude and the settling time of $f_{g,es,ro}$ with respect to $f_{g,es}$.

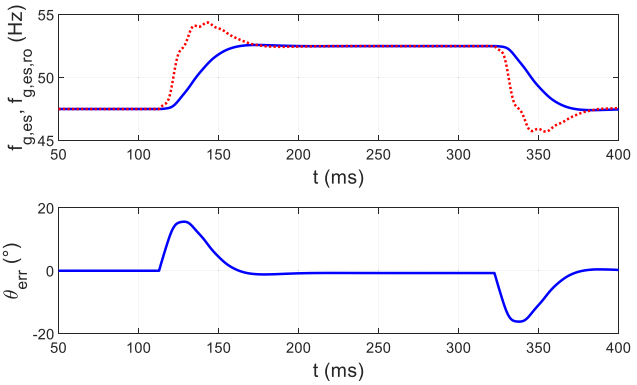

FIGURE 12. Response to frequency steps: $f_{g,e}$ (red dotted line), $f_{g,e,ro}$ (blue solid line) and $\theta_{g,err}$ (blue solid line) with 64-bit resolution and large LUT.

VI. TOSsG IMPLEMENTATION AND PRELIMINARY TESTS

The TOSsG and the PLL with ZFBP have been implemented in the firmware of a Texas TMS320F28335 DSC. It has a clock frequency of 150 MHz and operates with 32-bit floating-point numbers [29]; if needed, libraries are available with 64-bit floating-point mathematical routines.

Besides the two LUTs described in the previous Section and the relevant interpolation routine, in the memory of the DSC has been stored another LUT for the computation of the sin(·) and cos(·) functions used in the Park transform. A section of the memory has been arranged in four arrays, each with 2048 elements, used to store the samples of the outputs and of other quantities related to the TOSsG and the PLL. During the experimental tests, the content of the arrays has been transferred from the DSC memory to a PC using the USB connection of the DSC development board and

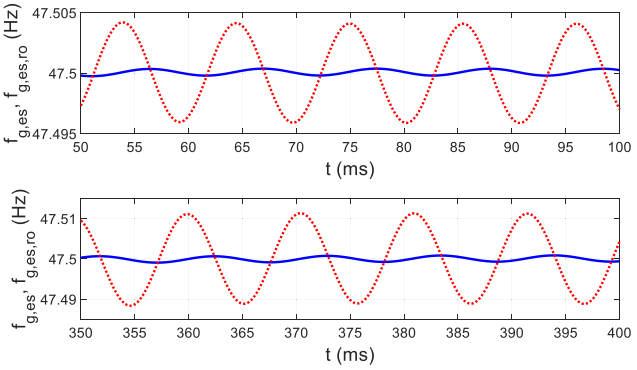

FIGURE 13. Magnification of the response to a frequency step: $f_{g,e}$ (red dotted line) and $f_{g,e,ro}$ (blue solid line) with 64-bit resolution and large LUT (top) and small LUT (bottom).

has been post-processed in the Matlab environment to check the TOSsG and PLL performance and to draw the figures reported in this and in the next Sections.

A preliminary series of tests have been performed to assess the effects of the finite resolution of the DSC and of the size of the LUTs used to tune the filters gains. In order to get rid of all the non-idealities due to the conditioning, acquisition, and conversion of the grid voltage, the preliminary tests have been carried out generating the samples of v_g by means of a firmware routine run by the DSC together with those that implement the TOSsG and the PLL. To this aim, a ramp counter has been implemented to generate θ_g and from it, using the sin(·) LUT, v_g has been computed. Sudden variations of ω_g have been obtained by changing the incremental step of the counter.

The first test has been performed in the best conditions, i.e. with 64-bit resolution and using the large LUT. Fig. 12 reports the response to two frequency steps of v_g, from 47.5 Hz to 52.5 Hz and then back to 47.5 Hz.

In the upper half of the figure, the frequency estimates $f_{g,es}$ and $f_{g,es,ro}$ are plotted with the red dotted line and the blue solid line, respectively. As expected, $f_{g,es,ro}$ exhibits a much smoother behavior than $f_{g,es}$, nonetheless they reach the steady-state condition nearly in the same time. The lower half of the figure shows the corresponding $\theta_{g,err}$ expressed in degrees; it reaches a maximum value of about 17°.

The upper half of Fig. 13 reports a magnification of the initial time interval considered in Fig. 12. It shows that at steady-state $f_{g,es}$ oscillates with a peak to peak amplitude of about 8 mHz around the correct value, instead, considering $f_{g,es,ro}$, the maximum error is about ten times lower. The same values are found also considering the steady-state condition at $f_g = 52.5$ Hz. The steady-state average phase error, not shown in the figures, is about null in both cases, but oscillates with an amplitude of 0.002°.

The lower half of Fig. 13 reports the results obtained performing the same test using the small LUT. With $f_g = 47.5$ Hz it operates in the worst condition, and indeed the peak to peak amplitude of the oscillation of $f_{g,es}$ increases

FIGURE 15. Experimental setup.

to about 22 mHz whereas for $f_{g,e,ro}$ it reaches 1.8 mHz. The corresponding average phase error is null but its oscillation reaches an amplitude of about 0.003°.

The computation time required to implement the PLL algorithm with 64-bit resolution resulted nearly equal to the sampling period, i.e. 100μs, thus not leaving enough time to implement any useful control application. For this reason, the performance of the PLL implementation with a 32-bit resolution has been checked by repeating the test with the small LUT.

The obtained responses, plotted at the scale of Fig. 12, are not distinguishable from the previous ones. However, at a magnification comparable with that of Fig. 13, some differences can be recognized, as shown in Fig. 14. The upper half of the figure refers to the steady-state condition at $f_g = 47.5$ Hz and should be compared with the lower half of Fig. 13. With the 32-bit resolution the waveform of the oscillations of $f_{g,es}$ become almost triangular rather than sinusoidal and their peak to peak amplitude increases up to 50 mHz; instead, the oscillations of $f_{g,es,ro}$ are still nearly sinusoidal even if their peak to peak amplitude reaches 6 mHz. The lower half of Fig. 14 refers to steady-state condition at $f_g = 52.5$ Hz and shows that the behavior $f_{g,es}$ and $f_{g,es,ro}$ is nearly equal to that found at the lower frequency.

Implementation of the PLL algorithm with 32-bit resolution reduces the execution time to about 5.7 μs still

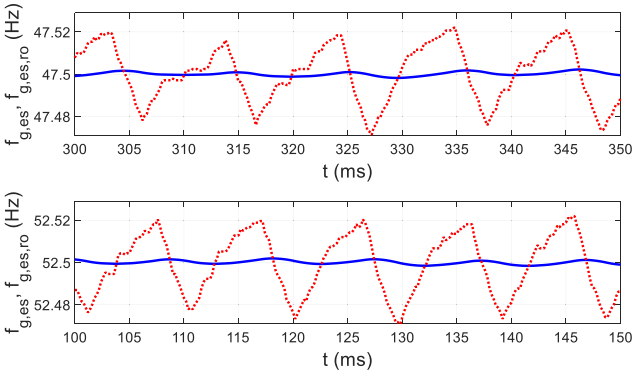

FIGURE 14. Magnification of the response to a frequency step: $f_{g,e}$ (red dotted line) and $f_{g,e,ro}$ (blue solid line) with 32-bit resolution and small LUT.

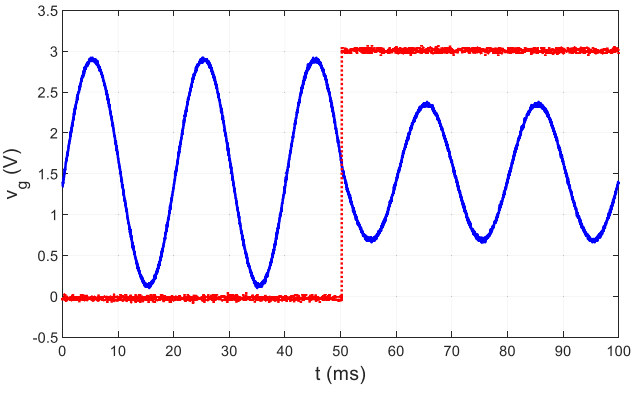

FIGURE 16. Waveforms generated by the PSoC and acquired by the oscilloscope during a test related to a step of v_g amplitude.

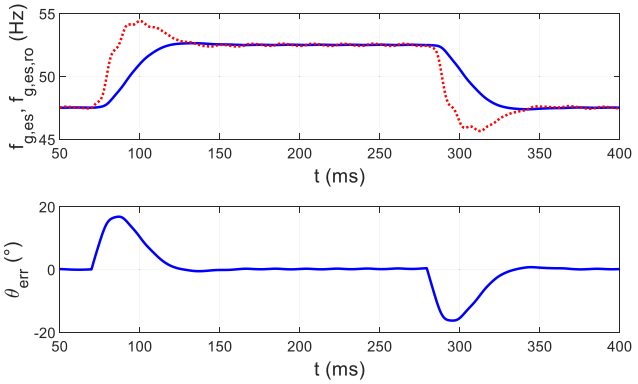

FIGURE 17. Experimental response to frequency steps: $f_{g,e}$ (red dotted line), $f_{g,e,ro}$ (blue solid line), and θ_{err} (blue solid line).

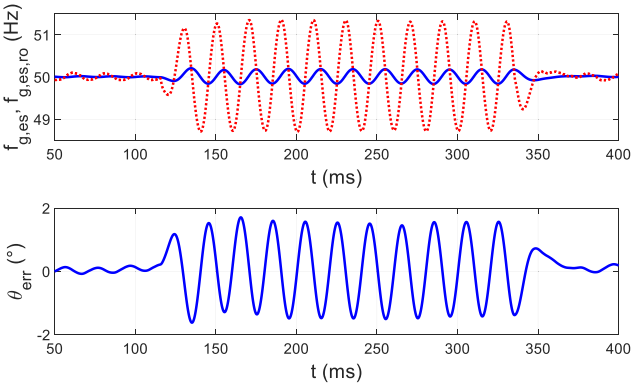

FIGURE 19. Experimental response to offset steps: $f_{g,e}$ (red dotted line), $f_{g,e,ro}$ (blue solid line) and θ_{err} (bottom).

maintaining the precision in the frequency estimate is in the order of the mHz. For these reasons, the final experimental tests have been performed with this resolution and using the small LUT.

VII. FINAL EXPERIMENTAL TESTS

The final tests consisted in five experiments carried out as far as it was possible in the same conditions and with the same solicitations reported in [21] in order to perform a fair comparison with the results of that papers, where the performance of a total of eight different types of PLL are reported. In the referenced paper the PLL algorithms were implemented in a 64-bit microprocessor with a sample time of 100 μs whereas in this paper the same sample time is maintained, but the algorithms are implemented with a 32-bit resolution. As shown in the previous Section, this limitation degrades the performance of the proposed TOSsG method and of the overall PLL, but in any case, as it will be demonstrated, the obtained experimental results are comparable if not better than those of the algorithms analyzed in [21].

In these tests, the same conditions that would be met in a real application, where v_g comes from a circuit that transduces the grid voltage, have been reproduced by generating v_g using the 12-bit DAC of a Cypress PSoC 5LP microcontroller [30]. The signal v_g is then acquired by the DSC by means of its embedded 12-bit ADC. The development boards of the PSoC and of the DSC and the relevant connections are shown in Fig. 15.

The PSoC has been programmed to drive the DAC with an update frequency of 10 kHz and to generate the sinusoidal signal v_g with a nominal offset of 1.5 V and a maximum amplitude of 1.5 V to comply with the ratings of the ADC of the DSC. An LPF, designed according to the PSoC data sheet, has been connected at the output of the DAC to smoothen the quantization steps of the generated signal; it is constituted by the light blue polyester capacitor connected to the Cypress board. The frequency, amplitude, offset, instantaneous phase and harmonic content of v_g have been controlled independently in order to test the PLL algorithm in different conditions. The waveform of v_g has been monitored by means of a digital oscilloscope finding that it is actually sinusoidal with a frequency accuracy of about ± 0.02 Hz. Fig. 16 reports an example of the waveforms obtained processing by Matlab the samples of v_g acquired by the oscilloscope. The red dotted stepwise waveform is an auxiliary digital signal generated

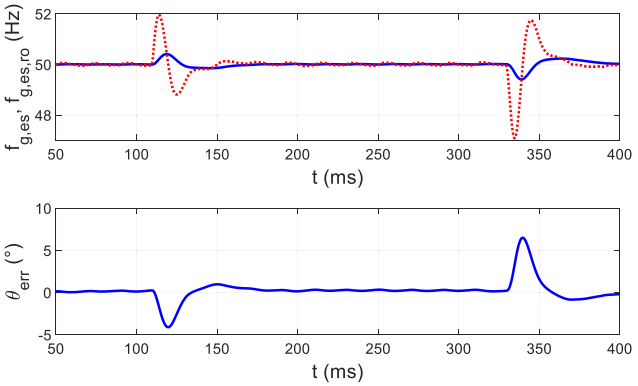

FIGURE 18. Experimental response to amplitude steps: $f_{g,e}$ (red dotted line), $f_{g,e,ro}$ (blue solid line) and θ_{err} (blue solid line).

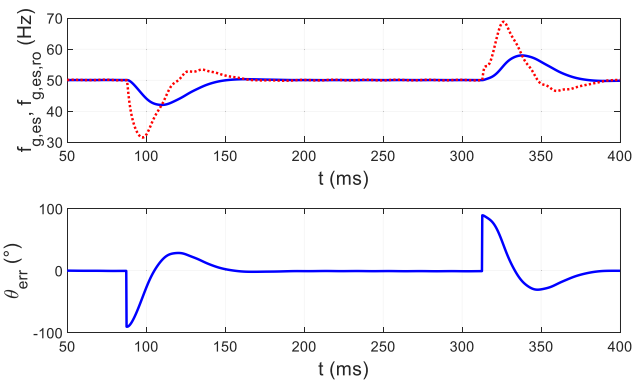

FIGURE 20. Experimental response to phase steps: $f_{g,e}$ (red dotted line), $f_{g,e,ro}$ (blue solid line) and θ_{err} (bottom).

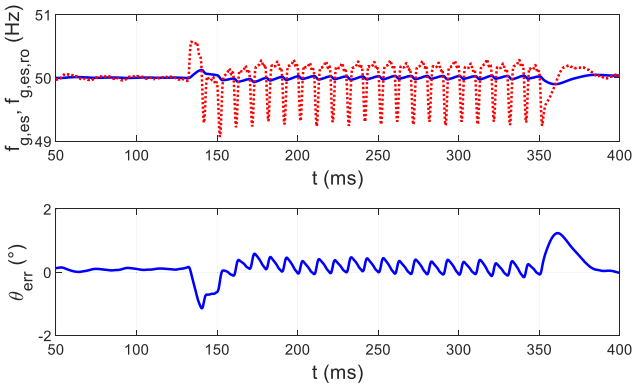

FIGURE 21. Experimental response to harmonic application: $f_{g,e}$ (red dotted line), $f_{g,e,ro}$ (blue solid line) and θ_{err} (bottom).

by the PSoC and acquired by the DSC. Its transitions are synchronized with the variations superimposed to v_g and are used to make easier the post-processing of the samples stored in the DSC memory.

The first experiment has been performed in the same conditions as Fig. 12, i.e. imposing to v_g a stepwise frequency variation from 47.5 Hz to 52.5 Hz and then back to 47.5 Hz.

The frequency estimate and phase error obtained in this experiment are reported in Fig. 17. The general behavior of $f_{g,e}$, $f_{g,e,ro}$ and θ_{err} is the same as the one reported in Fig. 12 of the previous Section, with $f_{g,es}$ and $f_{g,es,ro}$ subjected to a maximum overshoot of about 1.9 Hz and 0.01 Hz, respectively. The maximum phase error is of 16.8°. A more careful analysis reveals that, with respect to results of the preliminary tests, the oscillations superimposed to $f_{g,es}$ and $f_{g,es,ro}$ increase up to 0.07 Hz and 12 mHz, respectively. Both the estimated frequencies are about 0.02 Hz higher than the theoretical ones, but this error falls within the accuracy of the signal generated by the PSoC. The phase error at steady-state oscillates with an amplitude of 0.1°. This error is not significant because, at the nominal frequency, the actual phase of v_g varies of about 1.8° within one sampling period.

In the second experiment, the amplitude of v_g is subjected to two sudden steps from $V_{g,N}$ to 0.6 $V_{g,N}$ and then back to $V_{g,N}$. As shown in Fig. 18, in this case both the frequency estimates and the phase error are affected by transient variation caused by the two amplitude steps but at the steady state they have the same behavior both for $V_g = V_{g,N}$ and $V_g = 0.6\ V_{g,N}$. The maximum frequency estimates errors can be evaluated in 2.9 Hz for $f_{g,es}$ and 0.6 Hz for $f_{g,es,ro}$, and happen in correspondence to the falling step of V_g whilst on the rising step the frequency estimates errors are 1.9 Hz and 0.4 Hz, respectively. The maximum phase error is equal to 6.5° at the falling step and to 4.1° at the rising step.

The third experiment involved the sum of an offset equal to 0.05 $V_{g,N}$ to v_g and then its removal. The relevant results are shown in Fig. 19. While the offset is applied, the amplitude of the oscillation of $f_{g,es}$ increases up to 1.33 Hz and that of $f_{g,es,ro}$ reaches 0.18 Hz. In both cases these values are maintained until the offset is removed. The average value of the frequency estimates is not influenced by the offset and in this test results of 50.01 Hz. The phase error due to the offset reaches 1.7° and oscillates with about constant amplitude while the offset is applied. After the removal of the offset, $f_{g,es}$, $f_{g,es,ro}$ and θ_{err} reach the steady state in about 31 ms, 61 ms, and 45 ms, respectively.

The fourth experiment consisted in forcing a sudden negative step of 90° to the phase of v_g and then a positive step having equal amplitude. Fig. 20 shows that the two frequency estimates exhibit a sensible reaction to the phase steps. In this case, the maximum frequency error for $f_{g,es}$ is of nearly 20 Hz and its maximum overshoot after recovering the correct value is about 3.4 Hz. The maximum frequency error for $f_{g,es,ro}$ is about 8 Hz and its overshoot is 0.3 Hz. The maximum phase error is obviously 90° and after crossing the zero it has a maximum overshot of 30°.

In the last experiment, three harmonics have been added to v_g: a 3rd and a 5th harmonic with amplitude 0.05 $V_{g,N}$ and a 7th harmonic with amplitude 0.04 $V_{g,N}$. Harmonics have been enabled and disabled abruptly obtaining the responses

TABLE 3. Experimental results comparison.

		TOSsG ($f_{g,es}$)	TOSsG ($f_{g,es,ro}$)	Delay [10]	Deri [31]	Park [11]	SOGI [14]	DOEC [32]	VTD [33]	CCF [13]	TPFA [20]
5 Hz Step f_g	a) $f_{g,es}$ Settling time (ms)	**57.4**	**43.6**	70	70	72	53	72	90	75	90
	b) $f_{g,es}$ Overshoot (Hz)	**1.9**	**0.14**	2.2	2.0	2.5	2.1	2.5	3.5	8.1	2.6
	c) $\theta_{g,err}$ Max (°)	**16.8**		16.0	12.5	17.0	15.5	17.0	25.0	21.0	25.0
40% Step V_g	d) $f_{g,e}$ Settling time (ms)	**25.6**	**14.2**	22	0.0	60	55	16	20	30	15
	e) $f_{g,e}$ Overshoot (Hz)	**2.9**	**0.6**	2.9	0.0	2.5	2.5	0.7	0.7	10.0	1.5
	f) $\theta_{g,err}$ Max (°)	**6.5**		3.3	0.0	6.7	6.0	2.0	2.5	5.5	3.5
0.05% Offset	g) $f_{g,e}$ Peak-to-Peak (Hz)	**2.6**	**0.3**	3.8	8.7	1.1	1.2	0.9	0.0	1.5	0.0
	h) $\theta_{g,err}$ Peak-to-Peak (°)	**3.0**		1.7	1.5	1.8	1.9	0.0	0.0	3.8	1.2
90° Step θ_g	i) $f_{g,es}$ Settling time (ms)	**76.0**	**60.0**	40	40	81	70	82	71	104	105
	j) $f_{g,es}$ Overshoot (Hz)	**18.5**	**8.0**	17.0	17.0	18.9	22.0	18.9	12.4	16.6	17.1
	k) $\theta_{g,err}$ Max (°)	**28.6**		16.2	16.0	37.0	25.0	40.5	10.8	17.8	28.8
Harmonics	l) $f_{g,e}$ Peak-to-Peak (Hz)	**1.0**	**0.0**	3.8	8.7	1.1	1.2	0.9	0.0	1.5	0.0
	m) $\theta_{g,err}$ Peak-to-Peak (°)	**0.5**		0.8	2.2	0.4	0.4	0.3	0.0	0.6	0.0

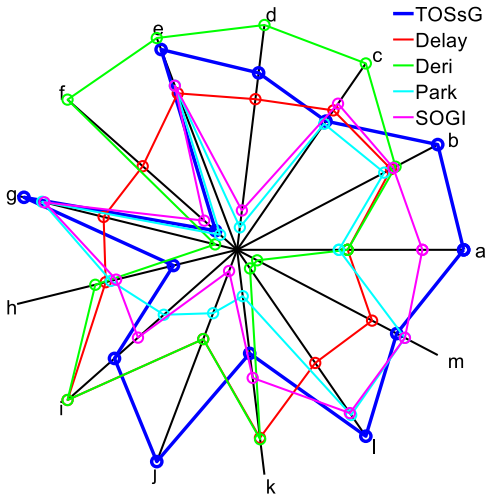

FIGURE 22. Performance comparison of TOSsG, Delay, Deri, Park and SOGI.

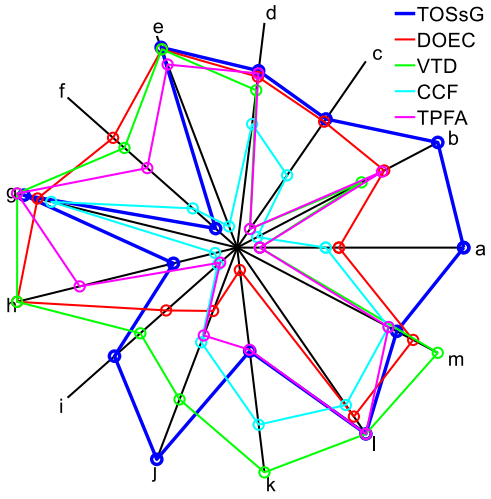

FIGURE 23. Performance comparison of TOSsG, DOEC, VTD, CCF and TPFA.

reported in Fig. 21. While the harmonics are enabled both $f_{g,es}$ and $f_{g,es,ro}$ have a steady oscillation with an amplitude of about 1 Hz and 0.05 Hz, respectively. At harmonics appearing and disappearing there is a little overshoot in $f_{g,es,ro}$ that reaches 0.13 Hz. The same behavior can be recognized also in $\theta_{g,es}$, with a steady oscillation of about 0.5° and an overshoot of 1.2°.

The outcomes relevant to the frequency and phase estimates of the above described experiments are summarized in the first two columns of Table 3, which report the results relevant to $f_{g,es}$ and $f_{g,es,ro}$, respectively. The other columns are filled with the data coming from [21] and relevant to the results obtained from different types of PLLs subjected to the same five solicitations considered in this paper.

VIII. DISCUSSION

Analysis of Table 3 shows that the proposed OSG-PLL pair is in the average comparable if not superior to other solutions found in the literature. Considering separately the outcomes of five experiments, the following considerations can be drawn.

- Frequency step: the frequency estimate $f_{g,es}$ has the smallest overshoot with respect to the other OSG-PLL pairs and $f_{g,es,ro}$ performs more than ten times better than $f_{g,es}$ itself. Only the SOGI PLL gives a settling time lower than that of $f_{g,es}$ but the settling time of $f_{g,es,ro}$ is lowest among all the considered PLLs. Only the derivative OSG (Deri) is sensibly superior to the TOSsG from the point of view of the maximum phase error whereas the Delay, Park, SOGI, and DC offset error compensation (DOEC) OSG-PLL pairs have about the same performance. Instead, variable time delay (VTD), complex coefficients filter (CCF), and three-phase frequency-adaptive (TPFA) OSG-PLL pairs are characterized by higher maximum phase errors.
- Amplitude step: not considering the Deri OSG, which is unaffected by amplitude steps, it can be seen that $f_{g,es}$ has average performance from the point of view of the settling time, being comparable with Delay, VTD, and CCF. On the other hand, it is slower than DOEC and TPFA, and more than two times faster than Park and SOGI. The $f_{g,es,ro}$ estimate, instead, exhibits the shortest settling time if Deri is not considered. The overshoot of $f_{g,es}$ is among the highest and is exceeded only by that relevant to CCF, which has an overshoot more than three times higher. On the contrary, the overshoot of $f_{g,es,ro}$ is the lowest among all the considered OSG-PLL pairs but Deri. The phase estimate has a maximum error that lies among the highest, being comparable with that of SOGI and a little smaller than that of Park.
- Offset: when the offset is applied or removed from v_g, the peak-to-peak error of the frequency estimate $f_{g,es}$ falls in the middle between those of Delay and Deri OSG-PLL pairs, which perform worse, and those of the other pairs, which perform better. Instead, the peak-to-peak error of $f_{g,es,ro}$ exceeds only those of VTD and TPFA while is more than three times smaller than the peak-to-peak error of Park, which is the third-best from this point of view, and nearly 30 times smaller than the error of Deri, which is the worst. The performance of the phase estimation is rather poor being the peak-to-peak error from two to three times higher than the average of the other OSG-PLL pairs and slightly lower than the error relevant to CCF, which is the maximum.
- Phase step: both the settling times of $f_{g,es}$ and $f_{g,es,ro}$ after the application of a phase step are in the average, with the difference that $f_{g,es}$ settles more slowly than SOGI and VTD while $f_{g,es,ro}$ settles more quickly than them. The overshoot of $f_{g,es}$ is in the average and a little smaller than that of Park and DOEC whereas the overshoot of $f_{g,es,ro}$ is the minimum among all the considered OSG-PLL pairs. The corresponding maximum phase error is in the average and is comparable with that of SOGI and TPFA.

- Harmonics: in presence of harmonics the peak-to-peak error of $f_{g,es}$ is in the average, comparable with those of Park and DOEC and a little smaller than those of SOGI and CCF. Also in this case, $f_{g,es,ro}$ performs better than $f_{g,es}$ and its peak-to-peak error is comparable with that of the best OSG-PLL pairs. The peak-to-peak phase error is in the average and falls between those of Park, SOGI and DOEC, which perform a little better, and those of Delay and CCF, which perform a little worse.

The spider charts of Figs. 22 and 23 summarize the comments reported above. In each chart the performance of TOSsG relevant to $f_{g,es,ro}$ and $\theta_{g,err}$ are compared with those of other four OSG-PLL pairs specified in the legend. The axes of the charts, labeled with the letters from 'a' to 'm' in correspondence with the rows of Table 3, are linearly scaled so that the best performance reaches the position furthest from the origin while the worst is at one tenth of this distance.

IX. CONCLUSION

The paper presented a proposal to enhance the performance of the single-phase PLL algorithms. It deals with the generation of the orthogonal signal needed to actually perform the phase estimate. The proposal has been described in details and implemented in the firmware of a DSC considering the issues related to the limited memory and the resolution available to represent the different quantities manipulated by the PLL algorithm. The experimental results obtained processing a signal subjected to steps of frequency, phase, magnitude, offset, and harmonic content confirm that the proposed algorithm performs as expected and that, in comparison with other kinds of PLLs, it offers a good estimate of the input signal angular frequency and phase with low sensitivity to the different disturbances superimposed to the input signal.

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