A Three-Level Single Stage A-Source Inverter With the Ability to Generate Active Voltage Vector During Shoot-Through State

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ABSTRACT Single-stage boosting capability of impedance network (IN) inverters makes this family of inverters an attractive choice for DC/AC applications with low input DC voltage. A specific time of shoot-through (ST) state is required to achieve the required voltage gain. Conventionally ST state and zero output voltage vector should be applied simultaneously. This constraint limits the modulation index and increases the voltage stress of the semiconductor devices, particularly for applications requiring a high boosting factor. In this paper, as the boosting stage for a three-level inverter, a new modified configuration of A-source IN with two series outputs is proposed and connected to a 10-switches three-level inverter. Besides generating two outputs by a single IN, the proposed DC/AC inverter is able to apply an active voltage vector during the ST state. This capability improves the DC/AC voltage gain, increases the modulation index, and decreases the required ST time. The operation principles are described, and the steady-state relations are derived. It is compared with other magnetically coupled INs in terms of boost factor and voltage stress of switches. Considering the 10-switches three-level inverter as the front-end inverter, an adopted maximum boost strategy using the space vector modulation is developed targeting minimum ST time. Finally, a laboratory prototype of the converter is developed, and several tests are carried out. The results validate the given theories and simulations.

INDEX TERMS Impedance source network, A-Source impedance network, multi-level inverter, maximum boost space vector, PWM.

I. INTRODUCTION

As renewable energy is getting more sustainable and viable, a more substantial movement is underway to reduce the dependency on the depleting fossil fuels over the last few decades [1], [2]. One of the primary renewable sources is solar energy led by photovoltaic (PV), which is overgrowing due to its prominent advantages such as flexibility, minimal maintenance required, and easy installation either in small or large scales [3], [4]. Considering the limitations and challenges of the stand-alone operation or grid integration of these power sources, many research works are conducted to improve the required power electronic interface regarding

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boosting capability, the number of elements, efficiency, and power quality [5]–[7].

Conventional 2-level and multi-level voltage source converters (VSCs) are buck converters [8], so normally a dc/dc converter is used as a voltage booster between PV and VSC. Alternative topologies such as switched-capacitor (SC) topologies with boosting feature is another solution, wherein capacitors are charged and discharged in parallel and series configurations with dc input source [9], [10]. In parallel, impedance source converters have gathered much attention [11] for voltage boosting because of several advantages such as:

- Single-stage operation
- A fewer number of active switches
- High voltage gain

- Improved reliability due to short circuit immunity

In total, the impedance source converters are more reliable than VSI and SC topologies since they are not vulnerable to short-circuit in the DC link. Several impedance networks (IN) such as Z-Source [12], [13], T-Source, Quasi T-Source [14], [15], Y-Source, Quasi Y-Source [16], [17], and A-Source [18] networks have been introduced in the literature and reviewed in [11], [15]. Studying the configurations demonstrates that the magnetically coupled INs (MCIN) such as Y-source, coupled Trans Z-source, ΓZ-source [19], and A-source are appropriate candidates to improve the boost factor. Accordingly, the magnetically coupled inductor used in IN reduces the number of circuit elements, makes the system lightweight, improves power density, and enhances voltage gain and modulation index simultaneously, with a lower DC-link voltage for DC/AC systems. However, leakage inductance is generally a concern in these structures.

A-source IN with autotransformer was suggested in [18] to obtain a higher DC voltage gain. Compared to other MCINs, A-source IN requires a fewer turn ratio (1:1 (N_2/N_1)) to achieve a higher voltage. Moreover, it is a suitable choice for renewable energy applications such as PVs and fuel cells (FC) due to its continuous input current [14], [15], [20].

The combination of inverters and voltage boost elements such as INs have been investigated in several studies and used in many applications such as uninterruptable power supplies (UPS), electric vehicles, and grid-connected PVs [21]–[23]. Some researches are conducted on the connection of INs to the multi-level inverters [24], [25]. In [26], two Z-source INs are connected to a neutral point clamped (NPC) inverter, which requires two isolated DC input power sources. Owing to the discontinuous input current of the proposed topology in [26], an alternate topology containing two quasi-Z-source networks and two DC-link capacitors is applied [27]. To eliminate these two DC-link capacitors, a new topology, including two quasi-Z-source networks with Space Vector Modulation (SVM) technique, is proposed in [28]. The drawbacks of utilizing two independent INs, such as the excessive number of passive elements and requiring two isolated DC sources, pose a limitation to its application. A three-level Z-source NPC inverter and DC-link cascaded inverters, using a single IN and a single non-isolated DC source has been proposed in [29]. Nevertheless, the low boost factor and tendency to reduce the number of passive elements caused offering alternate INs, such as an NPC inverter with LC switching [30], which has improved the boost factor with two extra switches and a three-level modified Z-source NPC inverter using maximum boost control technique to increase the boost factor is presented [24]. In [31], a hybrid 2/3 level converter has been proposed containing a main three-phase bridge and an auxiliary leg with four switches. The merit of this configuration is in combining the features of two- and three-level converters with fewer semiconductors, which reduces losses and improves the efficiency as well as the reliability of the renewable energy system [32]. This inverter can operate either as a two- or three-level inverter, depending on the requirements. Despite the hybrid 2/3 level converter advantages, the lack of medium vectors compared to NPC can be mentioned as its limitation [33], [34].

This paper goes a step further and proposes a new modified A-source IN with two different output voltage levels, specially designed for multi-level inverters, in this case, the hybrid 2/3 voltage level inverter. The maximum boost control based on space vector pulse width modulation (SVPWM) is employed to control the inverter. The paper is organized as follows: first, the proposed topology is introduced in section II, and the operation principles and control method are investigated. Also, the main relations of the converter, such as voltage gain, voltage stress, shoot-through duty cycle, and modulation index, are formulated. In section IV, a maximum boost control strategy based on SVPWM is proposed and described. A comparison to other magnetically coupled INs in terms of boosting factor and voltage stress is provided in section V. Finally, experimental results are explained in section VII and used to revalidate the theoretical analysis.

II. CONFIGURATIONS, SPECIFICATIONS, AND BASIC OPERATION PRINCIPLES OF THE MODIFIED A-SOURCE

In this section, the modified A-source IN with a single switch as the switching system is described. Connecting to a 10 switch inverter is discussed in section III. As shown in Fig. 1(a), a conventional A-source IN contains an input inductor (L), two capacitors (C_1 and C_2), an autotransformer, a controlled switch, and a diode (D_1). According to the inverter or filter network output voltage requirements, the peak output voltage of A-source IN (V_o) is generated. The boosting factor is written as follows [18]:

$$B = \frac{V_o}{V_{in}} = \frac{1}{(1 - (1 + N)T_{ST}/T)} \quad (1)$$

$$N = \frac{N_1 + N_2}{N_1}, \quad N > 1 \quad (2)$$

where T_{ST}, T, N, N_1, N_2, V_{in}, and B are the shoot-through (ST) time interval, the switching time period, the auto-transformer turns ratio, the primary turns, the secondary turns, the input DC voltage, and the boost factor, respectively.

Fig. 1(b) illustrates the proposed topology configuration besides the conventional A-source IN. The modified structure contains two more elements, which are a capacitor C_3 and a diode D_2. Capacitor C_3 is charged during the ST state and provides the second output. Two individual output voltage levels of the network are represented as V_{O1} and V_{O2}.

In the following, the steady-state operation principles of the converter are described. The steady-state analysis is provided based on the following hypotheses:

- The passive elements are linear, time-invariant, and frequency-independent
- The converter works in continuous conduction mode (CCM)
- The capacitors are large enough to maintain the DC voltages across them with a low switching ripple
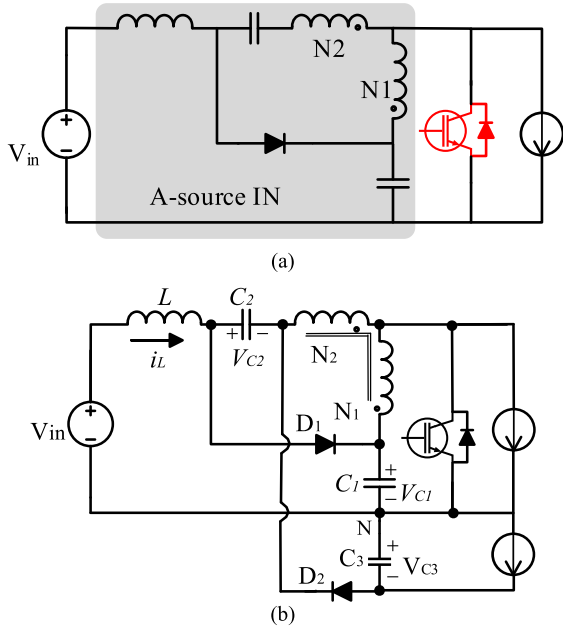
FIGURE 1. Schematic configuration of a single switch A-source IN with a constant current load. (a) conventional structure; (b) the modified structure with two outputs.

FIGURE 2. The proposed A-Source equivalent circuit in modes. (a) Shoot-through state; (b) non-shoot-through state.

- The parasitic elements of the transformer, such as magnetizing inductance, the leakage inductances, the winding resistances, and the stray capacitances, are ignored
- The semiconductor devices are ideal, therefore switching transients and parasitic elements are negligible
- The load impedance can be modelled as a current sink

The two switching states are described in the following.

A. SHOOT-THROUGH (ST) STATE

During this state (Fig. 2(a)), which lasts for $D_{ST}T$ seconds (D_{ST} is the ST duty cycle and T is the switching period), the switch is turned on, and D_2 is forward-biased. The voltage across L is positive; therefore, its current (i_L) increases. The voltage across L_p, V_{Lp} (equals to C_2 voltage V_{C2}) is positive; therefore, V_{xN} is negative and C_3 charges through D_2. The equivalent circuit and current paths in this state are shown in Fig. 2(a). Applying Kirchhoff's voltage law yields the steady-state equations as follows:

$$\begin{cases} V_L = V_{in} + V_{C2} + aV_{C1} \\ V_{LP} = V_{C1} \\ V_{LS} = aV_{LP} = aV_{C1} \end{cases} \tag{3}$$

$$V_{D1} = -V_{C2} - V_{C1}(1+a) \tag{4}$$

$$\left.\begin{cases} V_{O1} = 0 \\ V_{O2} = V_{C3} \\ V_{C3} = aV_{C1} \end{cases}\right\} \Rightarrow V_O = V_{C3} = V_{O1} + V_{O2} \tag{5}$$

where $\alpha = N_2/N_1$ and N_1 and N_2 are the primary and secondary winding turns of the transformer, respectively.
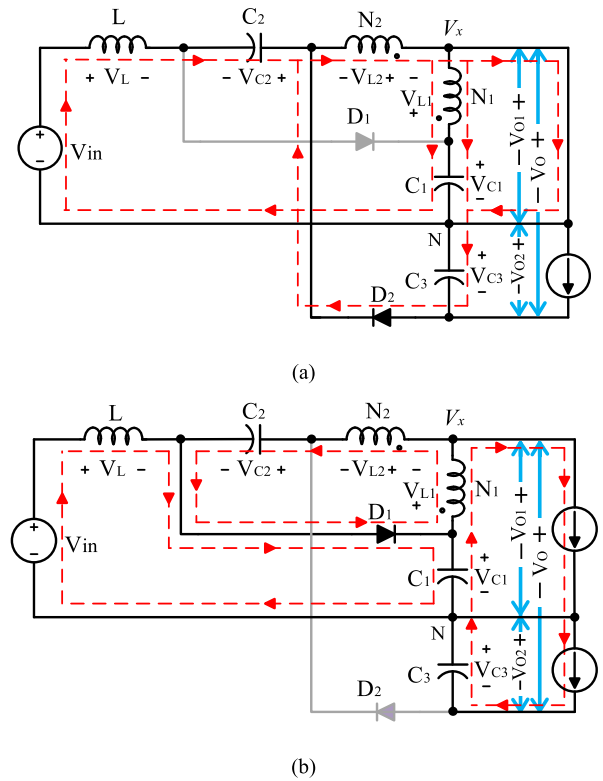
B. NON-SHOOT-THROUGH (NST) STATE

During this state, which lasts for $(1-D_{st})T$ seconds, D_1 is forward-biased, and D_2 is reversed-biased. The stored energy in C_3 and L is delivered to the load. As a result, the network's output voltage is increased during the NST, while the stored energy in passive elements is gradually decreased. The equivalent circuit and current paths are shown in Fig. 2(b). The main equations in this state are as follows:

$$\begin{cases} V_L = V_{in} - V_{C1} \\ V_{LS} = -NV_{C2} \\ V_{LP} = V_{Lm} = aV_{LS} = -NaV_{C2} \end{cases} \tag{6}$$

$$V_{D2} = -V_{C1} - V_{C2} - V_{C3} \tag{7}$$

$$\left.\begin{matrix} V_{O1} = V_{C1} - V_{L1} \\ V_{O2} = V_{C3} \end{matrix}\right\} \Rightarrow \begin{cases} V_O = V_{O1} + V_{O2} \\ V_O = V_{C3} + V_{C1} - V_{LP} \end{cases} \tag{8}$$

Considering the IN circuit in ST and NST states, the main waveforms extracted, which are shown in Fig. 3.

Applying the inductor volt-second and capacitor charge balance principles, averaged values of the inductor current, capacitor voltages, and output voltages obtained:

$$I_L = \frac{V_{in}(D_{ST} - 1)N_1}{R((2+a)D_{ST} - 1)((2D_{ST} - 2 + a)D_{ST} + 1)} \tag{9}$$

$$V_{C1} = \frac{1 - D_{ST}}{1 - (2+a)D_{ST}} V_{in} \tag{10}$$

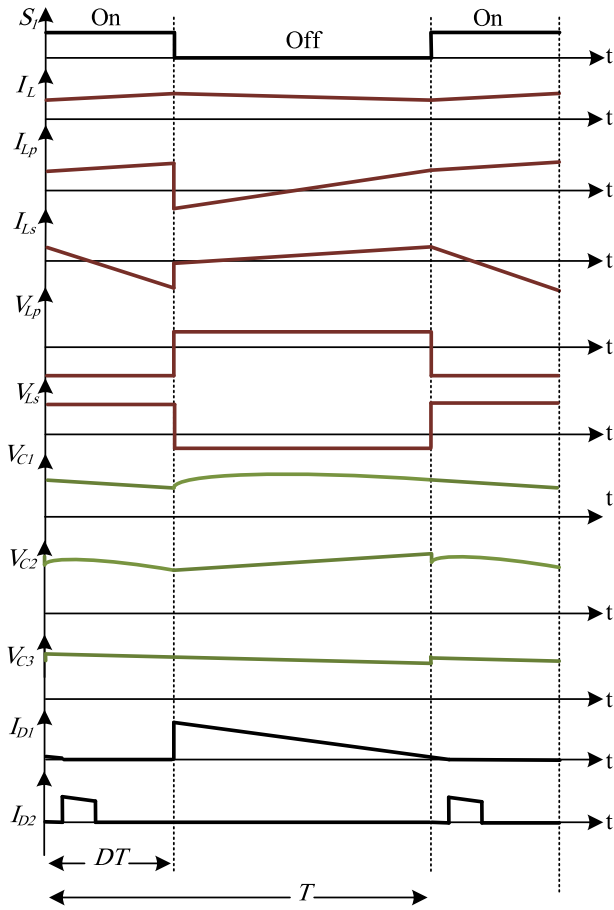$$V_{C2} = \frac{(1+a)D_{ST}}{1 - (2+a)D_{ST}} V_{in} \tag{11}$$

FIGURE 3. Key waveforms of the modified A-Source structure.

FIGURE 4. Schematic configuration of the proposed three Level A-source network connected to a hybrid 2/3 Level Inverter.

TABLE 1. Leg switching states.

switching state	S_1	S_2	S_3	S_4	V_O
L	on	off	off	on	$V_{o1} + V_{o2}$
P	on	off	on	off	V_{o1}
N	off	on	off	on	V_{o2}
Z=0	off	on	on	off	0
STN=0	on	on	off	on	V_{o2}

TABLE 2. The three-phase bridge switching states.

switching state	$S_1(a,b,c)$	$S_2(a,b,c)$
A	on	off
B	off	on

$$V_{C3} = \frac{a(1 - D_{ST})}{1 - (2 + a)D_{st}} V_{in} \qquad (12)$$

$$\left. \begin{array}{l} V_{O1} = \dfrac{V_{in}}{1 - (2 + a)D_{ST}} \\[2mm] V_{O2} = V_{C3} = \dfrac{a(1 - D_{ST})V_{in}}{1 - (2 + a)D_{ST}} \end{array} \right\}$$

$$V_O = V_{in} \frac{(1 + [1 - D_{ST}]a)}{1 - (2 + a)D_{ST}} \qquad (13)$$

Using (13) the boost factor (B) can be expressed as:

$$B = \frac{\hat{V}_o}{V_{in}} = \frac{1 + a(1 - D_{ST})}{1 - (2 + a)D_{ST}} \qquad (14)$$

In the proposed network, the output DC-link average can be achieved in both ST and NST states as follows:

$$\begin{cases} <V_O> = \hat{V}_{O2}D_{ST} + \hat{V}_O(1 - D_{ST}) \\[2mm] <V_O> = \dfrac{V_{in}((1 - D_{ST})(1 + a))}{1 - (2 + a)D_{ST}} \end{cases} \qquad (15)$$

III. MODIFIED A-SOURCE THREE-LEVEL INVERTER

The next step to develop the three-level DC/AC system is connecting an inverter to the IN. Therefore the three-phase hybrid 2/3 level inverter is connected to the two series output of t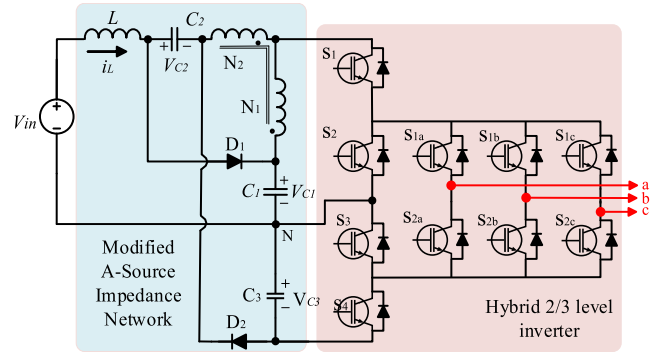he modified A-source IN (Fig. 4). A reduced number of semiconductor devices is the main merit of this inverter, which makes it a proper choice for low-power, low-voltage applications.

In the following, the switching modulation strategy of the inverter is described. For IN-based Inverters, providing maximum boost with the minimum modulation index is the goal. Due to the SVPWM control method's several advantages, such as less switching number, easier digital implementation, and wider linear operation range [35], a combination of SVPWM and maximum boost technique is investigated to control the converter's switching. Generating higher possible output voltage with lower voltage stress across the switches is the main criterion for determining the vector number and applying the time interval.

The three-phase hybrid 2/3 level inverter has 40 switching states, including 24 active and 16 zero states. Generally, the magnitude of V_{O1} and V_{O2} may have different values; therefore, the vectors can be classified into four groups:

- Long vectors: V_1 to V_6 with the length of $(2/3)V_O$
- Medium vectors: V_7 to V_{12} with the length of $(2/3)V_{O1}$
- Small vectors: V_{13} to V_{24} with the length of $(2/3)V_{O2}$
- Zero vectors: V_{25} to V_{40} with the length of zero

The switching states that generate these vectors are easy to extract and not mentioned here for brevity. The space vectors diagram is plotted in Fig. 5.
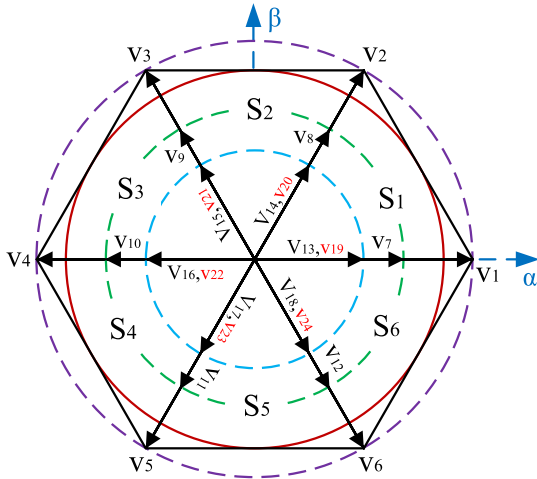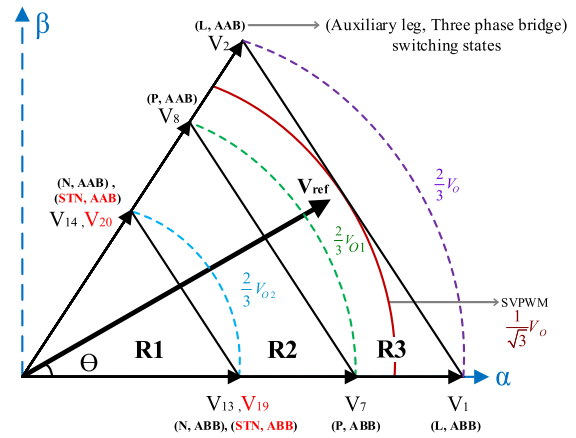
FIGURE 5. Three-level A-source space vectors diagram.

FIGURE 6. Space vector diagram of Sector 1 for the proposed A-source impedance network connected to the hybrid 2/3 level inverter.

IV. SVPWM-BASED MAXIMUM BOOST CONTROL STRATEGY

The inverter's optimized operation is guaranteed if the minimum value of V_O (V_{Omin}) is generated to produce the required output voltage (it causes minimum voltage stress on the semiconductor devices and passive elements, and consequently, reduces the switching power loss). In the conventional IN-based inverters, a zero voltage vector should be applied during the ST interval. Therefore the magnitude of the output voltage is limited to the generated voltage during the NST states. Consequently, higher V_O is required, which means higher D_{ST} and voltage stress. In the proposed inverter, an active vector (small vector) can be applied during the ST. For this purpose, S_1 and S_2 should be ON (shoot-through operation), and S_3 and S_4 should be OFF and ON, respectively (providing a small active vector). To achieve the maximum output (to achieve V_{Omin} for a specified output), a small active vector (V_{13} to V_{24}) should be applied during the entire ST interval. The vector number depends on the instantaneous sector of the reference voltage (V_{ref}).

The space vector diagram is divided into six sectors (S_1 to S_6), where each sector includes three regions ($R1$, $R2$, and $R3$) (see Fig. 6 for sector 1). While V_{ref} is in sector 1, the voltage vector implementation is described here, and it can be easily extended to other sectors. If the operating conditions are adjusted to achieve V_{Omin}, it is easy to understand that V_{ref} would be in R3. In sector 1, V_1 and V_2 as the NST vectors and V_{19} and V_{20} as the ST vectors would be implemented to generate V_{ref}. No zero vectors are applied, so the ST state is provided by implementing small-type active vectors V_{19} and V_{20}. The vectors' time intervals can be calculated using the fundamental relations for SVM [36]:

$$\overrightarrow{V_{ref}} = \frac{T_1}{T}\overrightarrow{V_1} + \frac{T_2}{T}\overrightarrow{V_2} + \frac{T_{19}}{T}\overrightarrow{V_{19}} + \frac{T_{20}}{T}\overrightarrow{V_{20}} \quad (16)$$

$$T = T_1 + T_2 + T_{19} + T_{20}, \ T_{ST} = T_{19} + T_{20} \quad (17)$$

where T_1, T_2, T_{19}, and T_{20} are the time intervals for implementing V_1, V_2, V_{19}, and V_{20}, respectively. T_{ST} is the time interval of the ST state.

Separating the direct and quadrature components of (16)results in:

$$V_{ref}\begin{bmatrix} \cos(\omega t) \\ \sin(\omega t) \end{bmatrix} T$$

$$= V_1\begin{bmatrix} \cos(0) \\ \sin(0) \end{bmatrix} T_1 + V_2\begin{bmatrix} \cos\left(\frac{\pi}{3}\right) \\ \sin\left(\frac{\pi}{3}\right) \end{bmatrix} T_2$$

$$+ V_{19}\begin{bmatrix} \cos(0) \\ \sin(0) \end{bmatrix} T_{19} + V_{20}\begin{bmatrix} \cos\left(\frac{\pi}{3}\right) \\ \sin\left(\frac{\pi}{3}\right) \end{bmatrix} T_{20} \quad (18)$$

where $\theta = \omega t$ is the instantaneous angle of V_{ref}, $\omega = 2\pi f$, and f is the frequency of the output AC voltage. Considering $V_1 = V_2$, $V_{19} = V_{20}$, and using Thales theorem, another relation between vectors' time intervals can be written as (19).

$$\frac{T_1}{T_2} = \frac{T_{19}}{T_{20}} \Rightarrow T_1 \times T_{20} = T_2 \times T_{19} \quad (19)$$

Furthermore, the relation between the output voltage and the modulation index (m) is as follows:

$$m = \sqrt{3}V_{ref}/V_O \quad (20)$$

$$V_O = V_{O1} + |V_{O2}| = V_{O1} + V_O\left(\frac{a(1-d_{ST})}{1+a(1-d_{ST})}\right) \quad (21)$$

Using (17)-(22), the time intervals are calculated as follows:

$$T_1(\theta) = \frac{1}{2}\frac{\left(2\sqrt{3}\,kk_\alpha + 4mk_\beta^2 - 2k_\beta k - 3m\right)T}{(k-1)\left(\sqrt{3}\,k_\alpha + k_\beta\right)} \quad (22)$$

$$T_2(\theta) = \frac{k_\beta\left((\sqrt{3}\,k_\alpha + k_\beta)m - 2k\right)T}{(1-k)(k_\beta + \sqrt{3}\,k_\alpha)} \quad (23)$$
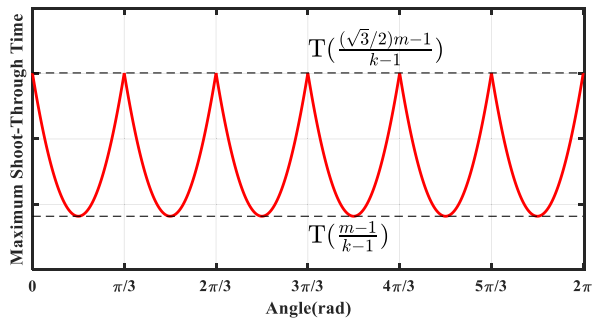
FIGURE 7. The maximum ST time interval for different reference voltage angles of θ.

FIGURE 8. Variation of the maximum boost voltage gain versus modulation index of the proposed IN connected to the hybrid 2/3 level inverter with different turn ratios.

$$T_{19}(\theta) = \frac{\left(4mk_\beta^2 + 2\sqrt{3}\,k_\alpha - 3m - 2k_\beta\right)T}{2\left(1-k\right)\left(\sqrt{3}\,k_\alpha + k_\beta\right)} \quad (24)$$

$$T_{20}(\theta) = \frac{k_\beta\left(\sqrt{3}\,mk_\alpha + mk_\beta - 2\right)T}{(1-k)(k_\beta + \sqrt{3}\,k_\alpha)} \quad (25)$$

$$T_{ST}(\theta) = \frac{\begin{cases} Tk_\alpha\left(m - 4/(3k_\beta)\right)\sqrt{3} + \\ 3T\left(8k_\beta k_\alpha^2 m + mk_\beta - 4\left(k_\alpha\right)^2 - 2\right) \end{cases}}{4\left(k-1\right)\left(\sqrt{3}\,k_\beta k_\alpha + k_\alpha^2 + 1/2\right)} \quad (26)$$

where

$$k = \frac{a(1 - d_{ST})}{1 + a - d_{ST}\,a} \quad (27)$$

$$k_\alpha = \cos(\theta) \quad (28)$$

$$k_\beta = \sin(\theta) \quad (29)$$

Fig. 7 illustrates the dependency of T_{ST} to the angle of θ. As it can be seen, the maximum values of T_{ST} are happened at $\theta = n\pi/3$, while the minimum values acquire at $\theta = n\pi/6$. Due to the dependency of the voltage boost on the T_{ST} and according to the varying nature of the duty cycle due to the dependence on θ, the capacitor voltages and the inductor current contains low-frequency ripples, which are inversely proportional to the switching frequency, meaning that a bulkier inductor is required to reduce the significant current ripple when operating in low frequencies. Therefore, if a constant ST interval is desired, the minimum ST time interval should be used, as shown in Fig. 7. In other words, this method is called the maximum constant boost technique, which has a lower maximum output voltage compared with the intermittent ST time interval.

Vectors' time intervals are calculated likewise for all other sectors. Because the variations of the T_{ST} for all sectors are similar to that of sector 1, the averaged value of the T_{ST} ($\bar{T}_{ST}$) can be calculated to eliminate the dependency of the T_{ST} to θ.

$$\bar{T}_{ST} = \frac{(3m - \pi)}{\pi(k-1)}T \quad (30)$$

Considering (27), the boost factor and the voltage gain of the proposed inverter can be calculated as follows and plotted
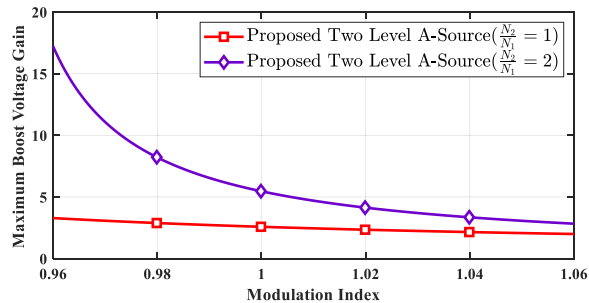
in Fig. 8 for different modulation indexes.

$$\begin{aligned} \text{B} &= \frac{1 + a(1 - T_{ST}/T)}{1 - (2+a)T_{ST}/T} \\ &= \frac{\pi(a+1)}{(3m-\pi)a^2 + (6m-2\pi)a + 6m - \pi} \end{aligned} \quad (31)$$

$$G = B \times m = \frac{m\pi(a+1)}{(3m-\pi)a^2 + (6m-2\pi)a + 6m - \pi} \quad (32)$$

Accordingly, employing the maximum boost control method for the proposed network leads to voltage-boost even at the unity modulation index. As mentioned before, this is achieved because of the capability of the proposed inverter to provide an active vector during ST state. One of the consequent advantages of the inverter is reducing voltage stress. Due to employing the maximum boost control method, to derive the stress voltage across the three-phase bridge switches and the auxiliary leg, separate investigations must be used, which are represented in (33), (34), and (35), respectively.

$$V_{STRESS} = BV_{in} \quad (33)$$

$$V_{STRESS(SW1,SW2)} = B_1 V_{in} \quad (34)$$

$$V_{STRESS(SW3,SW4)} = B_2 V_{in} \quad (35)$$

V. COMPARISON WITH OTHER TOPOLOGIES

Achieving a higher boost factor with fewer turn ratios at lower duty cycles in magnetically coupled INs is desirable, which is a key feature of the proposed structure. Fig. 9 illustrates a comparison between the proposed IN and other magnetically coupled IN topologies in terms of the boost factor.

As illustrated, the modified A-Source IN has a higher boost factor for D_{ST} higher than 0.2. Although TZ-Source IN shows a higher boost factor, it should be considered that it requires four coupled inductors, which increase the noise, size, and cost of the system. Furthermore, there are limitations to designing some of the magnetically coupled INs, such as choosing the turn ratio. For instance, the turn ratio of ΓZ-source is limited to $1 < N_1/N_2 \leq 2$. The impact of the turn ratio and the ST duty cycle on the proposed network's boost factor is illustrated in Fig. 10.
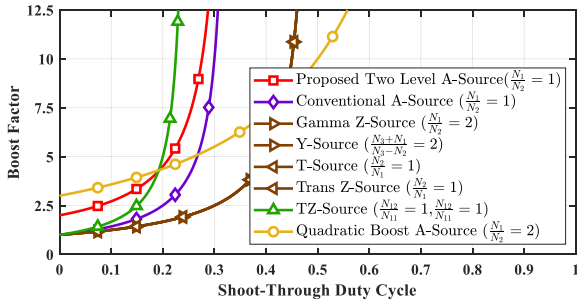
FIGURE 9. Boost factor versus D_{ST} for different magnetically coupled INs.
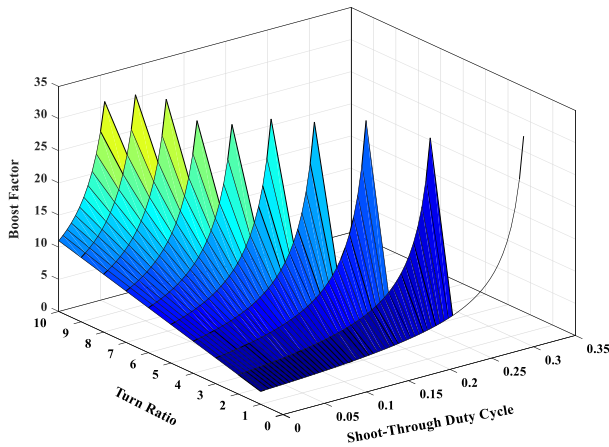

FIGURE 10. Comparison of the proposed network's boost factor in different STs and turn ratios $a = N_2/N_1$.
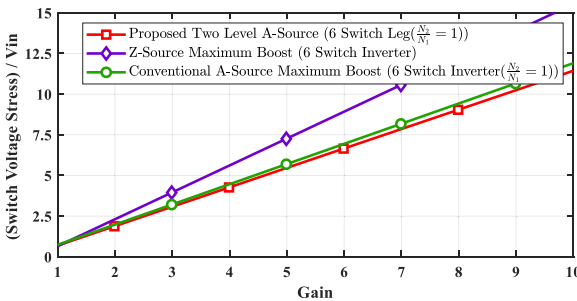

FIGURE 11. Comparison of the normalized voltage stress across switches of the three-phase bridge versus voltage gain.

A comparison between the normalized voltage stress across the switches of the proposed converter and other three different topologies that used the maximum boost control for impedance networks connected to the H-bridge inverter, including the Z-source impedance network connected to the H-bridge inverter [35], [37] represented in Fig. 11. As can be seen, the proposed two-level A-source impedance network has lower voltage stress across the inverter's switches than the other topologies.

According to the two different output voltage levels of the proposed impedance network, the voltage stress across switches of the auxiliary leg is investigated independently for each voltage level. The NPC inverters, which have a
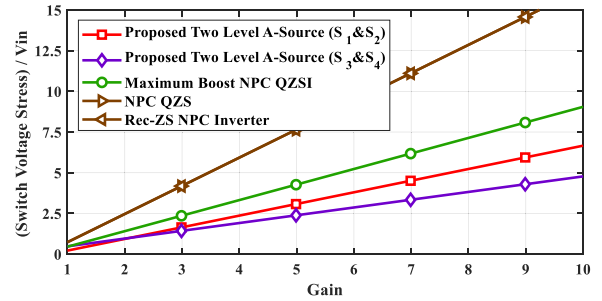
FIGURE 12. Comparison of the normalized voltage stress across switches of the auxiliary leg versus gain.

similar leg to the auxiliary leg of the hybrid 2/3 level inverter, are suitable to be compared with. A comparison of the normalized voltage stress across the switches of the hybrid 2/3 level inverter's auxiliary leg supplied by two impedance networks with the maximum boost control [38], without the maximum boost control [28], and the impedance network in [39] illustrated in Fig. 12. As can be seen, the proposed impedance network has relatively lower voltage stress across the auxiliary leg switches for both output voltage levels than the other topologies.

VI. COMPONENT DESIGN AND EFFICIENCY
A. INDUCTOR DESIGN
Inductor value is determined according to the desired current ripple (Δi_L), inductor's voltage (V_L), switching frequency (f_s), transformer turn ratio (a), and ST duty cycle (D_{ST}).

$$L = \frac{D_{ST}V_{in}}{f_s \Delta I_L}\left(\frac{1 + a - D_{ST}(1 - a)}{1 - (2 + a)D_{ST}}\right) \qquad (36)$$

B. CAPACITOR SELECTION
The capacitor size can be calculated as follows based on voltage ripple (ΔV_C):

$$C_1 = \frac{(I_L - I_{out2})(1 - D_{ST})}{f_s \Delta v_{C1}} \qquad (37)$$

$$C_2 = \frac{I_L D_{ST}}{f_s \Delta v_{C2}} \qquad (38)$$

$$C_3 = \frac{I_{out2}(1 - D_{ST})}{f_s \Delta v_{C3}} \qquad (39)$$

C. VOLTAGE STRESS ACROSS THE SWITCHES AND DIODES
Voltage stress is calculated by considering the off state of the switches and diodes. The voltage stress across switches are presented in (33)-(35). The voltage stresses across D_1 and D_2 are calculated using (40)-(41).

$$V_{D1} = BV_{in}(1 + a) \qquad (40)$$

$$V_{D2} = BV_{in}(D_{ST} - 2 - a) \qquad (41)$$

D. CONVERTER LOSSES AND EFFICIENCY
The converter losses generally include two parts: conduction losses and switching losses. The non-idealities considered
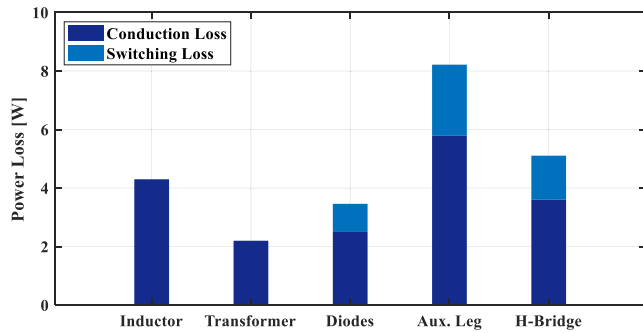
FIGURE 13. Theoretically calculated power losses of the proposed converter.

for conduction losses are the conduction resistance of the inductors (r_L), switch on-state resistance (r_S), and diodes forward voltage (V_f).

$$P_{COND(L)} = R_L I_L^2 \tag{42}$$

$$P_{COND(SW)} = R_{on} I_{sw}^2 \tag{43}$$

$$P_{COND(D)} = V_f I_D \tag{44}$$

The diode reverse recovery phenomenon and switch current and linear voltage variation during switching transients are considered the source of switching losses. MOSFET switching losses ($P_{SW(S)}$) is evaluated based on the dissipated amount of energy (E_{SW}) in the switches during switching transitions [40], [41] and given by (45).

$$E_{SW} = (\alpha_{on} + \alpha_{off})(V_{SW1} I_{SW1} + V_{SW2} I_{SW2}) \tag{45}$$

where,

$$\alpha_{on} = \frac{\left(3t_{fv} - 3t_{fv}t_{ri} + t_{ri}^2\right)}{6}$$
$$\alpha_{off} = 0.5(t_{rv} + t_{fi}) \tag{46}$$

The diodes reverse recovery loss (P_{rr}) is also estimated by (47), where $Q_{rr(D)}$ is the diode recovered charge. $Q_{rr(D)}$ can be calculated using the diode's datasheet.

$$P_{rr} = f_s(Q_{rr(D1)} V_{D1} + Q_{rr(D2)} V_{D2} + Q_{rr(Do)} V_{Do}) \tag{47}$$

The theoretically calculated converter power losses are shown in Fig. 13. The value of the parasitic elements and converter specifications used for efficiency calculations are the same as the prototype specifications used for model validation in section VII. Accordingly, the overall estimated efficiency of the converter is 92%.

VII. EXPERIMENTAL AND SIMULATION VALIDATION
To demonstrate the performance of the proposed converter and validate the theoretical concepts, a laboratory prototype is developed (Fig. 14) with the parameters in TABLE 3. The prototype contains the proposed A-Source IN connected to the 10-switches three-level inverter (Aux. leg+H-Bridge inverter) with a three-phase *RL* load.
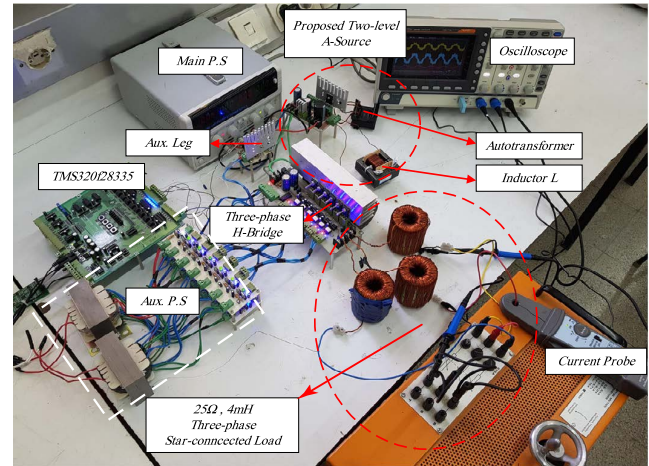

FIGURE 14. Experimental setup for the laboratory prototype.

TABLE 3. Experimental parameters.

Parameter	Symbol	Value	
		Scenario 1	Scenario 2
Output power	P_{out}	300W	
Input voltage	V_{in}	25V	20V
Output line RMS voltage	V_{out}	110V	
Voltage frequency	f	60Hz	
Switching frequency	f_s	10kHz	
Inductive load	R_L, L_L	25Ω, 4mH	
Modulation index	m	0.8985	0.8856
ST duty cycle	D_{ST}	0.2487	0.2673
Inductance	L	1mH	
Inductor resistance	R_L	30mΩ	
Autotransformer turn ratio	N_2/N_1	1	
Primary winding resistance	r_p	15mΩ	
Primary leakage inductance	L_{Lp}	5μH	
Secondary winding resistance	r_s	15mΩ	
Secondary leakage inductance	L_{Ls}	5μH	
Capacitance	C_1, C_3	220μF	
	C_2	470μF	
Diode conduction resistance	R_{d1}, R_{d2}	1mΩ	
Diode forward voltage	V_{f1}, V_{f2}	0.4V	
Switch conduction resistance	R_{on}	18mΩ	

The experimental tests were carried out under two different scenarios of input voltage to evaluate the converter response to different modulation indexes. Therefore, to generate the AC output voltage of 110*V* RMS, the modulation index was determined to be 0.8985 and 0.8856 according to (31)-(32) and the values in TABLE 3. Hence, the total output voltage of the two-level network should be 6.2 and 7.5 times the input voltage.

In the following, the input inductor current waveform is shown in Fig. 15. The input voltages of the 2/3 hybrid inverter,
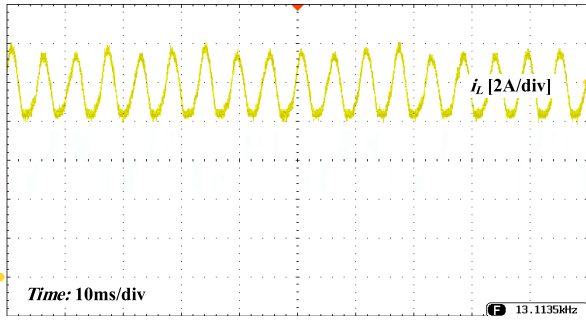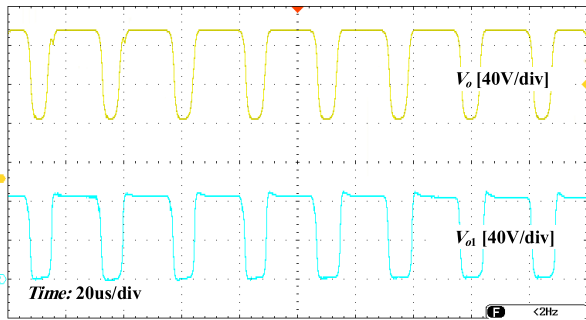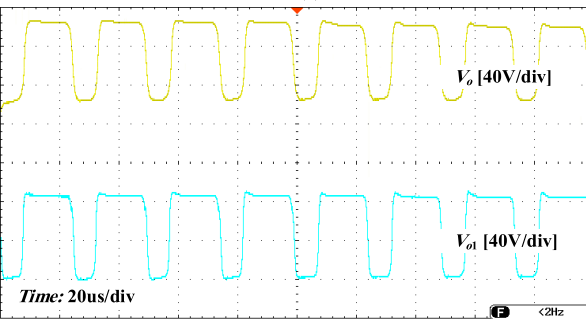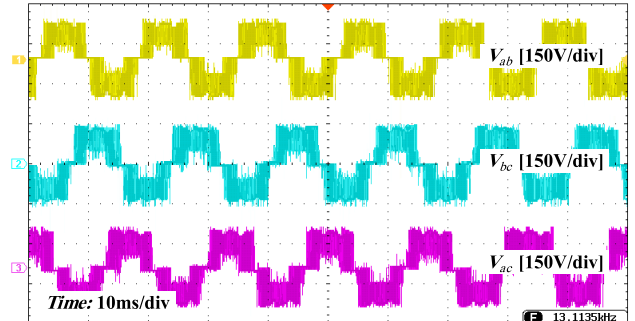
FIGURE 15. Experimental results for inductor current i_L.

FIGURE 16. Experimental results for IN output voltages V_O and V_{O1}: (a) $V_{in} = 25$ V; (b) $V_{in} = 20$ V.

FIGURE 17. Experimental results for inverter output with $V_{in} = 25$ V: (a) three phase PWM output voltage; (b) Up: line-line voltage (V_{ab}), middle: phase-line voltage (V_{aN}); down: phase current (I_{aN}).

FIGURE 18. Experimental results for inverter output with $V_{in} = 20$ V: (a) three phase PWM output voltage; (b) Up: line-line voltage (V_{ab}), middle: phase-line voltage (V_{aN}); down: phase current (I_{aN}).

V_O and V_{O1}, are shown in Fig. 16. According to Fig. 15, the experimental peak value of the two-level network (V_o) is 155V for both cases, which is following (31)-(32). The three-phase output voltage, load current, and load voltage for phase-A are shown in Fig. 17(a) and Fig. 18(a), and the three-phase output voltage in Fig. 17(b) and Fig. 18(b), which emphasizes the correct operation of the inverter with RL load in generating the 110V RMS line voltage with different values of input voltage and modulation indexes. It should be noted that the negligible difference between the theoretical and experimental results is due to the existence of leakage in the transformer and parasitic elements. Finally, efficiency curve of the laboratory prototype is measured and shown in Fig. 19.

Furthermore, simulation are performed under two scenarios of perturbation on the input voltage and duty cycle to validate the given theor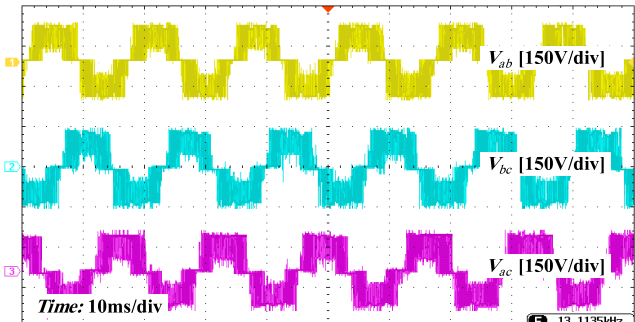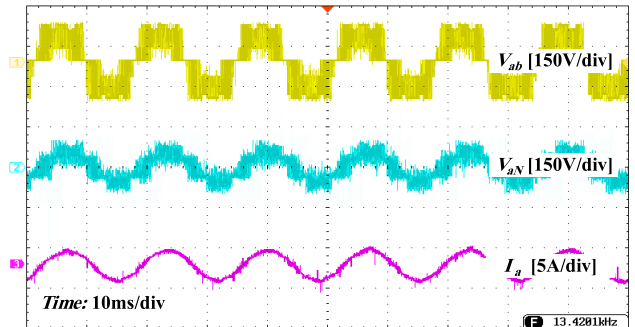ies and especially dynamic behavior of the converter. In the first scenario, shoot-through duty cycle (d_{ST}) increased from 0.89 to 0.9 at 0.08 seconds.
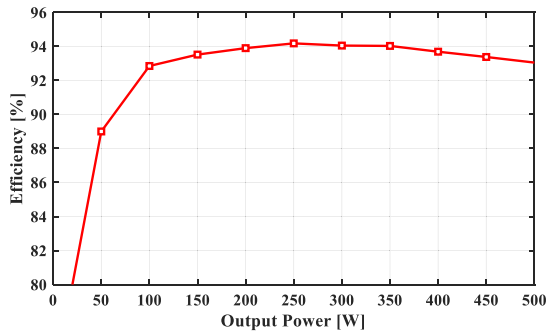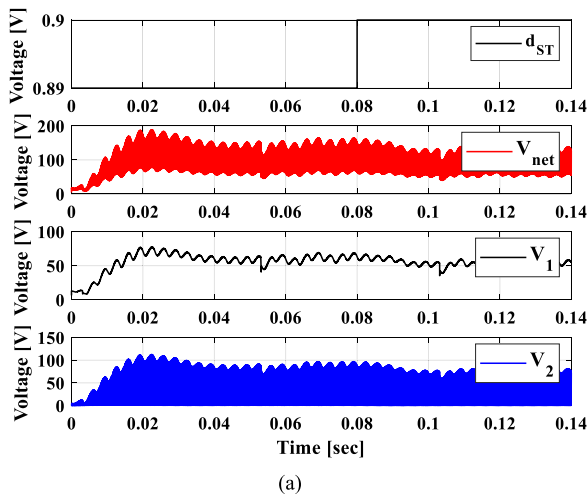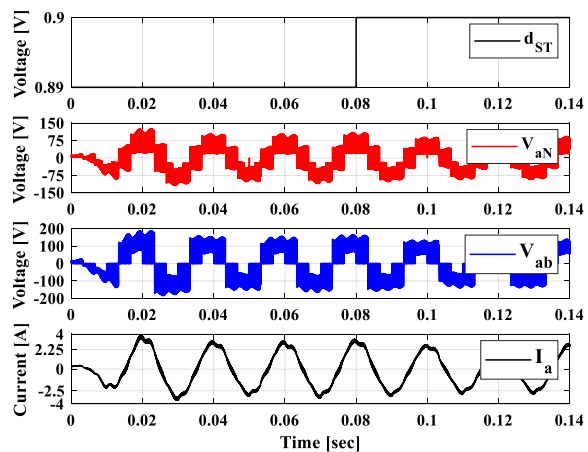
FIGURE 19. Experimental measured efficiency of the laboratory prototype.

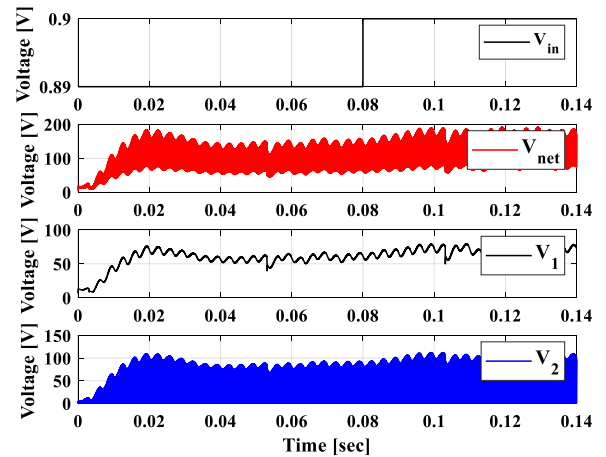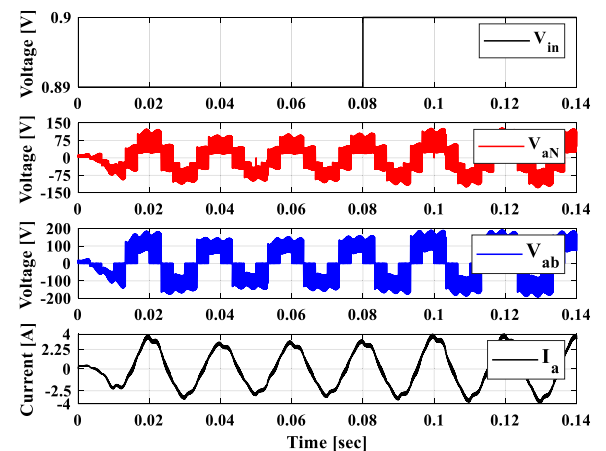**FIGURE 20.** Simulation results for a step in the duty cycle (dST). (a) Output voltages of the impedance network. (b) Output voltages and current of the inverter.

Output results are according to Fig. 20. As expected, output voltages have been increased and their final values are according to theoretical concepts. Furthermore, in the second scenario, input voltage (V_{in}) increased from 25V to 30V at 0.08 seconds. Output results are according to Fig. 21. As expected, output voltages have been decreased and their final values are according to theoretical concepts.

FIGURE 21. Simulation results for a step in the input voltage (V_{in}). (a) Output voltages of the impedance network. (b) Output voltages and current of the inverter.

VIII. CONCLUSION

In this paper, a new three-level A-source impedance network and its connection to a 2/3 hybrid inverter were discussed. The structure's main feature is the capability to apply an active voltage vector during the shoot-through state. This improves the boosting ability and reduces the required DC-link voltage of the inverter. The space vector PWM modulation with the maximum boost strategy was presented, and equations were derived. A comparative study with several topologies was performed in terms of the voltage gain and switches voltage stress, which demonstrated the advantages of the proposed inverter. Finally, the validation of the given theories was provided by experimental results with a laboratory prototype.

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