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A Novel Frequency Locked Loop With Current Harmonic Elimination Method for the Three-Phase Grid-Connected Inverter

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ABSTRACT In order to eliminate the harmonics of the grid connected inverters accurate harmonic detection is essential. Though there are many kinds of different harmonic detection methods are available, it can hardly be achieved without the help of grid frequency detection of the fundamental component. In this paper a novel Lock-In Amplifier based Frequency Locked Loop (LIA-FLL) is proposed for the improved harmonic elimination of the grid-connected three phase inverters. Due to the outstanding performance of the LIA-FLL, the harmonics can be detected and compensated accurately under the grid frequency variation. To demonstrate the superiority of the proposed method, it is applied to a 10 kW three phase grid connected inverters. The results obtained by the proposed method are compared with those obtained by the harmonic elimination method with no FLL. The principle of LIA-FLL is discussed and its performance for the harmonic elimination is proved by the simulation and experiments with a 10KW three phase grid connected inverter under the highly polluted grid condition.

INDEX TERMS Frequency locked loop, lock-in amplifier, harmonic elimination, three-phase grid-connected inverter.

I. INTRODUCTION

In recent years, a large quantity of renewable energy sources appeared in the distributed generations (DGs). Therefore, the use of Grid-Connected Inverters (GCIs) incorporated with the renewable energy sources are increasing at rapid rate to inject the power to the grid. Due to the conversion of power from DC to AC by using Pulse Width Modulation (PWM) technique, the output of the GCI can hardly be purely sinusoidal due to the switching operation of the converter. Hence, the harmonics are also injected to the grid as well as the fundamental component during the operation of GCIs. In particular, GCIs should have low current harmonic distortion to avoid the adverse effects on other equipment connected to the grid. Therefore, Total Harmonic Distortion (THD) of the output current of GCIs must be maintained below 5% at the rated inverter output by the standard such as IEEE P1547 [1].

THD contains the information of all of the harmonics in the GCI's output. It is well known that the output of an inverter may be distorted due to the dead-time effects, the conduction voltage drops across the switches and the extensive use of non-linear loads. The conventional harmonic elimination strategies can be divided into two categories: one is to use the additional elimination circuit [2] and the other is to use the current-harmonic elimination algorithm in parallel with the fundamental current controller [3]. The Active Power Filter (APF) is one of the common solutions that functions as an active conductance to damp out the harmonics from GCI's output [3], [4]. However, the additional hardware increases the power loss as well as the cost of the overall system. Hence, the current harmonic elimination method without the additional hardware is preferred as presented in several researches [5]–[13].

The resonant controller is used to eliminate the harmonics in the DQ frame control [14]. Its performance in terms of harmonic elimination is satisfactory as it is capable of tracking sinusoidal references with zero steady state error [9]. However, this method is very complex to implement since it is required to implement the harmonic controller on D and Q axis, respectively. Typically, the PR based harmonic elimination method is used with a large gain to eliminate the harmonics more accurately [15]. However, the harmonic

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elimination with PR controllers is very sensitive to frequency variation as its performance degrades significantly due to its narrow bandwidth characteristics. The PI controller can also be used to eliminate the harmonic components [16]. However, the method needs as many digital filters as the number of specific harmonics to be eliminated as well as the accurate phase information of the harmonics. The SOGI based harmonic elimination technique is presented to eliminate the harmonics by the dead time in the grid connected inverters [8]. The performance of this method also gets deteriorated when the grid frequency varies due to the attenuation of the filters. Several kinds of low-order harmonic elimination methods are presented in [17]. Since those methods do not adopt any means for the grid frequency tracking in the grid integration mode, the performance of the harmonic elimination gets deteriorated when the grid frequency is not constant. The dual predictive current controller is suggested as the fundamental current controller in [18], [19] and the constant power flow with harmonic rejection capability can be achieved. However, the performance of the control gets deteriorated if the accurate grid frequency information is not provided.

As described above all of the conventional harmonic elimination methods have a limitation is that their performances get deteriorated when the grid frequency varies and the best performance in the harmonic detection and elimination can be obtained only when the grid frequency is constant. To achieve the best performance in harmonic elimination the grid frequency should be measured and applied to the harmonic elimination. Therefore, the detection of the frequency variation is a highly important issue in the harmonic elimination of the GCIs. In order to overcome the frequency variation related issue in the harmonic elimination of the GCI the frequency locked loop (FLL) needs to be introduced and used for the better performance of the harmonic elimination under the grid frequency variation.

A Frequency Adaptive Loop (FAL) was first introduced in [20], where FAL was associated with Synchronous Reference Frame (SRF) based Phase Locked Loop (PLL) to tune the dual SOGI. Researchers also addressed this FAL as a Frequency Locked Loop (FLL) due to its frequency tracking characteristics [20]. The advantage of FLL is that it helps improve the harmonic elimination performance by providing the accurate information of the grid frequency [21]. In addition, the FLL does not contain any Voltage-Controlled Oscillator (VCO) module which makes the system complex and increases the computational burden. The first introduced FLL consists of a notch filter and the adaptive loop [22]. In the previous studies, the notch filter can be divided into two types, Real Coefficient Filter (RCF) and Complex Coefficient Filter (CCF). The RCF based notch filter [22], [23] is employed for the Quadrature Signal Generation (QSG), while the CCF based notch filter can be employed for the positive or negative sequence component extraction [24]. In [25], the author has analyzed several different FLLs and suggested a general theory behind it for the easier understanding of the FLL algorithm. Several CCF structures are mathematically derived in [23], [26] to develop the FLL for the GCIs. In [24], a Reduced Order Resonant controller FLL(ROR-FLL) is proposed, which can accurately and rapidly extract the harmonic components from the polluted grid. However, its quality factor is sensitive to the grid frequency variation. In order to cope with it a Reduced Order Generalized Integrator FLL (ROGI-FLL) is proposed in [23], which can rapidly and accurately extract the frequency and the positive/negative sequence components from the grid signal. However, it is disadvantageous in that its performance get deteriorated when the grid signal has a dc-offset. In [26], a Multiple Adaptive Vectorial Filter FLL (MAVF-FLL) is proposed, which can detect the different harmonic components from the unbalanced and distorted grid voltage. However, the performance of the filter gets deteriorated when the power network is highly distorted or has a dc offset.

It can be concluded from the above review that most of the FLL methods developed so far have major drawbacks such as complexity in implementation and the tuning of the filter. In addition, the low performance of the SOGI based FLL is mainly attributed to the inaccurate extraction of the frequency information and their performances get deteriorated when the grid signal has a dc offset.

A novel harmonic elimination method based on Lock-In Amplifier (LIA) in the stationary reference-frame current controller has been introduced in [29]. The method can detect the harmonics and then feed them into the controller to eliminate the harmonics. However, its performance of the harmonic elimination gets deteriorated when the grid frequency varies since the frequency of the reference signal used in LIA is assumed to be constant at 60Hz.

In this paper, a novel Lock-In Amplifier based FLL (LIA-FLL) is proposed to cope with the performance degradation issue in the harmonic elimination under the grid frequency variation. The working principle of the LIA and its effectiveness have been already presented in the reference [29]. The LIA can extract a certain frequency harmonic component buried under the noisy by using two reference signals as shown in Fig. 1. The Phase Sensitive Detector (PSD) generates the double frequency components of the reference signal superimposed on a DC component. The Low Pass Filter (LPF) is used to eliminate the double frequency components so that only the dc components, which contain the amplitude and phase information of the target frequency component, can be obtained. Then the extracted harmonics are reconstructed and fed into the current controller to eliminate it perfectly. Though the performance of the LIA based harmonic controller is outstanding its performance on the harmonic extraction depends on the quality of the reference signal used. When the frequency of the grid changes it is inevitable that its performance to extract the harmonics gets deteriorated hence the performance of the harmonic compensation. It can be improved by changing the frequency of the reference signal by sensing the frequency variation of the grid in real-time and by varying the frequency of the reference signal. Here, the frequency variation of the grid is

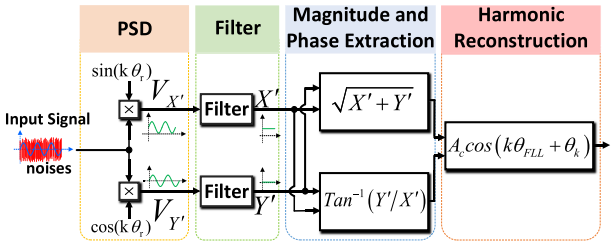

FIGURE 1. Block diagram of lock-in-amplifier.

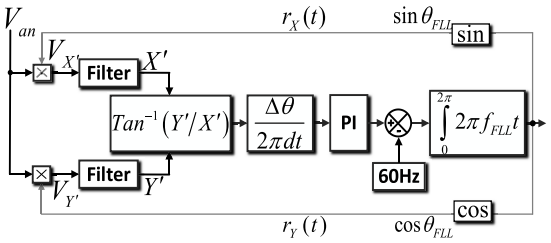

FIGURE 2. Block diagram of the proposed LIA-FLL.

detected by the proposed LIA-FLL method and it is used to change the frequency of the reference signal. Therefore, the harmonic detection by the LIA can be improved and hence the performance on the harmonic compensation can be improved.

The proposed FLL method by using LIA has following advantages as compared to the conventional methods.

I. The proposed LIA-FLL does not require additional hardware.
II. It is immune to the DC offset in the feedback signals.
III. The performance of the frequency tracking by the proposed LIA-FLL is not affected by the harmonics present in the grid.
IV. The frequency variation can be detected fast enough to satisfy the standard such as IEEE P1547.

This paper is organized as follows. Section II describes the principle of the Lock-In Amplifier. The proposed LIA based FLL method is discussed in Section III. Section IV presents the Harmonic Elimination method based on LIA and LIA-FLL. The simulation and experimental results are presented in Section V. Finally, the conclusion is given in Section VI.

II. PROPOSED LOCK-IN-AMPLIFIER BASED FREQUENCY LOCKED LOOP

The block diagram of the Lock-In Amplifier (LIA) is shown in Fig. 1, where, the phase of the reference signal and the order of the harmonic is represented by θ_r and k, respectively. θ_k stands for harmonics phase. The LIA is capable of extracting the amplitude and phase information of a certain component under extremely noisy environments. It employs a homodyne detection scheme and low-pass filtering to measure the amplitude and phase of a certain frequency signal relative to a periodic reference with the same frequency. The LIA extracts signals in a defined frequency band around the reference frequency by efficiently rejecting all other frequency components. The best instruments on the market today have a dynamic reserve of 120 dB [27], which means that they are capable of accurately measuring a signal in the presence of noise up to a million times higher in amplitude than the signal of interest [28].

The main function of the LIA is to get the magnitude and the phase information of a signal of interest by utilizing two reference signals. This information can be achieved by using dual modulation Lock-In strategy, where input signal is separately multiplied to the in-phase reference signal and the quadrature-phase reference signal, respectively. Basically, the Phase Sensitive Detection (PSD) of LIA locks a certain frequency component of the input signal. Each output of the PSD is composed of a DC and a double frequency component of the reference signal. In order to eliminate the double frequency component from the output of PSD Low Pass Filters (LPFs) are required to extract a DC component. The DC component has the information about the amplitude and phase of a signal to be extracted by the LIA, where the output of the PSD with in-phase signal contains the amplitude of the signal and that with quadrature-phase contains the phase of the signal.

A. PROPOSED LIA BASED FLL

In this paper, a novel Lock-In Amplifier based Frequency-Locked Loop (LIA-FLL) is proposed for the detection of the fundamental frequency of the grid under the frequency variation. Though the LIA detects a certain frequency harmonic component with high accuracy its performance depends on the frequency of the reference signal used as mentioned earlier. Therefore, its performance gets deteriorated when the frequency of the input signal varies. In order to maintain the high accuracy in the harmonic detection the frequency of the reference signal should be varied according to the frequency variation of the input signal. Here, the novel LIA based FLL is proposed to track the frequency variation of the fundamental component hence the harmonics, thereby achieving the high accuracy of the harmonic detection and elimination.

The block diagram of the proposed LIA based FLL is shown in Fig. 2. In the proposed LIA-FLL method, the Lock-In amplifier extracts the error in theta between the input signal and the reference signal (60Hz). It is converted into the frequency error by taking its derivative. Then, the frequency error is fed into the PI controller and the result is added to the reference frequency value (60Hz) to produce the new reference frequency value. The new reference theta can be obtained by the integration and used to produce the new reference signal for the PSD in the LIA-FLL.

In the PSD the grid voltage signal is multiplied with the in-phase and quadrature-phase of the reference signal. Each of two outputs of the PSD is composed of a DC component and a double frequency component of the reference frequency as will be explained in this section later. In order to get the

pure DC component, the double frequency component needs to be filtered out. Here, a 2nd order Notch-filter combined with a 1st order low-pass filter is used. Though the magnitude and the phase of input signal (Grid-voltage) can be calculated with the extracted DC signals only the phase information is used to implement the FLL.

In order to describe the principle of the LIA-FLL in Fig. 2 following equations are used.

$$V_{an}(t) = V_m sin(2\pi f_{an} t + \theta_{an}) \quad (1)$$

$$r_X(t) = sin(2\pi f_{FLL} t + \theta_{FLL}) \quad (2)$$

$$r_Y(t) = cos(2\pi f_{FLL} t + \theta_{FLL}) \quad (3)$$

where, V_{an} is the phase voltage with its amplitude V_m, f_{an} is the frequency of the phase voltage and θ_{an} is the phase of V_{an} with respect to the reference signal, respectively. θ_{FLL} represents the angle of the grid fundamental and f_{FLL} represents the frequency of the reference signal. $r_{X(t)}$ and $r_{Y(t)}$ are the reference signals to be multiplied to the phase voltage which are displaced by 90 degrees each other. When two reference signals are multiplied to the phase voltage the resulting signals can be represented by Eq. (4) and Eq. (5) using simple trigonometric identity.

$$V_{X'} = \frac{V_m}{2}\left[\begin{array}{c}\overbrace{cos\{2\pi(f_{an}-f_{FLL})t+(\theta_{an}-\theta_{FLL})\}}^{\text{'}DC\text{' Term}} \\ \underbrace{-cos\{2\pi(f_{an}+f_{FLL})t+(\theta_{an}+\theta_{FLL})\}}_{\text{'}2f\text{' Term}}\end{array}\right] \quad (4)$$

$$V_{Y'} = \frac{V_m}{2}\left[\begin{array}{c}\overbrace{sin\{2\pi(f_{an}-f_{FLL})t+(\theta_{an}-\theta_{FLL})\}}^{\text{'}DC\text{' Term}} \\ \underbrace{+sin\{2\pi(f_{an}+f_{FLL})t+(\theta_{an}+\theta_{FLL})\}}_{\text{'}2f\text{' Term}}\end{array}\right] \quad (5)$$

As mentioned earlier the outputs of the PSD is composed of a DC component and a double frequency component of the reference signal. In order to eliminate the double frequency component from the output of the PSD, the combined filter shown in Fig. 3 is employed.

Since the grid frequency in this paper is 60Hz the double frequency component at the output of the PSD is 120Hz ripple. Fig. 4. shows the outputs of the PSD and their FFT results.

In order to get the magnitude of 60Hz component, a combined 2nd order notch-filter with a 1st order Low-pass filter is employed in the proposed method. Then main function of this filter is to eliminate the 120Hz ripple from the PSD output.

Transfer function of the combined 3rd order filter ($H_{CF}(s)$) can be expressed as follows.

$$H_{CF}(s) = \left[\frac{s^2+2\zeta_2 w_n s+w_n^2}{s^2+2\zeta_1 w_n s+w_n^2}\right] \times \left[\frac{w_c}{s+w_c}\right] \quad (6)$$

where, w_n is the natural frequency of the notch-filter and the cut-off frequency for the low-pass filter is w_c. In the notch filter tuning, the damping factor ζ_2 must be smaller than ζ_1 ($\zeta_2 \ll \zeta_1$) and w_n is 120Hz. The cut-off frequency of the low-pass filter is selected at 20Hz to attenuate the high order frequency components.

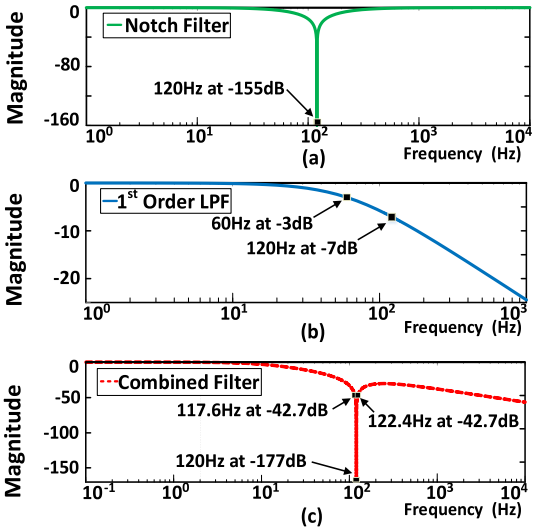

FIGURE 3. Bode plot of the combined 3rd order filter.

Fig. 3 shows the bode plot of the combined 3rd order filter used to filter out the 120Hz and low frequency components. The filter shows −177dB gain at 120Hz, which is enough to effectively attenuate the 120Hz ripple component when the grid frequency is 60Hz.

Then the outputs of the combined filter can be expressed as follows.

$$X' = \frac{V_m}{2}[cos\{2\pi(f_{an}-f_{FLL})t+(\theta_{an}-\theta_{FLL})\}] \quad (7)$$

$$Y' = \frac{V_m}{2}[sin\{2\pi(f_{an}-f_{FLL})t+(\theta_{an}-\theta_{FLL})\}] \quad (8)$$

Eq. (7) and Eq. (8) show the output of the combined filter, where the double frequency component is removed and only the DC component remains. Then the phase difference $\Delta\theta_{FLL}$ in between the reference signal and the fundamental component of the input signal can be extracted by the

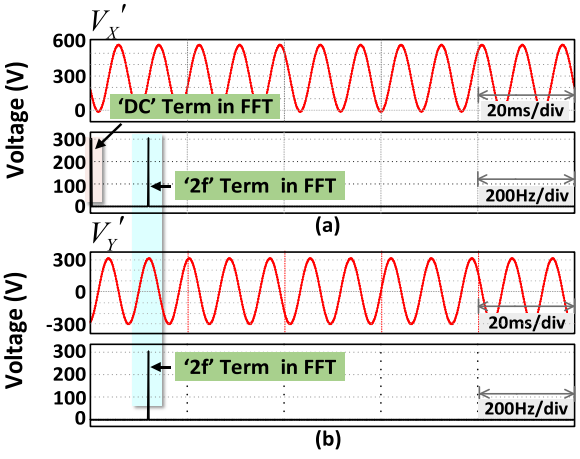

FIGURE 4. Outputs of PSD and their FFT results by PSIM simulation.

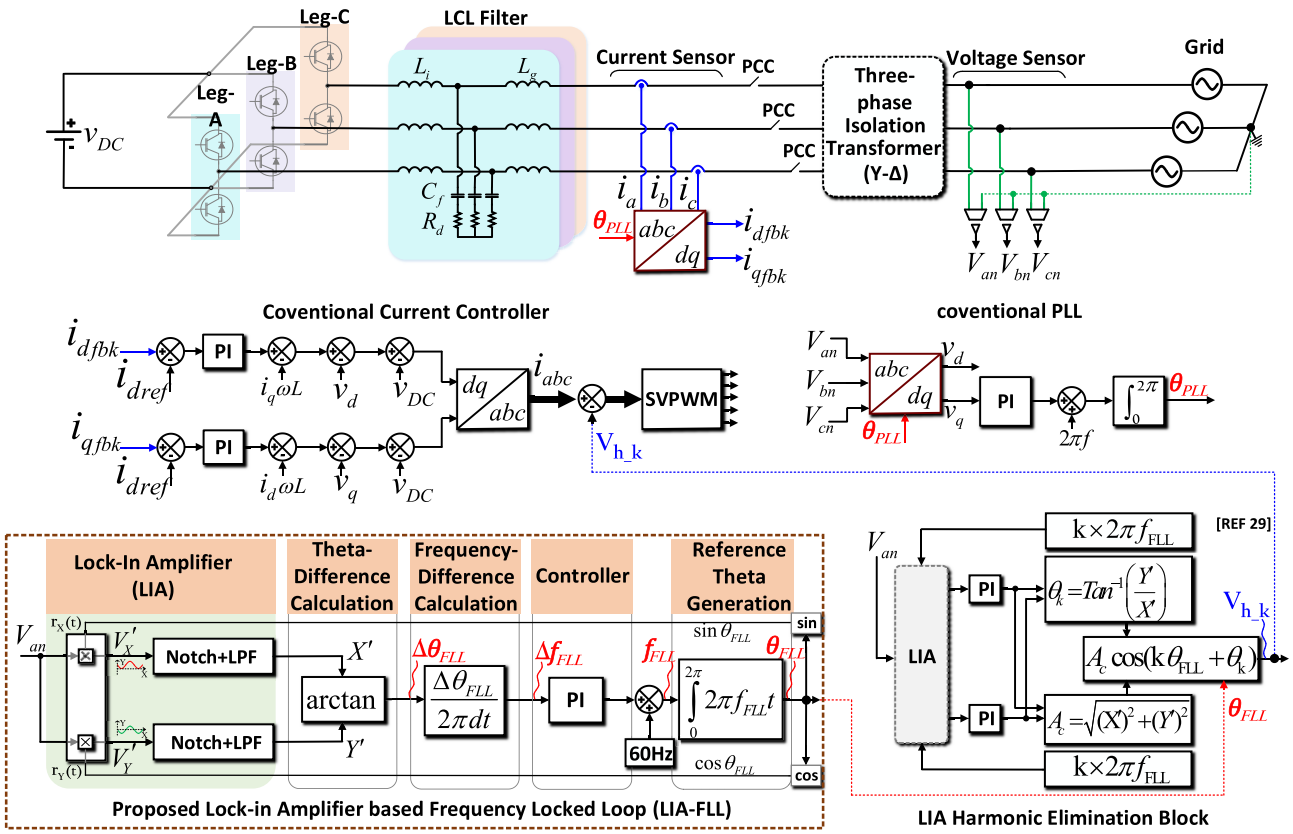

FIGURE 5. Proposed harmonic elimination scheme with LIA-FLL.

following equation.

$$\Delta\theta_{FLL} = Tan^{-1}\left\{\frac{\frac{V_m}{2}\left[sin\{2\pi(f_{an}-f_{FLL})t+(\theta_{an}-\theta_{FLL})\}\right]}{\frac{V_m}{2}\left[cos\{2\pi(f_{an}-f_{FLL})t+(\theta_{an}-\theta_{FLL})\}\right]}\right\} \tag{9}$$

Further simplifications can be performed as expressed in Eq. (10).

$$\Delta\theta_{FLL} = \overbrace{\{2\pi(f_{an}-f_{FLL})t+(\theta_{an}-\theta_{FLL})\}}^{Phase\ Difference} \tag{10}$$

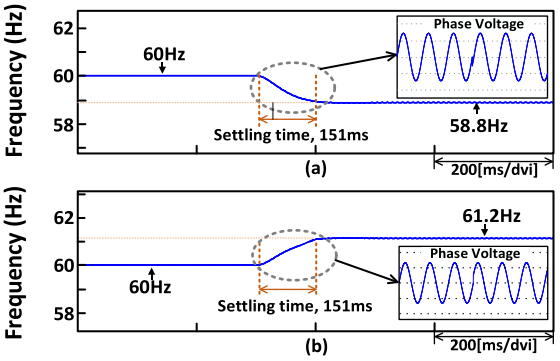

FIGURE 6. Grid-frequency tracking by LIA-FLL (a) fundamental frequency changed from 60Hz to 58.8Hz (b) from 60Hz to 61.2Hz.

In order to get the frequency difference from the phase difference the derivative function is used as follows.

$$\Delta f_{FLL} = \frac{1}{2\pi}\left\{\overbrace{\frac{d}{dt}\left[\{2\pi(f_{an}-f_{FLL})t+(\theta_{an}-\theta_{FLL})\}\right]}^{Derivative\ Function}\right\} \tag{11}$$

Eq. (11) can be further simplified to get the frequency difference as shown in Eq. (12).

$$\Delta f_{FLL} = (f_{an}-f_{FLL}) \tag{12}$$

Then, a PI controller is used to compensate for the error by the feedback loop. The gains of the PI controller such as kp and ki are chosen 0.001 and 4.44 by using SISOTOOL in MATLAB. The output of the PI controller is added to the reference frequency value (60Hz) to get the fundamental frequency (f_{FLL}) information. It is used to generate the reference signal for the LIA for the harmonic elimination.

Fig. 6 shows the simulation results of the proposed LIA-FLL method. In the simulation the grid frequency changes from 60Hz to 61.2Hz and from 60Hz to 58.8Hz. It can be observed that the frequency tracking can be achieved within 151ms. Hence, it can satisfy the standard such as IEEE P1547 [1].

Finally, the theta (θ_{FLL}) needs to be generated from the fundamental frequency (f_{FLL}) by using a resettable integrator in Eq. (13) and it is used to reconstruct the harmonics.

$$\theta_{FLL} = \int_0^{2\pi} 2\pi f_{FLL} t \tag{13}$$

III. SIMULATION RESULS BY THE PROPOSED HARMONIC ELIMINATION METHOD BY LIA-FLL

In this section, the PSIM simulation results of the proposed harmonic elimination method are presented. The proposed harmonic elimination method with LIA-FLL scheme is shown in Fig. 5.

In the proposed method harmonic is eliminated by detecting it using LIA and reconstructing it using the frequency and phase information provided by the LIA-FLL as expressed in,

$$V_{h\_k} = A_c cos(k\theta_{FLL} + \theta_k) \tag{14}$$

where, V_{h_k} represents the 'k^{th}' order of reconstructed harmonics, and A_c stands for the amplitude of the reconstructed harmonic. As mentioned earlier if the frequency of the reference signals used to detect the harmonic is fixed its accuracy gets deteriorated when the grid frequency varies. Therefore, the grid frequency and phase information are detected by the LIA-FLL and provide it for the LIA for the harmonic detection and elimination.

Since the harmonic elimination using LIA is already presented in [29], [30], [34] it will not be covered in detail here. All the system parameters of the Three-phase 10kW grid connected inverter for the simulation and experiments are shown in Table 1.

Fig. 7(a) shows FFT results of the output current of the inverter when the grid frequency is 61.2Hz. Fig. 7(b) shows the 5^{th} harmonic detected by the proposed LIA-FLL and its amplitude is well matched with the real value. However, as shown in Fig. 7(c), the error in the amplitude of 5^{th} harmonic is large when FLL is not applied since no frequency information of the fundamental component is provided for the reference signal used in the LIA to detect the harmonic. Though the grid frequency is 61.2Hz, the frequency of the reference signal used in the LIA is still 60Hz, thereby causing a large error in the detection of the harmonic.

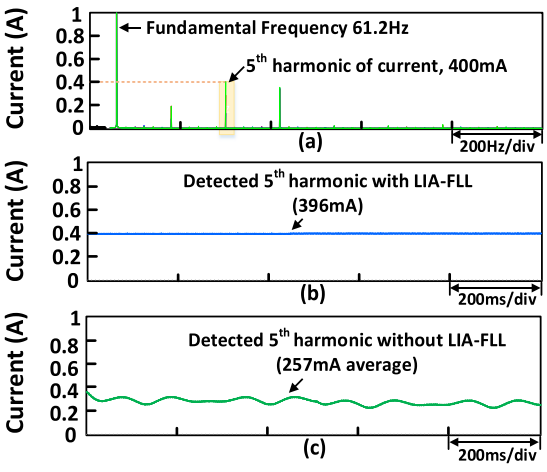

FIGURE 7. Detection of the inverter output current harmonics when the grid frequency is 61.2Hz (a) FFT results (b) 5th harmonic detected with LIA-FLL (c) 5th harmonic detected without LIA-FLL.

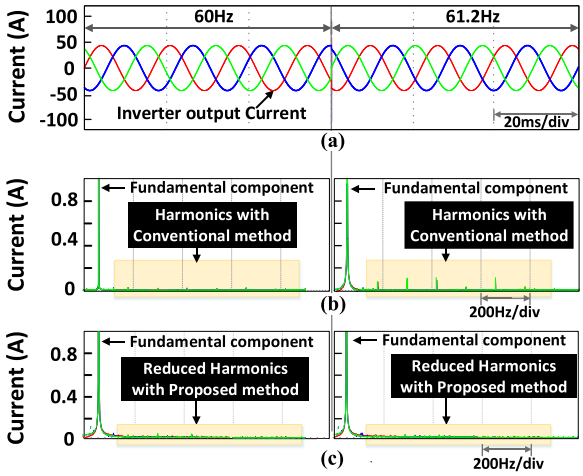

FIGURE 8. Performance of the harmonic elimination under the different frequency condition (a) Three-phase inverter currents (b) harmonic Elimination with conventional FLL, (c) harmonic Elimination with the proposed LIA-FLL.

Fig. 8 shows the comparison of the harmonic elimination methods under the different grid frequency conditions. Fig. 8(a) represents the three-phase inverter current waveforms at 100% load (10KW power) and the grid frequency is changed from 60Hz to 61.2Hz. Fig. 8(b) shows the simulation results with conventional harmonic elimination method with no FLL. It can be observed that the current harmonics such as 3^{rd}, 5^{th} and 7^{th} are eliminated when the grid frequency is 60Hz. However, the harmonics are not completely eliminated when the grid frequency is changed to 61.2Hz. Fig. 8(c) shows the simulation results with the proposed LIA-FLL method. As observed in Fig. 8(c) the current

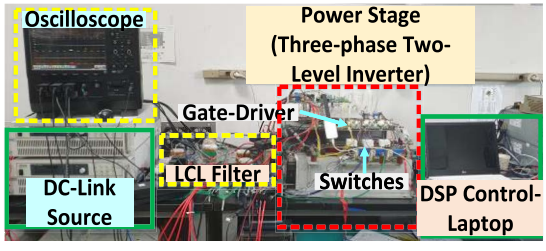

FIGURE 9. Experimental setup of 10KW three-phase grid-connected inverter.

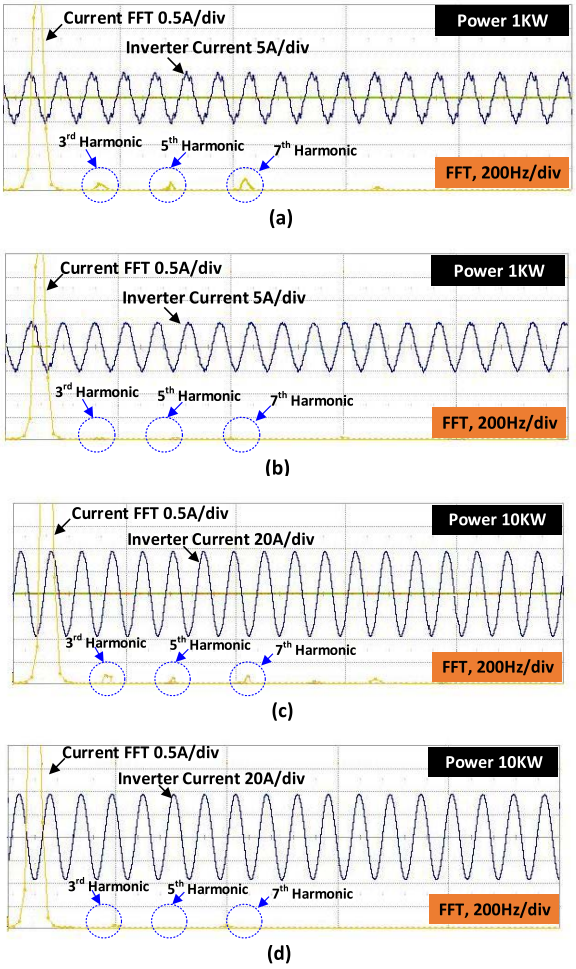

FIGURE 10. Experimental results of Performance in harmonic elimination (a) without LIA-FLL at 1KW (b) with LIA-FLL at 1KW (c) without LIA-FLL at 10KW (d) with LIA-FLL at 10KW.

harmonic can be perfectly eliminated regardless of the grid frequency.

IV. EXPERIMENTAL RESULTS

In order to prove the performance of the proposed method a 10KW three phase grid connected inverter has been built as shown in Fig. 9. The power stage is composed of three IGBT modules (SKM75GB12T4, Semikron) and the gate drivers (SKHI22BH4, Semikron) are used to operate each switching device. The inverter control is performed by a DSP (TMS320F28335, Texas Instrument). A DC power supply (Ainuo AN51015-1000(F)) is used to supply 400V DC to the inverter.

Fig. 10 shows the experimental results obtained by operating the three-phase grid connected inverter at 1kW and 10kW, respectively. Since the grid frequency cannot be changed by intention the experiments for the harmonic elimination are conducted under the normal grid condition, where the grid frequency is varying in between 58.8Hz and 61.2Hz.

TABLE 1. System parameters for the simulation and experiment.

Symbol	Parameters	Values
P_o	Rated Power	10kW
I_{max}	Rated Current	37.1A
t_d	Dead time	1.7µs
V_{DC}	DC-Link	400V
L_i	Inverter side inductor	760uH
L_g	Grid side inductor	450uH
C_f	Filter capacitor	10.0µF
R_d	Damping resistor	1.0 ohm
V_g	Inverter voltage (L-L)	$220V_{rms}$
f_g	Grid frequency	60Hz

As shown in Fig. 10, the 3rd, 5th and 7th current harmonics are perfectly eliminated at light and heavy load conditions, thereby proving the validity and the effectiveness of the proposed method. As shown in Table 2, the THD of the inverter output current is improved from 4.26% to 2.1% at 1kW with the proposed LIA-FLL based harmonic elimination method. It is improved from 2.62% to 1.31% at 10KW while 1.51% THD is achieved at 10kW with LIA only as shown in [29]. It should be noted that only 3rd, 5th and 7th harmonics are compensated in these experiments.

Table 3 shows a comparison among some of the state-of-art PLLs/FLLs and the proposed LIA-FLL method in terms of peak frequency error in response to phase angle jump, frequency overshoot at frequency step mode and the harmonic rejection capability. The peak frequency error in response to 40° phase-angle jump with the proposed FLL is 1.6Hz, which is the least among the results with other methods. The proposed method shows the 0Hz frequency overshoot in response to 10Hz frequency step change, which is also better result than those by other methods. In addition, the proposed method has better harmonic rejection capability due to the accurate harmonic detection by the outstanding frequency tracking performance.

TABLE 2. THD reduction with proposed LIA-FLL method for harmonic compensation at 60Hz ± 1.2Hz.

Power	Without LIA-FLL	With LIA-FLL	% Harmonic Reduction
1 KW	4.26%	2.21%	98%
2 KW	3.93%	2.10%	97.3%
3 KW	3.71%	1.98%	96%
4 KW	3.50%	1.91%	95.1%
5 KW	3.25%	1.84%	94%
5 KW	3.10%	1.73%	93%
7 KW	2.97%	1.66%	92.2%
8 KW	2.88%	1.54%	91%
9 KW	2.70%	1.42%	90%
10 KW	2.62%	1.31%	89%

TABLE 3. Comparisons of the advanced PLLs/FLLs and the proposed LIA-FLL.

References	1*	2*	3*
[32]	16.4 Hz	8.6Hz	Good
[26]	9.8 Hz	2.2 Hz	Poor
[31]	5.1 Hz	0.5 Hz	Good
[33]	6.1 Hz	0 Hz	Good
Proposed	1.6 Hz	0 Hz	Excellent

1*: Peak frequency error in response to 40° phase-angle jump

2*: Frequency overshoot in response to 10 Hz frequency step change

3*: Harmonic and DC offset rejection capability

V. CONCLUSION

In this paper a harmonic elimination method with novel LIA-FLL is proposed. The FLL is implemented by using a LIA and the frequency information obtained is used to adjust the frequency of the reference signal for the LIA to detect and eliminate the harmonics. Since the grid frequency varies all the time the grid frequency tracking is very important to eliminate the harmonics perfectly. Therefore, only the fundamental frequency power can be injected to the grid by the grid-connected inverter with the proposed method.

Due to the outstanding performance of LIA the proposed FLL is immune to the DC offset or other harmonics. In addition, the transient time for the frequency tracking by the proposed LIA-FLL is less than 160ms, which can satisfy the requirement specified in the IEEE standard P1547.

The feasibility and the effectiveness of the proposed LIA-FLL has been verified through the simulation and experiments with a 10kW three-phase grid-connected inverter. The proposed method can be utilized for the harmonic elimination of the grid-connected inverters and it can contribute to lower the grid pollution. The future work can be described as followings. Since the computational burden of the proposed LIA-FLL is relatively larger and the settling time is little bit longer, further research is required to improve the dynamics and to reduce the computational burden.

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