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# Highly Reliable Quadruple-Node Upset-Tolerant D-Latch

**SEYEDEHSOMAYEH HATEFINASAB[1], AKIKO OHATA[2], ALFONSO SALINAS[3], ENCARNACION CASTILLO[1], AND NOEL RODRIGUEZ[1]**
[1]Department of Electronics and Computer Technology, University of Granada, 18071 Granada, Spain
[2]High Energy Accelerator Research Organization (KEK), Oho, Tsukuba, Ibaraki 305-0801, Japan
[3]ECsens Group, University of Granada, 18071 Granada, Spain

Corresponding author: Seyedehsomayeh Hatefinasab (hatefi@correo.ugr.es)

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**ABSTRACT** As CMOS technology scaling pushes towards the reduction of the length of transistors, electronic circuits face numerous reliability issues, and in particular nodes of D-latches at nano-scale confront multiple-node upset errors due to their operation in harsh radiative environments. In this manuscript, a new high reliable D-latch which can tolerate quadruple-node upsets is presented. The design is based on a low-cost single event double-upset tolerant (LSEDUT) cell and a clock-gating triple-level soft-error interceptive module (CG-SIM). Due to its LSEDUT base, it can tolerate two upsets, but the combination of two LSEDUTs and the triple-level CG-SIM provides the proposed D-latch with remarkable quadruple-node upsets (QNU) tolerance. Applying LSEDUTs for designing a QNU-tolerant D-latch improves considerably its features; in particular, this approach enhances its reliability against process variations, such as threshold voltage and (W/L) transistor variability, compared to previous QNU-tolerant D-latches and double-node-upset tolerant latches. Furthermore, the proposed D-latch not only tolerates QNUs, but it also features a clear advantage in comparison with the previous clock gating-based quadruple-node-upset-tolerant (QNUTL-CG) D-latch: it can mask single event transients. Specific figures of merit endorse the gains introduced by the new design: compared with the QNUTL-CG D-latch, the improvements of the maximum standard deviations of the gate delay, induced by threshold voltage and (W/L) transistors variability of the proposed D-latch, are 13.8% and 5.7%, respectively. Also, the proposed D-latch has 23% lesser maximum standard deviation in power consumption, resulting from threshold voltage variability, when compared to the QNUTL-CG D-latch.

**INDEX TERMS** Power-delay product (PDP), soft errors (SE), single event upset (SEU), high impedance state (HIS), single event transient (SET), dual interlocked storage cell (DICE), triple path DICE (TPDICE), quadruple-node upsets (QNUs).

## I. INTRODUCTION

Nano-scaling integrated circuits and systems rises a sensitivity challenge to soft errors generated by radiation-induced charges when the size of the transistors is reduced [1]. There are different designs of hardened D-latch against soft errors such as single-node upsets [2] and double-node upsets (resulting from a striking particle injected to double nodes [3]–[5]). Furthermore, the reduction of transistor size can cause a striking particle to affect multiple nodes (more than two). This effect can cause multiple-node upsets (MNUs), leading to triple-node upsets [6] and quadruple node upsets [7]. This represents a huge concern to design reliable storage modules, especially for their safe application when used in harsh radiative environments [8].

There is a lot of investment in hardened circuit structures to reduce the side effect of soft errors. These circuits comprise memory cells [9], [10], flip-flops [11], [12], and latches [13]. But yet most of the existing hardening approaches face limitations; for example, some hardened D-latches cannot recover reliably after flipping, even if the output node stores its value. Some D-latch designs have overcome this drawback proposing complete self-recovery after single-node upset (SNU) [14]. However, even if they can self-recover from SNU, they cannot recover fully against double-node upset (DNU). Later in time, some of DNU hardened D-latches [15]

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have been proposed to face this issue, nonetheless, in their designs there is one-pair of their nodes that cannot tolerate high charges, which means they are not completely DNUs self-recoverable. One step beyond is given in [5], [16]–[18], where DNU D-latches able to fully self-recover are presented, however, those designs are lacking the triple-node-upset (TNU) tolerance. This latter challenge has been addressed in [8], [19] where TNU can be tolerated but not self-recovered. By the best knowledge of the authors of this manuscript, there is not a complete self-recovery TNU D-latch [20]. Finally, there are some recent quadruple-node-upset-tolerant D-Latch (QNU) [7] and memory cell [21] designs, which are not self-recoverable.

Since D-latches have a long holding time due to power consumption constraints, the possibility of being affected by striking particles in rigid conditions, such as QNUs is always present. The importance of QNU is supported by the fact that only double-node upset D-latches can be fully self-recovered and there are not TNU D-latches that can be fully recovered. If a DNU-tolerant D-latch is affected by TNU, as it cannot recover itself, the error will take place and the output will be not correct. As the holding time is long, the D-latch can be also affected by SNU; the combination of both TNU and SNU can lead to QNU. Based on the explanation in [8], the occurrence possibility of single event multiple upset (SEMU) or multiple event multiple upset (MEMU) increases sharply by reducing the size of transistors in nano-scale technology. Also, in [22], the authors demonstrate that CMOS technology below 90nm node has an unneglectable QNU probability, being this possibility dramatically increased below 40nm node.

The possibility of QNU happening in nano-CMOS circuits depends on different parameters, such as layout topology (using adjacent transistors decrease single event upset (SEU) probability [23], and using the master-salve interleaving approach enhances dual interlocked storage cell (DICE) against the SEU tolerance [24]), technology data [22], the type of particles, temperature environment, and supply voltage.

The above discussion of reliability issues of hardened D-latch has encouraged the development of a quadruple-node-upset-tolerant D-latch. In this manuscript, a low power consumption, single event transient (SET) filterable, and high reliable quadruple-node-upset-tolerant D-Latch is presented. The proposed D-latch consists of two connected low-cost single event double-upset tolerant (LSEDUT) cells [25], and a clock-gating triple-level soft error interceptive module (CG-SIM), which consists of three levels of CG-based 2-input C-elements connected to each other. Three nodes of each LSEDUT cell are connected to three inputs of the first stage of the CG-SIM. The second stage input of the CG-SIM is connected to the output of the first stage of the CG-SIM and the output of the second stage of the CG-SIM is connected to the third stage of the CG-SIM. Following the strategy of the LSEDUT latch in [25], implementing a triple-input Muller C-element (TMCE) to filter soft errors, the proposed D-latch features two LSEDUT cells, and a triple-level CG-SIM is used to perform the same function as TMCE of LSEDUT D-latch. The simulation results show that any QNUs for all internal and output nodes can be tolerated. Also, this latch can filter SET pulses in the transparent mode and there is not high impedance state (HIS) at the output node.

The manuscript is organized as follows: Section II revisits previous approaches of hardened D-latches. In Section III, the proposed D-latch design, immunity, characteristics, and implementation are presented. In Section IV, simulation results on the robustness and a comparison with previous latches are reported, followed by the conclusions in Section V.

## II. PREVIOUS HARDENED D-LATCHES

### A. DICE

Many techniques have been presented to mitigate SNU in D-latches and among those hardened D-latches, DICEs are very effective [26]. In Fig. 1(a), the schematic of a DICE structure is shown. This structure can recover from any SNU and it is self-recoverable to the DNUs in some nodes.

### B. CLCT

Circuit and layout combination technique (CLCT), which is shown in Fig. 1(b), operates based on clock-gating technology, in which there are not positive feedback loops of its DICE in the transparent mode to prevent current competition in the output node [15]. The data at holding time can be retained in the DICE and keeper; then can be transferred to the output by a C-element tolerating both SNU and Single Event Double-Upset (SEDU).

CLCT [15] has a high impedance state in the output node when SNU or SEDU take place; for example, when SNU happens in the keeper or SEDU happens in CG-based DICE, the output goes to a high impedance state. Also, this D-latch is not fully hardened against SEDU.

### C. TPDICE-BASED D-LATCH

Triple path DICE (TPDICE) is a hardened D-latch alternative with immunity against SET, SNU, DNU, and a HIS insensitivity [27], which is shown in Fig. 1(c). In this structure, a TPDICE is used for retaining the data in holding time; furthermore, it includes a three-input C-element for filtering SEDU, an embedded Schmitt trigger inverter (STI) for filtering the SET in the transparent path, and a keeper for avoiding a high impedance state in the output node.

### D. LSEDUT D-LATCH

Fig. 1(d) shows the LSEDUT latch having full use of its interlocked node character to make it reliable for saving data with a CG-based C-element to transfer the stored data to the output in holding time. A three-input C-element is used to filter SNU or SEDU, and a keeper to avoid a high impedance state [25]. This structure is based on the TPDICE but three transmission gates of the input are connected to four

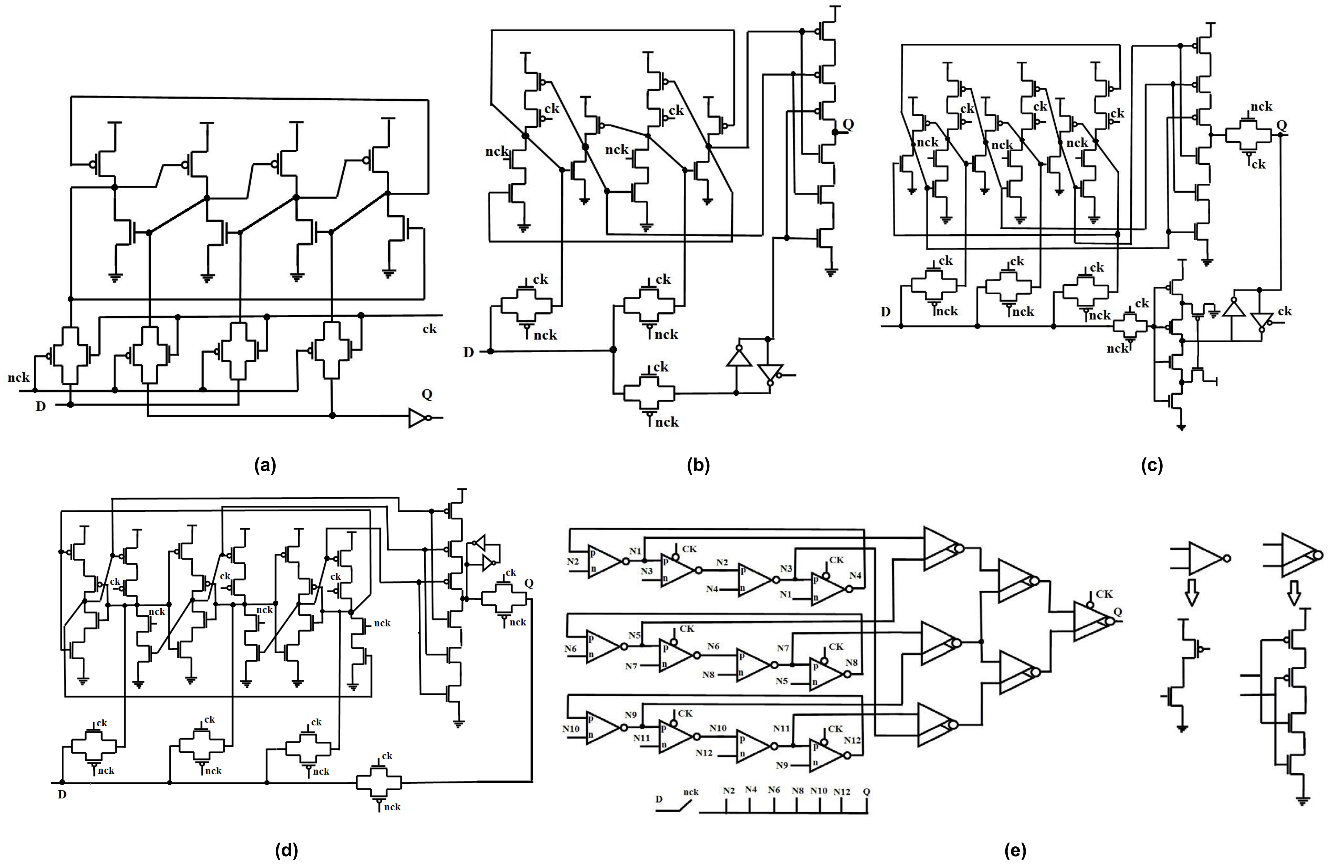


**FIGURE 1.** (a) DICE [26], (b) CTCL latch [15], (c) TPDICE-based D-latch [27], (d) LSEDUT D-latch [25], (e) QNUTL-CG D-latch [7].

transistors, which yields a larger capacitance at the input node to store data in comparison with TPDICE in [27].

### E. QNUTL-CG D-LATCH

The clock gating-based quadruple-node-upset-tolerant latch (QNUTL-CG D-latch) has been presented against MNUs [7] and it is reproduced in Fig. 1(e). This D-latch has three CG-based DICEs and a triple-level soft-error interceptive module (SIM) for filtering soft errors. Since CG-based DICE can tolerate SNU and these three-level C-elements can filter SNU, QNUTL is immune against the QNU.

## III. PROPOSED D-LATCH

Fig. 2(a) shows the LSEDUT-based proposed D-latch with triple-level CG-SIM and two CG-inverters to filter SET in transparent mode. The layout of the device is shown in Fig. 2(b). In this latch, D and Q are the input and output; **ck** and **nck** are the clock circuit and inverter clock circuit rails, respectively. When ck = 1, nck = 0, the latch works in the transparent mode and the gate of transistors connected to N2, N4, N6, N8, N10, N12, and Q are charged or discharged by the D input through transmission gates. Then, the D input propagates through six 2-input C-elements and stablishes the values of N1, N3, N5, N7, N9, and N11. In the transparent mode, the positive feedback of the LSEDUT part is not active, and the triple-level CG-SIM is not connected to the output node to avoid current competition, which also decreases power consumption and delay. Moreover, this hardened D-latch has SET-filtering feature in transparent mode. If a SET arrives at D from a previous combinational part before the D-latch, it will pass through the CG-inverter and will arrive at x1 node reversing the SET. Then, by passing through the second CG-inverter and achieving the Q node, the SET is filtered by the delay introduced by these two inverters. For example, if SET comes and D becomes low, a positive SET (low-high-low) at x1 will appear. But, the right value of x1 is low and the NMOS transistor of the second inverter is off. Therefore, the value of Q cannot change until x1 becomes high, which needs time to charge the NMOS capacitors of the second inverter. In the transparent path, these two CG-inverters are applied to introduce delay for filtering the SET.

In the latching time, when ck = 0 and nck = 1, N2, N4, N6, N8, N10, N12, and Q are disconnected from the D input, however, two LSEDUTs with triple-level CG-SIM are connected to Q. This implies that Q is driven by a triple-level CG-SIM instead of the D input in the transparent path. Additionally, the feedback loops of each LSEDUT are activated to hold values. Therefore, the proposed D-latch can properly store values and drives valid values to the output node (Q). The output node does not present any HIS in

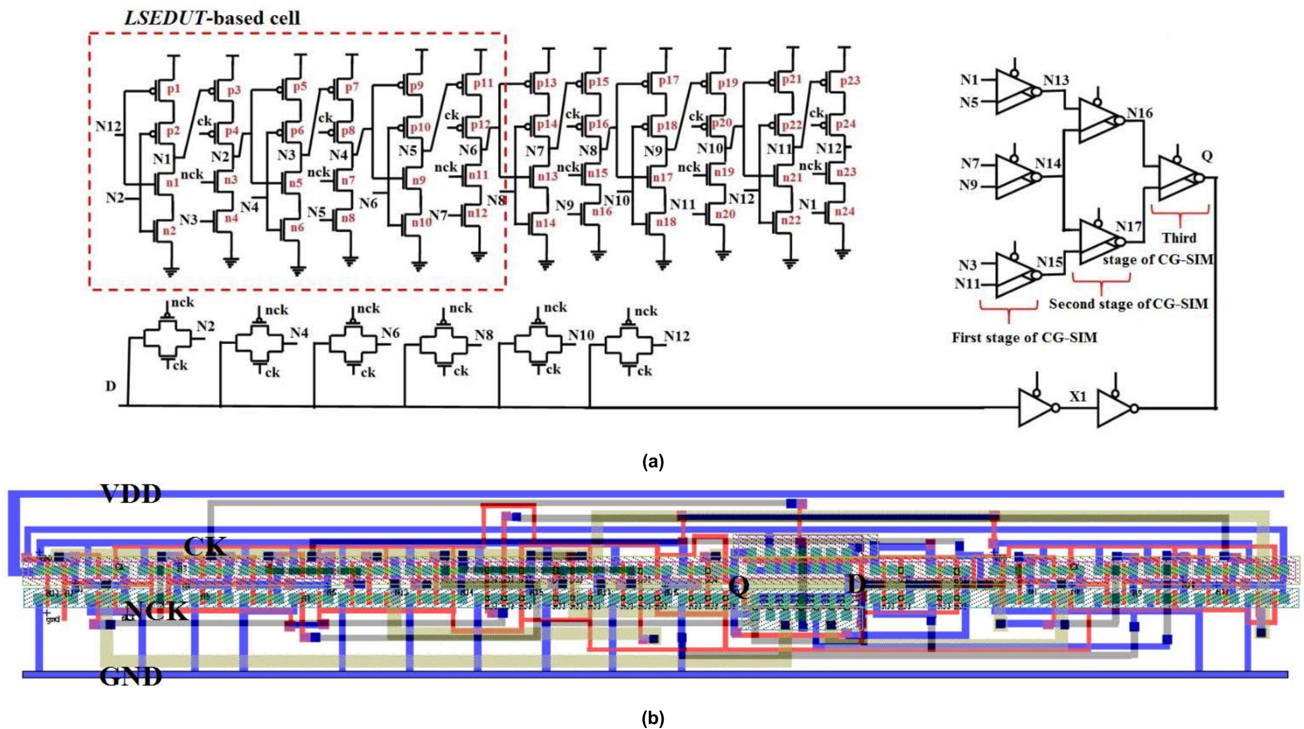


**FIGURE 2.** Proposed D-latch (a) schematic, (b) layout.

the holding time when SNU, DUN, TUN, or QUN take place.

It is worth mentioning that the triple-level CG-SIM has three stages CG-3 input C-elements, which are less power demanding, but as this part does not connect to Q in transparent mode, the values of N13, N14, N15, N16, N17 are floating.

If any particle strikes at any node of the proposed D-latch as one SNU, this structure is self-recoverable like an LSEDUT latch. In the following subsections, we cover different situations where different levels of upsets occur at different nodes of the proposed D-latch and its immunity is systematically evaluated.

### A. IMMUNITY AGAINST SNU

Since the proposed design is very symmetric, N1, N3, N5, N7, N9, and, N11 have the same value (inverted input data) and N2, N4, N6, N8, N10, and N12 have the same value as the input value. Also, N13, N14, N15 have the same value as the input value (D-input passes through two inverters), and N16, N17 present the same value as the inverted value of the input. So, five different cases (e.g., N1, N2, N13, N16, and Q) should be investigated for a SNU. For the internal nodes of the LSEDUT, N1 or N2, if one of them suffers from a SNU, for example, N1 is affected when D = 0 (N2 = 0, N1 = 1), then it will be discharged to 0, p3 is turned one, and N2 becomes unstable, but this charge cannot make N2 turn into high level, because n4 is ON; as the result, N1 and N2 can be recovered by N12 and N3, respectively. Even, if this charge is large enough to change the value of N2, it will be filtered by the tripe-level CG-SIM. This SNU cannot affect the output of the proposed D-latch. If any SNU affects the N2 node, the analysis of recovery is the same as for N1. When N13 or N16 are affected by SNU, as they are derived by LSEDUTs connected to the first stage of the CG-SIM, they can recover their value. If Q is affected by a SNU, it will flip temporarily, but as the LSEDUTs and the triple-level CG-SIM save their values and they are not affected by the SNU, therefore, Q will be recovered. As a summary, the proposed D-latch is immune against any SNUs.

### B. IMMUNITY AGAINST DNU

After evaluating against SNU, the immunity of the proposed D-latch against DNU is considered. As this circuit is symmetric, three cases can be studied for this immunity analysis. In the first case, when two nodes are inside of the LSEDUT, there are different analysis for the two pairs of nodes inside of LSEDUT [25], which yields three cases: 1a, 1b, and 1c.

*Case 1a:* if these pairs of nodes are inside of the LSEDUT and the triple-level CG-SIM is not affected by DNU. There are six key pairs of LSEDUT nodes [25]. These pairs are <N1, N2>, <N3, N4>, <N5, N6>, <N7, N8>, <N9, N10>, and <N11, N12>, which have the same situation against DNU. The explanation of their immunity is as follows. When D = 0, N2, N4, N6, N8, N12 are set on the low logic state and all of the PMOSs of the 2-input C-elements are turned ON, and, N1, N3, N5, N7, N9, and N11 are set to high

logic state: if N1 and N2 are affected (N1 is discharged to 0 and N2 is charged to 1), n24 and p2 transistors are turned off and transistors p3, n2, n5 are turned ON. Since n6 is off, N3 cannot discharge through n5 to the ground. So other nodes in the LSEDUT except N1, and N2 are not affected by DNU, then N1, and N2 self-recover from N12 and N3, respectively. This shows immunity of the proposed D-latch against DNU in case 1a.

*Case 1b:* in this case, the pairs inside the LSEDUT to be considered are (1) <N1, N4>, <N3, N6>, <N5, N8>, <N7, N10>, <N9, N12>; (2) <N2, N3>, <N4, N5>, <N6, N7>, <N8, N9>, <N10, N11>, <N12, N1>; (3) <N2, N5>, <N4, N7>, <N6, N9>, <N8, N11>, <N10, N1>, and <N12, N3>. When D = 0, N4 = 0 and N1 = 1, if, for example, N1 and N4 are affected, N1 will become 0 and N4 will become 1, and n24, p6, and p9 will be turned off and p3, n6, and n9 will be turned ON. Since p3 is ON, N2 is unstable but N5 cannot discharge because n10 is turned off and there isn't any path through n9 to the ground. Although N2 is unstable, it cannot turn to high logic level by any SNU. N4 and N1 are self-recovered by N5 and N12, respectively. Even, if N2 is affected by SNU, it becomes high logic level, N2 and N4 can upset N3, which means that N2 and N4 cannot be self-recovered; however, this upset cannot change the value of N16 because N14 isn't affected. This shows immunity of the proposed D-latch against DNU in case 1b.

*Case 1c:* in this case, the two pairs affected are inside the LSEDUT including (1) <N1, N3>, <N3, N5>, <N5, N7>, <N7, N9>, <N9, N11>, <N11, N1> (2) <N2, N4>, <N4, N6>, <N6, N8>, <N8, N10>, <N10, N12>. If N1 and N3 are affected, for example when D = 0, N2 = 0, and N1 = 1 and after charge injected to N1 and N3, N1 and N3 are discharged to "0", n24 and n4 are turned off and p3 and p7 are turned ON. This situation makes N2 to turn to the high logic level and n4 becomes unstable which means that N2 and N4 cannot be self-recovered. In spite of that, this soft error can be filtered by the triple-level CG-SIM and it will not appear at Q which means the proposed D-latch is immune against DNU in case 1c.

*Case 2:* DNU affects one node in the triple-level CG-SIM and one node of LSEDUTs. This situation for LSEDUTs and the triple-level CG-SIM is the same since they are affected by SNU. As the structure of the proposed D-latch is symmetric, the pairs that should be considered are <N1, N13>, <N1, N16>, and <N1, Q>. In this situation, as explained before if N1 is upset, N3 will not be affected and the LSEDUT is self-recovered from SNU; therefore, SNU in N1 cannot change the value of N13. Even if there is a SNU in N13 simultaneously, as N14 is not affected by any DNU, N16 will not be affected and it would have the valid value, therefore Q will store its valid data. Also, other pairs of nodes in case 2 have the same analysis, which means that Q is immune against DNU in this case, therefore, this proposed D-latch is immune against DNU in case 2.

*Case 3:* the DNU affects only two nodes of the triple-level CG-SIM, and as the triple-level CG-SIM is symmetric, the following pairs of nodes should be considered, <N13, N14>, <N13, N16>, <N13, N17>, <N13, Q>, <N16, N17>, and <N16, Q>. As the LSEDUTs of the D-latch is not affected by DNU and they have valid data, the data of N1, N3, N5, N7, N9, N11 are valid and they can recover the data of the triple-level CG-SIM and Q after being affected by the charge injected. This recovery means that the proposed D-latch is immune against DNU in case 3.

When D = 1, the performance of the proposed D-latch is similar to the case when the input data is D = 0. This structure is immune against DNU when two charges are injected inside of the LSEDUTs and the triple-level CG-SIM.

### C. IMMUNITY AGAINST TNU

In this section, we detail the characteristics that make the proposed D-latch immune against TNU. For this test, there are four cases described below:

*Case 1:* there is no charge affecting the LSEDUTs and all three charges affect the triple-level CG-SIM. As the SIM is a symmetric circuit, only five triplets of nodes should be considered for TNU, being those <N13, N14, N15>, <N13, N14, N16>, <N13, N14, N17>, <N13, N16, Q>, and <N16, N17, Q>. As for all of these situations LSEDUTs are not affected, therefore, N1, N3, N5, N7, N11 have valid values and the LSEDUTs can recover the value of the triple-level CG-SIM and Q. This means that the proposed D-latch is immune against TNU in case 1.

*Case 2:* one charge affects one node of the LSEDUTs and the two other charges affect the triple-level CG-SIM. As the circuit is symmetric, five situations should be considered, being those <N1, N17, Q>, <N1, N13, N14>, <N1, N13, N16>, <N1, N13, Q>, and <N1, N16, N17>. This situation for the LSEDUTs is similar to the case when the LSEDUTs experiences an SNU and as it was explained, the LSEDUTs are immune against SNU and they can tolerate SNU. As LSEDUTs can be self-recovered from SNU, N1, N3, N5, N7, N9, and N11 have valid values and even if two charges are injected into the triple-level CG-SIM, these two nodes can be recovered by the LSEDUTs. Therefore, this TNU cannot change the value of Q and the proposed D-latch is immune against TNU in case 2.

*Case 3:* two charges injected to the LSEDUTs and one charge injected to the triple-level CG-SIM. As the proposed D-latch has a symmetric structure, there are six groups of triplets of nodes that must be considered under this situation: <N1, N2, N13>, <N1, N2, N16>, <N1, N2, Q>, <N1, N3, N13>, <N1, N3, N16>, and <N1, N3, Q>. In the DNU section, it was explained how <N1, N2> can be self-recovered whenever there is a DNU injected into the LSEDUT. Therefore, the LSEDUT has valid values and N1, N3, N5, N7, N9, N11 have valid values to launch the triple-level CG-SIM, which can be recovered from LSEDUTs. Also, if two charges are injected to the case of <N1, N3>, even if they lose their value, Q cannot change its value because N5, N7, N9, N11 do not lose their values. The values of N13, N14, and N15 are not changed by the upset of N1 and

N3 because they are connected to different C-elements of the CG-SIM and they cannot change the value of N13 or N15. If N13 is upset, it could not change the value of N16 and Q either. The case of <N1, N3, N16> follows the same analysis since N1 and N3 cannot change the value of the triple-level CG-SIM and if N16 is upset and loses its data, still N17 has a valid value, which means that Q will retain the valid value. Also, for the case of <N1, N3, Q>, as the charges injected to N1 and N3 cannot change the value of N13, N14, and N15, these nodes have valid data and even if Q becomes upset due to the charge injection, it can recover by N16 and N17, which have valid data. As the result, Q maintains its value and the proposed D-latch is immune against TNU in case 3.

*Case 4:* three charges injected to the LSEDUTs and due to the symmetric structure, there are six situations to be considered: <N1, N2, N3>, <N1, N2, N7>, <N1, N3, N4>, <N1, N3, N7>, <N2, N3, N4>, <N2, N3, N7>. We consider first the case of D = 0, N2 = 0, N1 = N3 = 1, (n2, p3, p7 are off and n4, p2, p5 are ON). If charges are injected to N1, N2, N3, they will lose their data and N2 = 1, N1 = N3 = 0. In this situation, p3, n5, and p7 are ON, and n24, p2, p5, n4 are off; therefore, N4 is unstable and N1, N2, N3 cannot recover their data, but nodes N5, N7, N9, and N11 do not lose their data and have valid values. Therefore, N13, N14, and N15 do not lose their values and N16 and N17 have valid values, which implies that Q maintains its valid value and therefore, these soft errors cannot change the value of the proposed D-latch. The next case of triplet should be considered is <N1, N2, N7> being D = 0, N2 = 0, N1 = N7 = 1, and n24, n12, p5, and p2 are ON and p3, p15, n2, and n5 are off. If there is any charge injected to N1, N2, N7, and their values change to N2 = 1, N1 = N7 = 0 as a consequence, p3, p15, n2 will be ON and n24, p5, n12 will be off and N3 will become unstable; however, this situation will not change the value of N3, and N12 because N4, and N11 are not affected by these charges. Since only N1 and N7 are affected and N3 and N11 are not affected, these soft errors can be filtered by the first stage of the CG-SIM, and the value of N13, N14, and N15 are valid. Therefore, Q has a valid value, which means these charges injected do not affect the value of Q. For <N1, N3, N4>, <N1, N3, N7>, <N2, N3, N4>, and <N2, N3, N7> groups of nodes, the same analysis holds. As a result, the proposed D-latch is immune against TNU in case 4.

### D. IMMUNITY AGAINST QNU

In this section, we detail the immunity against QNU of the proposed D-latch in five cases, which is described as below:

*Case 1:* all four charges injected to the triple-level CG-SIM and none of the charges is affecting the LSEDUTs. This situation has three quadruplets of nodes to be analyzed <N13, N14, N16, Q>, <N13, N14, N15, N16>, and <N13, N16, N17, Q>. In the <N13, N14, N16, Q> case, there is a temporary flip of state in N13, N14, N16, but these nodes can be recovered by the LSEDUTs which are not affected by the QNU and N1, N3, N5, N7, N9, and N11 have valid values. Thus, the value of N13 and N14 can be recovered and then, N16 can be recovered from N13 and N14. In the end, Q can be recovered through N16 and N17 after the temporary flip. The quadruplet <N13, N14, N16, Q> can recover from the QNU, and the two other quadruplets have the same analysis, which means that the proposed D-latch is self-recovered from QNUs in case 1.

*Case 2:* one node of LSEDUTs is affected by the charge injected, and three other charges are injected to the triple-level CG-SIM. As the proposed D-latch is symmetric, these situations should be considered: <N1, N13, N16, Q>, <N1, N13, N14, N16>, <N1, N14, N16, N17>, and <N1, N13, N14, N15>. When one charge is injected into an LSEDUT node, such as N1, the node can recover; then as LSEDUTs can be self-recovered, so do N1, N3, N5, N7, N9, and N11 having yet valid values, and even if the triple-level CG-SIM is affected by three charges injected to different nodes, Q can be recovered by the LSEDUTs. As a result, the proposed D-latch is immune and self-recoverable against QNU in case 2.

*Case 3:* two nodes of the LSEDUTs are affected by QNU, and two other charges affect the triple-level CG-SIM. For this case, these node quadruplets should be considered: <N1, N5, N13, N16>, <N1, N5, N16, N17>, <N1, N5, N14, N15>, and <N1, N5, N17, Q>. As the LSEDUT is not self-recoverable when charges are injected to N1 and N5, in this case, there is a soft error. This soft error can affect the value of N13 and when N14 is affected by the charge injected, they can change the value of N16. But, as the triple-level CG-SIM has six inputs and despite the fact that two of them lose their value, the four others keep their valid values, in this case, N3, N7, N9, and N11 do not lose their values and N17 has valid value; therefore, Q is not being affected by these soft errors. Moreover, in the case of <N1, N5, N16, N17>, a similar explanation holds considering soft errors in N1 and N5. The value of N13 is affected by these soft errors and N13 is upset, but despite the soft errors in N16 and N17 and the potential effect on Q, this effect is temporary because N3, N7, N9, and N11 hold valid values, and therefore can recover the values of N16 and N17. The value of Q can be recovered by the last stage of the CG-SIM, which means that the output is not affected by QNU. In the cases <N1, N5, N14, N15> and <N1, N5, N17, Q>, the analysis is the same and the value of Q is not affected by QNU. Therefore, QNU cannot induce a change of the value of Q in the proposed D-latch, which is immune against QNU in case 3.

*Case 4:* in this case, three charges affect the LSEDUTs and just one charge is affecting the triple-level CG-SIM. In this situation, the quadruplets of nodes <N1, N3, N5, N13>, and <N1, N5, N7, N13> should be analyzed. If three charges are injected into one LSEDUT, it cannot be self-recovered from the TNU. Therefore, there will be soft errors taking place in one LSEDUT. When N1, N3, and N5 lose their values, N13 is upset by QNU, but this soft error cannot change the value of N16 because N14 has a valid value. As a consequence, these soft errors cannot change the value of the output and

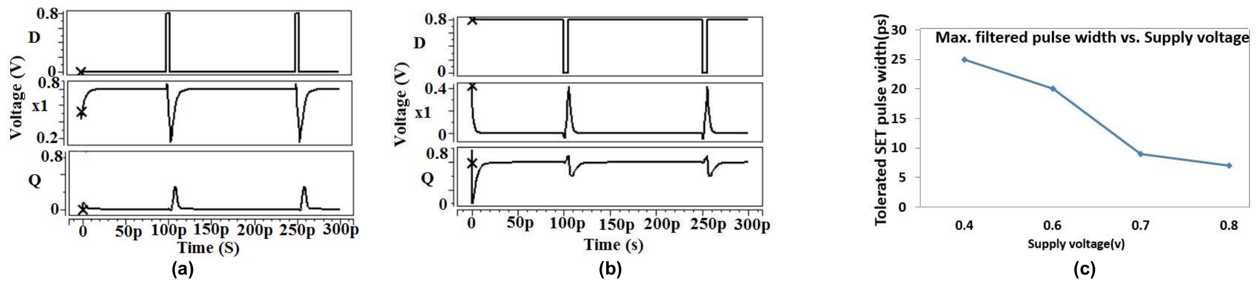


**FIGURE 3.** (a) SET positive pulse filtering capability of the proposed D-latch (b) SET negative pulse filtering capability of the proposed D-latch (c) maximum pulse width of SET filtered by the proposed D-latch at various supply voltages.

**TABLE 1.** Key pattern of SNU, DNU, and TNU injections of the proposed D-latch in Fig. 4.

| Time (ns) | SNUs/DNUs/TNUs | State | Time (ns) | SNUs/DNUs/TNUs | State | Time (ns) | SNUs/DNUs/TNUs | State | Time (ns) | SNUs/DNUs/TNUs | State |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5.15 | N1 | Q =1 | 16.0 | Q | Q=0 | 26.8 | N1, N16, N17 | Q =1 | 36.0 | N1, N13, N16 | Q=0 |
| 5.2 | N2 | Q =1 | 16.2 | N1, N2 | Q=0 | 27.0 | N1, N2, N13 | Q =1 | 36.2 | N1, N13, Q | Q=0 |
| 5.4 | N13 | Q =1 | 16.4 | N1, N3 | Q=0 | 27.2 | N1, N2, N16 | Q =1 | 36.4 | N1, N16, N17 | Q=0 |
| 5.5 | N16 | Q =1 | 16.6 | N1, N4 | Q=0 | 27.4 | N1, N2, Q | Q =1 | 36.6 | N1, N2, N13 | Q=0 |
| 5.6 | Q | Q =1 | 16.8 | N2, N3 | Q=0 | 27.6 | N1, N3, N13 | Q =1 | 36.8 | N1, N2, N16 | Q=0 |
| 5.7 | N1, N2 | Q =1 | 17.0 | N2, N5 | Q=0 | 27.8 | N1, N3, Q | Q =1 | 37.0 | N1, N2, Q | Q=0 |
| 5.8 | N1, N3 | Q =1 | 17.2 | N2, N4 | Q=0 | 28.0 | N1, N3, N16 | Q =1 | 37.2 | N1, N3, N13 | Q=0 |
| 5.9 | N1, N4 | Q =1 | 17.4 | N1, Q | Q=0 | 28.2 | N1, N2, N3 | Q =1 | 37.4 | N1, N3, Q | Q=0 |
| 6.0 | N2, N3 | Q =1 | 17.6 | N13, Q | Q=0 | 28.4 | N1, N2, N9 | Q =1 | 37.6 | N1, N3, N16 | Q=0 |
| 6.2 | N2, N5 | Q =1 | 17.8 | N1, N13 | Q=0 | 28.6 | N1, N3, N4 | Q =1 | 37.8 | N1, N2, N3 | Q=0 |
| 6.4 | N2, N4 | Q =1 | 25.2 | N13, N14, N16 | Q =1 | 28.8 | N1, N3, N9 | Q =1 | 38.0 | N1, N2, N9 | Q=0 |
| 6.5 | N1, Q | Q =1 | 25.4 | N13, N14, N17 | Q =1 | 29.0 | N2, N3, N4 | Q =1 | 38.2 | N1, N3, N4 | Q=0 |
| 6.6 | N13, Q | Q =1 | 25.6 | N13, N16, Q | Q =1 | 29.2 | N13, N14, N15 | Q =1 | 38.4 | N13, N14, N16 | Q=0 |
| 6.8 | N1, N13 | Q =1 | 25.8 | N16, N17, Q | Q =1 | 29.4 | N2, N3, N9 | Q =1 | 38.6 | N13, N14, N17 | Q=0 |
| 15.2 | N1 | Q=0 | 26.0 | N1, N17, Q | Q =1 | 35.2 | N13, N16, Q | Q=0 | 38.8 | N1, N3, N9 | Q=0 |
| 15.4 | N2 | Q=0 | 26.2 | N1, N13, N14 | Q =1 | 35.4 | N16, N17, Q | Q=0 | 39,0 | N2, N3, N4 | Q=0 |
| 15.6 | N13 | Q=0 | 26.4 | N1, N13, N16 | Q =1 | 35.6 | N1, N17, Q | Q=0 | 39.2 | N13, N14, N15 | Q=0 |

the proposed D-latch will remain immune against QNU in case 4.

*Case 5:* in this case, all of the charges are affecting the LSEDUTs. These lists of nodes can be considered for the analysis, <N1, N2, N3, N4>, <N1, N3, N7, N9>, and <N1, N3, N5, N7>. In this situation, the four charges can affect one LSEDUT, as <N1, N2, N3, N4> or three of them like <N1, N3, N5, N7>, or just two charges injected affect one LSEDUT like <N1, N3, N7, N9>. For the situation <N1, N3, N7, N9>, if two charges are affecting N1 and N3, they cannot recover by themselves and there are soft errors taking place in the LSEDUT. Also, N7 and N9 will have the same situation and they could not recover by themselves. This situation produces soft errors at the first stage of the triple-level CG-SIM and as N1, N3, N7, and N9 are upset, N14 upsets and loses its value. Nevertheless, these soft errors cannot change the value of N15 and N13 because N5 and N11 do not lose their values. The upset of N14 cannot change the value of N16, because N13 has the valid value. Consequently, Q is not affected by QNU. Other cases follow the same analysis and as a result, the proposed D-latch is immune against QNU in case 5.

## IV. SIMULATION

In this section, the DICE [26], TPDICE-based D-latch [27], high performance SEU tolerant (HSPT) latch [28], DNUCT [29], LSEDUT D-latch [25], QNUTL-CG D-latch [7], 4NUHL latch [30], and the proposed D-latch are simulated at 0.8 V supply voltage and 250 MHz frequencies at room temperature using Synopsys® HSPICE in 22 nm PTM technology. In this simulation, PMOS transistors have an aspect ratio W/L = 35 nm/22 nm, and NMOS transistors have an aspect ratio W/L = 24 nm/22 nm.

First, SET masking capability of the designed D-latch is tested. The proposed D-latch can filter undesirable pulses which are generated in the combinational digital circuit of previous D-latch stages. In the transparent mode, SET can be filtered by two clock-gating inverters in the direct path, which increases the delay but gives the extra feature to the proposed design. In Fig. 3(a) and 3(b), the input square positive and negative signals with 8 ps wide SET pulse at 0.8 V are shown demonstrating how this D-latch is designed to filter the SET pulse with the input signal in transparent mode (CLK = 1), based on simulation on [29].

As the SET filtering depends on the supply voltage, the maximum width of SET pulses filtered by the proposed D-latch at different supply voltages is shown in Fig. 3(c).

### A. RELIABILITY COMPARISON

One of the important test should be addressed is the evaluation of the proposed D-latch against SNU/DNU/TNU and QNU with a current transient (current source) simulating the charge injection given by the following mathematical

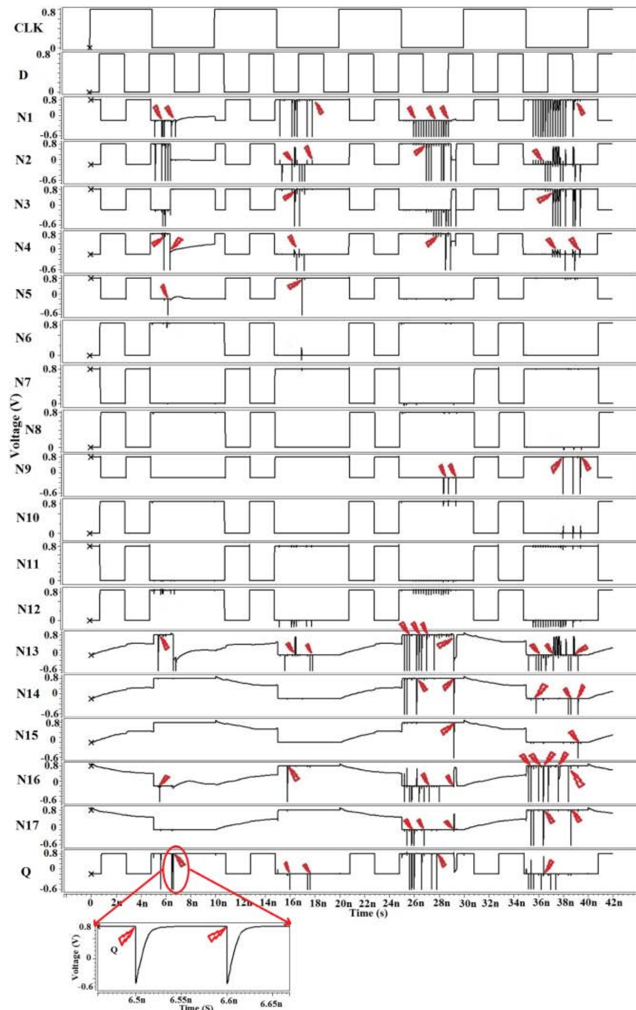

FIGURE 4. Simulation of the key patterns of SNU, DNU, and TNU injections for the proposed D-latch.

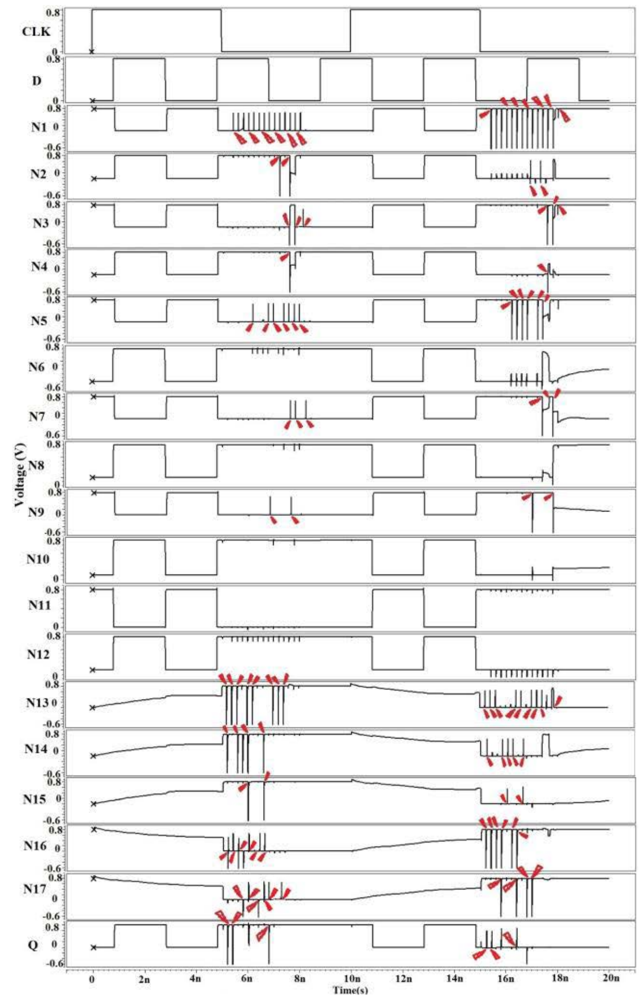

FIGURE 5. Simulation results of QNUs injected in the proposed D-latch.

expression [31]:

$$I = \frac{Q_{total}}{T\sqrt{\pi}}\sqrt{\frac{t}{T}}e^{-t/T} \tag{1}$$

In this simulation, $T$ is the value of the time constant of the injected current charge, which is 0.3 ps. $Q_{total}$ is the total charge injected being 50 fC in the worst case, which is large enough to prove immunity of the proposed D-latch against SNU/DNU/TNU and QNU [7].

For SNU simulation, one charge is injected to different nodes while the output node is monitored. When the output does not lose its logical value after this injection, it means it is immune against it. For DNU test, two charge injections are applied, three charge injections for TNU test, and four charge injections for QNU in different cases. As can be seen in Fig. 4, the output node does not change its value after SNUs, DNUs, and TNUs. Table 1 shows the key patterns of SNUs, DNUs, and TNUs used for the charge injection in Fig. 4. As can be seen, different key pattern injections of SNU, DNU, and TNU do not change the logical value of the output node, which means that the proposed D-latch is immune against SNUs, DNUs, and TNUs.

In Fig. 5, the simulation results of QNUs injection are shown. The pattern of injected QNUs is indicated in Table 2 in which "State" shows the value of the output node and "Time" shows the time of QNUs being injected into the proposed D-latch. As can be seen, the value of the output node does not change after the key patterns of QNUs are injected and proves that the proposed D-latch is immune against QNUs. But, this D-latch is not self-recoverable against QNUs.

Table 3 summarizes the immunity against SNUs, DNUs, TNUs, QNUs, featuring a high impedance state at the output node, and SET filtering comparison between the proposed D-latch and previous hardened D-latches. The DICE, HPST D-latches are only immune against SNU, whereas the TPDICE-based D-latch, DNUCT, and the LSEDUT D-latch are just immune against SNU and DNU.

Moreover, the 4NUHL and QNUTL-CG D-latches present immunity against SNU, DNU, TNU, and QNU, but they are not capable of filtering SET. Besides, the proposed D-latch has full immunity against SNUs, DNUs, TNUs, and

**TABLE 2.** Key patterns of QNUs injected in the proposed D-latch.

| Time (ns) | QNUs | State | Time (ns) | QNUs | State | Time (ns) | QNUs | State |
|---|---|---|---|---|---|---|---|---|
| 5.2 | N13, N14, N16, Q | Q =1 | 7.2 | N1, N2, N5, N13 | Q =1 | 16.2 | N1, N5, N13, N16 | Q=0 |
| 5.4 | N1, N13, N16, Q | Q =1 | 7.4 | N1, N5, N7, N13 | Q =1 | 16.4 | N1, N5, N16, N17 | Q=0 |
| 5.6 | N1, N13, N14, N16 | Q =1 | 7.6 | N1, N2, N3, N4 | Q =1 | 16.6 | N1, N5, N14, N15 | Q=0 |
| 5.8 | N1, N14, N16, N17 | Q =1 | 7.8 | N1, N3, N7, N9 | Q =1 | 16.8 | N1, N5, N17, Q | Q=0 |
| 6.0 | N1, N13, N14, N15 | Q =1 | 8.0 | N1, N3, N5, N7 | Q =1 | 17.0 | N1, N9, N13, N17 | Q=0 |
| 6.2 | N1, N5, N13, N16 | Q =1 | 15.2 | N13, N14, N16, Q | Q=0 | 17.2 | N1, N2, N5, N13 | Q=0 |
| 6.4 | N1, N5, N16, N17 | Q =1 | 15.4 | N1, N13, N16, Q | Q=0 | 17.4 | N1, N5, N7, N13 | Q=0 |
| 6.6 | N1, N5, N14, N15 | Q =1 | 15.6 | N1, N13, N14, N16 | Q=0 | 17.6 | N1, N2, N3, N4 | Q=0 |
| 6.8 | N1, N5, N17, Q | Q =1 | 15.8 | N1, N14, N16, N17 | Q=0 | 17.8 | N1, N3, N7, N9 | Q=0 |
| 7.0 | N1, N9, N13, N17 | Q =1 | 16.0 | N1, N13, N14, N15 | Q=0 | 18.0 | N1, N3, N5, N7 | Q=0 |

**TABLE 3.** Immunity against SNU, DNU, TNU, and QNU, and his insensitivity, and set filtering of the proposed D-latches.

| D-latch | Full Immune SNU | Full Immune DNU | Full Immune TNU | Full Immune QNU | HIS insensitive | Filtering SET |
|---|---|---|---|---|---|---|
| DICE [26] | ✓ | × | × | × | × | × |
| TPDICE based D-latch [27] | ✓ | ✓ | × | × | ✓ | ✓ |
| HPST [28] | ✓ | × | × | × | × | × |
| DNUCT [29] | ✓ | ✓ | × | × | ✓ | × |
| LSEDUT [25] | ✓ | ✓ | × | × | ✓ | × |
| QNUTL-CG [7] | ✓ | ✓ | ✓ | ✓ | ✓ | × |
| 4NUHL [30] | ✓ | ✓ | ✓ | ✓ | ✓ | × |
| Proposed D-latch | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

QNUs and it has two other beneficial features such as HIS insensitivity and SET filtering. Also, following this section, the simulation results of the process variations show that this design is more robust against (W/L) transistor aspect ratio and threshold voltage variability.

### B. COST COMPARISON

To stablish a fair comparison, the previous hardened D-latches (DICE, HPST, TPDICE-based D-latch, DNUCT, LSEDUT, 4NUHL, and QNUTL-CG D-latches) and the proposed D-latch are designed with the same PMOS and NMOS aspect ratios as stated at the beginning of Section 4, as the same strategy in [7]. Table 4 shows a comparison of D-latches related to area consumption, delays, power consumption, and PDP (Power-Delay Product), AOSF (ability of SET filtering), and minimum charge injections. These reported numbers are rounded.

As can be stressed out, the area penalty of the proposed D-latch is not unrestrained (especially compared to QNUTL-CG) and it provides better reliability. For example, DICE has 1 $\mu m^2$ area consumption, but it has just immunity against SNU also is sensitive to high impedance state and cannot filter SET. The more recent D-latch, QNUTL-CG D-latch, is immune against SNU, DNU, TNU, and QNU, but it is not able to filter SET.

Another important parameter to be consigned is the (D-Q) delay and (CLK-Q) delay. As can be seen from Table 3, the two D-latches that can filter SET are the TPDICE-based D-latch and the proposed D-latch; this characteristic impacts on the delay, thus, the proposed D-latch does not feature the minimum delay (in the proposed D-latch, a Schmitt trigger inverter is not used as in the TPDICE-based D-latch because of its penalty on process variation and huge (D-Q) delay). Also, (D-Q) delay can be calculated just in the transparent mode because in the holding time mode, there is not any connection between input and D-latch. Moreover, the latch is working based on switching, therefore, the setup time for data should be calculated, which can be delay (D-Q) pulse to delay (clk-Q).

One of important parameter for benchmarking the proposed D-latch SET filtering is AOSF (ability of SET filtering), defined in [1]. This parameter is calculated from the ratio of maximum width of filtering SET divided by delay (D-Q) (in percentage). The better AOSF of the proposed D-latch compared to the TPDICE-based latch is due to the huge delay introduced by the Schmitt trigger (despite it features a better SET filtering). Moreover by tuning the aspect ratio of the transistors, the SET filtering capability in the transparent path can increase beyond 8 ps, which is a common technique in the STI approach [27].

Based on the reliability of the hardened D-latch against charge injections, the minimum charge injections that can produce SNU in different nodes of latches are calculated [32].

As the proposed D-latch is designed based on clock-gating C-elements and uses two different paths for transparent mode and holding time mode, the power consumption is much lower in comparison with the TPDICE-based D-latch, DICE, LSEDUT, DNUCT, 4NUHL D-latches, and features the same

**TABLE 4. Comparative area of D-latches.**

| D-latch | Proposed D-latch | TPDICE-based | LSEDUT | DICE | QNUTL-CG | 4NUHL | HPST | DNUCT |
|---|---|---|---|---|---|---|---|---|
| Area $(\mu m)^2$ | 4.6 | 2.1 | 2.1 | 0.9 | 3.9 | 3.3 | 0.94 | 3.1 |
| Power consumption $(\mu W)$ | 0.5 | 1.0 | 3.0 | 0.74 | 0.5 | 4.3 | 0.18 | 0.53 |
| (D-Q) Delay $(ps)$ | 8.3 | 11.8 | 0.56 | 18.2 | 0.53 | 0.48 | 0.48 | 0.53 |
| (CLK-Q) Delay $(ps)$ | 4.47 | 9.8 | 0.65 | 21.62 | 0.62 | 0.57 | 0.56 | 0.63 |
| Delay(set up data) $(ps)$ | 12.77 | 21.6 | 1.21 | 39.82 | 1.15 | 1.05 | 1.04 | 1.16 |
| PDP $(10^{-18}\times W)$ | 4.27 | 12 | 1.7 | 13.4 | 0.3 | 2.1 | 0.09 | 0.28 |
| AOSF | 84.3% | 67.8% | - | - | - | - | - | - |
| Qcrit (fc) | 20 | 10 | 6 | 4 | 10 | 15 | 6 | 5 |

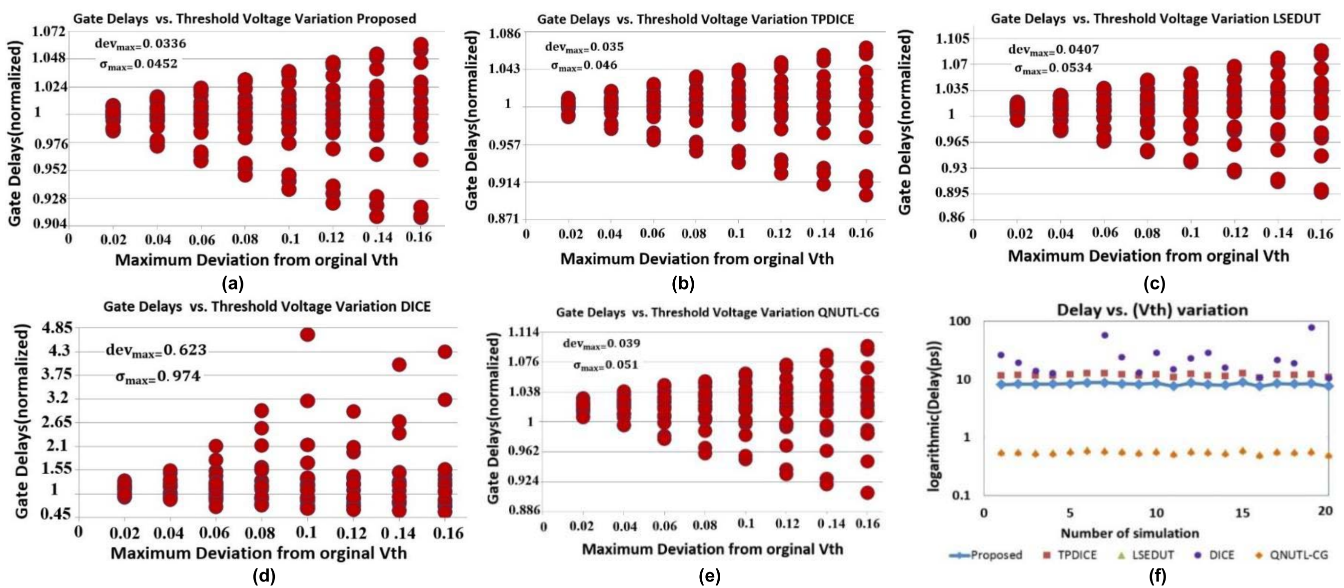


**FIGURE 6.** Threshold voltage variation effect on the D-latch delay: (a) proposed D-latch (b) TPDICE-based D-latch (c) LSEDUT latch (d) DICE (e) QNUTL-CG latch (f) delay of D-latches with maximum deviation, 0.16, from original threshold voltage.

power consumption that QNUTL-CG, even if it has extra sub-circuit to filter SET.

### C. PROCESS VARIATION

Due to the technology scaling race, process variability has become one challenging issue for integrated circuits [33]. In this section, we carry out a comparison of the impact on the gate delay and power consumption of the process variability induced by (W/L) and transistor threshold voltage fluctuations in the proposed D-latch and some of previous D-latches. For this comparison, Monte Carlo simulations with Gaussian distribution are used to model (W/L) and threshold voltage variability [33]. The maximum deviations of the original value of (W/L) and threshold voltages are between 2% to 16% with 20 simulations [33]. These simulations are run for each of these deviations, and the effects of these variations are monitored on power consumption and delay.

In Fig. 6, the effect of threshold voltage variability on delay is shown. As can be seen, the threshold voltage variability has a lesser impact on the delay variation in the proposed D-latch compared with other existing hardened D-latches. The maximum standard deviations of gate delays are given in the insets for each D-latch. These numbers for the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 0.0336, 0.035, 0.0407, 0.623, and 0.039, respectively. Furthermore, the maximum variance of the gate delay of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 0.0452, 0.046, 0.0534, 0.974, and 0.051, respectively. This comparison demonstrates that the delay of the proposed D-latch has less variation when threshold voltages of transistors are changed.

The maximum standard deviation improvements of the gate delay of the proposed D-latch compared with TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 4%, 17.4%, 94.6%, and 13.8%, respectively. The maximum variance improvements of the gate delay of the proposed D-latch compared with TPDICE-based D-latch,

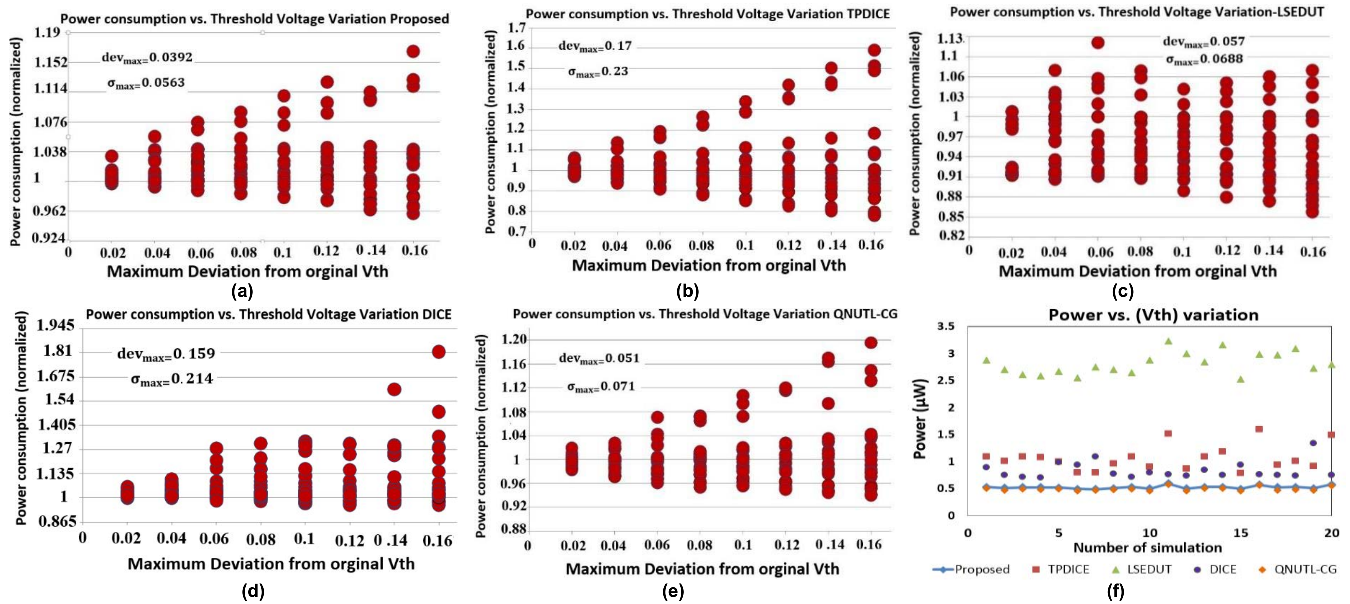


**FIGURE 7.** Threshold voltage variation effect on power consumption: (a) proposed D-latch (b) TPDICE-based D-latch (c) LSEDUT latch (d) DICE (e) QNUTL-CG latch (f) power consumption of D-latches with maximum deviation, 0.16, from original threshold voltage.

LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 1.7%, 15.3%, 95%, and 11.3%, respectively.

In Fig. 7, the power consumption of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch is shown when the threshold voltages of the transistors are subjected to variability reproduced with Monte Carlo simulations. The maximum standard deviations of power consumption of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 0.0392, 0.17, 0.057, 0.159, and 0.051, respectively. The maximum variance of the power consumption of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 0.0563, 0.23, 0.0688, 0.214, and 0.071, respectively. The result of this comparison shows that the variance and standard deviation of the power consumption are minimum for the proposed D-latch. The maximum standard deviation improvements of the power consumption for the proposed D-latch compared with TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 76.9%, 31%, 75%, and 23%, respectively. The maximum variance improvements of the power consumption of the proposed D-latch compared with TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 75%, 18%, 73.6%, and 20.7%, respectively.

The lower impact from process variation can be attributed to the non-active feedback loop in transparent mode, as the positive feedback loop increases the circuit sensitivity to parameters of process variations [34]–[35]. Also, to filter SET in the transmission mode, two inverters are applied in this proposed D-latch instead of Schmitt trigger circuit which is used in the TPDICE-based D-latch [27] (the Schmitt trigger inverter, due to the hysteresis property, impacts noticeably on parameters related to process variation). Also, the heavy use of stacked transistors decreases the impact of process variation parameters on delay and power consumption [3].

The other parameter seriously affected by process manufacturing variability is (W/L) transistor aspect ratio, which as in the case of the threshold voltage can be simulated by Monte Carlo methods with a Gaussian distribution. Results on the impact of this variability on the gate delay and power consumption are described next through Fig. 8 and 9.

In Fig. 8, the gate delay variation of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch in regard to the maximum variability of the original W/L is shown. The lower gate delay variation of the proposed D-latch in comparison with those of TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch is worth mentioning. The maximum standard deviations of gate delay of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 0.0147, 0.016, 0.017, 0.483, and 0.0156, respectively.

Also, the maximum variance of gate delay of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 0.0179, 0.022, 0.0205, 0.746, and 0.0198, respectively. The maximum standard deviation improvements of the gate delay of the proposed D-latch compared with TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 8.1%, 13.5%, 96.9%, and 5.7%, respectively. The maximum variance improvements of gate delay of the proposed D-latch compared with the TPDICE- based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 18.6%, 12.6%, 97.6%, and 9.5%, respectively.

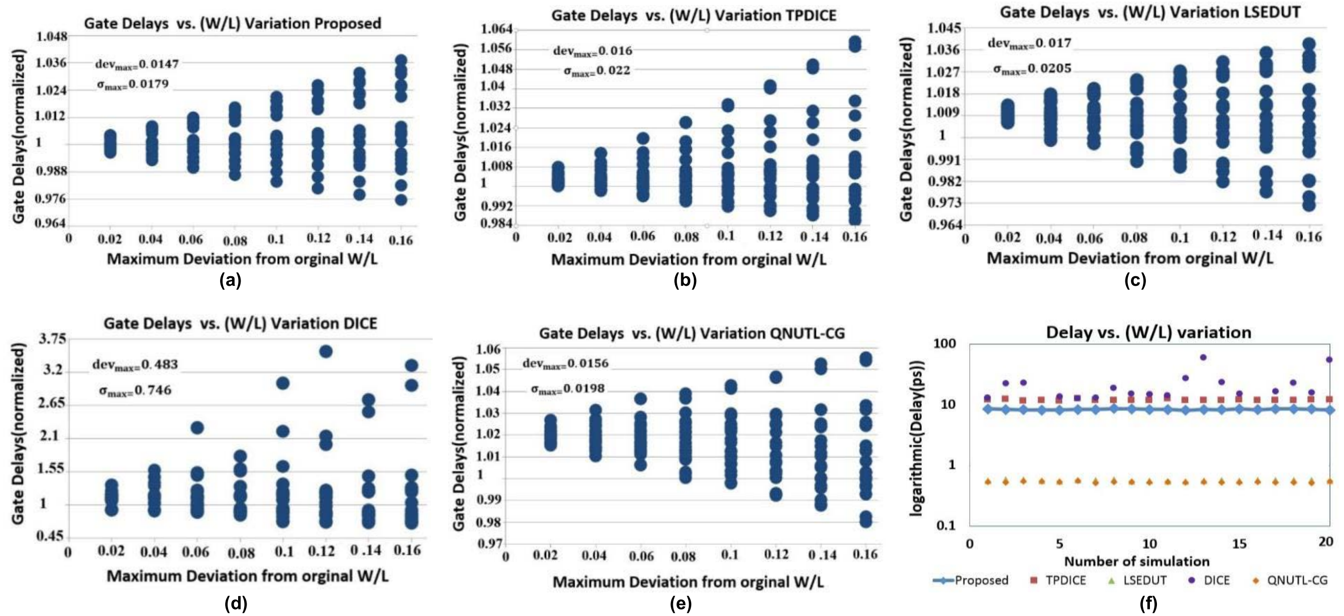


**FIGURE 8.** (W/L) variation effect on D-latch delay: (a) proposed D-latch (b) TPDICE-based D-latch (c) LSEDUT latch (d) DICE (e) QNUTL-CG latch (f) delay of D-latches with maximum deviation, 0.16, from original W/L.

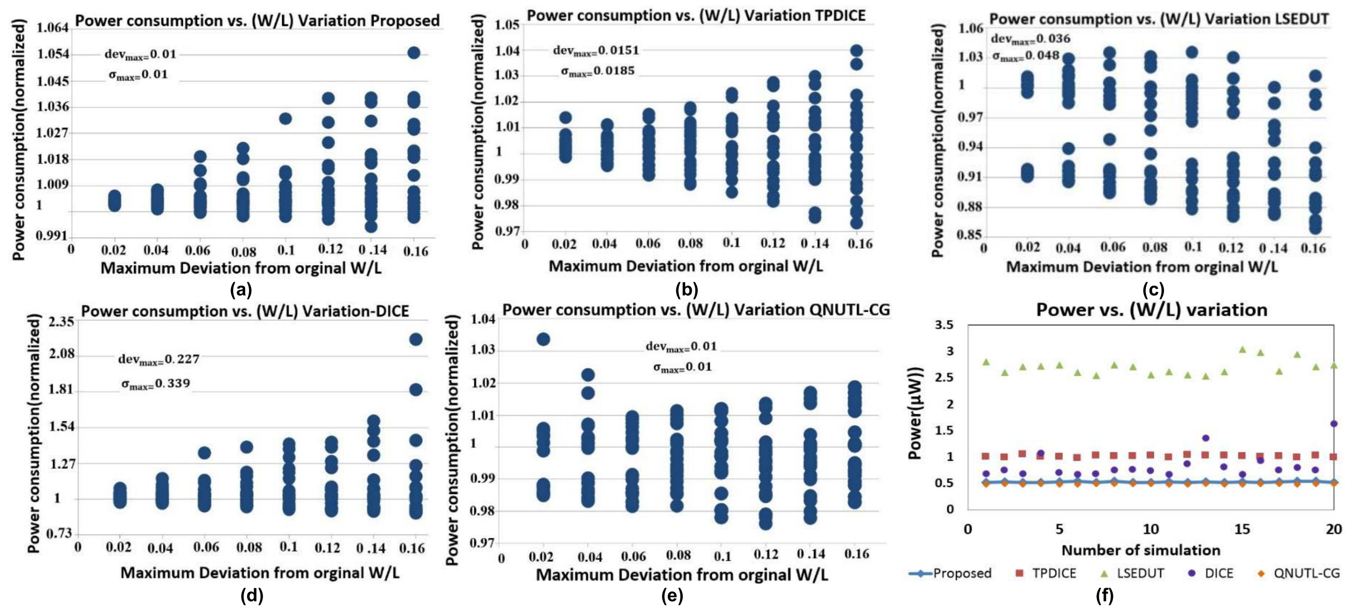


**FIGURE 9.** (W/L) variation effect on power consumption: (a) proposed D-latch (b) TPDICE-based D-latch (c) LSEDUT latch (d) DICE (e) QNUTL-CG latch (f) power consumption of D-latches with maximum deviation, 0.16, from original W/L.

In Fig. 9, the power consumption variation as the result of (W/L) transistor variability of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch is shown. The maximum standard deviations of power consumption of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 0.01, 0.0151, 0.036, 0.227, and 0.01, respectively. The maximum variances of power consumption of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 0.01, 0.0185, 0.048, 0.339, and 0.01, respectively. The result of this comparison shows that the variance and standard deviation of the power consumption are minimum for the proposed D-latch. The maximum standard deviation improvements of the power consumption of the proposed D- latch compared with TPDICE-based D-latch, LSEDUT D-latch, and DICE are 51%, 72%, 95.5%, respectively. The maximum variance improvements of the power consumption of the proposed

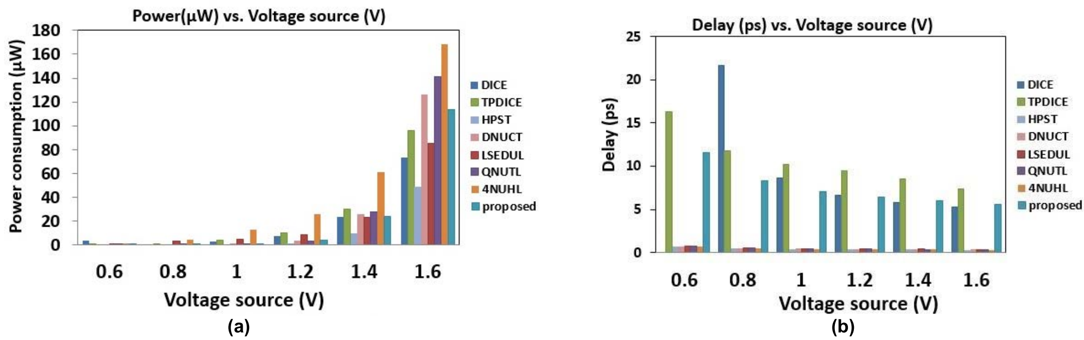


**FIGURE 10.** Impact of supply voltage variation on: (a) Power consumption (b) Delay.

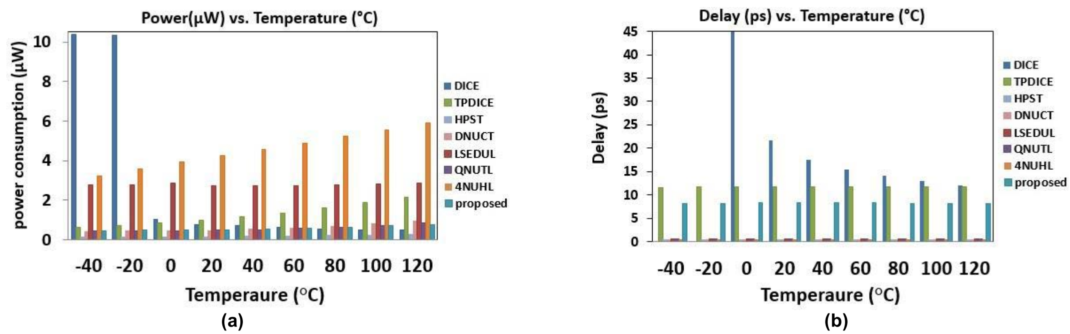


**FIGURE 11.** Impacts of temperature variation on: (a) Power consumption (b) Delay.

D-latch compared with the TPDICE-based D-latch, LSEDUT D-latch, and DICE are 45.9%, 79%, and 97%, respectively. The maximum variance and standard deviation of proposed D-latch and QNUTL-CG D-latch present the same value.

### D. PVT VARIATIONS

One additional parameter that should be considered to evaluate the performance of hardened D-latches is the impact of voltage and temperature (PVT) variations on the delay and power consumption. In this subsection the PVT variations impact of the proposed D-latch and previous D-latches are examined and benchmarked.

Figure 10 shows the impact of the variation of supply voltages (0.6 V-1.6 V) on the power consumption and delay (D-Q). In figure 10 (a), the power consumption rises by increasing the supply voltage. The reason is that by increasing the supply voltage, dynamic and static power increase (capacitors accumulate more charge and transistors drive more current [3]). Additionally, the delay of D-latches reduces due to the large current driven by the transistors, as shown in figure 10 (b).

In figure 11, the impact of temperature variation on the power consumption and delay (D-Q) is shown. The temperature variation has been evaluated in the industrial range from −40° C to 120° C. As the mobility of carrier reduces by rising temperature, power consumption increases. But, the delay is not affected by the temperature expect for the case of DICE, since most of D-latches have one transmission gate from input to output in transparent mode. Two D-latches, TPDICE and proposed D-latch have more sub-circuits to filter SET, but their delays are not affected by temperature range. As can be seen in figure 11, the proposed D-latch is the less affected by the impact of temperature variation on power consumption and delay in comparison with other previous D-laches.

## V. CONCLUSION

Scaling CMOS technology increases the demand for D-latch reliability to tackle harsh radiative environments. Under this premise, in this manuscript, a high reliability D-latch against temperature, process variation, and immunity against SNUs, DNUs, TNUs, and QNUs is presented. Moreover, the proposed D-latch has an additional feature with regard to the recently proposed QNUTL-CG D-latch (able to tolerate QNUs): it can mask SET in the input signal, without impacting on the power consumption (as compared with the QNUTL-CG D-latch). This lower power consumption with the extra SET masking feature and better process variation reliability is achieved by using clock-gating technology. Furthermore, compared with the QNUTL-CG D-latch, the improvements of the maximum standard deviation of the gate delay, which are the result of threshold voltage and (W/L) transistors variability of the proposed D-latch, are 13.8% and 5.7%, respectively and the improvement of the maximum standard deviation of power consumption, which is the result of threshold voltage variability of the proposed

D-latch, is 23%. The improvements of the maximum variance of the gate delay, which are the result of threshold voltage and (W/L) transistors variability of the proposed D-latch are 11.3% and 9.5%, respectively and improvement of the maximum variance of power consumption, which is the result of threshold voltage variability of the proposed D-latch is 20.7%. Finally, the maximum standard deviation and variance of the power consumption induced by (W/L) transistor variability of the proposed D-latch are similar to QNUTL-CG D-latch. Furthermore, the additional benefits and high reliability do not come at a huge increase of the maximum value of area, power consumption, delay and PDP reached by the other hardened alternatives.

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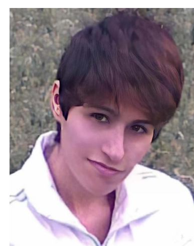

**SEYEDEHSOMAYEH HATEFINASAB** received the bachelor's and master's degrees in electrical, electronic engineering. She is currently pursuing the Ph.D. degree with the University of Granada, Spain. Previously, she was working in analog and digital circuits in several research institutions and companies. Her research interests include VLSI, microelectronics reliability, and fault tolerance. She has published several manuscripts on these topics.

**AKIKO OHATA** received the B.Sc. degree in applied physics from Waseda University, and the M.Sc. degree in applied physics and the Ph.D. degree in electronics engineering from the Tokyo Institute of Technology, Tokyo, Japan. She worked with the Toshiba Re-search and Development Center, Osaka City University, Utsunomiya University, and the Institute of Space and Astronautical Science (ISAS). She was a Visiting Researcher at the IBM-Thomas J. Watson Research Center (USA) and Grenoble-INP (France). She currently works at High Energy Accelerator Research Organization (KEK), Japan. Her research interests include small-sized semiconductor devices and scaling effects.

**ALFONSO SALINAS** was born in Granada, Spain, in 1978. He received the M.Sc. degree in chemistry and the Ph.D. degree in analytical chemistry from the University of Granada, in 2001 and 2005, respectively. He is currently working as a Researcher at the ECsens Group, University of Granada. His current research interests include optical sensors and biosensors, luminescent nanoparticles, and colorimetric sensors.

**ENCARNACION CASTILLO** received the M.A.Sc. and Ph.D. degrees in electronic engineering from the University of Granada, in 2002 and 2008, respectively. From 2003 to 2005, she was a Research Fellow at the Department of Electronics and Computer Technology, University of Granada, where she is currently a Tenured Professor. All this work has led to the publication of 33 articles in indexed journals and more than 50 contributions to international conferences. She has coauthored two patents in Spain and contributed to 11 projects in the several national and regional programs, as well as 11 technology-transfer contracts. Her current research interests include cryptoprocessors on FPGA, memory devices, smart instrumentation, and acquisition and processing of biosignals.

**NOEL RODRIGUEZ** received the B.Sc. and M.Eng. degrees in electronics engineering from the University of Granada, in 2004, and the dual Ph.D. degree from the University of Granada and the National Polytechnic Institute of Grenoble, France, in 2008. From 2017 to 2020, he was the Head of the Pervasive Electronics Advanced Research Laboratory (PEARL), University of Granada. He is currently a Tenured Professor of electronics at the Department of Electronics and Computer Technology, University of Granada. He has coauthored 15 international patents several book chapters and more than 100 peer-reviewed scientific contributions. His current research interests include low-power energy conversion, memory devices, and new materials and devices for electronic applications. He received the First National Award of University Education and the Extraordinary Award for his Ph.D. degree.