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Model Identification to Validate Printed Circuit Boards for Power Applications: A New Technique

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ABSTRACT The idea of using model identification techniques in order to validate the design of printed circuit boards (PCBs) is proposed in this communication. With the term identification, it is intended to obtain the mathematical model of a system from input/output data. Actually, the quality requirements of PCB systems working with power devices are highly demanded by costumers of semiconductor companies. Due to the increasing market of power devices, the topic is of wide interest. In this note, a new approach is presented. It is based on both CAD techniques, used to simulate the board, and identification techniques, mainly based on linear models, to validate the board performance in the design phase. The main results regarding the analysis of the PCB design allow to establish if the PCB CAD procedures can be improved in order to elicit the parasitic effects aiming at compensating possible nonlinearity in the systems, thus providing the customers with reliable and simple models.

INDEX TERMS PCB for power systems, CAD, imperfections, model identification.

I. INTRODUCTION

The increase of power electronics in industrial applications has been extraordinary in the last decades, and the future trends will be further highly positive. The traditional applications will grow, moreover revolutionary very high-speed markets are actually pushing, such as automotive and power distribution. These fields will require semiconductor devices with growing reliability and performance. Moreover the Internet of Things is creating a power systems market displaying similar impressive strengths [1].

The semiconductor companies must today furnish the customer not only the semiconductor stocks but, if they want to be competitive, also a suitable layout of the printed circuit boards (PCBs) where the components are placed, in order to guarantee that parasitic effects and electromagnetic and thermal behavior of the complete system achieve the customer requirements.

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The problem of semiconductor companies is therefore not only to design the semiconductor devices and test the stocks but also to guarantee their performance when placed in the final systems. Computer-Aided-Design (CAD) packages to design electronic devices are not sufficient to cope with these market specifications. The companies must design and realize the boards with the performance required by the customers. Therefore the task of semiconductor companies is to approach such problems in the scenario of the systems-of-systems engineering world [2].

The complexity engineering approach is therefore the new strategy that must be followed in the next future. Companies are just approaching the PCB design by using and proposing new CAD tools [3], moreover in the next future it should be accomplished by specialized techniques that allow further improvements. As discussed in details in the following sections, extraction and characterization of parasitic effects are fundamental steps in the CAD of PCB layouts. Highly accurate methods based on curve fitting approaches [4] or supply chains [5] have been recently introduced with the aim of proposing design strategies which optimize the PCB

layout by minimizing parasitic effects. A strategy based on linking genetic algorithms with CAD software has been proposed in [6] in order to optimize the PCB layout of a DC-DC converter in terms of electromagnetic compatibility. The strategy is based on extracting the parasitic components and use simulated data to determine the layout which minimizes the parasitic effects. The analysis of parasitics impact in high-frequency operating conditions has been proposed in [7], where the optimized design of the PCB layout for high-frequency inverters devoted to wireless power transfer systems has been approached.

In this communication, we aim at reconsidering parasitic effects in PCBs showing how their presence, under specific circumstances, may regularize the global behavior of the circuit. From a series of experiences in the field, in fact, the problem of validating the dynamical behavior of PCB systems can be addressed during the design phase recurring to model identification techniques, where with the term *identification* we mean to derive a mathematical model from input/output data [8]. In particular, after an analysis of the boards and of the considered devices, the CAD simulation results are used as input signals to identify reliable models. The correct matching between the identified models with the data, gives the PCB designers the correct information for the successive optimization procedure which will finally lead to the physical implementation of a suitable PCB.

Therefore the model identification technique is proposed as an easy validation of the CAD project. The aim is to achieve a fast and guaranteed validation approach in order to reduce the time delays in delivery for the semiconductor companies. Moreover, from a scientific point of view, this approach will cover another aspect of the recent literature that regards the fact that imperfections can play a positive role in the system design [9], [10].

Moreover, even if the presence of the parasitic dynamics may elicit the nonlinear behavior of switching devices, thus providing nonlinear oscillations during the steady-state behavior, a qualitative modeling strategy can be integrated to the linear analysis giving a more accurate knowledge to the PCB designers. The literature reports several examples of experimental observation of unexpected chaotic oscillations in electronic devices and especially in power applications, even in simple circuit configurations [11]. Moreover, the chaotic effects discovered in the simulated model have been practically detected in AC-AC converters [12]. The strategy outlined in the paper ensures the possibility to understand the sources of nonlinear behavior and to reveal the presence of chaotic oscillation even before that the circuit has been implemented. A similar strategy has been also adopted in the literature with reference to integrated circuits [9], [12] allowing to determine analogous mathematical models whose behavior mimics the nonlinear oscillations observed in experiments.

The paper is organized as follows. In the Section II, the half-bridge power module and the designed PCB used in our experiments will be described. In the Section III, the main concepts on parasitic extraction are presented, while the CAD results deriving from the simulation of the board are discussed in the Section IV. The Section V will introduce the identification technique details and the obtained results will be presented, providing a critical discussion on the proposed approach. The qualitative analysis to model the nonlinear oscillations due to the parasitic dynamics is outlined in Section VI. In the Conclusions, the summary of the research is presented and the perspectives of the approach will be outlined.

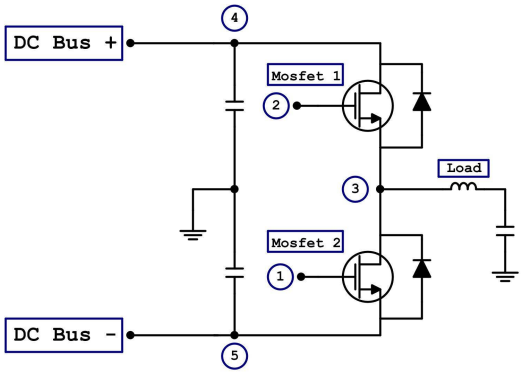

FIGURE 1. Schematic representation of the MOSFET-based half-bridge circuit: (1-2) inputs driving the low side gate and the high side gate, (3) intermediate output node between the two switches, (4) and (5) identifies the DC bus.

II. HALF-BRIDGE MODULE FOR POWER APPLICATIONS

The system under investigation is an advanced power system-on-board that supports gate drivers and two MOSFETs in half-bridge configuration on the same board. Applied in numerous circuit solutions, the half-bridge configuration, also known as *totem pole*, is one of the most common switching topologies currently used in power electronics.

From a topological point of view, the single phase Half Bridge circuit has two switches (typically MOSFETs) occupying the two sides, Low Side and High Side, of the bridge, defining the typical cascode configuration. The circuit is essentially a 5-points topology, as reported in Fig. 1.

Despite its circuit simplicity, in terms of design, construction and operation, this configuration has a number of critical issues that must be made clear to the designers. Among these critical points, we must consider the drive waveforms of the switches, the drive circuits of the MOSFET gates and the layout of the board.

For its proper working, the half-bridge requires a MOSFET driver system. In particular, the two-branch topology of the system requires the High Side gate driver circuit to be referenced to the output node voltage, while the Low Side gate driver is referenced to ground.

The two MOSFETs are switched on and off alternately, inserting a dead-time between the switching on of one and the switching off of the other, in order to prevent the two devices

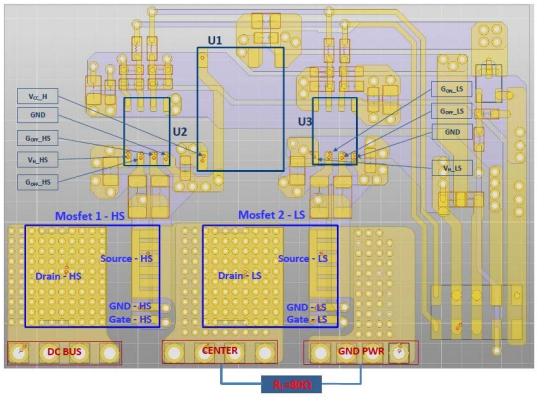

FIGURE 2. PCB of the designed half-bridge power system.

from being switched on at the same time leading the system to short-circuiting.

The MOSFETs gates drive circuit depends on the switching frequency, the intensity of the current to be switched and the construction characteristics of the MOSFETs. Naturally, in defining the complexity of the drive circuit, these parameters become increasingly critical as the corresponding values become higher and higher.

The PCB which is going to be designed for this circuit is a double layer board, as shown in Fig. 2. The components arrangement on the board represents another critical point in the implementation of the system. It is essential that the shortest possible connections are made between the drive circuits and their gates, and it must be ensured that not suitable ground connections do not cause latch-up of the gates driving circuit, as well as electromagnetic interference, or faulty switching. With reference to the schematic diagram in Fig. 1, the components are allocated on the PCB as reported in Fig. 2. In particular, the high side and low side MOSFETs are allocated in the lower part of the PCBs, where the connectors to the load are also present. The rest of the board allocates the driving circuitry.

III. PCB SIMULATIONS AND PARASITIC ELEMENTS

Many designers are used to think about system behavior in terms of circuit models only. These models and circuit diagrams are correct up to a point, but they lack some important information that determines the system behavior. Circuit boards traces are always associated with parameter values of equivalent resistors, capacitors, and inductors. The information that is missing from a circuit diagram is the geometry of a real PCB layout, which determines how elements in a system electrically and magnetically couple with each other.

This is governed by the interaction between the electromagnetic field and the matter, but a conceptual way to summarize signal behavior in a complex system is to think of coupling in terms of parasitic circuit elements.

Bringing parasitic circuit elements into a circuit model helps to explain unintended or undesired signals and power behavior in a real system, making parasitic modeling tools very helpful for understanding real circuit behavior. When board parasitic elements are not modeled during design simulations, their effect on circuit operation is not known until physical prototype testing, a phase in which it is expensive to make changes.

There are many aspects of a real system that create unintended parasitic elements in a PCB layout which cannot be considered in a circuit diagram.

- Geometry. The distance between various conductors, their arrangement on a board, and their cross-sectional area will determine DC resistance, parasitic capacitance, and parasitic inductance.
- Dielectric constant. PCB dielectrics have a high dielectric constant, which determines the parasitic capacitance between circuit elements.
- Magnetic permeability. For magnetic components, the magnetic permeability also plays a role in determining signal and power behavior as these components create parasitic inductance. Ferrite transformers and other magnetic components can act like inductors or radiators when operating at high frequencies.
- Traveling wave behavior. Any signal propagating in a real PCB and interconnects is a propagating waveform. The propagation of electromagnetic waves produces transmission line effects in interconnects, which cannot be modeled with a simple circuit diagram.

Parasitic elements include:

- Parasitic Capacitance is the, usually undesirable, inherent capacitance of a component, e.g., in a transformer, the capacitance between windings.
- Parasitic Inductance is the, usually undesirable, inherent inductance in a component, e.g., the inductance of a wirewound resistor.
- Parasitic Resistance is the, usually undesirable, inherent resistance of a component, e.g., in a capacitor, the finite resistance of the package leads.

Accounting for layout parasitic elements early in the design process reduces risk of downstream design iterations and is key to keep a project on time, on budget, and meeting specification. Furthermore, having this information during design development helps engineers ensure their designs will meet performance and reliability targets.

PCB mechanically supports and electrically connects electrical or electronic components using conductive tracks, pads and other features etched from one or more sheet layers of copper laminated onto and/or between sheet layers of a non-conductive substrate. Components are generally soldered onto the PCB to both electrically connect and mechanically fasten them to it. PCB complexity mandates performing different analysis types to ensure robust board performance.

This complexity is brought on by the ever-increasing bus data rates to provide large throughput; the need for maintaining constant impedance of nets, spanning multiple form factors; the high transmission loss caused by lossy laminate materials; the high-thermal power loss and temperature rise in

components and copper traces; and failure tests which need to be carried out for product qualifications. Success in electronic design often hinges on running simulations. Whether signal integrity, power integrity, electromagnetic compatibility, analog, or even thermal simulations, they reveal information about design feasibility, margins and limitations. We may perform simulations both before and after board layout, with different purposes, but the goal remains the same: to drive design changes. There exist different tools to analyze and simulate PCB. In general terms these simulation tools use a similar approach to solving a particular problem.

The key steps in the simulation process include:

1) Creation of the Physical Model: this step will usually involve the creation of the layout geometry together with the definition and assignment of material properties to objects contained within the layout geometry.
2) EM Simulation Setup: this step will usually include defining the extents of the simulation and the boundary conditions, the assignment of ports and specific simulation option settings.
3) Performing the EM Simulation: the physical model (layout geometry) must be discretized using 'mesh cells'. The field/current across the mesh cell is then approximated using a local function. The function coefficients are adjusted until the boundary conditions are satisfied.
4) Post-processing: Calculation of S-parameters, Far Field Radiation Patterns etc....

Thus, to produce a highly efficient PCB, a new design methodology should be followed to predict the PCB interconnect parasitic present in the layout:

1) Design the circuit schematic
2) Design the PCB layout
3) Perform a pure circuit simulation and achieve the performance requested
4) Create S-parameters model that includes parasitic effects using EM-simulation or extract the parasitic resistances, inductances and capacitances
5) Co-simulate the S-parameters model in the circuit schematic to analyze PCB interconnect parasitics effects on the circuit performance.

IV. CAD PERSPECTIVES FOR PCB MODELING AND SIMULATION

In order to get the simulated data from the design PCB layout described in the previous section, Ansys Electronics Desktop and Ansys SIwave [3], [13], [14] CAD tools have been used.

Ansys Electronics Desktop is a unified platform for electromagnetic, circuit and system simulation. Tools like Ansys HFSS, Maxwell, Q3D Extractor, and Simplorer are built natively in the Electronics Desktop, which serves as a universal Pre/Post processor for these tools. With Ansys Electronics Desktop, one can integrate electromagnetic analysis with system and circuit simulation. Schematics can be used to wire up different field solver models and create a model of a high-level system through dynamic links that combine 3D EM and SPICE circuit analyses.

Ansys SIwave is a specialized design platform for design of IC packages and PCBs. A hybrid 2.5D full wave EM field solver is able to model layered structures (Chip, PKG, PCB), and perform analysis related to Signal Integrity, Power Integrity, DC IR drop, EMI / EMC, decoupling capacitor optimization, etc. As a design and analysis platform, SIwave incorporates, or allows data exchange, with a series of tools that permit it to perform the assigned tasks optimally. In this way it is possible to access tools capable of predicting DC power delivery issues within PKGs and PCBs, Joule heating and temperature analysis (Icepak Solver), Parasitic extraction (CPA).

The simulations concern with the PCB analysis of the drive and power/switching section of the Master GaN Half-Bridge. In particular we distinguish two simulation scenarios:

- Pure Circuit Simulation (PCS): The system is simulated by considering the simple schematic in which the components are described by their circuit models, complete with all internal parasitic parameters, without taking into account the presence and influence of the PCB. The connections between the components are ideal. The schematic circuit diagram adopted to obtain Pure-Simulated data is reported in the Appendix B.
- Co-Simulation (CS): the system is simulated by considering the simple schematic in which the components are characterised from their pure circuit models, taking into account the presence and influence of the PCB. This is expressed through the action of ''parasitic components'' which, not present in the original schematic because they are not part of the models of components, nevertheless act on the dynamics of the system, altering the waveforms foreseen in the model formalised in the pure schematic. The schematic circuit diagram adopted to obtain Co-Simulated data is reported in the Appendix B.

The signals affected by the presence of parasitic parameters were sampled by SIwave at specific points on the PCB and related to topological areas linked to the dynamics of the controlled power components.

The examined area of the PCB is converted into an additional circuit element (highlighted in red) which contains the models of the circuit components present in the definition perimeter, the parasitic parameters deriving by the physics of the system and by the dynamic interaction between the tracks.

The importance of both PCS ans CS data relies on the fact that from the comparison of the respective models it is possible to gain information towards the validation of the PCB in the design phase, as discussed in the following.

V. IDENTIFICATION OF LINEAR MODELS FOR THE HALF-BRIDGE POWER SYSTEM

In accordance with the definition given by Lennart Ljung in [8], identification is an art for making mathematical models from input/output data. It can be said that the topic is

characterized by a small number of leading principles. The first one is the suitability of the data. The data that are available can be considered as a sequence of pulse response signals that are suitable for identification aims [15], [16], since any signal can be considered as a weighted sum of shifted impulses that are the condition to excite all the dynamical behavior of the system. The second fixed point is to consider signals free from noise. It is a certain sense guaranteed due to the fact that we are working with simulated data. The used models are linear time-invariant and the pole-zero maps, and therefore the models, are chosen in accordance both with the identification error and on some physical considerations. Even if noise is absent, the possible not good fitting of the model is often due to the intrinsic nonlinearities of electronic devices. A black-box identification approach is adopted, which is based on supposing that we neither have any information on the order of the system nor on some parameters. The classical least square method for model identification approach is used. In the appendix A, the main features of the used identification procedure are outlined. As concerns the choice of structure of the model, the number of poles n and zeros m of each identified model, with $n \geq m$, have been selected by using an integer optimization procedure that is applied to the normalized index $\Delta E = (\mathbf{y} - \tilde{\mathbf{y}})^{\mathrm{T}} (\mathbf{y} - \tilde{\mathbf{y}})$, where $\mathbf{y}$ is the considered output data and $\tilde{\mathbf{y}}$ is the estimated output.

In this section, we focus on the identification of linear model for the various input/output data. In particular, the following electrical quantities, referred to the scheme reported in Fig. 3, are extrapolated from simulations:

$V_{\mathrm{GS}}^{\mathrm{HS}}$: Voltage between Gate and Source in the High Side, in volts (V);
$V_{\mathrm{DS}}^{\mathrm{HS}}$: Voltage between Drain and Source on the High Side, in volts (V);
$V_{\mathrm{GS}}^{\mathrm{LS}}$: Voltage between Gate and Source in the Low Side, in volts (V);
$V_{\mathrm{DS}}^{\mathrm{LS}}$: Voltage between Drain and Source in the Low Side, in volts (V);

when the device is subjected to the inputs:

$V_{\mathrm{PWM}}^{\mathrm{HS}}$: Gate drive voltage in the High Side, in volts (V).
$V_{\mathrm{PWM}}^{\mathrm{LS}}$: Gate drive voltage in the Low Side, in volts (V).

The input/output data under consideration have been obtained when $V_{\mathrm{PWM}}^{\mathrm{HS}}$ and $V_{\mathrm{PWM}}^{\mathrm{LS}}$ are finite-duration pulses with duration $T = 0.1$ ms. A set of 35 measures for each scenario are used to identify the models discussed in the following subsections.

A. CASE 1

We estimate the transfer function between the input voltage $V_{\mathrm{PWM}}^{\mathrm{HS}}$ and the $V_{\mathrm{GS}}^{\mathrm{HS}}$ of the high side.

The identification by using the co-simulated data leads us to select a model with $n = 16$ and $m = 13$, as retrieved as the maximum of the surface illustrated in Fig. 4, where the model performance $\eta = 1 - \Delta E$ is computed for models with different number of zeros and poles. The same procedure

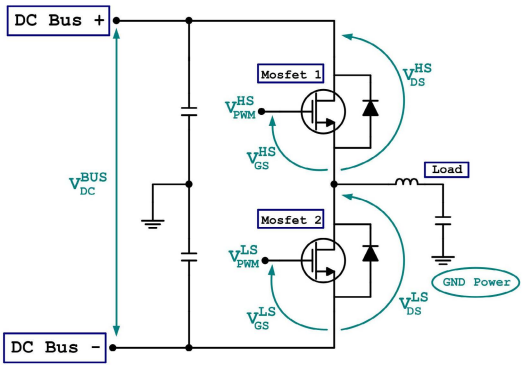

FIGURE 3. Schematic representation of the MOSFET-based half-bridge circuit explicating the voltages related to the input/output data under consideration.

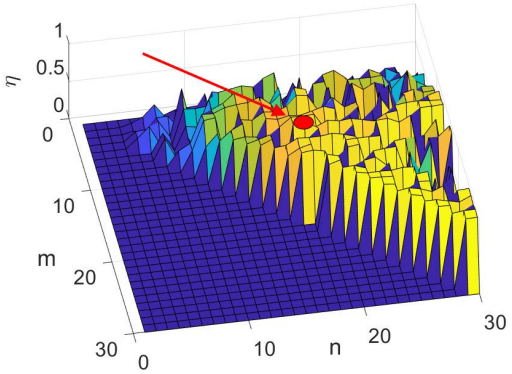

FIGURE 4. Evaluation of the optimal model structure for V_{GS}^{HS}/V_{PWM}^{HS}. The red patch indicates the best performance obtained for $n = 16$ and $m = 13$.

to determine the model structure is applied to all the cases discussed in the following. The pole-zero map and the trend of the output from the identified model are shown in Fig. 5. It is clear that the model matches the data both in the transient and during the duration of the pulse.

Let us consider now the data from a pure simulation, thus without the effect of the PCB. Of course we estimate a model with a lower order, in fact an optimal model that globally matches the behavior is obtained as illustrated in Fig. 6. However, even if the steady state of the pulse is completely matched, the transient does appear not well identified. The location of zeros and poles of the identified models are summarized in Tab. 1. Our experiments led us also to consider higher order models, moreover we observed that the performance tends to deteriorate both in transient and in the steady state. This means that in this case the PCB board plays a compensating role in mitigating both the non-idealities of the components and their possible nonlinearity.

The numerical evaluation of the model performances, as reported in Tab. 2, reflects and reinforces these considerations, as the error on the transient is always lower for the models from co-simulated data. This led us to conjecture that

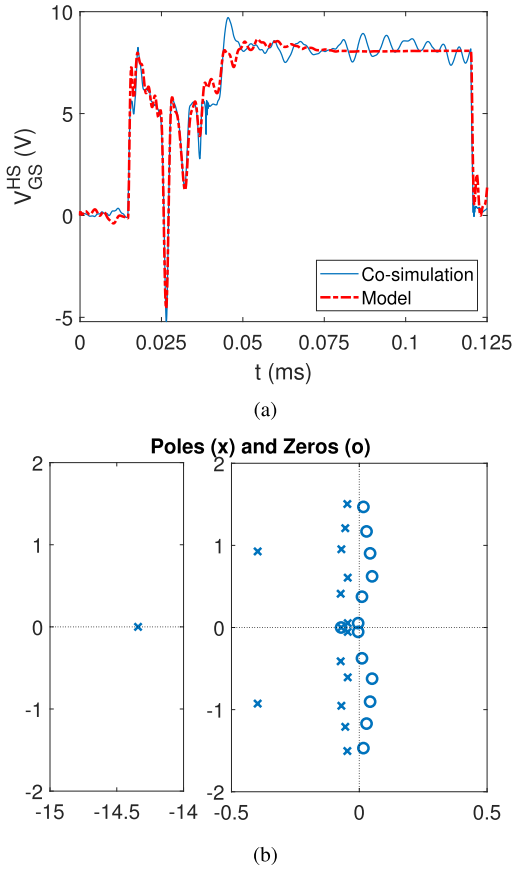

FIGURE 5. Modeling of V_{GS}^{HS}/V_{PWM}^{HS} in Co-simulation: (a) trends, (b) pole-zero map.

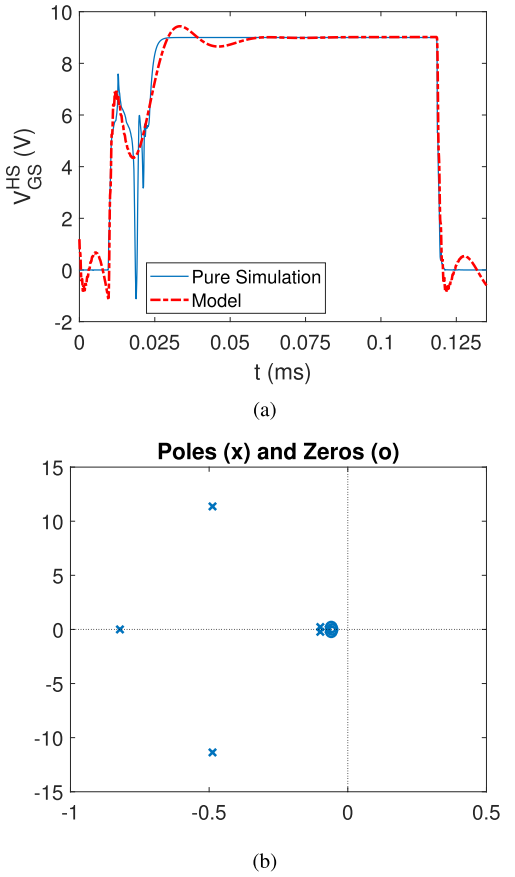

FIGURE 6. Modeling of V_{GS}^{HS}/V_{PWM}^{HS} in Pure-simulation: (a) trends, (b) pole-zero map.

TABLE 1. Normalized locations of zeros and poles of the identified linear models for V_{GS}^{HS}/V_{PWM}^{HS} (normalization factor 10^6 rad/s).

	PCS	CS
Poles	$-0.48 \pm 11.37j, -0.1 \pm 0.22j$ -0.82	$-0.04 \pm 0.05j, -0.047 \pm 1.5j$ $-0.05 \pm 1.2j, -0.07 \pm 0.95j$ $-0.04 \pm 0.6j, -0.07 \pm 0.4j$ $-0.39 \pm 0.93j, -0.07, -14.34$
Zeros	$-0.06 \pm -0.2j$	$0.02 \pm 1.47j, 0.03 \pm 1.17j$ $0.04 \pm 0.9j, 0.05 \pm 0.62j$ $0.01 \pm 0.38j, -0.004 \pm 0.05j$ -0.071

TABLE 2. Identification error (Mean Square Error, MSE) of the identified linear models for V_{GS}^{HS}/V_{PWM}^{HS}.

MSE	PCS	CS
Global	0.5226	0.5314
Transient fast-rise	1.1299	0.4315
Regime	0.2015	0.5290
Transient slow-down	0.6311	0.5212

PCB parasitic components play a good effect for a consistent and complete model identification.

B. CASE 2

Let us now consider the transfer function between the input voltage V_{PWM}^{HS} and the V_{DS}^{HS} of the high side. We remark that, the V_{DS}^{HS} trend is activated by the turning down of the high side input, therefore we focused only on its transient. The

TABLE 3. Normalized locations of zeros and poles of the identified linear models for V_{DS}^{HS}/V_{PWM}^{HS} (normalization factor 10^6 rad/s).

	PCS	CS
Poles	$-0.55 \pm 1.85j, -0.42$ -0.002	$-0.008 \pm 2.42j, -0.004 \pm 1.21j$ $-0.41 \pm 0.93j, -1.24 \pm 3.06j$ $-0.67, -0.001$
Zeros	$2.27, 0.1637$ -1.15	$0.45 \pm 2.43j, 0.64 \pm 1.4j$ $0.74 \pm 0.44j, -0.34 \pm 0.78j$

TABLE 4. Identification error (Mean Square Error, MSE) of the identified linear models for V_{DS}^{HS}/V_{PWM}^{HS}.

MSE	PCS	CS
Global	0.1591	0.1814
Transient fast-rise	0.2354	0.2342
Regime	0.023	0.069

effects of parasitic dynamics are not evident in both cases of pure and co-simulations, as shown in Figs. 7 and 8. In fact, the identification allows us to determine models, detailed in Tab. 3, which have generally good performance, summarized in Tab. 4.

C. CASE 3

Let us focus now on the low side of the half-bridge estimating the transfer function between the input voltage V_{PWM}^{LS} and

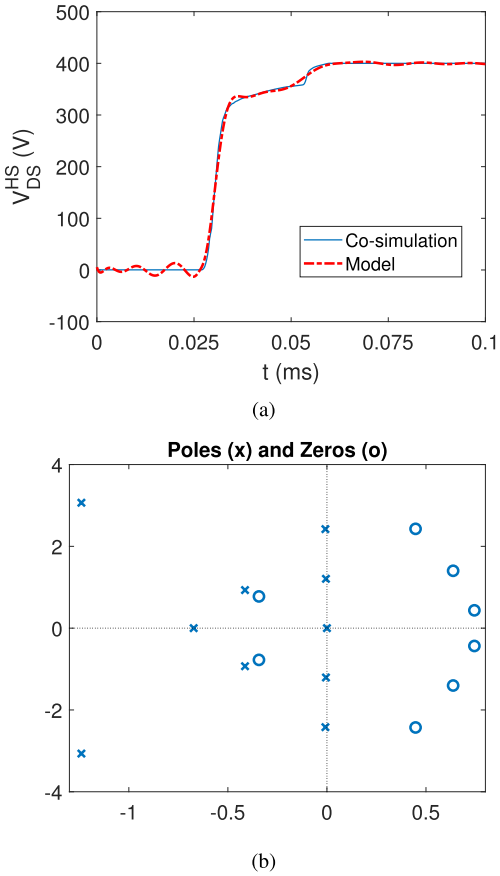

FIGURE 7. Modeling of V_{DS}^{HS}/V_{PWM}^{HS} in Co-simulation: (a) trends, (b) pole-zero map.

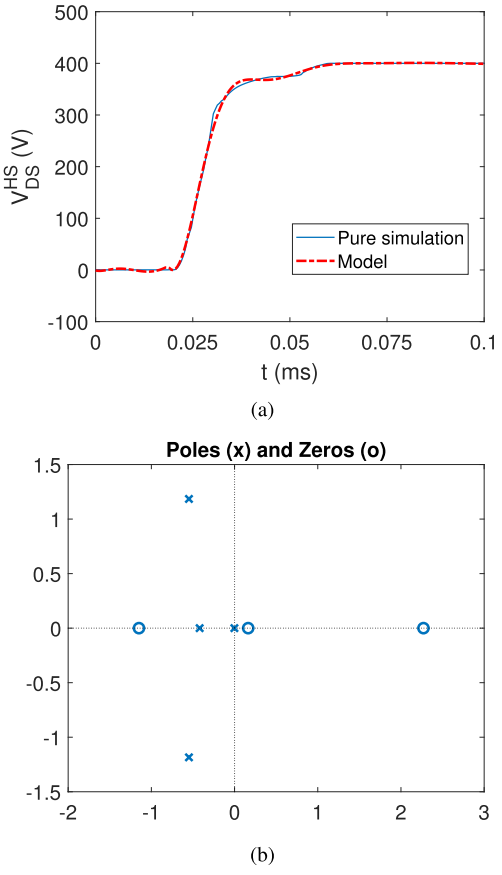

FIGURE 8. Modeling of V_{DS}^{HS}/V_{PWM}^{HS} in Pure-simulation: (a) trends, (b) pole-zero map.

TABLE 5. Normalized locations of zeros and poles of the identified linear models for V_{GS}^{LS}/V_{PWM}^{LS} (normalization factor 10^6 rad/s).

	PCS	CS
Poles	$-3.27 \pm 4.69j, -0.08 \pm 1.46j$ $-0.19 \pm 0.84j, -0.33 \pm 0.37j$ $-0.001 \pm 0.77j, -0.005 \pm 0.39j$ $-0.19 \pm 0.80j$	$0.0005 \pm 1.86j, -0.0004 \pm 0.19j$ $-0.01 \pm 1.1j, -0.03 \pm 1.445j$ $-0.03 \pm 0.67j, -0.04 \pm 0.35j$ $-0.05 \pm 0.5j, -0.07$ $-0.08 \pm 0.26j, -0.16 \pm 0.69j$ -1.04
Zeros	$0.05 \pm 0.75j, 0.04 \pm 0.43j$ $-0.03 \pm 1.47j, -0.01 \pm 0.88j$ $-0.115 \pm 0.23j$	$0.04 \pm 0.6j, 0.02 \pm 0.22j$ $0.001 \pm 0.41j, -0.01 \pm 0.71j$ $-0.06 \pm 0.01j, -0.08 \pm 0.35j$ -0.8

TABLE 6. Identification error (Mean Square Error, MSE) of the identified linear models for V_{GS}^{LS}/V_{PWM}^{LS}.

MSE	PCS	CS
Global	0.2173	0.3464
Transient fast-rise	0.2915	0.2513
Regime	0.2595	0.3639
Transient slow-down	0.2513	0.3452

the V_{GS}^{LS}. We emphasize that as regards the co-simulation data based identification, a good model is estimated as it follows with a good matching the data, as reported in Fig. 9. We remark that the trends are particularly attractive in the transient phases. However, it can be seen from Fig. 10 that this is not the case when pure simulation data are considered, and therefore it once again confirms our findings of Case 1, i.e. the presence of parasitic dynamics has a linearizing effect on the whole transfer function. The steady-state behavior is quite well estimated, but this does not occur in the transient also changing the structure of the model. The details of the estimated models are reported in Tab. 5, while their performance, reflecting the capability of the models from co-simulation of catching up with the transient behavior, are summarized in Tab. 6.

D. CASE 4

Finally, let us consider the estimation of the transfer function between the input voltage V_{PWM}^{LS} and the V_{DS}^{LS} of the low side. This last example remarks again the consideration made for examples 1 and 3, as the model from co-simulated data, shown in Fig. 11, is able to follow the co-simulated behavior especially in the transient phase, while the pure simulations lead to a model which catches up with the regime behavior, as reported in Fig. 12. The location of poles and zeros of the estimated models are reported in Tab. 7, and their performance are summarized in Tab. 8.

The previous examples have been chosen to remark a concept that arose during these studies. In fact, they are used to remark a strong principle. In some cases, the PCB behavior makes the system globally linear, therefore, the parasitic effects working in the board can improve the behavior of

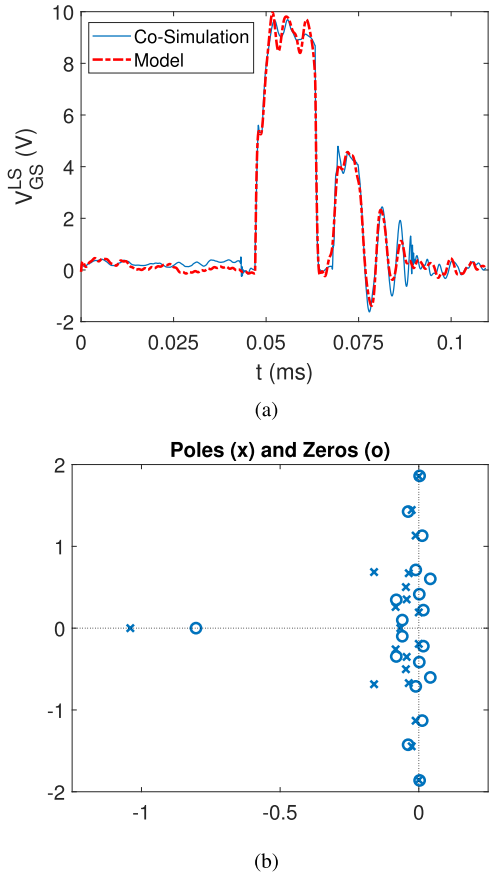

FIGURE 9. Modeling of V_{GS}^{LS}/V_{PWM}^{LS} in Co-simulation: (a) trends, (b) pole-zero map.

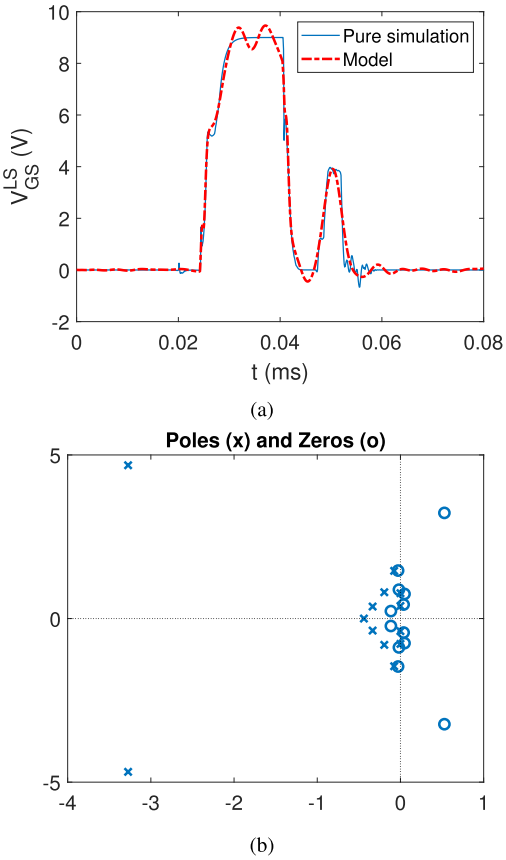

FIGURE 10. Modeling of V_{GS}^{LS}/V_{PWM}^{LS} in Pure-simulation: (a) trends, (b) pole-zero map.

TABLE 7. Normalized locations of zeros and poles of the identified linear models for V_{DS}^{LS}/V_{PWM}^{LS} (normalization factor 10^6 rad/s).

	PCS	CS
Poles	$-0.01 \pm 0.05j, -0.0005$ -0.02	$-0.00004, -0.002 \pm 0.07j$ $-0.003 \pm 0.06j, -0.007 \pm 0.037j$ $-0.01 \pm 0.02j, -0.009$
Zeros	$0.03 \pm 0.028j$	$0.02, 0.018 \pm 0.03j$ $-0.007 \pm 0.05j, -0.01$

TABLE 8. Identification error (Mean Square Error, MSE) of the identified linear models for V_{DS}^{LS}/V_{PWM}^{LS}.

MSE	PCS	CS
Global	0.2134	0.2242
Transient fast-rise	0.8021	0.1665
Regime	0.0971	0.2271

the board. This fact induces the possibility of using a new PCB design approach to favor this effect. Indeed, in classical design the PCB negative effects lead the designer to avoid parasitic effects. Moreover, in more cases we have processed, we discovered that the parasitic effects work in cooperation and improve the linear behavior of the board. This is particularly appealing, in fact it is shown in [9] that in some cases real imperfections or parasitic effects lead to some emerging unexpected behavior that improve the performance of the real system.

We started from the hypothesis that the global behavior of the PCB is affected by the parasitic dynamics that may play a feedback effect on the whole circuit and therefore achieving a linearization effect in spite of their generally undesired presence. The behavioral cases which may emerge from the outlined procedure can be scheduled as follows.

1) Both models identified from pure and co-simulated datasets lead to high performance (Case 2).
2) The models obtained from co-simulation data performs better than those identified from pure simulations. This means that the parasitic dynamics of the PCB plays a linearizing effect on the global circuit behavior, especially as concerns the transient dynamics (Case 1, Case 3 and Case 4).
3) Co-simulations lead to models with poorer performance with respect to models identified form pure simulated data. This implies to focus on the transient for the linear model, while approaching the nonlinear oscillations appearing in the steady-state with the qualitative analysis introduced in the following Section.
4) Both models are not good. This means that linear models are not sufficient to catch the behavior and therefore, fully nonlinear models must be accounted for.

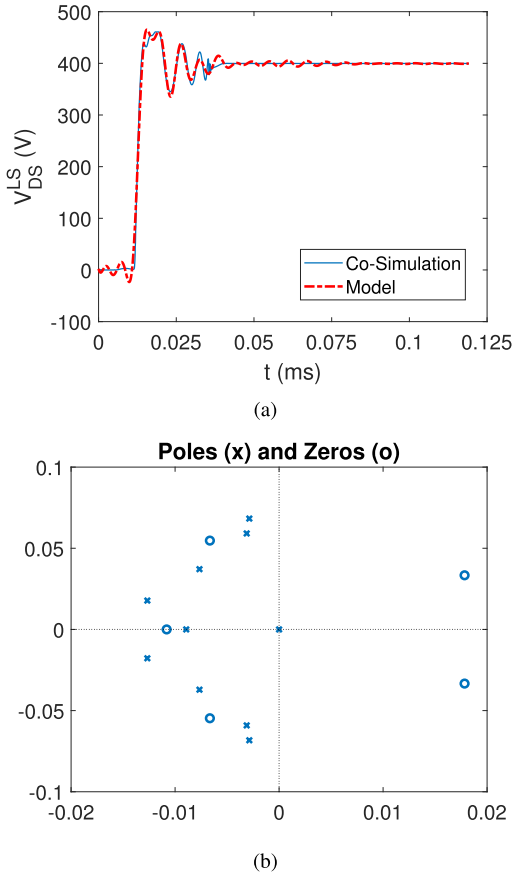

FIGURE 11. Modeling of V_{DS}^{LS}/V_{PWM}^{LS} in Co-simulation: (a) trends, (b) pole-zero map.

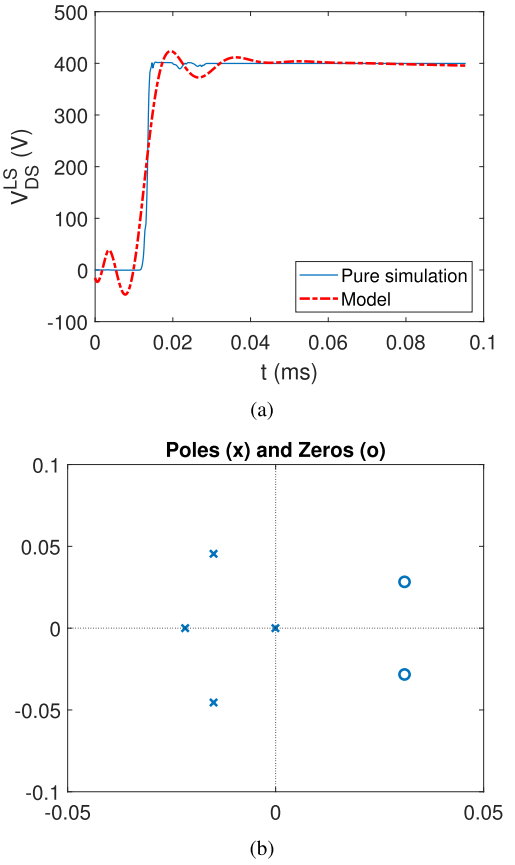

FIGURE 12. Modeling of V_{DS}^{LS}/V_{PWM}^{LS} in Pure-simulation: (a) trends, (b) pole-zero map.

Moreover, we want to remark that the scenario of the pole-zero maps may lead to the following considerations. Excluding the model from pure simulation dataset of Case 1, all the other models are non-minimum phase systems (i.e. contain zeros with positive-real part). Furthermore, the order of the models from co-simulated datasets are always higher than that of the respective pure simulations counterparts: this is clearly due to the presence of the parasitic dynamics in the simulation scenario.

VI. IDENTIFICATION OF THE STEADY-STATE STRANGE BEHAVIOR

In the previous section, we uncovered that a global linearizing effect can be played by parasitic dynamics. In this case, optimal linear models are in general able to fit better the transient. Moreover, the steady-state behavior of the data representing the outcome of the Co-simulation of the V_{GS}^{HS} and the V_{GS}^{LS} display the onset of weak nonlinear oscillations. These oscillations are clearly not produced by noise or by induced inputs exogenous to the board, as we are focusing on simulated datasets. Therefore, an intrinsic nonlinear behavior is generated by the coupling of nonlinearities of the active devices and the parasitic effects related to the PCB.

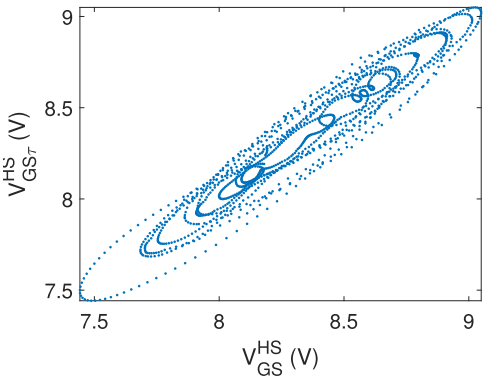

FIGURE 13. Strange attractor appearing during the steady-state of V_{GS}^{HS}, reconstructed with delay $\tau = 0.4\ \mu s$.

Let us focus at first on Case 1 of Section V. Indeed, as shown in Fig. 13, a strange attractor arises during the steady-state.

The onset of a nonlinear behavior is in agreement with previous results related to the appearance of a chaotic behavior in inductors/capacitors coupled to nonlinear effects of semiconductor devices in switching systems [12], [17].

In order to determine a procedure to obtain a qualitative model for these nonlinear behavior, we estimated a nonlinear

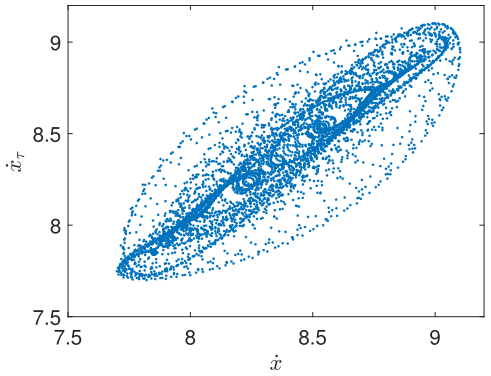

FIGURE 14. Strange attractor from the Duffing oscillator in Eq. (1) with parameter values as reported in the main text, obtained embedding $\dot{x}$ with delay $\tau = 0.4$ s.

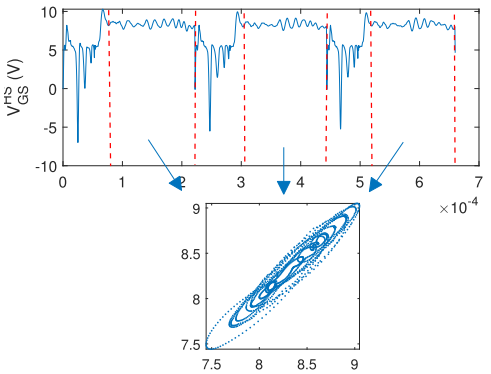

FIGURE 15. Strange attractor appearing during different steady-states of V_{GS}^{HS}, reconstructed with delay $\tau = 0.4$ μs.

model by analogy considering the dimensionless Duffing system [18] with the following equations:

$$\ddot{x} + \delta\dot{x} + \alpha x + \beta x^3 = \gamma \cos \omega t. \tag{1}$$

In particular, choosing $\delta = 0.4$, $\alpha = -1$, $\beta = 1.5$, $\gamma = 0.39$, and $\omega = 1.2$ rad/s, the strange attractor obtained embedding $\dot{x}$ with delay $\tau = 0.4$ s, as reported in Fig. 14, shows a strong agreement with that obtained with the PCB Co-simulation. Moreover, as shown in Fig. 15, the same nonlinear behavior is achieved considering different switching periods in the Co-simulation of the considered board. We remark that time-scales can be suitably matched by including a straightforward scaling of the time variable in Eq. (1).

Looking, now, at the steady-state oscillation of the V_{GS}^{LS}, a one-lobe attractor appears with embedding $\tau = 0.4$ μs, as reported in Fig. 17. The search for an analogous dynamics leads to different dynamical system, as the Duffing oscillator admits a two-lobe attractor. Therefore, the one-lobe chaotic attractor of the nonlinear forced RLC circuit [19] reported in Fig. 16 has been considered. The dynamical equations of this circuit can be written as [20]:

$$\begin{aligned} \dot{\phi} &= F - Ri(\phi) - V_1 \\ \dot{V}_1 &= \frac{1}{C} i(\phi) \end{aligned} \tag{2}$$

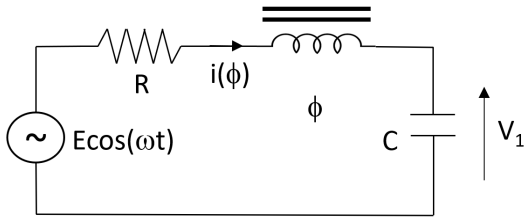

FIGURE 16. Electrical scheme of an RLC circuit with nonlinear inductor.

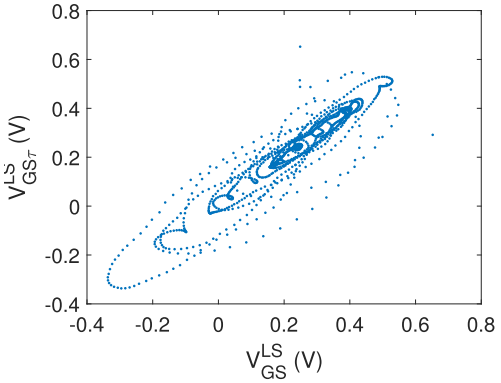

FIGURE 17. Strange attractor appearing during the steady-state of V_{GS}^{LS}, reconstructed with delay $\tau = 0.4$ μs.

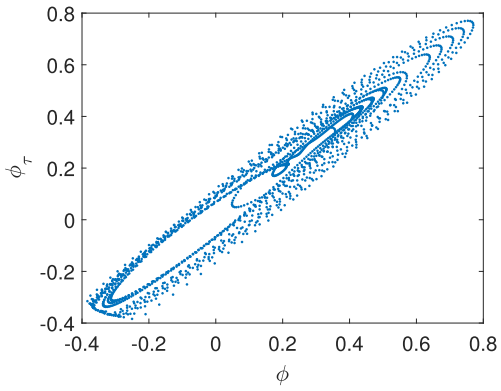

FIGURE 18. Strange attractor from the nonlinear RLC circuit in Eq. (2) with circuit parameters as indicated in the main text, obtained embedding ϕ with delay $\tau = 0.2$ s.

with

$$i(\phi) = \begin{cases} L_0^{-1}\phi & if\ \phi \le \phi_m \\ L_1^{-1}(\phi - \phi_m) & if\ \phi > \phi_m \end{cases} \tag{3}$$

where ϕ is the flux concatenated with the nonlinear inductor, V_1 is the voltage across the capacitor C, $i(\phi)$ is the nonlinear current-flow characteristic of the inductor, and $F = E\cos\omega t$ is the forcing signal.

In order to qualitatively model the behavior in Fig. 17, parameters in Eqs. (2) have been selected as $L_0 = 1$ H, $L_1 = 5$ mH, $\omega = 1$ rad/s, $E = 1$ V, $C = 0.49$ F, $R = 45.71$ mΩ, and $\phi_m = 0.9655$ Wb. The chaotic attractor reconstructed from the variable ϕ with delay $\tau = 0.2$ s is reported in Fig. 18, showing a strong agreement with the attractor retrieved from the steady-state analysis of V_{GS}^{LS}. It is interesting to remark

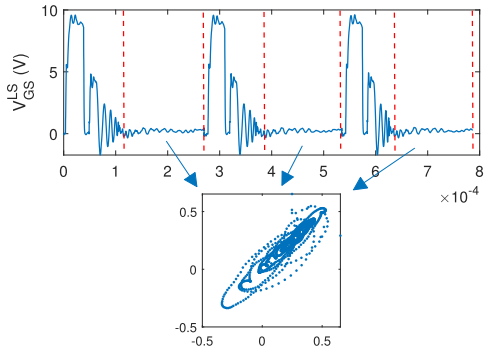

FIGURE 19. Strange attractor appearing during different steady-states of V_{GS}^{LS}, reconstructed with delay $\tau = 0.4$ μs.

that determining a qualitative model of the chaotic behavior in this case led to the choice of an attractor produced by a nonlinear RLC model. The Co-simulations, in fact, identify inductive parasitic effects due to the PCB whose nonlinear nature is reflected in the considered behavioral model. A fine tuning of the model parameters in Eqs. (2) can be, therefore, approached starting from the values of parasitic elements as determined by simulations in different working conditions [3].

The two cases discussed herein show that the analogies among attractors is fundamental for a qualitative identification of the peculiar steady-state behavior observed in Co-simulations.

VII. CONCLUSION

In this communication, the modeling and validation of PCB modules for power application in the design phase has been outlined with a strategy based on linear models identification.

Parasitic extraction is the main goal of the CAD simulation procedure in the PCB systems and the identification techniques are addressed to the validation of simulations and to obtain simple numerical models of the equipment, in order to give to the customer of the power devices not only the board but also simple behavior of that in terms of poles-zeros map, and therefore to furnish the users linear models of the equipment.

Moreover the parasitic elements introduce a filtering effect reducing the amplitude of some signals that make the nonlinearities not dominant in the global behavior of the board. It is therefore possible to say that two real negative effects could be useful to each other to achieve a linear behavior of the PCB. This item is of particular interest for the PCB designers that could use this information to arrange particular schemes with appropriate performances. Indeed it has been widely proved that some imperfections, if suitably handled, could improve the electronic circuit behavior [9], [10]. In the presented study this effect emerges again. It will be therefore a good strategy to establish a board layout in order to favour the parasitic elements in playing a positive role in the global behavior of the system.

We remark that this study has been devoted to the evaluation of CAD approaches to qualitatively identify models of the PCBs interactions. The CAD simulations of different modules have been adopted in order to simulate the complex behavior of the whole system made by semiconductor devices and PCB induced dynamics. Therefore, since the reliable validation of the simulated data has been performed working with not noisy data and without considering environmental disturbances, the effective behavior of the system can be detected and evaluated.

Therefore, the capabilities of CAD and simulation software to properly catch the real behavior of the circuit, once it has been effectively realized can be assessed during the design phase. The results presented in this paper, therefore, show that a reliable circuit design strategy must join software tools with linear and nonlinear model identification techniques. Hardware verification will be performed on the PCB layouts designed and realized following the proposed joint CAD simulation / model identification approach. This will be addressed in future as the fabrication process requires a suitable amount of efforts and time from the semiconductor Company.

However, some considerations on the improvements of circuit efficiency can be drawn from the presented results. The parasitic elements unavoidably introduced by the PCBs, which are often considered as detrimental for the circuit efficiency, can be suitably designed in order to make them interact with the nonlinear characteristics of the devices included in the board: e.g. the size of conductive traces and vias can be properly designed so that parasitic dynamics appears in a frequency range which filters the nonlinearity of the devices, thus improving circuit efficiency. This can be done at the design stage thanks to the proposed joint CAD simulation / model identification approach.

Moreover, two specific details must be emphasized. The transient behavior in the switching intervals can essentially be validated by using the techniques shown in Section V. The steady-state behavior, that is evaluated in a subsequent time interval, needs deeper considerations, as outlined in Section VI. Therefore the PCB designers have to take into account the two elements in order to improve the global behavior of the board: to mitigate the nonlinearities during the transient taking into account the positive effects of the parasitic elements, and to evaluate the cost of such parasitic elements which may favour the onset of weak strange attractors during the steady-state.

Therefore, a quantitative/qualitative identification technique can give suitable information for the optimization of the PCBs for power applications. This consideration opens a new design paradigm for PCB-based power circuits.

APPENDIX A
MAIN FEATURES OF THE USED IDENTIFICATION PROCEDURE

Let us consider the transfer function

$$G(s) = \frac{N(s)}{D(s)}$$

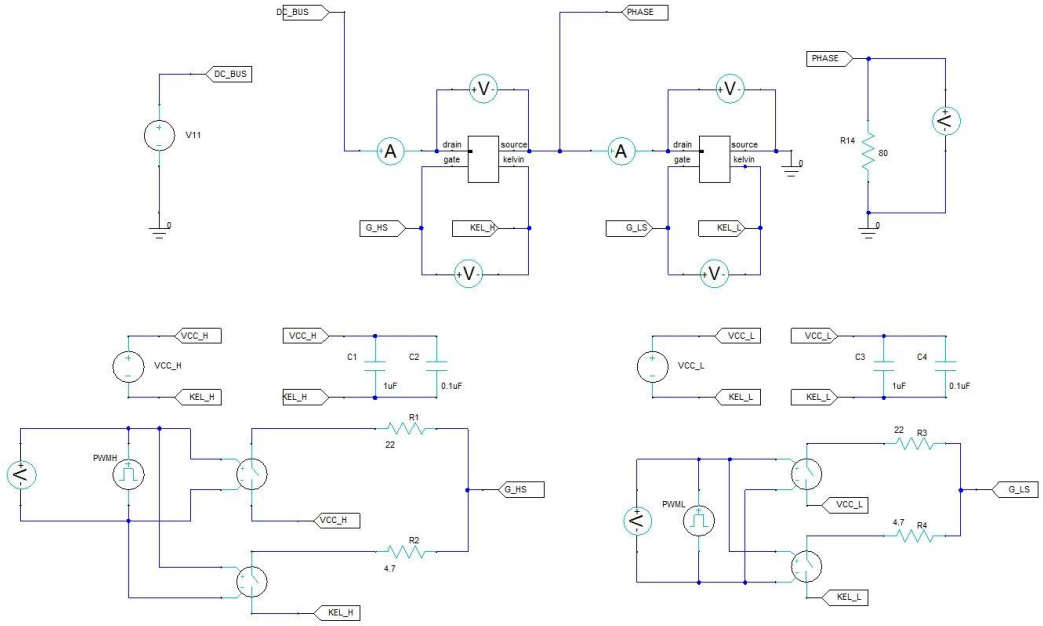

FIGURE 20. Half Bridge circuit diagram with two GaN switching devices implemented for Pure Simulation.

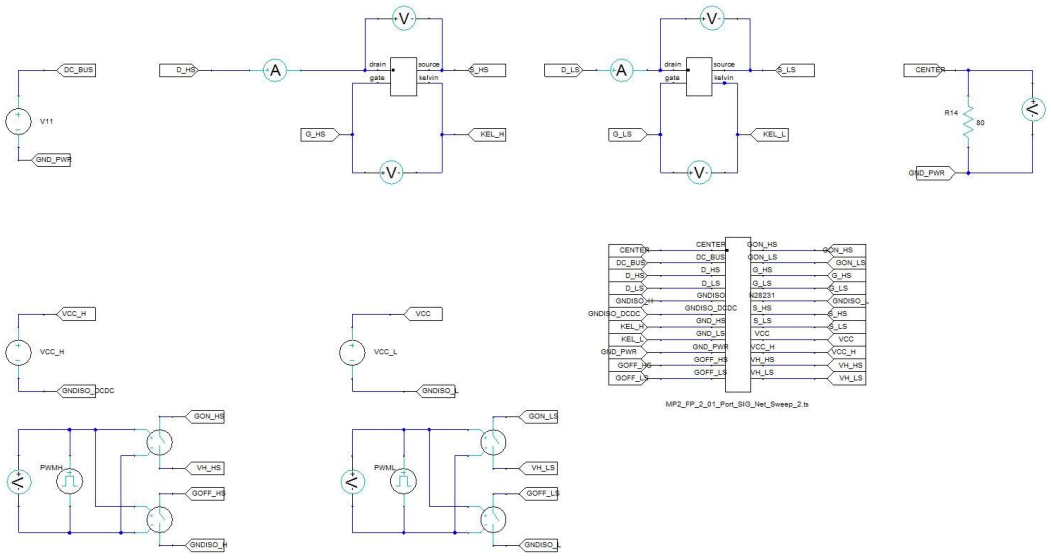

FIGURE 21. Half Bridge circuit diagram with two GaN switching devices implemented for Co-Simulation. Note the presence of the block in which the circuit section under examination is contained together with the parasitic parameters obtained.

where $N(s)$ is a polynomial in s of order m and $D(s)$ is a monic polynomial in s of order n, with $n \geq m$. It is further assumed that $N(s)$ and $D(s)$ do not contain common roots. In the case of input/output discrete sampled signals a discrete-time dynamical system with transfer function

$$G(z) = \frac{N_d(z)}{D_d(z)}$$

must be considered, being $z = \frac{1+s\frac{T}{2}}{1-s\frac{T}{2}}$ the inverse of the bilinear transformation $s = \frac{2}{T}\frac{z-1}{z+1}$, with T the sampling interval.

The transfer function $G(z)$ in the time-domain corresponds to a finite-difference equation relating the input sampled signal $u(kT)$ with the output sampled signal $y(kT)$. As T is constant, we can drop it without loss of generality. Therefore we have:

$$y(k+n) + a_1 y(k+n-1) + \ldots + a_n y(k) = \\ = b_1 u(k+m) + b_2 u(k+m-1) + \ldots + b_{m+1} u(k). \quad (4)$$

Eq. (4), taking into account more input/output sequences, can be rewritten in matrix-vector form as:

$$\mathbf{y} = \mathbf{F}\mathbf{p} \quad (5)$$

where

$$\mathbf{p} = \begin{bmatrix} -a_1 & -a_2 & \dots & -a_n & b_1 & b_2 & \dots & b_{m+1} \end{bmatrix}^{\mathrm{T}}$$

is the parameters vector, $\mathbf{F} \in \mathbb{R}^{M \times n+m+1}$ is the data matrix with $M \geq n+m+1$ structured as:

$$\mathbf{F}^{\mathrm{T}} = \begin{bmatrix} y(n) & y(n+1) & \cdots & y(M+n-1) \\ y(n-1) & y(n) & \cdots & y(M+n-2) \\ y(n-2) & y(n-1) & \cdots & y(M+n-3) \\ \vdots & \vdots & \ddots & \vdots \\ y(1) & y(2) & \cdots & y(M) \\ u(m+1) & u(m+2) & \cdots & u(M+m-1) \\ u(m) & u(m-1) & \cdots & u(M+m-2) \\ \dots & \dots & \ddots & \dots \\ u(1) & u(2) & \cdots & u(M) \end{bmatrix} \tag{6}$$

and

$$\mathbf{y} = \begin{bmatrix} y(1+n) & y(2+n) & \dots & y(M+N) \end{bmatrix}^{\mathrm{T}}$$

is the vector of outputs.

Eq. (5) by the least square method that leads to get $\mathbf{p} = \left(\mathbf{F}^{\mathrm{T}}\mathbf{F}\right)^{-1}\mathbf{F}^{\mathrm{T}}\mathbf{y}$, assuming that $\mathbf{F}$ full rank. This result can proved as follows.

Let us consider the least square error $E = \left(\mathbf{y} - \tilde{\mathbf{y}}\right)^{\mathrm{T}}\left(\mathbf{y} - \tilde{\mathbf{y}}\right)$, where $\tilde{\mathbf{y}}$ is the output vector estimated from the data. Therefore,

$$\begin{aligned} E &= \left(\mathbf{y} - \tilde{\mathbf{y}}\right)^{\mathrm{T}}\left(\mathbf{y} - \tilde{\mathbf{y}}\right) = \left(\mathbf{y} - \mathbf{F}\mathbf{p}\right)^{\mathrm{T}}\left(\mathbf{y} - \mathbf{F}\mathbf{p}\right) = \\ &= \mathbf{y}^{\mathrm{T}}\mathbf{y} - \mathbf{p}^{\mathrm{T}}\mathbf{F}^{T}\mathbf{y} - \mathbf{y}^{\mathrm{T}}\mathbf{F}\mathbf{p} + \mathbf{p}^{\mathrm{T}}\mathbf{F}^{\mathrm{T}}\mathbf{F}\mathbf{p} \end{aligned} \tag{7}$$

which can be written in the form

$$\begin{aligned} E = \mathbf{y}^{\mathrm{T}}\mathbf{y} - \mathbf{y}^{\mathrm{T}}\mathbf{F}\left(\mathbf{F}^{\mathrm{T}}\mathbf{F}\right)^{-1}\mathbf{F}^{\mathrm{T}}\mathbf{y} + \\ + \left[\mathbf{p} - \left(\mathbf{F}^{\mathrm{T}}\mathbf{F}\right)^{-1}\mathbf{F}^{\mathrm{T}}\mathbf{y}\right]^{\mathrm{T}}\mathbf{F}^{\mathrm{T}}\mathbf{F}\left[\mathbf{p} - \left(\mathbf{F}^{\mathrm{T}}\mathbf{F}\right)^{-1}\mathbf{F}^{\mathrm{T}}\mathbf{y}\right]. \end{aligned} \tag{8}$$

In Eq. (8), the first two terms are independent from the parameters vector $\mathbf{p}$, while the third term is a non-negative quantity that can be made null if and only if

$$\mathbf{p} = \left(\mathbf{F}^{\mathrm{T}}\mathbf{F}\right)^{-1}\mathbf{F}^{\mathrm{T}}\mathbf{y} \tag{9}$$

holds. Therefore, for this value of $\mathbf{p}$ the mean square error is minimized. The discrete-time model parameters can thus be obtained defining $G(z)$. The continuous-time model $G(s)$ is derived by using the inverse bilinear transformation.

APPENDIX B
CIRCUIT SCHEMATICS USED TO OBTAIN DATASETS

Figure 20 shows the circuit schematic for the system under pure simulation. It shows the high side and low side of the Half Bridge, and the GaN drive circuits.

Figure 21 illustrates the circuit schematic of the system in co-simulation. In addition to the schematics seen in the Fig. 20, it also shows the block containing the parasitic parameters of the PCB.

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Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union or the European Commission. Neither the European Union nor the European Commission can be held responsible for them.

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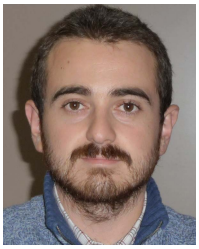

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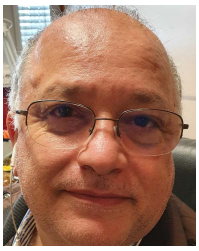

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