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# Numerical Investigations of Nanowire Gate-All-Around Negative Capacitance GaAs/InN Tunnel FET

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**ABSTRACT** We demonstrated a nanowire gate-all-around (GAA) negative capacitance (NC) tunnel field-effect transistor (TFET) based on the GaAs/InN heterostructure using TCAD simulation. In the gate stacking, we proposed a tri-layer  $\text{HfO}_2/\text{TiO}_2/\text{HfO}_2$  as a high-K dielectric and hafnium zirconium oxide (HZO) as a ferroelectric (FE) layer. The proposed GAA-TFET overcomes the thermionic limitation (60 mV/decade) of conventional MOSFETs' subthreshold swing (SS) thanks to its improved electrostatic control and quantum mechanical tunneling. Simultaneously, the NC state of ferroelectric materials improves TFET performance by exploiting differential amplification of the gate voltage under certain conditions. The most surprising discoveries of this device, which outperforms all previous results, are the very high  $I_{ON}/I_{OFF}$  ratio on the order of  $10^{11}$  and the enormous on-state current of  $135 \mu\text{A}$ . The incorporation of the NC effect with a 9 nm HZO results in the lowest SS of 20.56 mV/dec (52.38% lower than baseline TFET) and the highest voltage gain of 6.58. Furthermore, the output characteristics revealed a large transconductance ( $g_m$ ) of 7.87 mS ( $10^3$  order higher than the baseline TFET), drain-induced barrier lowering (DIBL) of 9.7 mV, and a threshold voltage of 0.53 V (37.65% lower than baseline TFET), all of which are significant. Thus, all of the results indicate that the proposed device structure may lead to a new route for electronic devices, creating higher speed and lower power consumption.

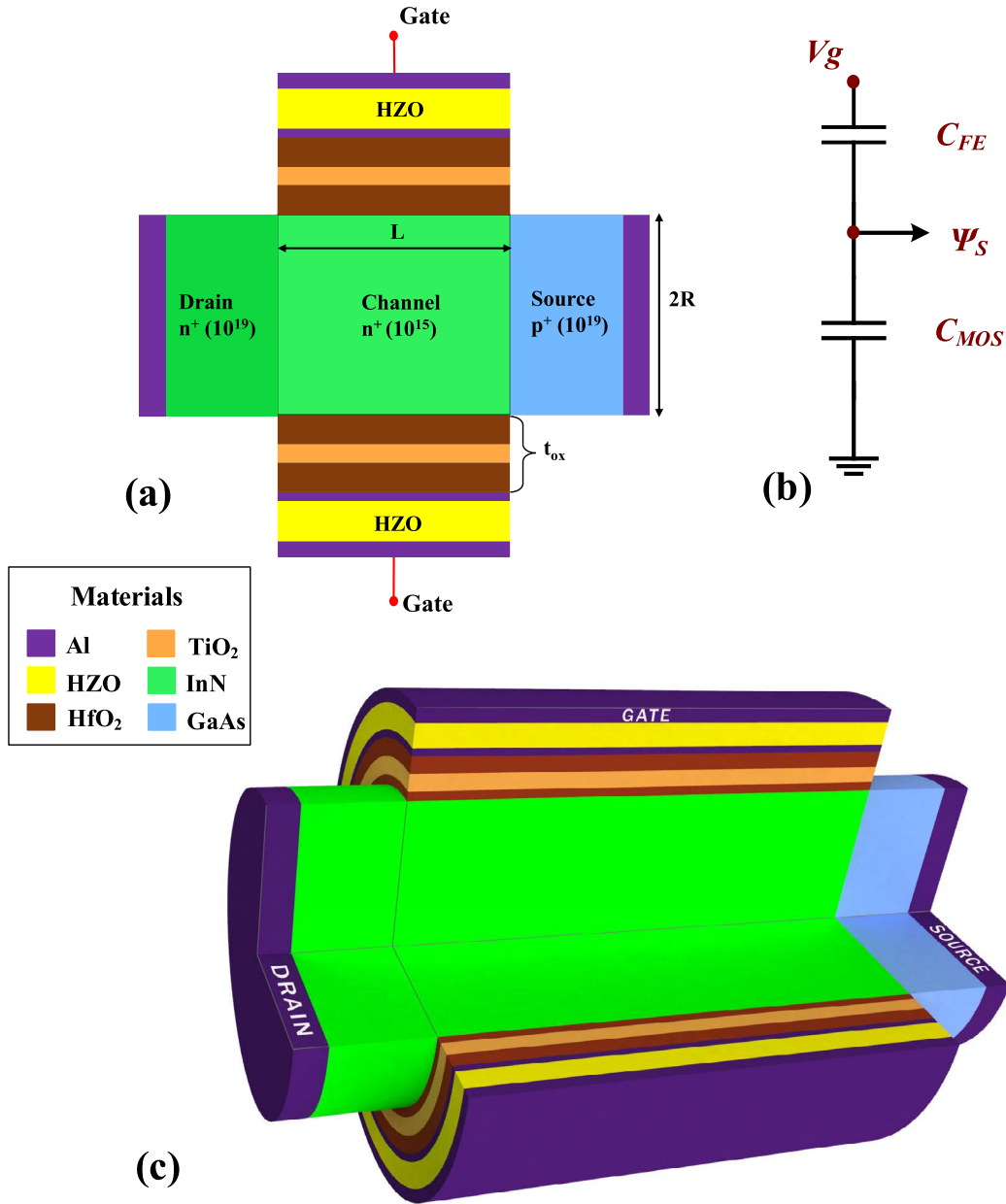
**INDEX TERMS** BTBT, gate-all-around structure, heterojunction, nanowire tunnel-FET, negative capacitance.

## I. INTRODUCTION

Scaling of complementary metal-oxide-semiconductor (CMOS) technology has been a primary focus of the semiconductor industry over the decades to minimize device per-function costs, increase speed, and decrease power consumption [1]–[3]. Numerous challenges have arisen as a result of the scaling down of the device size in MOSFETs, including short channel effects (SCEs), raising the leakage current, hot carrier effects (HCEs), drain induced barrier lowering (DIBL), and reliability issues [4]. Moreover, in case of MOSFETs, the 60 mV/decade limit on the inverse

subthreshold slope (SS) imposed by Boltzmann's tyranny hampered the scaling of supply voltage, as a means of reducing power dissipation in integrated circuits [5]. Therefore, for low standby power (LSTP) operation and ultra-low-power electronics, the tunnel field-effect transistor is often considered the utmost promising electrical switch, as it allows sub- $k_B T/q$  switching and low-voltage operation. Recently, Appenzeller *et al.* obtained a subthreshold slope of around 40 mV/dec from band to band tunneling FET device [6]. Identical outcomes are published to replace MOSFET through TFET [7]–[9] by resolving the issues related to low on current. Along with the attainability of a lower subthreshold swing, an extremely low OFF current can also be achieved from TFET devices using Si-based technologies [10]–[12].

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**FIGURE 1.** (a) 2D cross-sectional outlook of a nanowire gate-all-around-NC-tunnel-FET (NGAA-NCTFET) with highly doped drain and source and lightly doped channel, (b) the equivalent capacitance scheme, in which  $C_{MOS}$  represents the entire equivalent capacitance of the GaAs/InN heterostructure,  $C_{FE}$  is the FE layer capacitance combined in a series connection,  $V_g$  denotes the gate voltage, and  $\psi_s$  stand for the surface potential after the incorporation of HZO, and (c) schematic 3D view of the cylindrical nanowire gate-all-around tunnel-FET.

Though Si has obtained steeper subthreshold swings [13], [14], it will be more challenging to obtain enough high on currents in Si-based devices due to the indirect and wide bandgap [10], [11], [15]–[17]. To reduce the effective tunneling barrier height and ratify high on-current, III-V (e.g., Ge, SiGe, InAs, InGaAs) material-based heterostructure TFET devices have been established and show excellent performance [18]–[20]. For instance, a high-K dielectric double gate tunnel FET (DGTfET) was proposed by K. Boucart [10], which offers a significant ON current of 0.23 mA at 1.8 V gate voltage with an incredibly low OFF current value of less

than 1 fA. Besides, broken-gap alignment in heterojunction structures can boost the band to band tunneling (BTBT) relative to any other alignments and causes high ON-state current (close to 180  $\mu A/\mu m$ ) [21], [22]. In particular, the broken-band alignment between GaAs and InN is predicted to offer strong tunneling transmission and high current driving of any TFET at scaled dimensions and low supply voltage, making GaAs-InN based heterostructure TFETs appealing [23]. Another optimistic way to eliminate the short channel effects in device operation is by changing the geometry of the gate. For example, the gate-all-around (GAA) model has been

considered as a promising structure because of its significant electrostatic control over the gate and stimulates the carrier transport along the channel [24], [25]. In particular, the comparative study of the gate-all-around configuration was carried out by Zhang *et al.* [26] and stated that the Dual Material Gate Tunnel Field Effect Transistor (DMG TFET) has a smaller leakage current and comparative ON current related to the Single Material Gate Tunnel Field Effect Transistor (SMG TFET) system.

Recently, the concept of the negative capacitance of FE materials in the gate stack of TFETs has been presented as extremely advantageous for energy band bending because of the internal voltage amplification that increases the BTBT probability [27], [28]. In relation to the gate voltage  $\left(\frac{\partial V_g}{\partial \psi_s}\right)$  transition, the NC effect in FE materials further amplifies the difference in surface potential ( $\psi_s$ ) in field-effect transistors, shown in Fig 1 (b). Theoretically, Salahuddin and Datta [29] showed that a ferroelectric insulator working in the negative capacitance area could act as a step-up transformer, leading to several changes in the TFET configuration of  $SS$ ,  $I_{ON}$ , and  $I_{OFF}$ , providing a new promising alternative without altering the fundamental physics of the FET. Sub-threshold swing (SS) can be defined as,

$$SS = \left[ \frac{\partial \log_{10}(I_d)}{\partial V_g} \right]^{-1} = \underbrace{\left[ 1 + \frac{C_s}{C_{ox}} \right]}_{\text{Body Factor}} \underbrace{\left[ \frac{\partial \psi_s}{\partial \log_{10}(I_d)} \right]}_{\text{Transport Factor}} \quad (1)$$

where  $V_g$  denotes the gate potential,  $I_d$  represents the drain to source current,  $C_{ox}$  and  $C_s$  represents the gate oxide capacitor and semiconductor capacitor, respectively. When a negative value of  $C_{ox}$  is provided (means FE is in the NC region), the equivalent capacitance is greater than  $C_s$  and the combined capacitance of the gate ( $C_{total}^{-1} = C_s^{-1} + C_{ox}^{-1}$ ) is increased, which results in a lower voltage being required to generate the equal quantity of charge  $Q$ . This brings about the body factor  $< 1$ , which lowers the SS and increases the steep slope region. In this way, NC can help TFET's to achieve a sharp OFF-to-ON transition and an appropriate  $I_{ON}/I_{OFF}$  value. For instance, Kobayashi *et al.* [30] find an on-current of  $15 \mu A$  and  $I_{ON}/I_{OFF}$  of  $10^7$  which suppress the previously mentioned outcomes. To emphasize negative capacitance in TFET, Saeidi *et al.* [31], [32] experimentally figure out a lower SS value of 15 mV/dec and a comparatively high transconductance ( $g_m$ ) value of  $\approx 3$  mS. Despite the fact that various studies on NCTFETs have been undertaken, a novel device structure or physics is obviously necessary to boost performance even further.

In this paper, we introduced NC with a nanowire-GAA structure for the first time to improve TFET performance. We proposed and analyzed a GaAs/InN heterostructure-based nanowire gate-all-around negative capacitance tunnel FET (NGAA-NCTFET) using TCAD simulation. Here, we demonstrated the GaAs/InN heterostructure by considering several key properties, such as effective mass, narrow

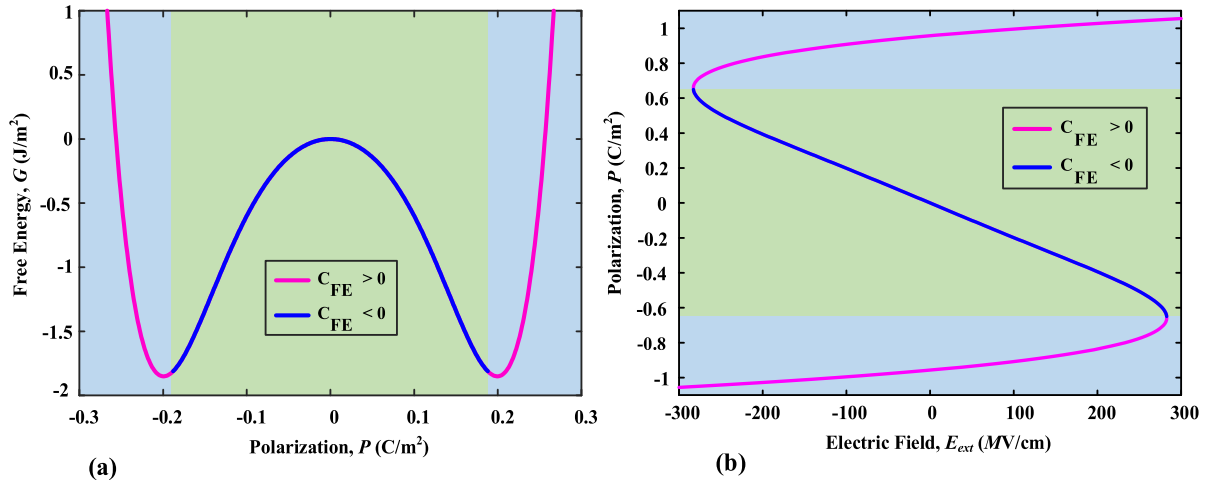
optical band gap, high saturation velocity, and high mobility of both GaAs and InN, which are very congruent for validating an excellent TFET [23]. Moreover, InN growth on a GaAs substrate [33] and the fabrication of GaAs/InN heterostructure-based photovoltaic cells [23] have also been accomplished recently. Internal polarization of the InN channel generates an uncompensated sheet charge at the GaAs/InN heterointerface, which can be utilized to generate substantial internal electric fields and significant interband tunneling. Furthermore, the piezoelectric characteristics of these materials, in combination with the lattice mismatch, add to the additional polarization discontinuity [34], [35].  $Hf_{0.5}Zr_{0.5}O_2$  ferroelectric material was used to create the NC effect in the proposed structure, and a tri-layer  $HfO_2/TiO_2/HfO_2$  high K-dielectric was used as the gate insulating oxide. The NC state showed a tremendous effect on the GAA-TFET, having an on-state current of  $135 \mu A$ , the  $I_{ON}/I_{OFF}$  ratio of  $10^{11}$ , a voltage gain of 6.58, and a transconductance of 7.87 mS, which outperforms all previous results. Furthermore, the SS decreases significantly, with the lowest SS observed to be 22.56 mV/dec and a threshold voltage of 0.53V. These outstanding findings of the proposed device add another dimension to the never-ending quest for better performance of nano-electronic devices.

The significant contributions to this work include the following: 1) we describe a nanowire GAA structure that improves device performance in terms of high on-state current, low DIBL, high transconductance, higher on/off ratio, and steeper sub-threshold slope by modifying the gate geometry in combination with the NC impact of FE; 2) the ability of current conduction and carrier controlling mechanisms of the device has been improved by using our suggested tri-layer high-k dielectric in the gate stack.

The following is an overview of the current task. The device architecture is introduced in Section II. The methodology is discussed in Section III. Section IV presents the results and discussion. The conclusions are presented in Section V, and the references are provided in the last section.

## II. DEVICE ARCHITECTURE

The proposed device architecture (2D & 3D) and the equivalent capacitance model is depicted in Fig. 1. Here, we have treated the overall structure, excluding the HZO layer, as the baseline GAA NCTFET. In the TFET structure, we chose 10 nm as the GaAs/InN nanowire radius (R). The lengths of the gate ( $L_G$ ), drain ( $L_D$ ), and source ( $L_S$ ) are 90 nm, 50 nm, and 50 nm, respectively. Table-1 shows the additional structural variables employed in this architecture, which are quite specific and sensible. We suggested a new tri-coating structure [36] in which  $TiO_2$  ( $\epsilon_{TiO_2} \approx 80$ ) is interspersed between two layers of  $HfO_2$  ( $\epsilon_{HfO_2} \approx 25$ ) for triggering high dielectric gate oxide on the InN channel. For resistive random-access memory devices, a similar type of tri-layer structure has recently been experimentally verified [37]. An aluminum (Al) layer is considered the gate contact above the tri-layer gate oxide to construct a baseline structure.



**FIGURE 2.** The negative capacitance feature of HZO is demonstrated in two graphs: (a) Free Energy vs. Polarization and (b) Polarization vs. Electric field curve. The blue regions denote a negative capacitance situation for both (a) and (b).

**TABLE 1.** The parameters used in the proposed nanowire GAA NCTFET.

Symbol	Parameter name	Value
$R$	Radius of the nanowire	10 nm
$L_G$	Gate length	90 nm
$L_D$	Drain length	50 nm
$L_S$	Source length	50 nm
$N_S$	Doping concentration of Source	$1 \times 10^{19} / \text{cm}^3$ (p-type)
$N_D$	Doping concentration of Drain	$1 \times 10^{19} / \text{cm}^3$ (n-type)
$N_C$	Doping concentration of Channel	$1 \times 10^{15} / \text{cm}^3$ (n-type)
$t_{\text{HfO}_2^+}$	Thickness of high-K gate oxide	0.5nm+1nm+0.5 nm
$\epsilon_{\text{TiO}_2^+}$	TiO <sub>2</sub> dielectric constant	80
$\epsilon_{\text{HfO}_2}$	HfO <sub>2</sub> dielectric constant	25
$Al$	Source and Drain contact	5 nm
$Al$	Gate contact	1.5 nm
$\Phi$	Gate work function	4.06 eV

In addition, the NC effect is implemented by including a  $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$  (HZO) FE layer on the gate stack. As a result of the validation of the capacitance matching approach, the HZO layer has a specific thickness of 9 nm. The drain and source areas are highly n-doped ( $10^{19}$  atoms/cm<sup>3</sup>) and p-doped ( $10^{19}$  atoms/cm<sup>3</sup>), respectively, to minimize series resistance [38], while the channel area is moderately n-doped.

### III. METHODOLOGY

The recommended nanowire gate-all-around negative capacitance GaAs/InN heterostructure-based TFET is simulated using the ATLAS Silvaco tool [39]. As part of the TCAD simulation, the nonlocal band-to-band tunneling model and the fermi-dirac distribution model have been solved self-consistently. The Schrodinger and Poisson equations, which were computed on the TCAD platform [39], are the most

important governing equations for the proposed structure.

$$-\psi(z) \frac{1}{dz^2} \frac{\hbar}{2m^*(z)} + \psi(z) V(z) = \Psi(z) E_i \quad (2)$$

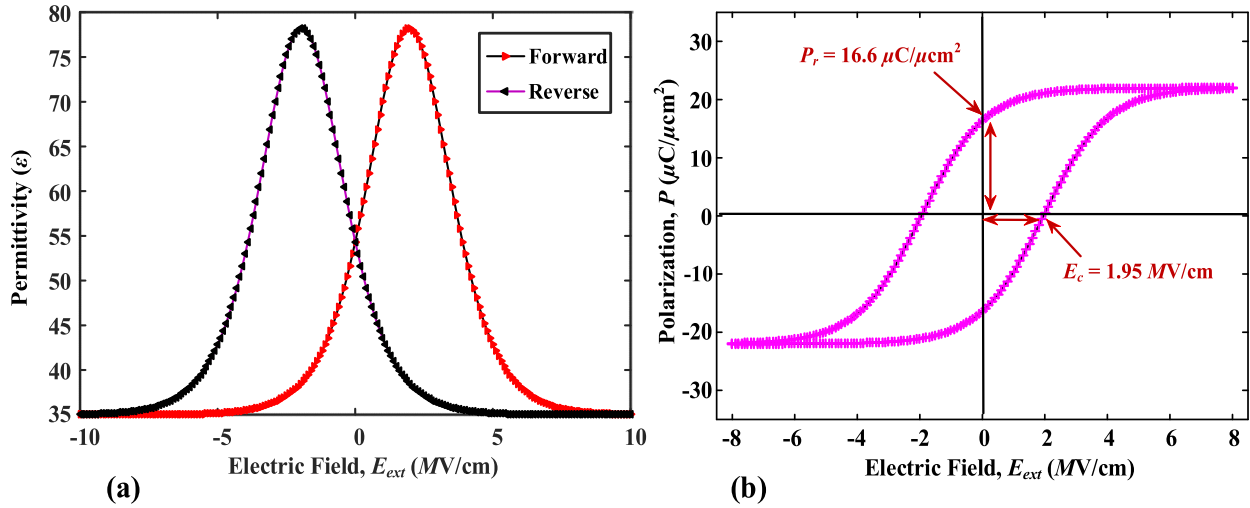
$$[n(z) - \sigma(z)] = -\nabla \cdot D(z) \quad (3)$$

The nodal coordinates of the mesh defined for the device configuration were used to solve these equations. The meshing density is enhanced at the interface part of two distinct materials in the recommended device structure, while coarse meshing is employed in other areas to boost the output. The TCAD simulation also makes use of the Shockley-Red-Hall recombination model, which employs constant minority carrier lifetimes, and the Auger recombination model, which is significant at high current densities [40]–[42]. Hosen *et al.* [25], Islam *et al.* [36], and Vijh *et al.* [34] also employed the same sorts of models to simulate the NCFET and NCTFET devices, which validates our simulation. For calculating the tunneling current, the non-local BTBT model is employed, since it is dependent on the local variation of the energy band, which allows for a more realistic simulation of the tunneling process. For an electron with longitudinal and transverse energy in the following model, the net current density is given by [35].

$$J(E) = \frac{e}{\pi \hbar} \iint T(E) [F_L(E + E_t) - F_R(E + E_t)] \times \rho(E_t) dE dE_t \quad (4)$$

Here,  $F_L$  and  $F_R$  denote the Fermi-Dirac functions on the left- and right-hand sides of the junction, respectively, using the quasi-Fermi-level. The probability of an electron tunneling through a barrier with longitudinal energy  $E$  may be expressed as,

$$T(E) \propto \exp\left(-\frac{4\sqrt{2m^*E_g^3}}{3|e|\hbar(E_g + \Delta\phi)} \left(\frac{\epsilon_s t_{ox} t_s}{\epsilon_{ox}}\right)^{\frac{1}{2}}\right) \Delta\phi \quad (5)$$



**FIGURE 3.** (a) Permittivity vs. electric field curve and (b) polarization vs. the electric field (under the dynamic sweep) for 9nm  $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$  FE, alludes to the value of coercive field ( $E_c$ ) and remanent polarization ( $P_r$ ) is 1.95 MV/cm and 16.6 C/cm<sup>2</sup>, respectively.

where,  $E_g$ ,  $t_s$  and  $\epsilon_s$  represent the energy bandgap, thickness, and dielectric constant of the semiconductor materials, respectively, and  $m^*$  and  $\Delta\varphi$  denotes the effective mass of electron and energy range, respectively, which causes tunneling. Quantifying the tunneling of electrons in (5), it is clear that it is directly related to their effective mass and bandgap energy. In addition, the simulation provides the charge generated in the device gate area, which was incorporated in the Landau model to reproduce the characteristics of the FE (HZO) capacitor. The Landau model has previously been validated to incorporate negative capacitance into FET devices [25], [29], [36], [43]. For an FE material, the free energy  $G(p)$  can be written as an even order polynomial of the polarization  $P$ , which has the following representation [43],

$$G(p) = \alpha P^2 + \beta P^4 + \gamma P^6 - E_{ext}P \quad (6)$$

Here  $E_{ext} = \frac{V}{t_{FE}}$ , is the external electric field energy;  $V$  and  $t_{FE}$  represents the voltage supplied through the FE and the thickness of the FE respectively,  $\alpha$ ,  $\beta$ , and  $\gamma$  are the anisotropic constant, where  $\beta$  and  $\gamma$  are temperature independent. The dynamics of free energy ( $G$ ) is given by,

$$\delta \frac{dP}{dt} = -\frac{dG}{dP} \quad (7)$$

Here,  $\delta$  denotes the polarization damping factor and material dependent parameter that addressed for dissipative process throughout the FE switching. Hence, (6) becomes,

$$E_{ext} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \delta \frac{dP}{dt} \quad (8)$$

In the steady-state  $\frac{dP}{dt} = 0$ , from (7) and (8) we get,

$$E_{ext} = 2\alpha Q + 4\beta Q^3 + 6\gamma Q^5 \quad (9)$$

As we know, for FE material  $Q = \epsilon E + P \approx P$ , (8) can be written as,

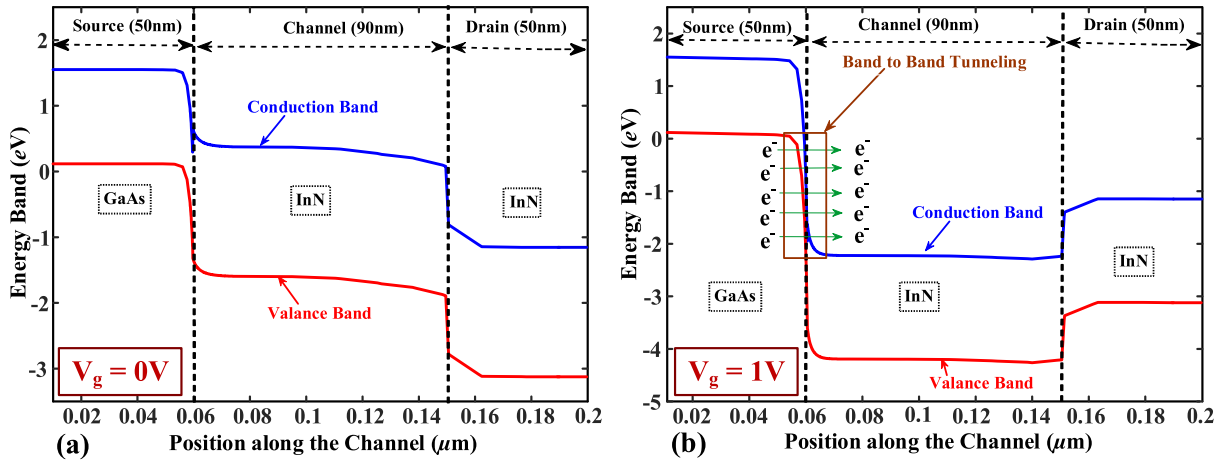
$$V = 2\alpha t_{FE} Q + 4\beta t_{FE} Q^3 + 6\gamma t_{FE} Q^5 + \delta \frac{dQ}{dt} \quad (10)$$

**TABLE 2.** HZO specifications utilized for the device analysis.

Symbol	Parameters	Value
$t_{FE}$	Thickness of HZO layer	9 nm
$\epsilon$	Dielectric constant	23
$P_r$	Remanent polarization	16.6 $\mu\text{C cm}^{-2}$ [44]
$P_s$	Spontaneous polarization	22.0 $\mu\text{C cm}^{-2}$ [44]
$E_c$	Coercive field	1.95 MV cm <sup>-1</sup> [44]

We used,  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$  as the FE layer with  $x=0.5$ , and the values of  $\alpha$ ,  $\beta$ , and  $\gamma$  are obtained from prior research [44]. Table 2 includes the HZO parameters that were used for the device simulation.

The energy landscape ( $G$ ) and polarization ( $P$ ) constituted by the HZO are depicted in Fig. 2 (a) and 2 (b), respectively. Landau's theory states that the electrical field characteristic of FE materials has a nonlinear relationship between polarization and electric field, with a negative slope towards the origin. Moreover, the energy vs polarization curve of the FE materials has an inverted parabolic shape, which indicates the presence of the NC effect in the HZO materials [43]. As shown in Fig. 2 (b), in the steady-state ( $\frac{dP}{dt} = 0$ ), HZO shows an 'S' shaped pattern across the origin with such a negative slope ( $\frac{dP}{dE_{ext}} < 0$ ), which is consistent with the theory. Whenever  $E = 0$  is reached, the negative-slope area surrounding the origin becomes unstable, which aims the polarization to fix into one of two residual states: either a negative or positive state. A non-zero  $P$ , at  $E = 0$ , indicates that the FE material is hysteresis-inducing in the anti-clockwise direction when applied to dynamic sweep. The factor  $\delta \frac{dP}{dt}$  in (7) causes the maximum rate of change in polarization,  $P$ . By deferring the variation in polarization ( $P$ ) in terms of a change in electric field  $E$ , it produces an anti-clockwise hysteresis. Figure 3 shows the hysteresis behavior of HZO



**FIGURE 4.** Energy Band diagram of n-channel GAA nanowire Tunnel-FET along X-position; (a) band diagram for OFF-state ( $V_g = 0V$  and  $V_d = 0.5V$ ), (b) band diagram for ON-state ( $V_g = 1V$  and  $V_d = 0.5V$ ).

containing a non-zero polarization under a zero electric field, which is consistent with previous findings. A modified version of Miller’s ferroelectric model [45] has been constructed in order to analyze the high dielectric coefficients of HZO. The permittivity utilized in Poisson’s Equation is inclined the following mathematical form in this model,

$$\epsilon(E_{ext}) = \epsilon_{FE} + P_s \cdot 2\delta \cdot \operatorname{sech}^2 \left[ \frac{E_{ext} - E_c}{2\delta} \right] \quad (11)$$

Here,  $\epsilon_{FE}$  is the ferroelectric permittivity,  $E_{ext}$  is the electric field,  $P_s$  is the saturation polarization, and  $E_c$  is the coercive field then  $\delta$  is given as follows:

$$\delta = E_c \left[ \log \left( \frac{1 + \frac{P_r}{P_s}}{1 - \frac{P_r}{P_s}} \right) \right]^{-1} \quad (12)$$

Here,  $P_r$  is the remanent polarization. Now, to match the experimental polarization-electric field ( $P - E_{ext}$ ) relationship in a FE capacitor, namely

$$P^+(E_{ext}) = P_s \cdot \tanh \left( \frac{E_{ext} - E_c}{2\delta} \right) + (\epsilon_{FE} \cdot \epsilon_0 \cdot E_{ext}) \quad (13)$$

$$P^-(E_{ext}) = -P^+(-E_{ext}) \quad (14)$$

From this model, both the permittivity- electric field ( $\epsilon - E_{ext}$ ) characteristic and polarization-electric field ( $P - E_{ext}$ ) characteristic has been generated, as seen in Fig. 3 (a) and Fig. 3 (b) respectively.

Consequently, the polarization of the HZO ferroelectric material is not directly proportional to the electric field and exhibits hysteretic behavior, as seen in Fig. 3. All dipoles tend to orient themselves towards the direction of the applied electric field when an electric field is being supplied. Since this NC-state of FE materials is very unstable and it is more difficult to maintain it when employing MOS devices, the dielectric capacitance should be generated in a certain direction such that a stable NC state is maintained in the series

arrangement of FE materials. To maintain the FE in the NC state, the ferroelectric-dielectric heterostructure must meet the requirements listed below,

$$|C_{FE}| > C_{MOS} \quad (15)$$

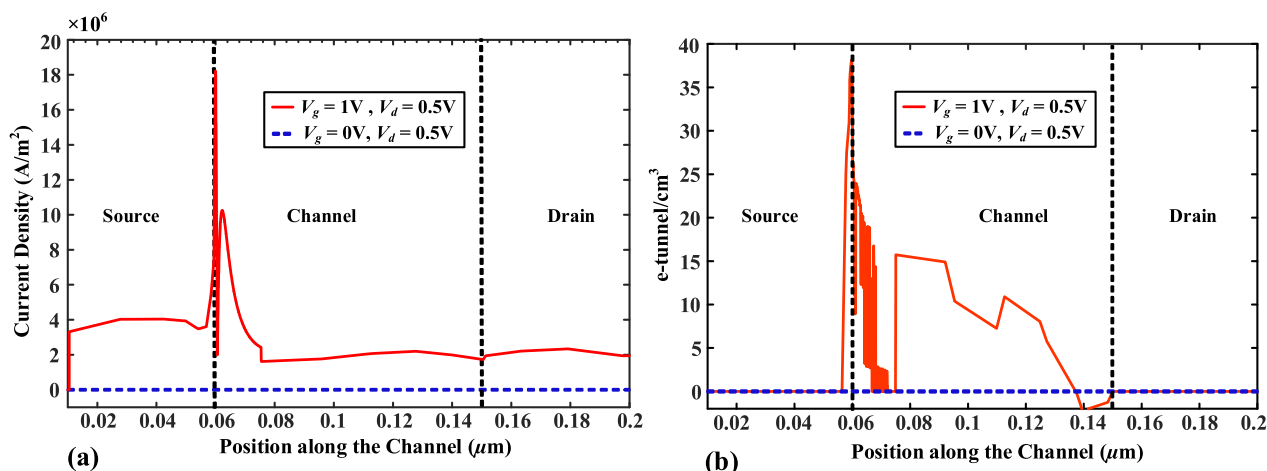
where the ferroelectric capacitance,  $C_{FE}$  is,

$$C_{FE} = \frac{dQ}{dV} = \left[ (2\alpha + 12\beta Q^2 + 30\gamma Q^4) \times t_{FE} \right]^{-1} \quad (16)$$

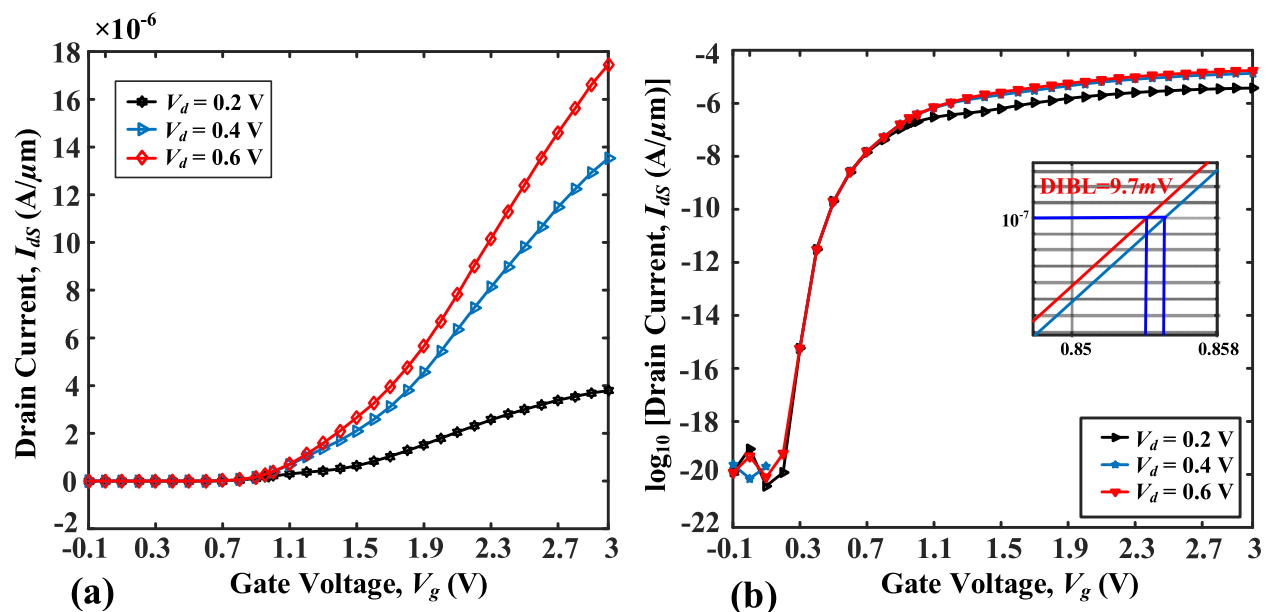
Whenever  $C_{MOS}$  is more than  $C_{FE}$ , a hysteretic jump through polarization arises, which prevents the NC effect shown by HZO from being seen. In this situation,  $C_{MOS}$  must be manufactured as close to  $|C_{FE}|$  as possible in order to get higher performance, since the performance of NCTFET’s is correlated with the best capacitance matching between the ferroelectric and dielectric layers in the device. The critical thickness for  $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$  has been determined to be 9 nm for the heterostructure that has been proposed. In Fig. 3 (b), the coercive field ( $E_c$ ) and remanent polarization ( $P_r$ ) of  $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$  at 9 nm thickness are revealed to be 1.95 MV/cm and 16.6 C/cm<sup>2</sup>, respectively. Therefore, by introducing an external electric field ( $E_{ext}$ ) that is greater than the coercive field ( $E_c$ ), it is possible to flip the polarization state of the ferroelectric material and produce differential negative capacitance [29].

#### IV. RESULTS AND DISCUSSION

In the first part of the investigations, we designed a nanowire gate-all-around tunnel-FET using a GaAs/InN heterostructure with no negative capacitance impact, which was then modified. The relevant energy band diagram of the GaAs/InN heterojunction with a broken gap alignment, which is formed in the source to channel region, is depicted in Fig. 4. As observed, to induce the tunneling phenomenon, the gate voltage must be raised, which narrows down the conduction band, and hence, a matching tunneling current emerges, allowing carriers to tunnel from the valence band into the



**FIGURE 5.** The distribution profile of the current density and e-tunneling along with the position of channel length in different gate voltages for the nanowire GAA n-channel Tunnel-FET; (a) current density vs position along the channel, showing a maximum value of  $1.8 \times 10^7$  A/m<sup>2</sup> (b) e-Tunneling in logarithmic scale vs position along the channel showing the highest value of  $\approx 10^{38}$ /cm<sup>3</sup>.

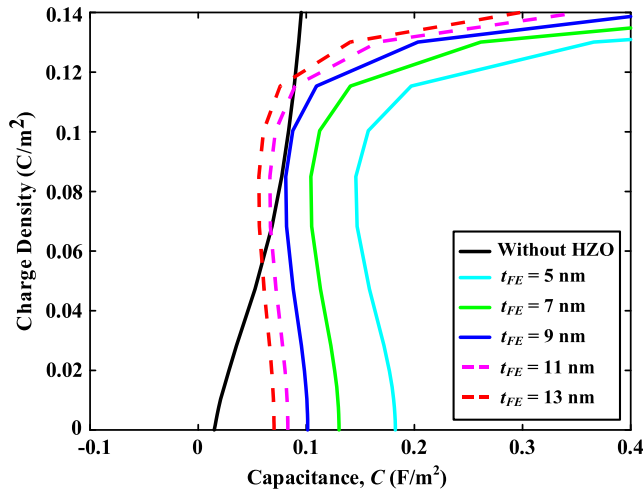


**FIGURE 6.** Transfer characteristics of the baseline NGA Tunnel-FET (a)  $I_{ds}$  vs  $V_g$ , showing a large saturation current of 17 μA and a maximum  $I_{ON}/I_{OFF}$  ratio of  $\approx 1.132 \times 10^9$  at  $V_d = 0.6V$ , and (b)  $\log_{10}$  ( $I_{ds}$ ) vs  $V_g$  curve by differing  $V_d$ , showing a low DIBL of 9.7 mV.

conduction band at the source end of the channel side, and then to the drain section of the device. Under the OFF-state condition ( $V_g = 0V$  and  $V_d = 0.5V$ ), as shown in Fig. 4 (a), there is no tunneling current because of the high barrier width in the source-to-channel junction, which means additional energy is needed to tunnel electrons out from the valence band of the source into the conduction band of the channel region. A voltage supplied to the gate causes the conduction band to bend downward because the applied electric field exerts a force on the conduction band when the voltage is greater than the threshold voltage ( $V_{th}$ ). Under the ON-state condition ( $V_g = 1V$  and  $V_d = 0.5V$ ), the appropriate energy band bending structure of the nanowire GAA TFET is illustrated

in Fig. 4 (b). It demonstrates that the conduction band bends downward because of the strain exerted by the supplied gate voltage, lowering the energy spectrum to  $-4.2eV$ . The charge density in the source to channel junction also grows, resulting in a decrease in the barrier width. The alignment was selected to provide the subsequent energy band diagram, allowing for a high drain current value. Because of this alignment, the prohibited energy gap will be wide enough to generate a low current value in the devices off state and compact enough to provide a significant amount of current in its on state, which will be a great advantage.

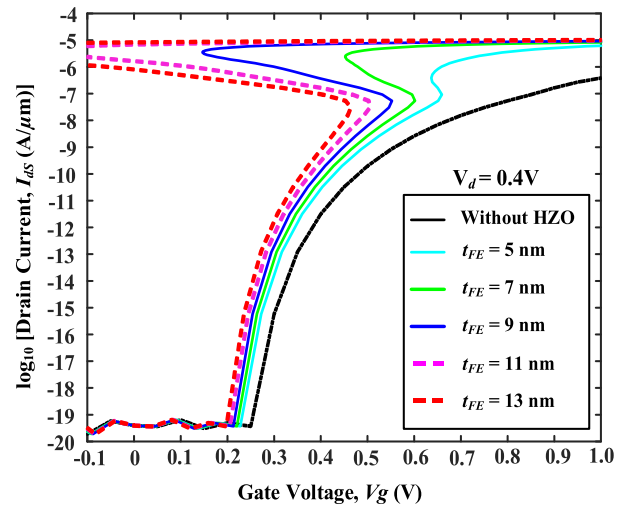
Moreover, the distribution of current density and e-tunneling rate in the band bending region is shown in



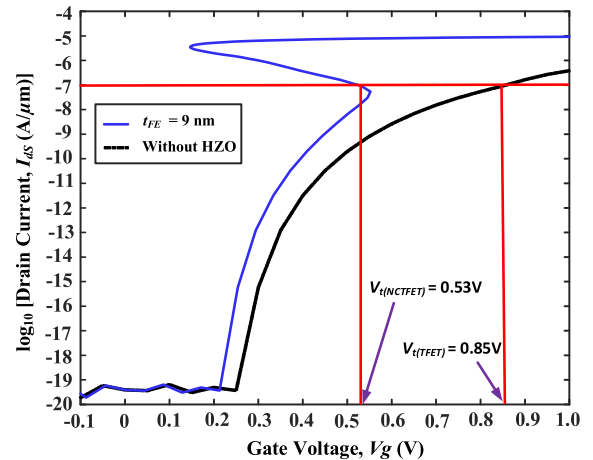
**FIGURE 7.** FE capacitance ( $C_{FE}$ ) and MOS capacitance ( $C_{MOS}$ ) for the trilayer ( $HfO_2/TiO_2/HfO_2$ ) gate oxide in terms of  $Q$ . The optimum HZO thickness is determined as 9 nm for the best capacitance matching.

Fig. 5 (a) and (b), respectively, for both the off-state and on-state conditions of this device. At on-state, the barrier width decreases as a consequence of improved coupling relating to the gate and the channel. Furthermore, charge density rises from the source region to the channel region, which offers an effective increase in the electric field. Hence, the current density is formed laterally near these two junctions when the device is turned on, as depicted in Fig. 5 (a). As a consequence, the localization of electrons at the source end increases and the peak tunneling of those electric fields occurs. Consequently, the BTBT rate is raised in the source to channel junction, as shown in Fig. 5 (b), which buttresses the on-state condition of Fig. 4 (a). Since the transmission through the barrier may be finite and vary exponentially, the wavefunction may vanish on the channel to the drain side and return on the source to the channel side in the on-state. The blue dashed line in Fig. 5 indicates the device is an off-state condition, hence no tunneling occurs.

Figure 6 presents the transfer characteristics of the baseline nanowire GAA Tunnel-FET. The drain voltage ( $V_d$ ) is changed from 0.2 V to 0.6 V using a 0.2 V step voltage. Traditional TFET structures have a low on-state current, as previously mentioned. On the other hand, the proposed baseline heterostructure has an on-state current of 17  $\mu A$  and offers a high ON-OFF ratio. Besides, increased drain voltage leads to the high on-state current as seen in Fig. 6, which ratifies good carrier conduction control. Furthermore, the suggested NGAA-TFET has a lower DIBL ( $\frac{V_{th}^{0.4V} - V_{th}^{0.6V}}{0.6 - 0.4}$ ) value of 9.7 mV, because the effect of the drain field may be minimized by the screening action of the resultant depletion area. The GAA design, in conjunction with the InN channel, provides better control over carrier conduction. Adjusting the gate voltage limit from 0.1 V to 0.6 V, the average SS obtained for the baseline heterostructure is 43.176 mV/dec. The charge inversion incident happens at  $V_g = 0.85$  V for the suggested



**FIGURE 8.** Transfer characteristics ( $I_{ds}$  vs  $V_g$ ) of nanowire gate all around NC Tunnel-FET for various HZO thicknesses. At  $t_{FE} = 9$  nm, the value of drain current is 135  $\mu A$ .

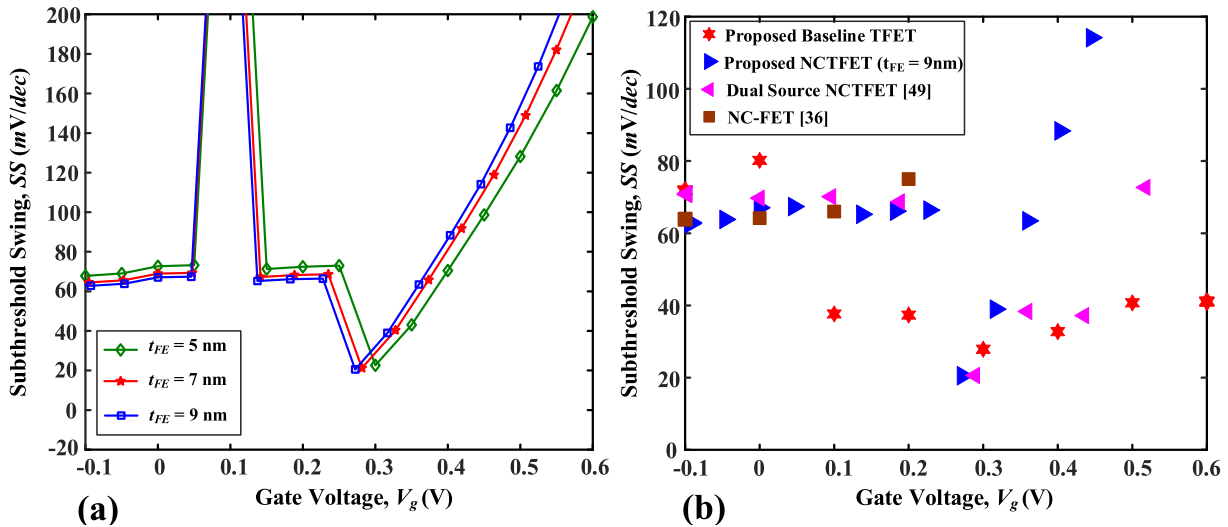


**FIGURE 9.** Performance evaluation of the proposed structure with and ferroelectric materials. The threshold voltage of the baseline structure is 0.85 V ( $V_{t(TFET)}$ ), whereas it reduces to 0.53 V ( $V_{t(NCTFET)}$ ) once the NC effect is introduced.

baseline heterostructure, which means that the current value drops significantly below this value to make the device shut down. By keeping the drain voltage constant at 0.4 V, all of the simulated outcomes for the baseline heterostructure were achieved. The  $I_{ON}/I_{OFF}$  and SS measured from the recommended baseline heterostructure are quite impressive, but the total device performance is negatively affected because of the insufficiency of on-state current. In this regard, negative capacitance is introduced into the baseline heterostructure to enhance the device’s overall performance.

The use of ferroelectric material as a gate insulator in the gate stack aids in the amplification of surface potential ( $\Psi_s$ ). The so-called “Boltzmann Tyranny” is broken in this study by using the NC effect of HZO materials and changing the transport mechanism that restricts the performance of conventional transistors. This negative capacitance effect must





**FIGURE 10.** (a) Subthreshold swing for the proposed nanowire gate-all-around NC GaAs/InN tunnel-FET at different thicknesses of HZO. The steepest slope (20.56 mV/dec) is observed at  $t_{FE} = 9$  nm. (b) Comparison of the proposed structure to the baseline and other state of the artworks.

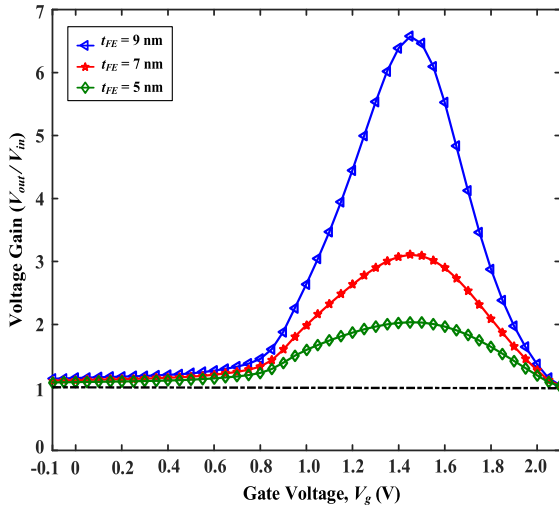
first be stabilized by associating the ferroelectric material with a gate dielectric in series connection [46]. The matching of capacitances is crucial in the design of NC devices. For better performance from this device, the thickness of HZO must be selected in a manner that also meets the requirement in (15). Hence, Fig. 7 shows the relationship between MOS capacitance ( $C_{MOS}$ ) and FE capacitance ( $C_{FE}$ ) with regard to the charge density by using (16), where the thickness of HZO varies from 5 nm to 13 nm. The solid black line in Fig. 7 shows the gate capacitance characteristics for our baseline TFET, which TCAD provides. The solid lines in this figure, ranging in thickness from 5 nm to 9 nm HZO, are always in compliance with the  $|C_{FE}| > C_{MOS}$  criterion. At the same time, the dashed lines with  $t_{FE} > 9$  nm produce intersections amongst  $C_{FE}$  and  $C_{MOS}$ , whereas the  $|C_{FE}| < C_{MOS}$  criterion is met throughout a specific region of the diagram. At 9 nm thickness, the MOS capacitance appears to be quite close to the FE capacitance, where the highest voltage is amplified and the device performs at its best. Hence, 9 nm is the critical thickness over which hysteresis may reveal itself.

In addition, the 9 nm HZO thin layer provides the smallest body factor ( $m = \frac{\partial V_g}{\partial \psi_s}$ ) through capacitance matching, which leads to the lowest sub-threshold slope in transistor by the non-hysteretic functioning when (15) is taken into consideration. As shown in Fig. 8, the nanowire GAA Tunnel-FET with an HZO capacitor above the gate oxide layer has good transfer characteristics. The dotted black line in the figure denotes the transfer curve of the suggested baseline nanowire GAA Tunnel-FET. The non-hysteretic functioning of the nanowire GAA NCTFET is shown by the next three solid lines in Fig. 8, where the width of the HZO layer is changed from 5 nm to 9 nm. According to (15), the maximum allowable thickness of HZO is about 9 nm; beyond this thickness, the requirements stated in (15) will be broken, and hysteretic

functioning of the transistor will occur. The hysteretic functioning of the Tunnel-FET is represented by the other two dashed lines, which have HZO thicknesses of 11 nm and 13 nm, respectively. In logic device applications, the hysteretic presence of the transfer curve is very undesirable and should be avoided [47]. Furthermore, the hysteretic movement suggests that HZO is unstable in its NC state, preventing it from being utilized for voltage amplification. As a result, a larger ON to OFF current ratio is produced, as depicted in Fig. 8, which increases the  $I_{ON}/I_{OFF}$  ratio of the baseline TFET that was previously given. The use of tri-layer dielectric ( $\text{HfO}_2/\text{TiO}_2/\text{HfO}_2$ ) over the InN-channel has increased the current conduction capability of the proposed device to a further level, allowing it to conduct more current. Furthermore, it is anticipated that the inclusion of the HZO layer would prompt a significant accumulation in the current conduction capacity. The implementation of the NC impact increases the value of on-current while concurrently decreasing the value of off-current. As shown in Fig. 8, a high on-current of  $135 \mu\text{A}$  and an on-off ratio of  $10^{11}$  are achieved. When compared to previous similar studies, the on-off current ratio of our proposed device is very significant [30]–[32], [48].

Moreover, threshold voltage plays a significant role in the low power operation of CMOS devices. The threshold voltage of the proposed device before and after applying the NC effect is shown in Fig. 9. When the HZO ferroelectric material is employed as the gate dielectric, the threshold voltage of the baseline heterostructure is lowered by 37.65 percent, resulting in a threshold voltage of 0.53 V. It also shows that when the NC effect is applied to the device, the on-state current is increased.

We also demonstrate the point sub-threshold swing of the proposed device as shown in Fig. 10 (a). The findings are presented specifically for the transistor's non-hysteretic



**FIGURE 11.** Voltage gain vs gate voltage at different thicknesses of HZO. The highest voltage gain of 6.58 is found at the critical thickness of HZO.

**TABLE 3.** Comparison of the findings in the present work with those of the earlier investigations.

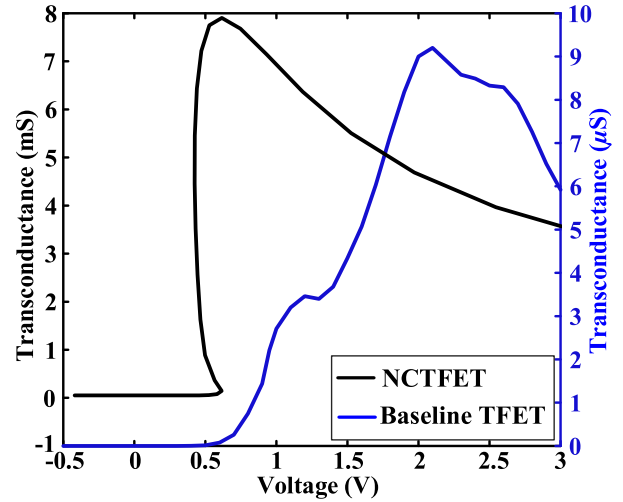
Performance Parameters	Present Work	Prior Works
On State Current ( $I_{ON}$ )	135 $\mu$ A	1.867 mA [48], 15 $\mu$ A [30], 10 mA [31]
On to Off Ratio ( $I_{ON}/I_{OFF}$ )	$10^{11}$	$10^7$ [30], $10^{10}$ [48], $10^6$ [31]
Sub-Threshold Swing (SS)	20.56 mV/dec	55 mV/dec for Arsenene & Antimonene [48], 39 mV/dec for WTe <sub>2</sub> [48], 15 mV/dec [32], 30 mV/dec [50], >60 mV/dec [31]
Transconductance ( $g_m$ )	7.87 mS	$\approx$ 3 mS [31]

functioning. With the trilayer HfO<sub>2</sub>/TiO<sub>2</sub>/HfO<sub>2</sub>, the early polarization state of the HZO at critical thickness is shifted to the opposite aligned state at 0.27V and exhibits the smallest subthreshold slope of 20.56 mV/dec., which is the smallest value reported so far [30]–[32], [48]. In Fig. 10 (b), this SS value is compared with the baseline and other states of the artwork. Therefore, the ferroelectric (HZO) based NC effect was used to reduce the SS value below the physical limit (60 mV/dec).

As voltage  $V_g$  is applied to the gate,  $\Psi_s$  appears across  $C_{MOS}$ , and voltage  $V_g - \Psi_s$  appears across the ferroelectric capacitor,  $C_{FE}$ , as depicted in Fig. 1 (b). Since they are connected in series, the charge on both capacitors is the same. Hence, internal voltage gain is calculated with relating (9),

$$A_v = \frac{\partial \Psi_s}{\partial V_g} = \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}} \quad (17)$$

As a result, capacitance matching between  $C_{FE}$  and  $C_{MOS}$  helps to improve the overall gain. The voltage gain of our suggested device for various HZO thicknesses is shown in Fig. 11. It is obvious that the maximum voltage gain is



**FIGURE 12.** Transconductance vs gate voltage for the baseline TFET and NCTFET. The highest transconductance value of 7.87 mS (at  $t_{FE} = 9$  nm) is revealed for NCTFET whereas the baseline devices have a transconductance value of 9.2  $\mu$ S.

obtained at the critical thickness of HZO (9 nm), and the obtained value is 6.58 times of the input voltage.

Finally, Fig. 12 depicts the increase in transconductance as a result of the modification. The highest transconductance value of about 7.87 mS (at  $t_{FE} = 9$  nm) is obtained from the NCTFET employing the trilayer dielectric (HfO<sub>2</sub>/TiO<sub>2</sub>/HfO<sub>2</sub>), whereas the topmost transconductance value of 9.2  $\mu$ S is found from the TFET without the NC effect, denoting a significant enhancement in the transconductance characteristics utilizing the influence of NC. The results of the present work are compared with those of earlier studies [30]–[32], [48], [50], as demonstrated in Table 3. The suggested GAA-NCTFET with a high dielectric trilayer of HfO<sub>2</sub>/TiO<sub>2</sub>/HfO<sub>2</sub> and an HZO layer of 9 nm enhances the overall device performance significantly.

## V. CONCLUSION

In summary, a hybrid nanowire GAA NCTFET structure is demonstrated by combining the GaAs/InN baseline TFET and a ferroelectric layer (HZO) in the gate stack. The use of large lattice-mismatched materials enables the staggered and broken bandgap alignment, and the GAA structure maintains better current conduction and carrier control capabilities of the device. The GAA TFET channel architecture and ferroelectric gate insulator are adjusted to obtain the optimum band-to-band tunneling and potential amplification, therefore the highest  $I_{ON}/I_{OFF}$  ratio of NCTFET is achieved. The optimized device structure produces an  $I_{ON}/I_{OFF}$  ratio on the order of  $10^{11}$  and a larger on-state current of about 135  $\mu$ A, which indicates the better channel control ability and current control capacity of the CMOS devices. With a 9 nm HZO in the gate stack, the lowest SS of 20.56 mV/dec and the maximum voltage gain of 6.58 are achieved, making this TFET structure promising as energy-efficient switches. The output characteristics also reveal a substantial transconductance ( $g_m$ ) of 7.87 mS, a DIBL of 9.7 mV, and a threshold voltage of 0.53 V (37.65% lower than the baseline TFET), all of

which are notable in comparison to all other state-of-the-art TFETs. The proposed GaAs/InN nanowire gate all around NCTFET ameliorates the limitations of scaling down the transistor size and reduces power consumption. Therefore, GaAs/InN nanowire GAA NCTFET creates a unique route for the ongoing advancement of the applicability of electronic devices, seems to be a viable option for an Internet of Things (IoT) technological platform.

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