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# Design-Window Methodology for Inductorless Noise-Cancelling CMOS LNAs

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**ABSTRACT** This paper presents an optimization methodology for inductorless noise-cancelling CMOS Low-Noise Amplifiers (LNA), whose performance typically depends on a tight balance in the design of two transistor stages. Due to the different functions of the two parts, noise-cancelling amplifiers become very difficult to analyze in detail by closed-form expressions or straight simulations: each section significantly affects the results of the other. In addition, opposed specifications, such as gain and cut-off frequency, suppose another grade of complexity due to the interplay of the two branches of the circuit. As a solution, the proposed methodology uses a visualization of the design window in 2-dimensional space to optimize the different parameters of the specifications without compromising the others. All specification constraints are represented in a single figure instead of one graph per parameter. Compared with most optimization methods, the design window methodology observes the design span instead of isolated design points that might not guarantee feasibility. Furthermore, as a simulation-driven exploration method, it benefits from complete device models with high-order effects that would be too complex to include in analytical expressions but critical to achieving maximum efficiency. As an example of the method, the paper describes the optimization of the well-known CS-CG noise-cancelling LNA in 65-nm standard CMOS technology. Final post-layout simulations report very competitive results with a 3.7-dB noise figure, a 17-dB gain, and a cut-off frequency above 7 GHz.

**INDEX TERMS** Design methodology, CMOS, optimization, low-noise amplifier, noise-cancelling, wideband receiver.

## I. INTRODUCTION

Communication systems already have a considerable impact on the present society; nonetheless, users expect that the new generation of communication systems will provide new services and transmit vaster amounts of data in the future. Consequently, designers must employ new strategies and more optimized devices to cope with the exponential growth of transmitted bits [1]. This work focuses on the improvement of the trade-offs when designing low-noise amplifiers (LNAs). The specifications of this critical part of receivers usually imply opposite restrictions. For example, improving linearity might lead to worsening noise or losing a good input impedance matching. Moreover, since structures rely on a balance between branches, each design variable affects several specifications. Additionally, the impact of second-order effects is hard to predict in an analytical approach due to the complexity of accurate models.

The proposed methodology faces the challenge of optimizing the trade-off between specifications instead of improving each one separately. Thanks to a graphical representation of the design window, the designer can observe the reachable specifications and the relationship between the target parameters [2]. Thus, the work can aim for the most advantageous trade-off for their particular application, in other words, the best ad hoc optimization.

Note that the optimization process and the graphical representation show the results of the design points and their

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surroundings, contrary to other methods that only center on individual points and neglect their environment. Thanks to this feature, the optimization can avoid false optimal points that achieve a good trade-off, but any minor disturbance causes a notable degradation. In other words, unlike methods based on random selections of values, the proposed systematic methodology provides a view of the surroundings of the desired point, thus, obtaining more reliable designs.

In a significant number of CMOS technologies, inductorless LNAs are preferred over LNAs with inductors to save area and reaching a wider bandwidth. Moreover, inductors typically have limited quality-factor in standard CMOS technology, and their use might not be recommendable.

Among inductorless LNA architectures, the noise-cancelling CG-CS topology [3] is widely used. This scheme provides practical trade-offs without inductors by combining a common-gate stage and a common-source stage to benefit from the advantages of both amplifiers. Besides, the structure includes the single-ended to differential conversion. Although several variants of this circuit exist in the literature [4]–[11], this paper explores the optimization of the classical CG-CS topology (Fig. 1). The simplicity of this topology provides a clear example of the method, although it is translatable to other topologies.

Despite its low number of components, optimizing these kinds of LNA present some difficulties that diverse methodologies try to overcome by different strategies ranging from analytical expressions [11] to synthesis algorithms [12] or intermediate approaches [13].

The proposed methodology employs contour maps in a different approach than usual. While the typical use of these graphics implies representing the gradient of a single parameter versus two variables [13]–[15]; contour maps from this work sacrifice gradient data to specification limit from several parameters.

This work is organized as follows. Section II describes the topology and provides first-order approach expressions. The paper emphasizes the complexity of the design and the optimization process in Section III. Section IV details the proposed methodology and the design window representation. Section V's practical case shows the application of the method in 65-nm CMOS technology, while Section VI explores the obtained results. Finally, in Section VII, conclusions are drawn.

## II. CG-CS TOPOLOGY

As an LNA must provide input impedance adaptation (typically 50 Ω), inductorless topologies require resistive feedback or a CG-stage. Unfortunately, the first one presents a significant disadvantage due to the severely constrained gain [16]. Moreover, a reduced gain might imply a higher noise figure (*NF*): the output signal will be lesser, but the added noise will remain.

On the other hand, a CG stage can also provide good input matching. Nevertheless, thermal noise in the transistor is proportional to transconductance, and this parameter must

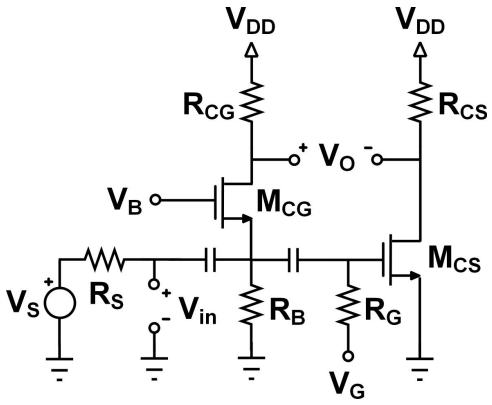


**FIGURE 1.** CS-CG LNA topology.

be relatively large to provide a 50 Ω input impedance. In order to compensate for this disadvantage, the designer should use a technique to cancel this noise [17] or reduce real transconductance by enhancing it virtually [18], [19].

As seen in Fig. 1, CG-CS LNA topology can implement a simple noise cancellation, as noise from the transistor of the CG stage ($M_{CG}$) has the same sign in its contribution to each output while the desired signal is in differential mode.

As a starting point, [17] includes some analytical expressions for specifications from a first-order approach. However, literature typically focuses on each specification separately and does not study in-depth the relationship between them. Nevertheless, as expressions can provide a clear vision of the main dependencies for the trade-off, the rest of the section aims at deducing missing terms and constraints due to their relationships.

### A. INPUT IMPEDANCE

From the relationship between voltage and current from the input source, the input impedance expression results on

$$Z_{in} = \frac{1}{g_{mCG}} // R_B \approx \frac{1}{g_{mCG}} \tag{1}$$

where $g_{mCG}$ is the transconductance of $M_{CG}$. $R_B$ is the resistor to bias CG-stage and whose value is much larger than desired impedance. Thus, it can be neglected, and the input impedance depends on $g_{mCG}$. Note that the resistor for CS gate voltage ($R_G$) is even larger, and for this reason, it has not been considered in the expression.

In conclusion, for adequate input impedance matching, the design should apply the following restriction:

$$g_{mCG} = \frac{1}{R_S} \tag{2}$$

### B. GAIN

From the small-signal model, the outputs of the CS and the CG stages are

$$V_{outCG} = g_{mCG} R_{CG} V_{in} \tag{3}$$

$$V_{outCS} = -g_{mCS} R_{CS} V_{in} \tag{4}$$

where $g_{mCS}$ is the transconductance of the transistor of CS, and $R_{CG}$ and $R_{CS}$ are the load resistors of CG and CS stages, respectively.

As the output signal is the difference between both results:

$$G = \frac{V_o}{V_{in}} = \frac{V_{outCG} - V_{outCS}}{V_{in}} = \\ = R_{CG} \cdot g_{mCG} + R_{CS} \cdot g_{mCS} \tag{5}$$

Note that the expression considers the input node as the reference, as usual in LNA, instead of voltage at the signal source. The relationship between $V_{in}$ and $V_s$ is, necessarily, $V_{in} = V_S/2$ if the input impedance matching is ideal.

### C. NOISE FIGURE

At the working range of frequency, thermal noise is the primary source of noise and, thus, a critical factor to noise figure. By calculating the contribution of thermal noise from each device of the circuit, the resultant $NF$ expression is

$$NF = 1 + \frac{(R_{CG} + R_{CS}) \cdot (1 + g_{mCG}R_S)^2}{(R_{CG}g_{mCG} + R_{CS}g_{mCS})^2 R_S} + \\ + \frac{\gamma g_{mCS} (R_{CS}g_{mCS}R_S - R_{CG})^2}{(R_{CG}g_{mCG} + R_{CS}g_{mCS})^2 R_S} + \\ + \frac{\gamma g_{mCS}R_{CS}^2 \cdot (1 + g_{mCG}R_S)^2}{(R_{CG}g_{mCG} + R_{CS}g_{mCS})^2 R_S} \tag{6}$$

where $\gamma$ is the bias-dependant channel thermal noise factor. The different terms come from CG and CS resistors as well as CG and CS transistors.

As a consequence of the noise-cancelling topology, the term of the CG transistor is neglectable if the two circuit branches fulfill a specific relationship, i.e., $R_{CS} \cdot g_{mCS} \cdot R_S - R_{CG} = 0$. Also, considering input impedance restriction (2), the constraint can be reorganized as

$$R_{CS} \cdot g_{mCS} = R_{CG} \cdot g_{mCG} \tag{7}$$

In other words, gain from CS and CG stages must be equal for ideal cancellation, and gain can be redefined as:

$$G = \frac{2R_{CG}}{R_S} \tag{8}$$

Therefore, the $NF$ expression can be rephrased and simplified to

$$NF = 1 + \gamma \frac{R_{CS}}{R_{CG}} + \frac{R_S}{R_{CG}} \left(1 + \frac{R_{CS}}{R_{CG}}\right) \tag{9}$$

This simplified expression is consistent with the observations from the study of the topology in [17]. Furthermore, it reveals that $R_{CG}$ being larger than $R_{CS}$ is beneficial for $NF$, especially since $\gamma$ is typically larger than 1 in submicron devices. Therefore, the input impedance matching condition implies that $g_{mCS}$ must have a higher value than $g_{mCG}$ to compensate for resistor imbalance.

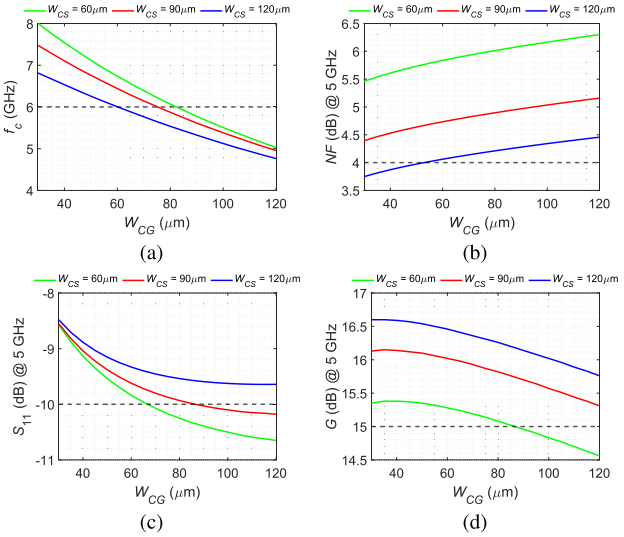


**FIGURE 2. Parameters of the LNA in function of $W_{CG}$ for different values of $W_{CS}$: a) cut-off frequency; b) noise figure; c) reflection coefficient; and d) gain. Dashed line represent the limit from specifications. $R_{CG} = 400\ \Omega$; $R_{CS} = 200\ \Omega$; and $R_B = 600\ \Omega$.**

### D. CUT-OFF FREQUENCY

Guidelines for $NF$ imply that $R_{CG}$ should be larger than $R_{CS}$ while gain promotes large load resistors. As a result, $R_{CG}$, in combination with parasitic capacitance at the output node, supposes a strict pole in the frequency response of the circuit, which is dominant over the several factors that might impact on the cut-off frequency. Thus, in a first-approach the parameter is:

$$f_C \approx \frac{1}{2\pi R_{CG} C_{load}} \tag{10}$$

$C_{load}$ being the parasitic capacitance due to the next stage at the CG output node.

## III. DESIGN ISSUES

According to first-order expressions, (7) is the condition for $M_{CG}$ noise cancellation, and therefore, sizing should be selected to satisfy that condition while minimizing CS noise [17]. Nevertheless, when the design is on the edge of technology specifications, second and third-order effects become significantly relevant. Due to these unconsidered impacts, each specification is dependent on more variables, and each design variable variation may affect more specifications. In other words, the net connecting design variables and specifications transmute into a much more complex system. There are two direct consequences from previous considerations: a) accurate device models are critical for any reliable simulation, and b) more intricate dependencies suppose difficulties in the optimization process.

Moreover, dependencies among the variables suppose another layer of complexity to the system. The effect of a variation in a variable depends not only on the own variable but also on the other variables values. For example, the sizing of $M_{CS}$ will significantly determine the impact of $R_{CS}$ on the

accomplishment of specifications, or the values of CS will depend on the design of the CG stage to be able to compensate noise and distortion. Thus, when more complex transistor models are employed, and higher-order effects become more significant, any design variable variation might change most if not all specification results.

These interplays increase the complexity of the optimization process, adding to the balance required between CS and CG. As a consequence, a single-variable parametric analysis will hardly find an optimum design. Also, the optimization process can quickly enter into an endless cycle. Or, what is worse, there might be incertitude about whether those desired specifications are achievable under any of the possible design conditions. Therefore, although first-order approach expressions are useful, they can provide the main dependencies; more delicate optimization requires another approach.

Additionally, conventional graphs of performance versus design variable or device parameter suffer from major limitations to represent the data of interest. First, they face the double dependence of the performance with both CS and CG stages. The conventional solution is to plot multiple curves versus one variable, each with different values for the second variable. However, clarity can dramatically restrict the number of points for the variable in the legend (especially if there are crossing among the curves). This translated into a limited resolution and potential incertitude for that second variable. Secondly, each graph cannot show more than one or two performance parameters without becoming illegible. This leads to requiring several separate graphs to evaluate each parametric.

The sum of both issues leads to the designer having to cope with half-dozen graphs, each one with its particular constraint for each parametric variable pair. In other words, obtaining a design window by this method is only possible after a tedious procedure and the results contain limited information (note the discretization of the second variable).

For example, Fig. 2 clearly shows that the width of one transistor affects the results when varying the other. Nevertheless, the estimation of LNA performance might have inaccuracies for values of $W_{CS}$ other than the three shown. Moreover, each value of $W_{CS}$ imposes a different $W_{CG}$ constraint for each performance parameter and, because of this, it takes some time to observe that there is not a valid $W_{CG}$ for the $W_{CS}$ shown. Still, the worst part is the difficulty of discerning whether a valid $W_{CS}$-$W_{CG}$ pair exists, but it is not represented. Note also that this example only uses four of the six specification parameters and the initial design point for simplicity.

All simulations included in this paper employ BSIM4.6 complete models from a 1.2-V 65-nm standard CMOS technology. In addition to the parasitics described on the technology device models, the simulation includes a capacitance load to simulate the following stage input impedance. Its value (50 fF) is a pessimistic estimation from the data of layout-level design characterizations in this technology.

**TABLE 1. Desired parameters.**

| *Specification* | *Target* |
|---|---|
| Noise Figure ($NF$) @ 5 GHz | $<4$ dB |
| Linearity ($IIP3$) | $>0$ dBm |
| Reflection Coefficient ($S_{11}$) @ 5 GHz | $<-10$ dB |
| Cut-off frequency ($f_C$) | $>6$ GHz |
| Gain ($G$) @ 5 GHz | $>15$ dB |
| Power Consumption ($P$) | $<6$ mW |

Table 1 shows target specifications for a state-of-the-art receiver. One application of interest is a WiFi alike communication protocol [20] operating in the 5-GHz range with narrowband signals (about 20 MHz), but the span of all channels covers almost a 1 GHz bandwidth and WiFi set of specifications are well-known and widely employed in the RF range. Other applications, such as software-defined radio (SDR) [21], [22], have reported an interest in wideband LNAs under similar specification requirements instead of the traditional banks of more selective (narrowband) LNA. Besides parameters studied in Section II, the specifications also include linearity and power consumption ($P$) constraints. As usual in the literature, input matching is shown in the form of the reflection coefficient $S_{11}$ and the Third-order Intercept Point referred to input ($IIP3$) models linearity.

## IV. DESIGN WINDOW METHODOLOGY

The solution lies in simplifying the optimization problem, i.e., reducing the number of simultaneously controlled variables. To this effect, identifying the most critical variables or embracing multiple variables in a new one is essential. Nevertheless, this simplification will have a cost, and the impact of non-critical variables may be difficult to estimate. Thus, the more descriptive selected design variables are, the more relevant information is retained.

On the other side, the topology employed in this work is compounded by two separate stages: a CG stage providing input impedance matching and a CS stage that implements the noise cancellation to allow a lower $NF$. If each stage can be controlled by one single variable, just two variables can control both stages and the balance between them.

Note that any topology based on noise-cancelling necessarily has two parts (the primary circuit and the noise-cancellation circuit). Moreover, this is also true for other inductorless LNA families like $g_m$-enhancement whose performance depends on two balanced parts.

The method defines the two selected design variables as the main variables, while all the rest variables conform to the scenario of the system driven by the two main variables.

The reduction to two main variables supplies another considerable advantage; it possibilities using them as axes X and Y, while axis Z represents one parameter from specifications. Besides, a two-dimensional contour graph can represent the three-dimensional surface of the parameter, similarly to the typical representation of height in a topographic map or

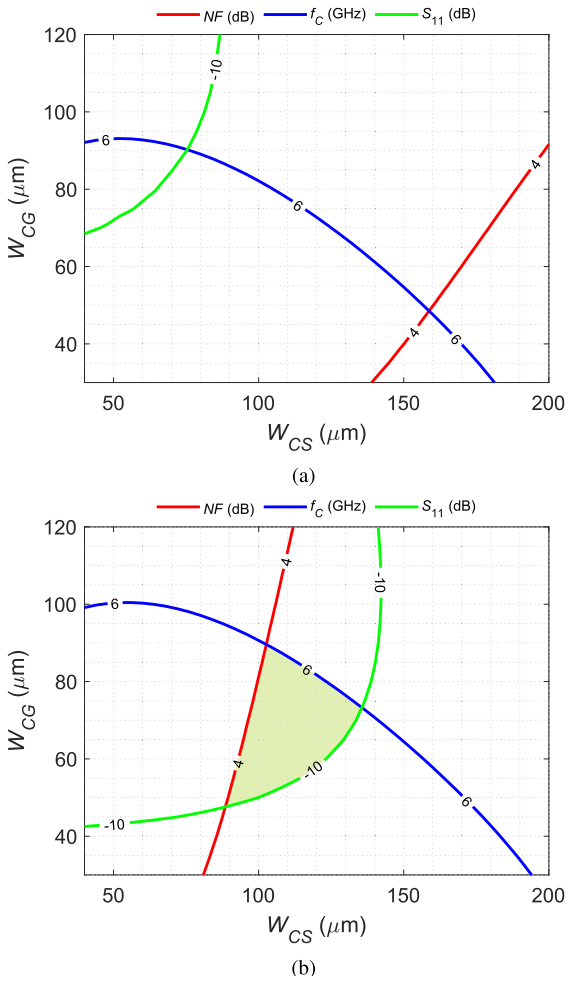


**FIGURE 3.** Representation of hypothetical case of design windows versus transistor width estimated ranges. In case a) green and red specifications are incompatible although both intersect with the blue limit. The case represented in b) presents a valid design window (green area). In this region, the system fulfils the three specifications.

the pressure in meteorological maps. In addition, the intention of the representation is determining if the specifications are fulfilled or not. Thus, the contour line of the parameter limit according to specifications contains the most critical information. Consequently, the isolines of different parameters can be drawn in the same graph. The designer can easily determine which sets of main-variable values fulfil all specifications, i.e., the design window. Therefore, optimum main-variable values are shown in the graph. Fig. 3 describes this representation with two hypothetical examples: one with incompatible specifications and another exhibiting a design window.

Due to the assumptions required for the representation, the contour map does not represent the gradient of the curves or the scenario variables' effect. However, additional isolines per parameter can reveal this data. On the other hand, optimization must evaluate all design variables, not only the main ones; in other words, the process cannot ignore scenario variables. Fortunately, they affect the size and shape of the design window, and the evaluation can be made according to those changes. Thus, a variation in these variables will be desirable when it improves the design window. There are two relevant considerations: a) the effect produced by scenario variables is more predictable than the influence of main variables, and b) the method does not evaluate the variations in a single design point but its environment. Thanks to these factors, the changes on the main variable trade-offs expose scenario variations, and the method provides an insight into dependencies between the whole set of design variables.

The methodology is employed as follows. Simulations require initial values, and hence, first, they must be obtained from first-approach expressions. These values will hardly be optimum, especially when constraints are highly demanding; however, they should be close enough to start the iterative process. Next, among design variables, two variables must be selected as the main ones. These variables should control or describe the disparate parts of the circuit. Thus, in topologies with a low number of devices, they will typically be related to transistor sizing due to their importance on the system performance. Then, the isograph of a main-variables parametric simulation can represent the design window. From this point, the designer will be iteratively modifying the scenario variables to modify the specifications isolines and to allow for a design window or enlarge it.

Each of these iterations implies a relatively high number of simulations as the points in parametric analysis grow exponentially with the number of variables. Consequently, simulations can suppose an elevated cost in time and resources if they are not meticulously prepared. Nevertheless, this strategy offers two advantages that generously rewards the initial inversion. Parametric simulations and the described representation allow the designer to easily observe the design window environment and not only isolated points. Thus, it can permit to determine whether there is any possible design window to fulfill certain specifications. Also, the optimization process will not face the risk of becoming an iterative cyclic process where a modification may lead to a variation chain that comes back to the initial point.

## V. PRACTICAL CASE

Returning to the noise-cancelling CG-CS LNA, transistor sizing and bias voltages and resistor values are the design variables. On behalf of transistors, the length should be set to the minimum available (60 nm in the selected technology) to diminish the parasitics capacitances that constraint cut-off frequency by reducing the area. Transistor width, by contrast, has an extensive range of possible values. Due to their impact on the LNA performance, the widths of the transistors become the main variables. Fig. 4 resumes the proposed methodology adapted to this topology.

The first step implies obtaining the initial scenario values. This means that resistors and bias voltage require a numeric value to carry out the simulations and obtain a design window representation. In the topology, there are two load resistors, $R_{CG}$ and $R_{CS}$. A large $R_{CG}$ provides high gain, although it will compromise bandwidth and linearity. Also, an excessively

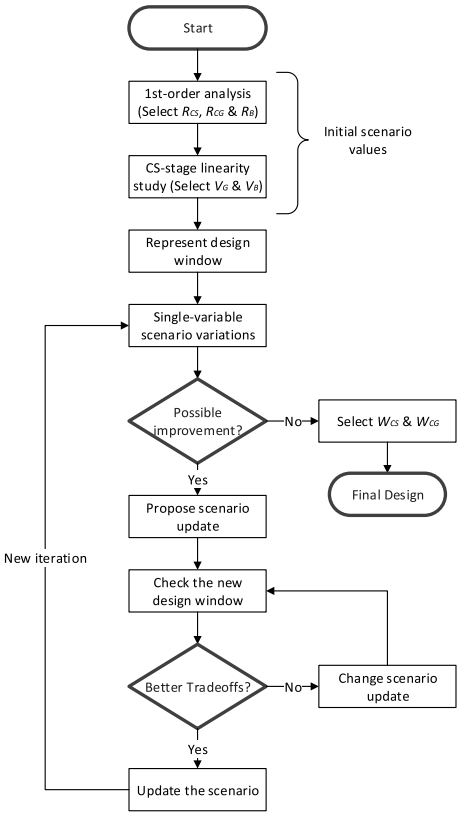


**FIGURE 4.** **Flowchart of proposed methodology.**

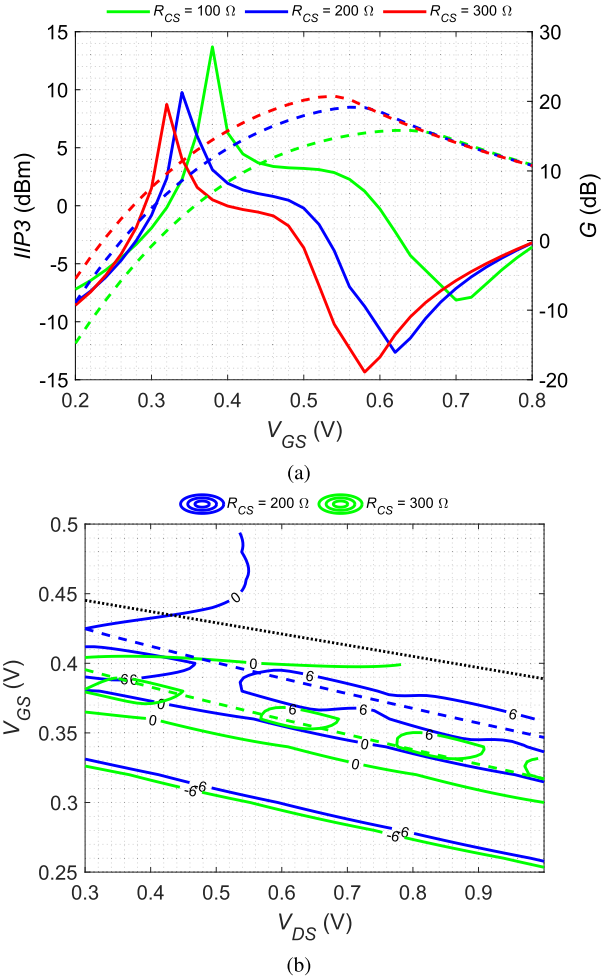


**FIGURE 5.** **Linearity of CS stage: a) *IIP*3 (solid line) and *G* (dashed line) in function of $V_{GS}$ for different values of $R_{CS}$; and b) contour map representing 200- and 300-$R_{CS}$ cases vs $V_{DS}$ and $V_{GS}$. Dashed line marks the 9-dB *G* isoline for the respective case. Dotted black line is the strict limit between saturation and cut-off, revealing that moderate inversion provides a better performance.**

high $R_{CG}$ might affect input impedance. In the case of $R_{CS}$, lower values will improve $NF$, but too much reduction would prevent the CS-stage gain. It should be remarked that in order to implement the cancellation, equation (7) must be fulfilled. In addition, another resistor $R_B$ is employed instead of the DC current source for CG biasing. To avoid a resistor divider with source impedance, $R_S$ must be negligible compared to $R_B$. This assumption also significantly simplifies the expressions.

As a first approach for sizing resistor values, $R_B$ should be around one order of magnitude larger than the source impedance ($R_s$), and $R_{CG}$ and $R_{CS}$ values between $R_B$ and $R_s$. Otherwise, the stage will not present enough gain and/or adequate linearity. The gain of the amplifier in first order is proportional to $R_{CG}/R_S$ and $R_{CS}/R_S$, thus, those resistors should be larger than $R_s$. However, if $R_{CG}$ is close to $R_B$, a constrained dynamic range will reduce linearity. Moreover, [17] recommends an $R_{CS}$ smaller than $R_{CG}$ for reducing non-cancellable thermal noise, and, as consequence, improving $NF$. Thus, as a first guess, resistor values should be selected to be $R_B$ (600 Ω) much larger than $R_s$ (50Ω); $R_{CG}$ (400 Ω), between $R_B$ and $R_s$; and $R_{CS}$ (200 Ω), between $R_{CG}$ and $R_s$.

On the other hand, the bias voltage ($V_G$ and $V_B$) are applied to transistor gates. They must place $M_{CG}$ and $M_{CS}$ in moderate inversion region to improve performance [23]. For the 1.2V-$V_{DD}$, this means a $V_B$ between 0.8 and 1.1 to provide enough $V_{DS}$. The actual value will depend on the trade-off between specifications. On the other side, $V_G$ strongly depends on linearity: ideally, the topology will cancel the distortion of $M_{CG}$ due to CG and CS balance. Thus, CS-stage linearity results critical to this end. According to [17], knowing the value of the $I_{DS}$ from $M_{CS}$ transistor as a function of $V_{GS}$ and $V_{DS}$, it is possible to calculate coefficients proportional to signal and harmonic power by derivation. Fig. 5 shows the results of *IIP*3 for CS stage, obtaining similar curves to [17]. Although the final value of $R_{CS}$ influences on the bias voltage value selection, an initial 0.4-V $V_{GS}$ presents a good trade-off for expectable $V_{DS}$. Lower values of $R_{CS}$ relax linearity constraints, but the stage presents a lower gain. For this reason, observing the trade-off between linearity and the gain is essential, and the gain appears in both representations of Fig. 5. Additionally, the CS-stage bias study provides an insight into the range of interest for CG bias voltage.

Once the initial values are obtained, the scenario and target specification will define the size and shape of the

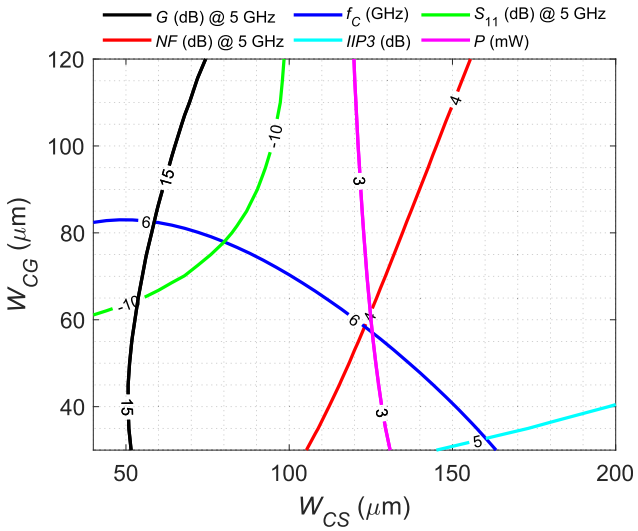


**FIGURE 6.** Initial operating point. Each isoline corresponds with an specification limit; however, P and IIP3 uses a different value for their appearance in the figure.

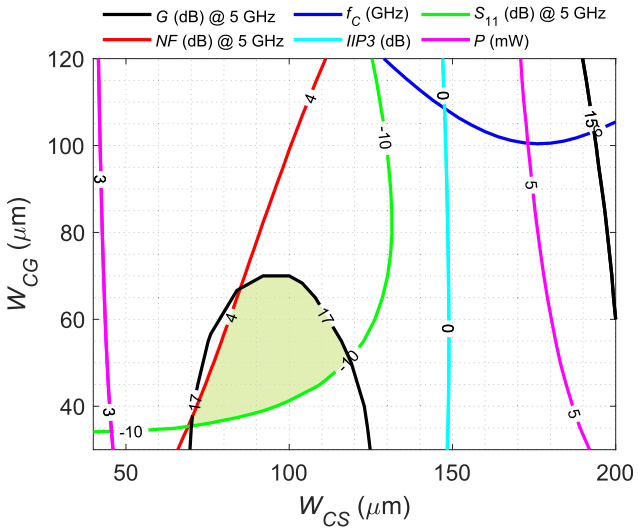


**FIGURE 7.** Intermediate operating point along the iterative design process. At this point, there is a valid design window that fulfil specifications, being *NF*, $f_C$ and $S_{11}$ the most critical parameters. On the other hand, gain limit can be stricter than initially proposed and, thus, figure represents 17-dB limit instead of 15-dB. Also power is much lower than the limit but two isolines provide a reference of its value around design window.

design window. Fig. 6 represents the design window obtained by simulation of the initial scenario conditions. The values of this scenario are selected to achieve good performance according to the conclusions drawn from first-order expressions. However, the simulation shows that *NF* and $S_{11}$ are incompatible under this scenario, as achieving perfect input impedance matching is not optimal in terms of noise performance. $f_C$ also imposes severe constraints due to the parasitic capacitances of transistors, which are not negligible for the high $R_{CG}$ value (400 Ω) selected to improve the *NF* without compromising the *G*. There is no valid design window and, even if the input matching condition is neglected, *NF* and $f_C$ suppose a narrow design window. The same is true if *NF* is disregarded and the design window depends on $S_{11}$, *G*, and $f_C$. Note that *P* isoline is far from the specification restriction, but it references this parameter value in the region of interest.

By changing the variables and, thus, the scenario, the designer can modify the position of most constraining lines and thus, to their convenience, shape or enable the design window. Fig. 7 shows the contour map of an intermediate point of the iterations to optimize the LNA. At the cost of a slight increment of power consumption, the variations have displaced $S_{11}$ limit to the right side of the graphic and *NF* to the left. Hence, the respective specifications become compatible. As a consequence of the change, the gain has been improved too, and the optimization process can aim to a better performance of this parameter. For this reason, the figure uses a 17-dB gain line instead of the 15-dB one. For $f_C$, the line shifts to a more permissive constraint for lower values of $W_{CS}$, although it continues to be a limiting factor in the design window region.

As Fig. 4 summarizes, the methodology iterates to optimize the performance. The first step of each iteration is evaluating the impact of single-variable variations on the current scenario. At this stage, the effect of varying each variable is observed separately for simplicity. If there is not any variation that could lead to improve the trade-off, the optimization process is complete, and the designer can select the best pair of $W_{CS}$ and $W_{CG}$ according to the isograph.

Otherwise, improvement is possible, and the designer must propose an update for the scenario according to the results. The update implies a change in the scenario variables that suppose a better performance. When the design window of the update is more advantageous than the previous scenario, it becomes the new scenario, and a new iteration starts. Otherwise, another update must be proposed.

Fig. 8 shows the design window for the final scenario. A reduction of $R_{CG}$ to 300 Ω relaxes the frequency constraint. Moreover, an increment of $V_B$ (0.9 V) and a reduction of $R_B$ (500 Ω) imply a larger $g_m$ for CG stage, widening the valid region for $S_{11}$. In combination with a larger $R_{CS}$ (300 Ω) and $V_G$ (0.5), the system can aim for better gain (17 dB instead of 15 dB), which also improves *NF* as the first approach expressions predict. The cost of all these improvements is a degradation in power consumption and linearity according to the initial point. However, Fig. 8 shows that *P* and *IIP*3 limits do not constrain the design window but lie in its boundary.

Although transistor widths are optimal as main variables in this topology, other parameters as $I_{DS}$ currents could replace transistor width in the axes. Fig. 9 shows the design window as a function of CS and CG currents. This substitution can be helpful in the case of low-power designs or more complex structures. Comparison between Fig. 8 and Fig. 9 deduces that $I_{CG}$ has slight variation in the design window as $R_B$ control DC current. Also, the figure reveals that CS consume most of the required power.

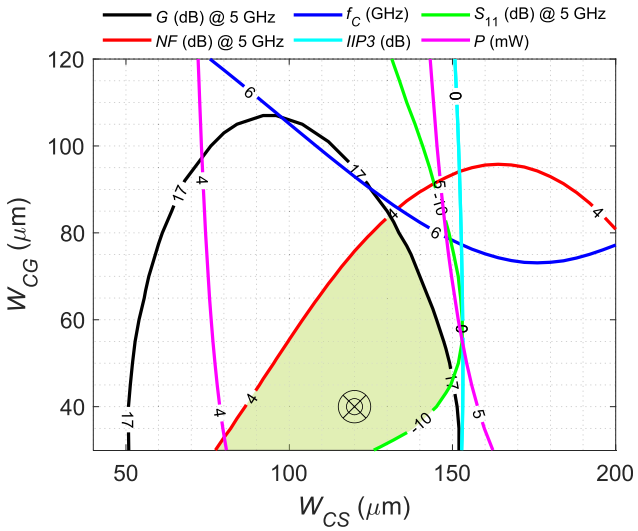


**FIGURE 8.** **Final design window. The mark inside the design window (green area) indicates the transistor width pair of the final design.**

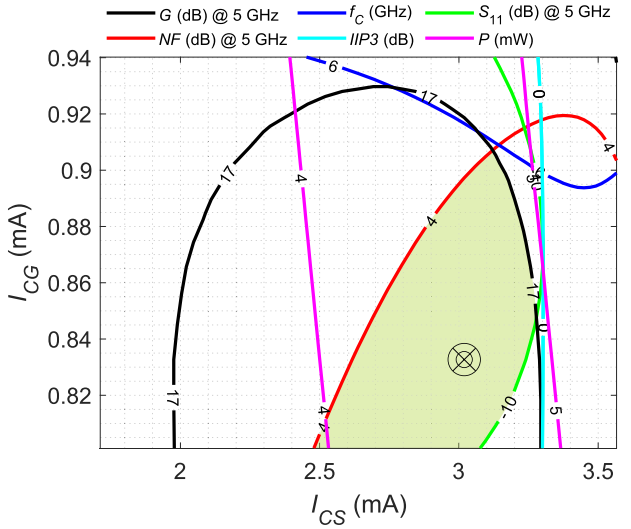


**FIGURE 9.** **Final design window using CS and CG DC currents as axes. The final design is marked on the design window.**

**TABLE 2.** **Montecarlo results (1024 samples).**

| | Mean | Std Dev | Spec | Yield |
|---|---|---|---|---|
| $NF$ @ 5 $GHz$ | 3.67 dB | 0.23 dB | 4 dB | 89.07 % |
| $S_{11}$ @ 5 $GHz$ | −11.8 dB | 0.32 dB | −10 dB | 100 % |
| $G$ @ 5 $GHz$ | 17.32 dB | 0.81 dB | 15 dB | 96.05 % |
| $f_c$ | 7.05 GHz | 402 MHz | 6 GHz | 100 % |
| $IIP3$ | 1.9 dBm | 1.2 dBm | 0 dBm | 90.86 % |
| $P$ | 4.61 mW | 0.46 mW | 5.5 mW | 98.56 % |

All specifications yield: 85.26 %

## VI. RESULTS

From Fig. 8, 120 $\mu$m and 40 $\mu$m are the selected values for $W_{CS}$ and $W_{GS}$, respectively. This point is not in the centre of the design window but closer to the $S_{11}$ limit. The reason for this decision is that $NF$ is the most susceptible parameter to process variations.

A 1024-samples Montecarlo analysis is carried out to evaluate the feasibility of the final design.

This simulation includes the parasitics extracted from the layout design and the estimated parasitic bonding inductance and input pad capacitance. Also, the layout-extracted model of a driver substitutes the load capacitor for improved accuracy, although measurements remains at LNA output (driver input) for consistency with previous results. The simulations employ the statistical process data from the technology and use random selection as a sampling method. Table 2 shows the results. Reverse isolation parameter is not included as its value is below -28 dB for the whole range of interest.

The system fulfills specifications in the large majority of cases. $NF$ is the main culprit for failed samples, although only a 3 % of the cases fall beyond 4.4 dB. The second term is $IIP3$, which is the responsible from most of the difference between $NF$ and global yields. Conversely, $G$, due to its correlation with $NF$ has little additional impact despite its percentage. Similar effect occurs with power consumption, whose specification can be constrained to 5.5 mW with a yield of 98.56 % (100 % for the initial 6 mW). It is worth mentioning that all these failed samples overlap with unsatisfied $G$ and $NF$. The percentage could be improved, as the system might benefit from specific adjust of bias voltages for each sample to correct deviations; however, for simplicity, this analysis of Montecarlo uses fix bias voltage.

Fig. 10 shows the parameters evaluated at 5 GHz versus frequency. Among the three curves, $S_{11}$ imposes the worst constraints due to its closer relationship to the input parasitics. Nevertheless, it exhibit valid results from 2.5 GHz to 6 GHz, much larger band than application requirements. However, applications demanding broader bandwidth can reduce lower cut-off frequency by using a larger input coupling capacitor (consuming more silicon area or using an off-chip capacitor). This will also enlarge $NF$ and $S_{21}$ frequency range.

The final design presents very competitive tradeoffs compared with similar designs from the literature (Table 3). In [2] the same topology is used, achieving better performance in terms of $NF$, $IIP3$ and power, but slightly lower in terms of gain and bandwidth, at the cost of employing a more advanced and expensive technology (45-nm SOI CMOS). Conversely, [17] employs the topology in similar technology, but it optimizes the performance using another approach and results in a much higher power consumption for similar or lower figures of merit. As a result, the proposed methodology improves the overall LNA performance while achieving different relationships between circuit components, i.e., while $R_{CG}$ is larger than $R_{CS}$ in [17] to reduce $NF$, our proposed LNA uses the same $R_{CG}$ and $R_{CS}$ to improve tradeoffs between $G$ and $f_C$ that eventually leads to $NF$ improvement. References [5] and [12] reach larger $G$ while decreasing $P$; however, there is a very high cost to those benefits: [5] suffers significantly high noise and an $S_{11}$ worse than the usual requirement; and [12] heavily sacrifices linearity and $f_C$.

**TABLE 3. Comparison of LNA performance.**

| Spec. | This work | [2] | [5] | [10] | [12] | [13] | [16] | [17] |
|---|---|---|---|---|---|---|---|---|
| Tech. (nm) | 65 | 45 SOI | 65 | 65 | 28 SOI | 65 | 65 | 65 |
| $V_{DD}$ (V) | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 0.8 | 1.2 | 1.2 |
| $NF$ (dB) | 3.7 | 2.5 | 5 | 3.7 | 3.6 | 4.6 | $2.9-5.9$ | 3.5 |
| $G$ (dB) | 17 | 16.8 | 20 | 18.8 | 22.9 | 14.5 | 20 | 15.6 |
| $f_C$ (GHz) | 7 | 6.2 | 7 | 7 | 4.5 | 2.7 | 10 | 5.2 |
| $S_{11}$ (dB) | $-11.6$ | $-12$ | $-6$ | $-10$ | $-10$ | $-10$ | $-10$ | $-10$ |
| $IIP3$ (dBm) | 0.7 | 1 | 2 | $-4.5$ | $-17$ | $-6.5$ | $-7$ | 0 |
| $P$ (mW) | 5.5 | 3.75 | 3.8 | 11.3 | 2 | 1.2 | 22 | 21 |

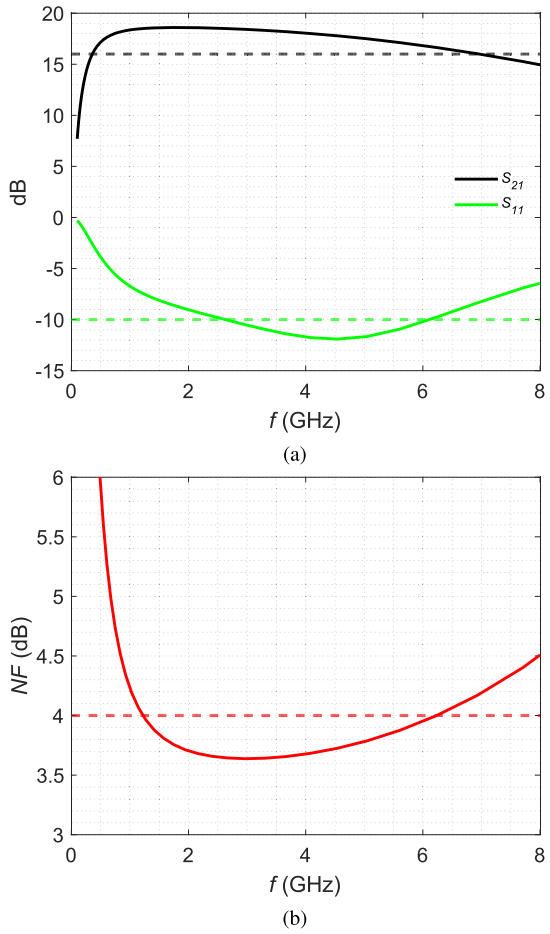


**FIGURE 10. Final design performance versus frequency: (a) $S_{11}$ and $S_{21}$; and (b) $NF$. Dashed lines references the specification limit ($S_{11}$ and $NF$) or 3-dB fall ($S_{21}$).**

Similarly, [13] presents minimum power consumption but at a high cost for all other parameters. On the other side, [10] and [16] increases $G$ at expenses of a much larger increase of $P$. Also, in [16], $NF$ has an important dependence with frequency, being around 4 dB at 5 GHz and quickly degrading to 5.9 at 10 GHz. Thus, even without considering the linearity, the global performance is less efficient than this work. The comparison reveals that the design-window methodology can achieve better global performance over other LNAs, even if they are more complex circuits. This is especially noticeable on the $IIP3$ parameter, which is vulnerable to other parameter optimization. In this work, the meticulous selection of $R_{CS}$ and $V_G$ maximizes its value, and monitoring (by the design-window representations) during the optimization process secures it.

## VII. CONCLUSION

The methodology provides the designer with a global insight into the design-window environment. Evaluating the results in a range of the most critical variables instead of an isolated point eases the optimization process. Moreover, it implies critical assistance to determine whether the desired trade-offs are viable and avoiding the local optimum point that would obscure better-performance design points. The cost of these decisive advantages is resource-intensive iterations; however, the additional information leads to faster convergence. Thus, the design requires fewer iterations to achieve its final variable values.

An essential distinction of the method is the emphasis on optimizing several parameters simultaneously instead of focusing on a particular one. The methodology aims to improve the trade-offs between specifications. A figure of merit could quantify the trade-offs or even establish an optimum point according to defined margins; however, the paper does not deepen on this application-related detail due to its general purpose.

The optimization process reveals exciting details as the one concerning topology resistor loads. Although the first-order approach predicts an improvement in $NF$ when $R_{CG}$ is larger than $R_{CS}$, the simulations show that equal values are more recommendable in this case. The reason behind this fact is the influence of the other specifications and the optimization according to the global trade-offs. A lower $R_{CG}$ implies a higher $f_C$ while the increase of $R_{CS}$ suppose a gain boost for the CS stage. These effects result in a larger $G$ and the consequent $NF$ improvement and enable a better input matching.

Noise cancellation topologies (among other LNA families) especially favor this kind of strategy. Their performance is heavily related to the balance between the two stages. Hence, it must exist a strong relationship between key variables of those two stages.

Simulations from this work have required a 65-nm standard CMOS technology to use detailed and reliable transistor models and obtain more realistic results. Nonetheless, the methodology is not technology dependent. Indeed, Table 3 includes the results of a circuit designed by this methodology in other technologies, including SOI one [2].

Besides, the methodology achieves competitive results in a very simple LNA, although its use is not restricted to it. Any topology can benefit from it, as long as two main variables can be identified.

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