IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received February 25, 2022, accepted March 5, 2022, date of publication March 8, 2022, date of current version March 18, 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3157859

Novel Tee-Shaped Topology Theory of Low- and High-Pass NGD Double-Type Function

HONGCHUAN JIA[1], FAYU WAN[1], (Senior Member, IEEE), JAROSLAV FRNDA[2,3], (Senior Member, IEEE), MATHIEU GUERIN[4], (Member, IEEE), WENCESLAS RAHAJANDRAIBE[4], (Member, IEEE), PREETI THAKUR[5], ATUL THAKUR[6], BENOÎT AGNUS[7], AND BLAISE RAVELO[1], (Member, IEEE)

[1]School of Electronic and Information Engineering, Nanjing University of Information Science and Technology (NUIST), Nanjing, Jiangsu 210044, China
[2]Department of Quantitative Methods and Economic Informatics, Faculty of Operation and Economics of Transport and Communications, University of Žilina, 010 26 Žilina, Slovakia
[3]Department of Telecommunications, Faculty of Electrical Engineering and Computer Science, VŠB—Technical University of Ostrava, 708 00 Ostrava, Czech Republic
[4]IM2NP UMR7334, CNRS, University of Toulon, Aix-Marseille University, 13007 Marseille, France
[5]Department of Physics, Amity University Haryana, Gurgaon 122413, India
[6]Amity Institute of Nanotechnology, Amity University Haryana, Gurgaon 122413, India
[7]SCIENTEAMA, 14610 Villons les Buissons, France

Corresponding author: Blaise Ravelo (blaise.ravelo@nuist.edu.cn)

This research work was supported in part by NSFC under Grant 61971230, and in part by Jiangsu Specially Appointed Professor program and Six Major Talents Summit of Jiangsu Province (2019-DZXX-022) and in part by the Startup Foundation for Introducing Talent of Nanjing University of Information Science & Technology (NUIST), in part by the Postgraduate Research & Practice Innovation Program of Jiangsu Province under Grant KYCX21_0996 and SJCX21_0351. This research was also supported by the Ministry of Education, Youth and Sports of the Czech Republic under the grant SP2021/25 and SP2022/5 conducted by VSB - Technical University of Ostrava, Czechia.

ABSTRACT Recent investigation reports that certain electronic circuits operate with the unfamiliar negative group delay (NGD) function. It is fundamentally stated that the NGD circuits can be classified in different types. For example, we have the simplest ones as LP and HP NGD circuit types. So far, all the NGD studies are focused on simple type function. In step up of the research about the NGD electronic circuit engineering, this paper develops an original theory of electronic circuit topology operating with double NGD-type behavior. The study consists in the theorization of three-port circuit simultaneously generating LP and HP NGD function types. The proposed three-port innovative circuit under study is innovatively composed of resistive-capacitive (RC) network of Tee-shaped topology. Moreover, the LP and HP double-NGD circuit is a first order cell which does not contain any inductive component. The LP and HP NGD analyses of the Tee-topology is based on the 3-D S-matrix modelling. Analytical investigation based on classical circuit theory is elaborated to determine the S-matrix model from the equivalent admittance matrix. The identification of the double-NGD function is established from the LP- and HP-NGD canonical forms. Hence, the specific double-NGD characteristics are defined in function of the R and C elements constituting the three-port topology. To validate the developed double-NGD theory, a proof-of-concept (PoC) of SMD lumped component-based three-port circuit is designed, simulated, fabricated and tested. The calculated, simulated and measured results from the three-port circuit PoC prototype in very good agreement confirm the double-NGD behavior. The proposed innovative NGD three-port circuit design is useful in the future for the synchronization of signals propagating through multi-way communication system.

INDEX TERMS Negative group delay (NGD), low-pass (LP) NGD function, high-pass (HP) NGD function, RC-network, circuit theory, three-port topology, LP-HP double-NGD analysis.

I. INTRODUCTION

To meet the users demand, the future of integrated circuit (IC) and printed circuit board (PCB) design trends to be challenging in terms of integration density [1], [2]. An adequate synthesis approach is needed to run the PCB routing notably for high density (HD) and high speed (HS) circuit [3], [4]. An innovative design method must be especially developed the digital PCB tree clock. Therefore, optimal methods of modelling [5] and simulation [6] are necessary.

The associate editor coordinating the review of this manuscript and approving it for publication was Sai-Weng Sin.

For example, innovative methods of clock signal distributions were proposed to ensure the electronic system synchronization [7]. A novel methodology for optimizing the global interconnect width and spacing of technology nodes was reported by International Technology Roadmap for Semiconductors (ITRS) [8].

The modelling of PCB electrical interconnects was initially performed by the resistive-capacitive (RC) [9]–[19] and resistive-inductive-capacitive (RLC) [20]–[23] tree networks. An estimation of tree interconnect signal delay [9]–[15] was used by the IC designers thanks to the Elmore first order model. The RC mesh networks were useful for studying the signal delay effect sensitivity [12], the delay effect minimization [14] the optimization of the time constant [16] and also assessment of slew metrics [19]. However, the first order-based RC model of interconnect lines present a significant error of propagation delay. Therefore, a second order transfer function based more accurate RLC model [20]–[23] of interconnect lines was introduced. Analytical models of interconnect lines equivalent to Elmore delay were proposed [20], [21]. The unified RLC model efficiency was verified with high-speed on-chip interconnects [21]. Because of the inductance effect, the RLC model enables to estimate the mutual inductance effect including the crosstalk influence [22], [23].

With the increase of interconnect design complexity, an efficient tree topology of electrical network [24]–[31] permitting to synchronize the clock signal distribution is necessary. Ones of the most developed topologies are constituted by symmetrical H- [24]–[28], T- [29] and Y-tree [30], [31]. An efficient modelling approach of these topologies of PCB interconnect is needed notably during the PCB design. We can emphasize following the examined bibliographical study of interconnect circuit theory that the IC and PCB interconnects are susceptible to generate undesired signal delays [9]–[16], [19]–[28]. The most popular solution to synchronize the clock or data signals propagating through the interconnect delay effects is to insert buffers at their input or output terminals [14], [32].

An alternative tentative solution to equalize the group or propagation delay effects was also initiated by using negative group delay (NGD) function [33], [34]. However, the NGD interconnect effect equalization is not well-developed because of the non-specialist electronic design engineer misunderstanding on the NGD function.

For this reason, further didactical research work on the NGD function must be forwarded. Design methods of NGD active circuits with amplifier associated to resistive-inductive-capacitive (RLC) network were so far developed [35]–[38]. It was stated that the NGD effect signature in the time-domain corresponds to the possibility to propagate the output signals in time-advance compared to the corresponding inputs [35], [36]. Because of such a counterintuitive effect, the interpretation of the NGD function intrigues most of electronic design and research engineers. Therefore, an easier to understand NGD theory inspired by the analogy with the filter function was initiated [39]. The similitude between the NGD and filter was established thanks to the regular conformity between the group delay (GD) and the magnitude of linear circuit following the Kramer-Koenig theorem. Certain lumped NGD circuits can be classified as low-pass (LP) [39]–[41] and high-pass (HP) [39], [42]–[44] NGD topologies. The NGD circuits [33]–[42] cited herein were constructed by using lumped R, L and C components. Moreover, in difference to the classical circuit theory as previously explored for the case of interconnect structures [9]–[31], the NGD circuits [33]–[44] available in the literature were designed as:

- Two-port topologies of passive or active circuits,
- Using RL, RC or RLC networks,
- Or using resonant networks.

Therefore, the existence of double type NGD topologies constituted by three-port circuits is the main focus of the present paper. The developed NGD theory is based on the original Tee-shaped passive topology of resistive-capacitive network. The paper is divided in six main sections as follows:

- Section II states the definitions of fundamental parameters allowing to represent the LP- and HP-NGD responses. For the basic understanding, the representation is using the case of two-port circuit.
- The simplest canonical forms of first order transfer functions representing LP- and HP-NGD circuit types are investigated in Section III.
- Section IV focuses on the analytical calculation of the S-matrix model representing the Tee-shaped topology.
- Section V describes the LP and HP double-NGD theorization of the Tee-shaped topology of RC-network. The main characteristics of the double-NGD topology are established in function of the capacitor parameters constituting the circuit.
- Section VI discusses the validation results by designing a three-port circuit which is a PoC of double-NGD prototype.
- Section VII finalizes the paper with the conclusion.

II. DEFINITION OF LP- AND HP-NGD CIRCUIT TYPE PARAMETERS

The present section addresses the main parameters necessary for the NGD analysis. Acting as an unfamiliar function compared to the classical ones (filter, antenna, amplifier, phase shifter, oscillator, ...), it is necessary to recall the LP- and HP- NGD specifications.

A. BASIC REPRESENTATION PARAMETERS FOR NGD ANALYSIS

By taking $s = j\omega$ as the Laplace variable in function of the angular frequency ω, for the case of symmetrical circuit, the S-matrix model generally shown by the black box of Fig. 1 can be expressed as:

$$S(s) = \begin{bmatrix} S_{11}(s) & S_{21}(s) \\ S_{21}(s) & S_{11}(s) \end{bmatrix}. \quad (1)$$

FIGURE 1. S-parameter black box.

The main parameters to be analyzed in this circuit are:

- The magnitudes of reflection and transmission coefficients, respectively:

$$\begin{cases} S_{11}(\omega) = |S_{11}(j\omega)| \\ S_{21}(\omega) = |S_{21}(j\omega)| \end{cases} \tag{2}$$

- The group delay (GD):

$$GD(\omega) = \frac{-\partial\varphi(\omega)}{\partial\omega} \tag{3}$$

in function of transmission phase:

$$\varphi(\omega) = \arctan\left\{\frac{\Im\left[S_{21}(j\omega)\right]}{\Re\left[S_{21}(j\omega)\right]}\right\} \tag{4}$$

with the real part $\Re\left[S_{21}(j\omega)\right]$ and imaginary part $\Im\left[S_{21}(j\omega)\right]$ of transmission coefficient:

$$S_{21}(j\omega) = \Re\left[S_{21}(j\omega)\right] + j\Im\left[S_{21}(j\omega)\right]. \tag{5}$$

The NGD response of circuit represented by S-matrix of Fig. 1 is defined by the existence of frequency band where the GD expressed in equation (3) becomes negative:

$$GD(\omega) < 0. \tag{6}$$

Similar to the filter behavior, we can distinguish different types of NGD responses related to the frequency band where condition (5) is satisfied. The NGD cut-off angular frequency, $\omega_0 = 2\pi f_0$, which should be unique for the case of first order circuit [39]–[44] is defined as the root of equation:

$$GD(\omega_0) = 0. \tag{7}$$

Based on these definitions, we can represent the LP- and HP-NGD function specifications.

B. LP-NGD SPECIFICATIONS

The LP-HP NGD specifications be represented by the GD spectral diagram shown in top of Fig. 2(a). Similar to the filter electronic function, in this case of LP-NGD type, the first parameter NGD bandwidth is equal to the cut-off frequency $\omega_0 = 2\pi f_0$. We can point out that condition (5) is satisfied when $\omega \leq \omega_0$. The NGD frequency band should not reach the shadowed part of the spectrum where the angular frequency $\omega > \omega_0$. The second parameter of LP-NGD type is the NGD value. It can be defined by:

$$GD(\omega \approx 0) = \tau_0 < 0. \tag{8}$$

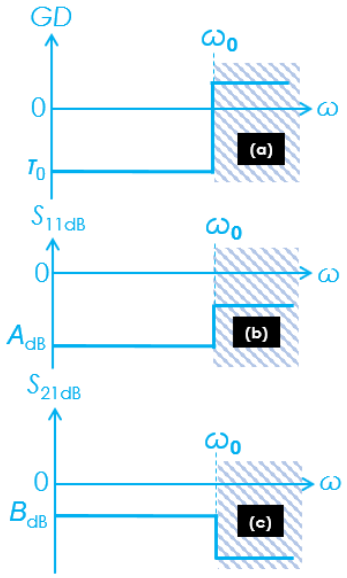


FIGURE 2. LP-NGD frequency ideal responses of (a) GD, (b) S_{11} and (c) S_{21}.

C. HP-NGD SPECIFICATIONS

Similar to the filter behavior, the HP-NGD type has an NGD frequency band in the opposite case of LP-NGD one defined in the previous subsection. The HP-NGD type ideal responses can be represented by Figs. 3. In this case, the GD spectral diagram is shown by Fig. 3(a).

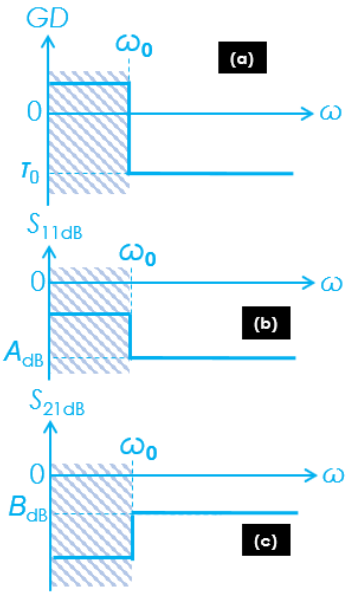


FIGURE 3. HP-NGD frequency ideal responses of (a) GD, (b) S_{11} and (c) S_{21}.

The cut-off frequency$\omega_0 = 2\pi f_0$ delimits the NGD frequency band $\omega \geq \omega_0$, where condition (5) is fully satisfied.

The shadowed parts of the diagram $\omega < \omega_0$ represent the out of band where $GD(\omega) > 0$. In the LP-NGD frequency band, we have the NGD value:

$$GD(\omega \geq \omega_0) = \tau_0 < 0. \tag{9}$$

In addition to the GD analysis, we should avoid the trivial case of $S_{11}(\omega) = 1$ and $S_{21}(\omega) = 0$ in the NGD frequency band.

Therefore, some specifications of the reflection and transmission coefficient responses will be proposed in the following subsection.

D. S-PARAMETER SPECIFICATIONS IN THE NGD FREQUENCY BAND

In addition to the GD specifications, the S-parameter magnitudes should satisfy some criteria in the NGD frequency bands. The reflection coefficient ideal responses of LP- and HP-NGD types are represented by Fig. 2(b) and Fig. 3(b), respectively. The reflection coefficient is specified by the given maximal value of real positive constant, $A < 1$ or $A_{dB} < 0$. In the NGD frequency bands ($\omega \leq \omega_0$ for the LP-NGD type and $\omega \geq \omega_0$ for the HP-NGD type), these magnitude diagrams are assumed to be plotted in dB. In this study, the reflection coefficients can be defined by:

$$S_{11}(\omega) \leq S_{11\,\max}(\omega) = A. \tag{10}$$

The transmission coefficient ideal responses of LP- and HP-NGD types are illustrated by Fig. 2(c) and Fig. 3(c), respectively. In these magnitude diagrams, these ideal responses are represented in dB. They are characterized in function of the given minimal value of real positive constant, $B < 1$ or $B_{dB} < 0$. In the NGD frequency bands, the transmission coefficients are specified by:

$$S_{21}(\omega) \geq S_{21\,\min}(\omega) = B. \tag{11}$$

As a more concrete approach, the canonical forms of LP- and HP-NGD circuit types are explored in the following section.

III. INVESTIGATION ON THE GENERAL CANONICAL FORMS OF 1ST ORDER LP- AND HP- NGD TRANSFER FUNCTION TYPES

The most practical way to study the NGD circuit is the consideration of canonical transfer function types. The present section is focused on the main parameters and properties of LP- and HP-NGD types with first order transfer function.

A. BASIC PARAMETERS OF THE TRANSMITTANCE CANONICAL FORMS

The simplest canonical transfer function forms of LP- and HP-NGD circuit types can be represented by first order system [39]–[44]. To write the fundamental transfer function associated to the LP-NGD and HP-NGD circuit types, we should consider the specification parameters represented by diagrams previously shown by Fig. 2(a) and Fig. 3(a), respectively. These canonical forms of transfer function can be expressed knowing the NGD specifications as:

- the cut-off frequency, ω_0 which is defined by equation (7),
- and also, the GD value at very low frequency defined by:

$$\tau_n = GD(\omega \approx 0) \tag{12}$$

By using these parameters, the most important canonical forms of NGD circuits will be expressed in the following subsection.

B. GENERAL TRANSFER FUNCTION ASSOCIATING LP- AND HP-NGD CIRCUITS

Once again, by inspiring from the LP- and HP-filter theory, the transfer functions of all LP- and HP-NGD circuits can be formulated by first order system. The main and basic transfer function can be identified by the expression written as:

$$T(s) = \frac{T_0(1 + a\,s)}{1 + b\,s} \tag{13}$$

with:

- The real positive constant $T_0 < 1$,
- The numerator real positive coefficient [40]:

$$a = \frac{\sqrt{4 + \omega_0^2\tau_n^2} - \omega_0\tau_n}{2\omega_0} \tag{14}$$

- And the denominator real positive coefficient [40]:

$$b = \frac{\sqrt{4 + \omega_0^2\tau_n^2} + \omega_0\tau_n}{2\omega_0} \tag{15}$$

According to the NGD theory [39]–[44], the GD at very low frequencies defined in equation (12) is given by:

$$\tau_n = b - a. \tag{16}$$

Furthermore, the NGD cut-off angular frequency is given by:

$$\omega_0 = \frac{1}{\sqrt{a\,b}}. \tag{17}$$

Now, we may wonder on how to identify if our canonical transfer function represents LP- or HP-NGD circuit types.

C. CASE OF LP-NGD CIRCUIT TYPE

More and more theoretical and practical validation studies [34]–[41] of LP-NGD circuit type are presented in the literature. So, we assume that this type of LP-NGD device type is more familiar to the NGD circuit researchers. The very simple and basic approach allowing to identify the LP-NGD circuit type can be reminded by as follows. For the case of LP-NGD type circuit, we should have the NGD value:

$$\tau_n = \tau_0 < 0. \tag{18}$$

This condition is satisfied when the coefficient of the transfer function given in equation (13) verify the inequality:

$$b < a. \tag{19}$$

As explored in the next subsection, the HP-NGD circuit type [42]–[44] is much more difficult to express.

D. CASE OF HP-NGD CIRCUIT TYPE

In the opposite case of $\tau_n > 0$, the canonical form represents the HP-NGD type function. We should characterize the circuit by the optimal angular frequency, $\omega_m > \omega_0$, defined by:

$$GD(\omega_m) = \min\left[GD(\omega)\right] \tag{20}$$

or:

$$\frac{\partial GD(\omega_m)}{\partial \omega} = 0. \tag{21}$$

By solving the last equation, we have:

$$\omega_m = \frac{\sqrt{1 + \sqrt{\frac{a}{b}} + \sqrt{\frac{b}{a}}}}{\sqrt{\sqrt{a\,b}}}. \tag{22}$$

The optimal GD defined by equation (20) is given by:

$$GD(\omega_m) = \frac{a\,b(a-b)}{(a+b)(\sqrt{a}+\sqrt{b})^2}. \tag{23}$$

The transmission coefficient magnitude $T(\omega) = |T(j\omega)|$ at the optimal frequency will be:

$$T(\omega_m) = \sqrt{\sqrt{\frac{a^3}{b^3}}}. \tag{24}$$

As application of the canonical transfer function forms, we need the expression of transmission coefficient of the circuit under study. The next section will develop the necessary S-matrix model.

IV. S-MATRIX MODEL OF THE TEE-SHAPED TOPOLOGY

The fundamental theory of lumped circuit is elaborated in the present section. By means of Tee-shaped topology, the present NGD theory is built with 3-D S-matrix analytical model. Before the analytical exploration, the proposed topology will be described. Then, based on the Kirchhoff circuit laws (KCL), the admittance equivalent model will be established before the S-matrix extraction.

A. TOPOLOGICAL INTRODUCTION

The general configuration of the proposed Tee-shaped topology under study is introduced in Fig. 4. It acts as a three-port circuit fed by voltage sources, $V_{k=1,2,3}$ through access node M_k. The middle node is denoted by M. Each branch M_kM presenting a series impedance, Z_k, is traversed by current, I_k with the subscript $k = 1,2,3$.

The fundamental and equivalent model of this proposed topology can be elaborated from the generalized Ohm's law expressed as:

$$\begin{bmatrix} I_1(s) \\ I_2(s) \\ I_3(s) \end{bmatrix} = [Y(s)] \times \begin{bmatrix} V_1(s) \\ V_2(s) \\ V_3(s) \end{bmatrix}. \tag{25}$$

The associated admittance matrix is analytically represented by:

$$[Y(s)] = \begin{bmatrix} Y_{11}(s) & Y_{12}(s) & Y_{13}(s) \\ Y_{21}(s) & Y_{22}(s) & Y_{23}(s) \\ Y_{31}(s) & Y_{32}(s) & Y_{33}(s) \end{bmatrix}. \tag{26}$$

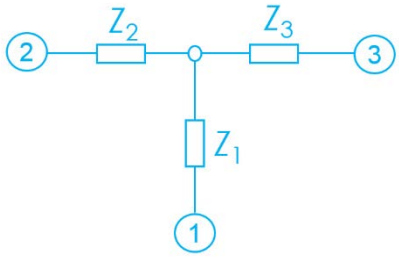


FIGURE 4. Tee-shaped topology general configuration.

To determine the constituting elements of this admittance matrix, we propose the theoretical investigation in the following paragraph.

B. ANALYTICAL EQUATIONS FOR EXTRACTING THE EQUIVALENT ADMITTANCE MATRIX

The proposed analytical expression of our proposed topology depicted by Fig. 4 can be established by the basic circuit theory. In this way, the application of the node Kirchhoff circuit law (KCL) at node M gives the equation:

$$I_1(s) + I_2(s) + I_3(s) = 0. \tag{27}$$

The KVL along the mesh GND-M_1MM_2-GND enables to write:

$$V_1(s) - Z_1(s)I_1(s) = V_2(s) - Z_2(s)I_2(s). \tag{28}$$

Under the similar way, the same law applied to mesh GND-M_3MM_2-GND gives:

$$V_3(s) - Z_3(s)I_3(s) = V_2(s) - Z_2(s)I_2(s). \tag{29}$$

These basic equations serve to the development of the Tee-shaped topology S-matrix equivalent model which will be obtained via the admittance matrix in the following subsection.

C. GENERAL EXPRESSION OF THE PROPOSED TOPOLOGY S-MATRIX FROM THE ADMITTANCE MATRIX

The expressions of the proposed topology branch current can be determined in function of the voltage sources and the branch impedances by solving the equation system constituted by relations (27), (28) and (29). The matrix representation of the rewritten solution lead to the Ohm's law of equation (26) with the admittance matrix:

$$[Y(s)] = \frac{\begin{bmatrix} Z_2(s)+Z_3(s) & -Z_3(s) & -Z_2(s) \\ -Z_3(s) & Z_1(s)+Z_3(s) & -Z_1(s)) \\ -Z_2(s) & -Z_1(s) & Z_1(s)+Z_2(s) \end{bmatrix}}{\zeta(s)} \tag{30}$$

with:

$$\zeta(s) = Z_1(s)\left[Z_2(s) + Z_3(s)\right] + Z_2(s)Z_3(s). \tag{31}$$

According the Y-to-S transform, the S-matrix can be determined from the admittance one expressed in equation (30):

$$[S(s)] = \{[Id_3] - R_0\,[Y(s)]\} \times \{[Id_3] + R_0\,[Y(s)]\}^{-1} \tag{32}$$

with:

- the 3-D identity matrix:

$$[Id_3] = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{33}$$

- and the reference impedance $R_0 = 50\ \Omega$.

Accordingly, we have the proposed topology following transmission coefficients in function the branch impedance:

$$S_{21}(s) = S_{12}(s) = \frac{2R_0\,[R_0 + Z_3(s)]}{D(s)} \tag{34}$$

$$S_{31}(s) = S_{13}(s) = \frac{2R_0\,[R_0 + Z_2(s)]}{D(s)} \tag{35}$$

$$S_{32}(s) = S_{23}(s) = \frac{2R_0\,[R_0 + Z_1(s)]}{D(s)} \tag{36}$$

with the denominator quantity:

$$D(s) = Z_1(s)\,[Z_2(s) + Z_3(s)] + Z_2(s)Z_3(s). \tag{37}$$

The associated reflection coefficients can be written as:

$$S_{11}(s) = \frac{\left\{\begin{array}{l} R_0\,[2Z_1(s) - R_0] + Z_2(s)Z_3(s) \\ +Z_1(s)\,[Z_2(s) + Z_3(s)] \end{array}\right\}}{D(s)} \tag{38}$$

$$S_{22}(s) = \frac{\left\{\begin{array}{l} R_0\,[2Z_2(s) - R_0] + Z_2(s)Z_3(s) \\ +Z_1(s)\,[Z_2(s) + Z_3(s)] \end{array}\right\}}{D(s)} \tag{39}$$

$$S_{33}(s) = \frac{\left\{\begin{array}{l} R_0\,[2Z_3(s) - R_0] + Z_2(s)Z_3(s) \\ +Z_1(s)\,[Z_2(s) + Z_3(s)] \end{array}\right\}}{D(s)}. \tag{40}$$

This general expression will be established to determine the RC network-based three-port circuit. Thus, the expressions enable to explore the NGD analysis in the next section.

V. NGD ANALYSIS OF THE THREE-PORT TEE-CIRCUIT

This section introduces the theoretical concept of the three-port Tee-shaped circuit NGD-type identification. The basic approach allowing the NGD analysis will be developed from the TF canonical forms explored in paragraph II-E.

A. S-MATRIX MODEL OF RC NETWORK-BASED THREE-PORT TOPOLOGY

Fig. 5 represents the corresponding Tee-shaped topology by using RC-network. This concrete three-port circuit is designed with RC-parallel network connected to port 1 to the middle point. The analytical expression can be obtained substituting the impedance by:

$$Z(s) = \frac{R}{1 + RCs}. \tag{41}$$

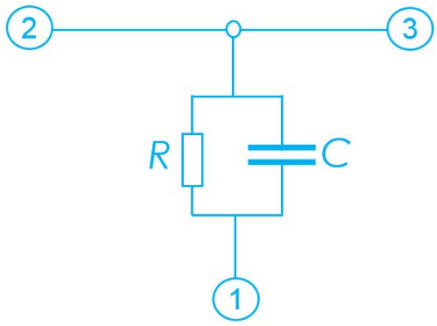


FIGURE 5. RC-network based Tee-shaped circuit.

Consequently, the reflection coefficients expressed in equations (34), (35) and (36) become respectively:

$$S_{21}(s) = S_{31}(s) = \frac{2R_0(1 + RCs)}{D_c(s)} \tag{42}$$

$$S_{32}(s) = \frac{2(R + R_0 + R_0RCs)}{D_c(s)}. \tag{43}$$

The corresponding denominator written in equation (37) becomes:

$$D_c(s) = 2R + 3R_0(1 + RCs). \tag{44}$$

Thus, the reflection coefficients expressed in equations (38), (39) and (40) becomes:

$$S_{11}(s) = \frac{2R - R_0 - R_0RCs}{D_c(s)} \tag{45}$$

$$S_{22}(s) = S_{33}(s) = \frac{-R_0(1 + RCs)}{D_c(s)}. \tag{46}$$

The NGD theorization of our lumped Tee-topology will be defined from this S-matrix model by means of the NGD canonical forms.

B. NGD ANALYSIS OF PORT①-PORT② TRANSMISSION

We can establish from the transmission coefficient expressed in equation (42) the NGD analysis corresponding to transmission through port① -port②. By identification with the TF expressed in equation (13), we have the following coefficients:

$$T_{021} = \frac{2R_0}{2R + 3R_0} \tag{47}$$

$$a_{21} = R\,C \tag{48}$$

$$b_{21} = \frac{3R_0R\,C}{2R + 3R_0}. \tag{49}$$

We can demonstrate that the GD at very LF will be:

$$\tau_{n21} = \frac{-2R^2C}{2R + 3R_0}. \tag{50}$$

We can remark that this GD is always negative whatever the values of R and C. Then, the cut-off frequency should be:

$$\omega_{021} = \frac{\sqrt{3(2R + 3R_0)}}{3R\,C\sqrt{R_0}}. \tag{51}$$

These last two formulas confirm that our three-port Tee-topology behaves as a LP-NGD type for the transmission through port① -port②.

C. NGD ANALYSIS OF PORT②-PORT③ TRANSMISSION

In this case, the analysis can be performed by considering the transmission coefficient expressed in equation (43). This corresponds to the NGD analysis associated to the transmission through port② -port③. By identification with the TF expressed in equation (13), we have the following coefficients:

$$T_{032} = \frac{2(R+R_0)}{2R+3R_0} \tag{52}$$

$$a_{32} = \frac{R_0 R\, C}{R+R_0} \tag{53}$$

$$b_{32} = \frac{3R_0 R\, C}{2R+3R_0}. \tag{54}$$

We can demonstrate that the GD at very LF will be:

$$\tau_{n32} = \frac{R^2 R_0 C}{(R+R_0)(2R+3R_0)}. \tag{55}$$

We can remark that this GD is unconditionally positive whatever the values of R and C. Then, the cut-off frequency should be:

$$\omega_{032} = \frac{\sqrt{3(R+R_0)(2R+3R_0)}}{3R_0 R\, C}. \tag{56}$$

These last two formulas confirm that our three-port Tee-topology behaves as a HP-NGD type for the transmission through port② -port③. The optimal frequency expressed in equation (22) becomes:

$$\omega_{m32} = \frac{\sqrt{\sqrt{3}(R+R_0)(2R+3R_0)\left[\frac{(2R+3R_0)}{3}+R+R_0+\sqrt{(R+R_0)(2R+3R_0)}\right]}}{\sqrt{3}\,R_0 R\, C}. \tag{57}$$

The minimal GD formulated in equation (23) is transformed as:

$$GD_{m32} = \frac{6\sqrt{3(R+R_0)(2R+3R_0)}}{5R+6R_0} - 3R_0 C. \tag{58}$$

Then, the attenuation at optimal frequency given in equation (24) becomes:

$$B_{32} = \sqrt{\sqrt{\frac{(2R+3R_0)^3}{27(R+R_0)^3}}}. \tag{59}$$

D. SYNTHESIS EQUATION FROM PORT①-PORT② LP-NGD SPECIFICATIONS

The methodology of LP-NGD type synthesis equations are elaborated in this subsection. The following synthesis equation is based on the desired values of:

- Attenuation, $A < 1$
- And the NGD value, $\tau_0 < 0$

1) RESISTOR SYNTHESIS EQUATION

By inverting equation (47), we have the synthesis equation of resistor:

$$R = \frac{R_0(2-3A)}{2A}. \tag{60}$$

It means that to get a realistic value of resistor, we must choose:

$$A < A_{\max} = 2/3. \tag{61}$$

By considering equation (60), Fig. 6 plots the variation of resistor R versus the attenuation A varied from -20 dB to -3.522 dB. We find that the resistor is decreasing from 0 to 425 Ω.

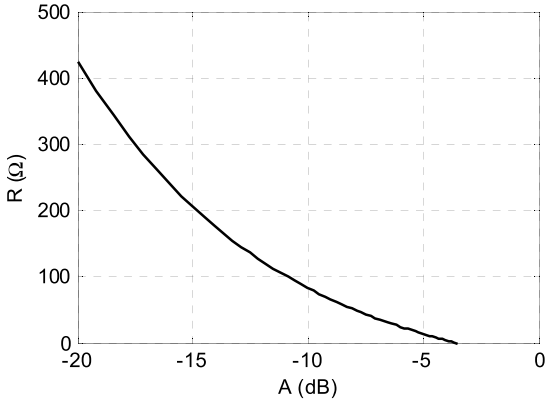


FIGURE 6. Plot of synthesized resistor versus attenuation.

2) CAPACITOR SYNTHESIS EQUATION

By inverting equation (50), we have the capacitor formula:

$$C = \frac{\tau_0(2R+3R_0)}{-2R^2}. \tag{62}$$

Substituting the resistor formula of equation (60) into previous one, we can also determine the capacitor by the equation:

$$C = \frac{-4A\ \tau_0}{(2-3A)^2 R_0}. \tag{63}$$

Fig. 7(a) represents the linear plot of ratio capacitor by absolute value of NGD value for attenuation A varied from -20 dB to -3.522 dB.

For the better understanding about the variation from 0.0028 F/s to 132 F/s, the y-scale semilogarithmic plot is proposed in Fig. 7(b).

The previously established synthesis formulas will also affect the other NGD parameters corresponding both port①-port② to port②-port③ and transmissions.

E. EFFECT OF SYNTHESIS FORMULAS ON PORT①-PORT② PARAMETERS

The LP-NGD synthesis formulas affect systematically the LP-NGD cut-off frequency and also the reflection coefficients. The analytical investigation on these impacts of chosen desired parameter as attenuation A will be studied in the following paragraphs.

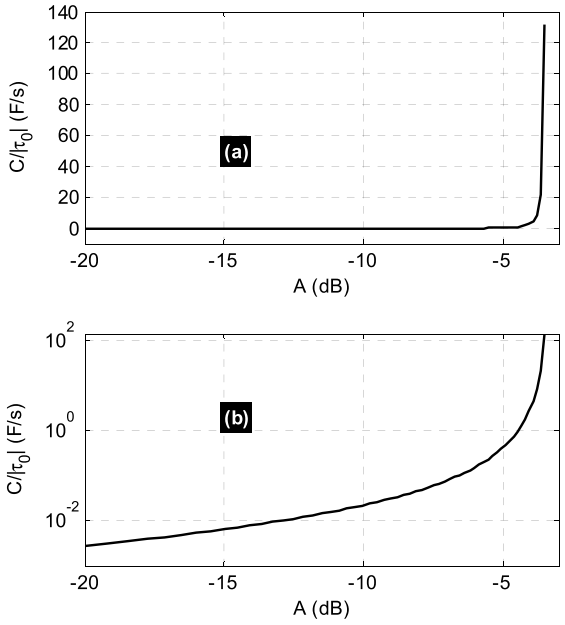


FIGURE 7. Plot of synthesized capacitor versus attenuation in (a) linear-linear and (b) y-scale semilogarithmic plots.

1) LP-NGD CUT-OFF FREQUENCY

Substituting the previously established formulas of R and C into the cut-off frequency written in equation (51), we can demonstrate that we have:

$$\omega_{021}(A, \tau_0) = \frac{3A-2}{\tau_0\sqrt{6A}}. \tag{64}$$

It yields from this equation the plot of product $\omega_{021}\tau_0$ shown by Fig. 8 for attenuation A varied from -20 dB to -3.522 dB. We can remark that the product is decreasing quite linearly when the attenuation is increasing.

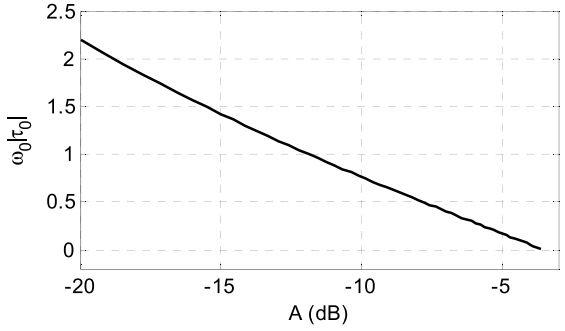


FIGURE 8. Product $\omega_0|\tau_0|$ versus A.

2) LF REFLECTION COEFFICIENTS VERSUS A

Moreover, under the same substitution, at very LF, the reflection coefficients ($S_{11}(\omega \approx 0) = |S_{11}(j\omega \approx 0)|$ and $S_{22}(\omega \approx 0) = |S_{22}(j\omega \approx 0)|$) expressed in equation (45) and in equation (46), become, respectively:

$$S_{11}(A) = 1 - 2A \tag{65}$$

$$S_{22}(A) = \frac{A}{2}. \tag{66}$$

The HP-NGD aspect parameters of transmission from port②-port③ will also be influenced by the synthesis equations.

F. EFFECT OF SYNTHESIS FORMULAS ON PORT②-PORT③ PARAMETERS

The LP-NGD synthesis formulas influence also the specifications of the HP-NGD behavior. The following paragraphs shows the expressions and ranges of variation of HP-NGD parameters as attenuation, frequencies and optimal GD versus chosen attenuation A varied from -20 dB to -3.522 dB.

1) HP-NGD ATTENUATION

Substituting the previously established synthesis formulas of equation (60) and equation (63) into the cut-off frequency written in equation (52), we have the transmission coefficient:

$$T_{032}(A) = 1 - \frac{A}{2}. \tag{67}$$

In this case, the HP-NGD function attenuation at very low frequency is decreasing from about -0.3 to $-.5$ dB as seen in Fig. 9.

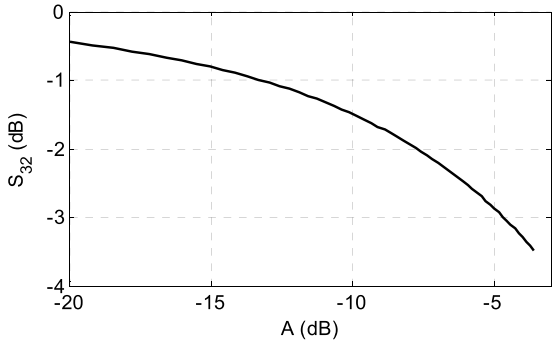


FIGURE 9. Attenuation T_{032} versus A.

2) HP-NGD CHARACTERISTIC FREQUENCIES

Following the same approach, the cut-off frequency of equation (56) is simplified as:

$$\omega_{032}(A, \tau_0) = \frac{(3A-2)\sqrt{2-A}}{2\sqrt{3}\,A\,\tau_0}. \tag{68}$$

Similarly, the optimal frequency given in equation (57) becomes:

$$\omega_{m32}(A, \tau_0) = \frac{(3A-2)\sqrt{\frac{\sqrt{3}}{2}\begin{bmatrix}(3A-10)\sqrt{2-A}\\ -2\sqrt{3}(2-A)\end{bmatrix}}}{6\tau_0 A}. \tag{69}$$

Fig. 10 plots the variations of:

- Product HP-NGD cut-off frequency:

$$f_{n32}\,|\tau_0| = \frac{\omega_{032}\,|\tau_0|}{2\pi} \tag{70}$$

- And product optimal frequency:

$$f_{m32}\,|\tau_0| = \frac{\omega_{m32}\,|\tau_0|}{2\pi}. \tag{71}$$

The corresponding abacuses are represented by black and red lines of Fig. 10, respectively. We can remark that despite the complexity of equations (68) and (69), both frequencies are decreasing until reaching zero value if we increase attenuation A.

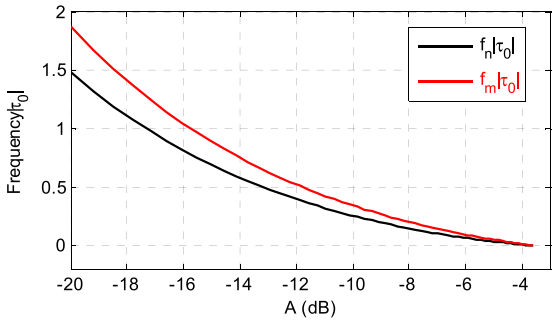


FIGURE 10. Product HP-NGD characteristic frequencies and NGD value versus A.

3) HP-NGD OPTIMAL NGD AND ASSOCIATED ATTENUATION

Moreover, the minimal GD expressed in equation (58) is transformed as:

$$GD_{m32}(A, \tau_0) = \frac{12A\ \tau_0}{(10-3A)\left[2+\sqrt{3(2-A)}\right]^2}. \tag{72}$$

In this case, we proposed to plot the ratio:

$$\frac{GD_{m32}}{\tau_0} = \frac{12A}{(10-3A)\left[2+\sqrt{3(2-A)}\right]^2}. \tag{73}$$

Fig. 11 represents the variation of the ratio versus attenuation A. We remark that the ratio is increasing with the attenuation.

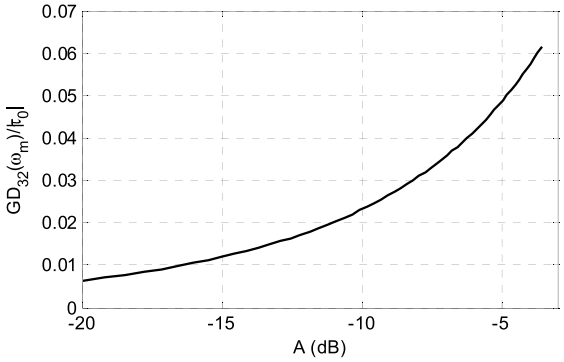


FIGURE 11. Ratio of HP-NGD optimal GD and NGD value versus A.

Then, the HP-NGD optimal attenuation previously established in equation (59) will become:

$$B_{32}(A) = \frac{2}{3}\sqrt{\frac{2}{2-A}\sqrt{\frac{3}{2-A}}}. \tag{74}$$

In this case, the variation of the HP-NGD optimal attenuation versus A is highlighted by Fig. 12.

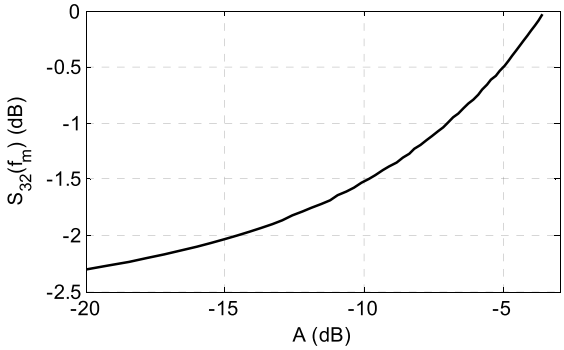


FIGURE 12. Attenuation S_{32} at the optimal frequency versus A.

As concrete illustration of this unfamiliar double NGD theory applied to three-port circuit, the following section introduces a verification study. The obtained experimental results from PoC circuits will be examined in the following section.

VI. VERIFICATION STUDY OF THE DEVELOPED DOUBLE NGD THEORY WITH TEE-CIRCUIT POC

The feasibility study of the developed double NGD theory is described in the present section. As PoC, a prototype of synthesized, designed and fabricated Tee-shaped circuit will be presented in the next subsection. Then, the calculated, simulated and measured results will be discussed.

A. POC DESCRIPTION

The prototypes of Tee-shaped circuit were designed and fabricated. The realization was carried out by means of preliminary calculations using the synthesis equations previously established in subsection V-D.

1) CALCULATED IDEAL COMPONENTS

The Tee-shaped circuit PoCs are designed in function of the desired LP-NGD specifications A and τ_0. Table 1 addresses the considered specification of three different cases of double NGD tee-shaped prototypes. The employed resistor and capacitor values were calculated following two synthesis equations of equation (60) and equation (63), respectively. Consequently, we get the calculated values of electrical parameters indicated in Table 1.

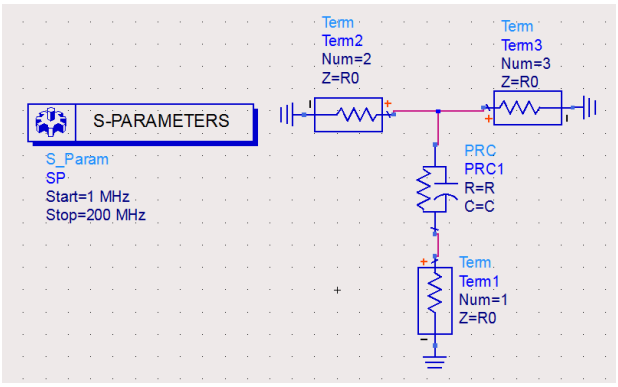
The values of corresponding LP- and HP-NGD cut-off frequencies calculated from formula (64) and equation (68) are also indicted in Table 1. To fabricate the associated circuit prototypes, we consider the resistor and capacitor nominal values belonging to E48 series. Therefore, we cannot have tolerances better than 5% of their nominal values.

2) DESIGNED AND FABRICATED CIRCUIT PROTOTYPES

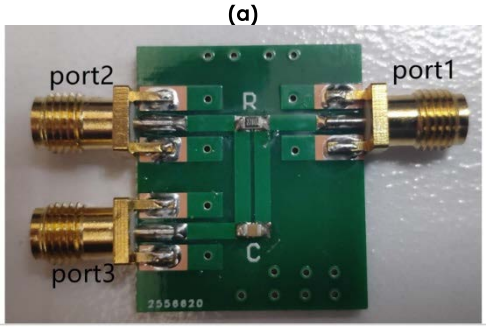
The Tee-shaped circuit prototypes were fabricated by using R and C SMD components. Before the realization, the

TABLE 1. Desired specifications and calculated ideal and normalized values of *R* and *C* components.

Description		Parameter	Name	Ideal value	Nominal value
(a) Prototype$_1$	Specifications	Attenuation	A	-6 dB	
		NGD value	τ_0	-3 ns	
		LP-NGD cut-off frequency	f_{21}	15.19 MHz	
		HP-NGD cut-off frequency	f_{32}	18.57 MHz	
	Calculated NGD circuit parameters	Resistor	R	24. 76 Ω	27 Ω
		Capacitor	C	488 pF	470 pF
(b) Prototype$_2$	Specifications	Attenuation	A	-7 dB	
		NGD value	τ_0	-3 ns	
		LP-NGD cut-off frequency	f_{21}	21.39 MHz	
		HP-NGD cut-off frequency	f_{32}	28.2 MHz	
	Calculated NGD circuit parameters	Resistor	R	36.94 Ω	39 Ω
		Capacitor	C	246 pF	270 pF
(c) Prototype$_3$	Specifications	Attenuation	A	-7 dB	
		NGD value	τ_0	-4 ns	
		LP-NGD cut-off frequency	f_{21}	16.04 MHz	
		HP-NGD cut-off frequency	f_{32}	21.15 MHz	
	Calculated NGD circuit parameters	Resistor	R	36.94 Ω	39 Ω
		Capacitor	C	328 pF	330 pF



(a)



(b)

FIGURE 13. (a) Schematic and (b) photograph of the fabricated Tee-shaped circuit with $R_0 = 50$ Ω.

circuits were designed in the ADS® schematic environment as shown by Fig. 13(a). The calculations of theoretical model were performed with MATLAB® commercial tool. The ADS® software is an RF and microwave circuit design and simulator commercial tool. Then, the photograph of the fabricated circuit is displayed by Fig. 13(b).

The Tee-shaped circuit prototypes were implemented on Cu-metalized FR4 dielectric substrate in hybrid technology. The substrate physical characteristics are indicated in Table 2.

TABLE 2. Physical parameters of the tee-shaped circuit substrate.

Structure	Description	Parameters	Values
Substrate	Relative permittivity	ε_r	4.5
	Loss tangent	$\tan(\delta)$	0.02
	Thickness	h	1.6 mm
Metallization conductor	Copper conductivity	σ	58 MS/s
	Thickness	t	35 µm

B. SIMULATED AND MEASUREMENT RESULTS FROM S-PARAMETERS

The experimental validation results of our double NGD theory of Tee-circuit will be elaborated in the following paragraphs.

1) EXPERIMENTAL SETUP

Similar to all classical microwave circuits, the NGD circuit measurement consists in recording the touchstone model of the circuit. Our experimental solution is based on the measurement of two-port S-parameters instead of three-port one which is the natural adequate solution for our LP-HP circuit. The illustrative diagram of the experimentation is displayed in Fig. 14(a). This experimental solution is due

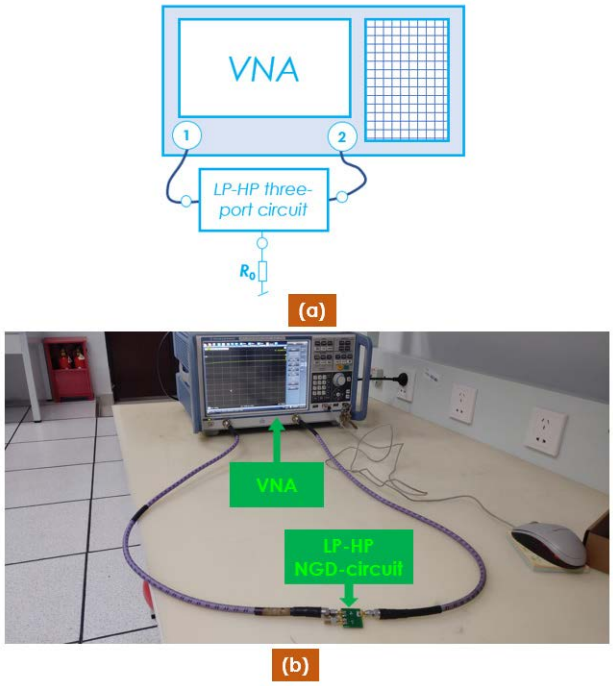


FIGURE 14. (a) Illustrative diagram and (b) photograph of the LP-HP NGD circuit experimental setup.

to the only available Vector Network Analyzer (VNA) in our laboratory. Accordingly, the fabricated Tee-shaped circuit prototype, previously introduced in Fig. 14(b), was measured with VNA (Rohde & Schwarz ZNB 20, within the frequency band 100 kHz to 20 GHz). It is noteworthy also that during the measurement process, the S-parameters test was made under SOLT calibration.

Thanks to the success of the experimental tests, we obtained the results discussed in the following paragraphs in the frequency band from $f_{min} = 100$ kHz (the lowest achievable with the available VNA) and $f_{max} = 100$ MHz.

2) DISCUSSION ON THE GD RESPONSE RESULTS

Comparisons between the GD responses of calculated (''Calc.'' plotted in black solid lines), simulated (''Simu.'' plotted in blue-sky dashed lines) and measured (''Meas.'' plotted in red dashed lines) results are discussed in the present paragraph. Indeed, the obtained results from two different key transmission coefficients are separately presented as follows:

For the first case, the GDs GD_{21a}, GD_{21b}, and GD_{21c} corresponding to transmission coefficients between port①-port② of Tee-shaped RC-network based prototype$_1$, prototype$_2$ and prototype$_3$ which are defined in Table 1 are plotted in Fig. 15(a), Fig. 15(b) and Fig. 15(c), respectively. It can be pointed out that the three GD responses plotted in Figs. 15 behave as a typical LP-NGD function. We can see in the zoomed plots of Fig. 17(a), Fig. 17(b) and Fig. 17(c) that based on the theoretical calculation and simulation, we can assess $GD_{21a}(f \approx 0) = -3$ ns, $GD_{21b}(f \approx 0) = -3$ ns,

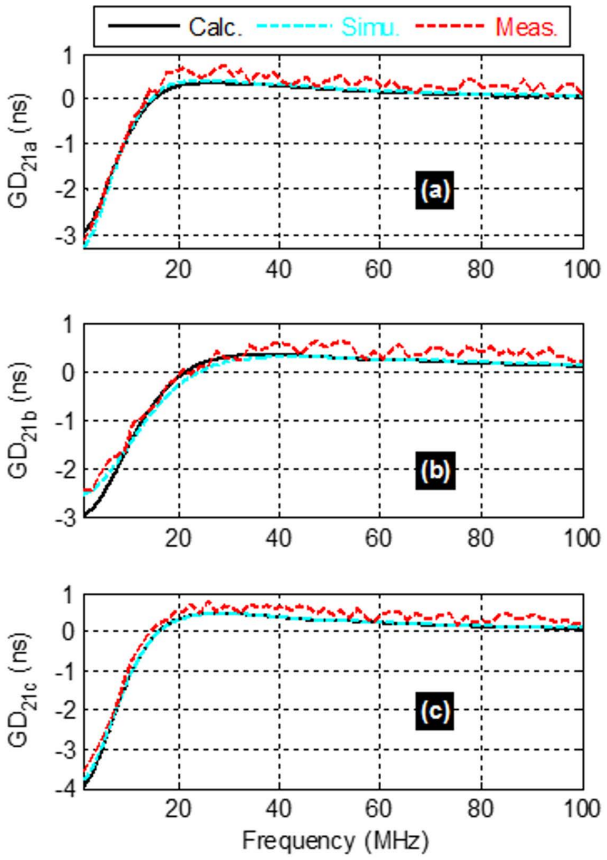


FIGURE 15. Comparisons of calculated, measured, and simulated GDs corresponding to port①-port② transmission coefficients: (a) prototype$_1$, (b) prototype$_2$ and (c) prototype$_3$.

and $G_{21c}(f \approx 0) = -4$ ns, as expected in the specifications addressed in Table 1. Then, very good correlations between the calculated, simulated and measured results of LP-NGD circuit are confirmed.

For the other case, GD_{32a}, GD_{32b}, and GD_{32c} corresponding to transmission coefficients between port②-port③ for the same tested prototypes are plotted in Fig. 16(a), Fig. 16(b) and Fig. 16(c), respectively. In this case, we can understand that the GD responses present rather typical HP-NGD behavior. We can see in the zoomed plots of Fig. 17(d), Fig. 17(e) and Fig. 17(f), that we have positive GDs at very low frequency. Furthermore, the GDs become negative when the frequency is higher than 18 MHz for the three tested circuit prototypes. Once again, the calculated, simulated and measured GDs are literally in good agreement.

Despite the successful verification of the double LP- and HP-NGD function behavior, we can underline here that the results from measurements are slightly shifted compared to the two other ones. The observed differences are mainly due to the dispersion of the circuit substrate parameters, the circuit electrical interconnections, the measurement systematic errors and also the used lumped component fabrication tolerances.

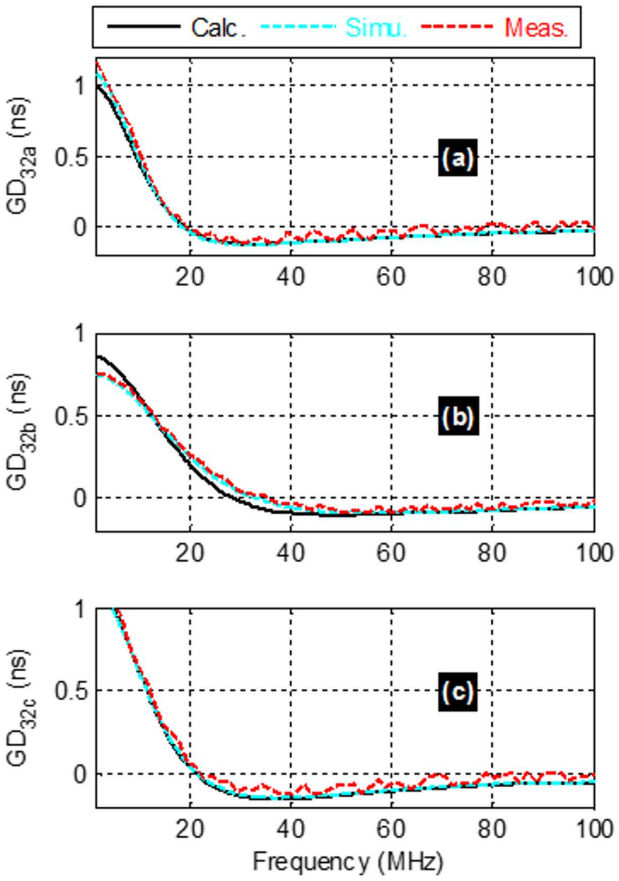


FIGURE 16. Comparisons of calculated, measured, and simulated GDs corresponding to port②-port③ transmission coefficients: (a) prototype$_1$, (b) prototype$_2$ and (c) prototype$_3$.

3) DISCUSSION ON THE S-PARAMETER MAGNITUDES

In addition to the GD responses, the RF NGD circuits are expected to operate under requirements with respect to the transmission and reflection coefficients. For this reason, comparisons between the calculated, simulated and measured results of transmission coefficient magnitudes are discussed in the present section.

The comparisons of transmission coefficients corresponding to port①-port② and port②-port③ are plotted in Figs. 18 and Figs. 19, respectively. As expected in Table 1, the transmission coefficients of Tee-shaped RC-network based port①-port② prototype$_1$, prototype$_2$ and prototype$_3$ are displayed respectively in Fig. 18(a), Fig. 18(b) and Fig. 18(c).

The transmission coefficients of port①-port② prototype$_1$, prototype$_2$ and prototype$_3$ are displayed respectively in Fig. 18(a), Fig. 18(b) and Fig. 18(c). As expected in Table 1, these transmission coefficients are higher than -6 dB, -7 dB and -6 dB, respectively. For the case of port②-port③, we have the transmission coefficients presented in Fig. 19(a), Fig. 19(b) and Fig. 19(c), respectively. In this case, all the transmission coefficients are better than -4 dB in the considered working frequency band lower than f_{max}.

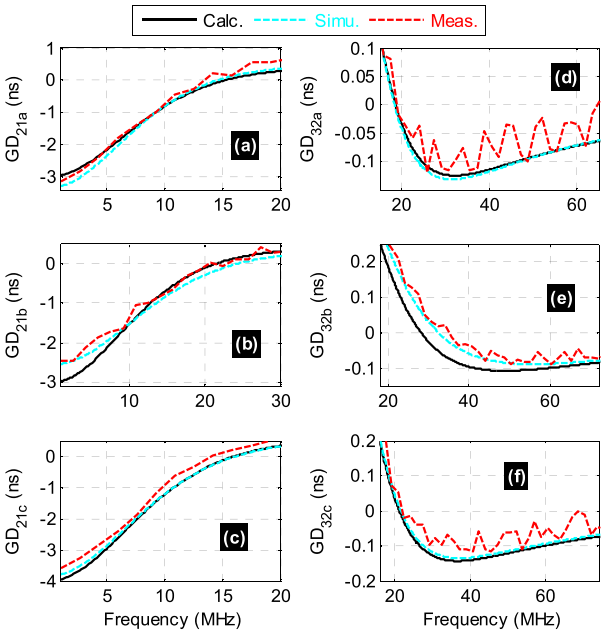


FIGURE 17. Comparisons of calculated, measured, and simulated GDs corresponding to (a) prototype$_1$, (b) prototype$_2$ and (c) prototype$_3$ port①-port② transmission coefficient GDs and (d) prototype$_1$, (e) prototype$_2$ and (f) prototype$_3$ port②-port③ transmission coefficient GDs.

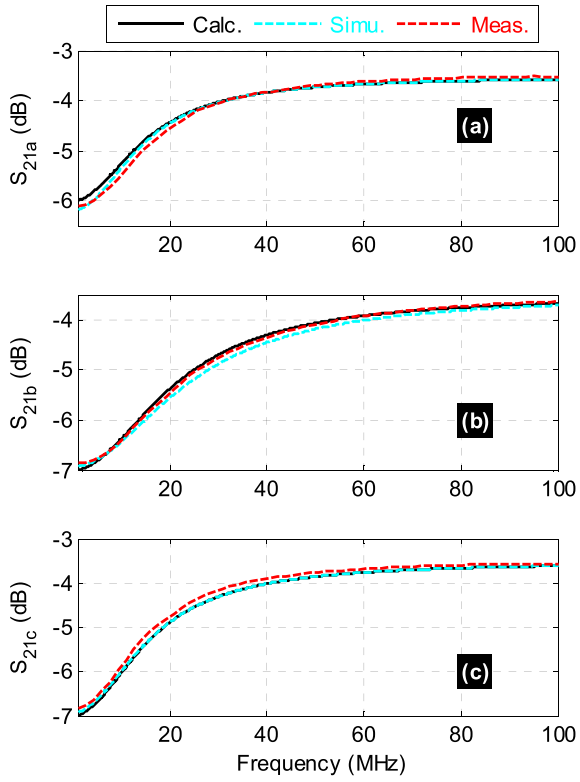


FIGURE 18. Comparisons of calculated, measured, and simulated port①-port② transmission coefficients: (a) prototype$_1$, (b) prototype$_2$ and (c) prototype$_3$.

The reflection coefficients of the double NGD three-port Tee-shaped RC-network based circuit were also investigated.

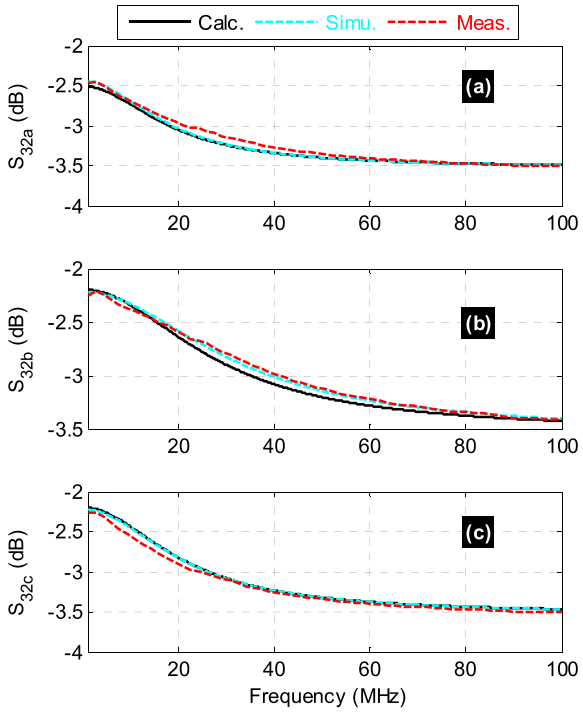


FIGURE 19. Comparisons of calculated, measured, and simulated port②-port③ transmission coefficients: (a) prototype$_1$, (b) prototype$_2$ and (c) prototype$_3$.

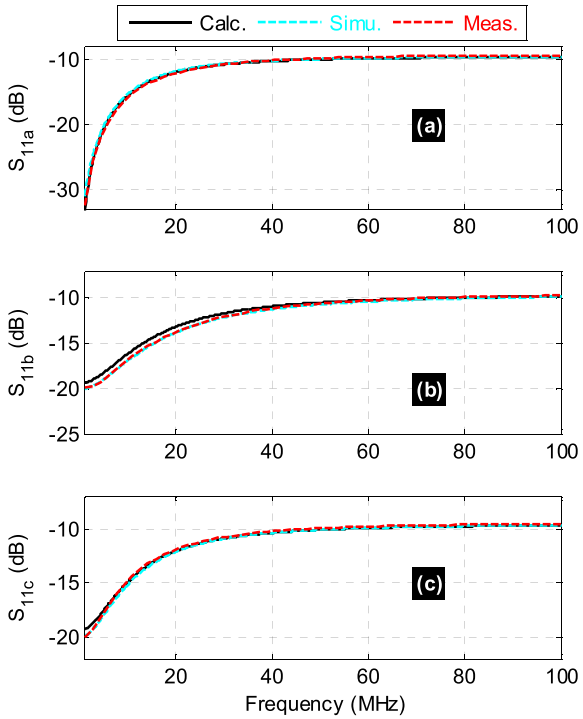


FIGURE 20. Comparisons of calculated, measured, and simulated S_{11} reflection coefficients: (a) prototype$_1$, (b) prototype$_2$ and (c) prototype$_3$.

Fig. 20(a), Fig. 20(b) and Fig. 20(c) display S_{11} of prototype$_1$, prototype$_2$ and prototype$_3$. Then, associated reflection coefficients $S_{22} \approx S_{33}$ are also proposed in Fig. 21(a), Fig. 21(b)

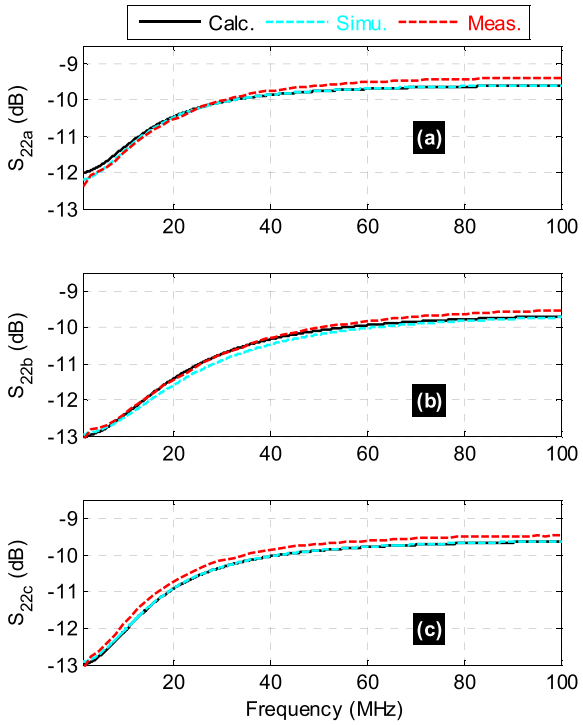


FIGURE 21. Comparisons of calculated, measured, and simulated S_{22} reflection coefficients: (a) prototype$_1$, (b) prototype$_2$ and (c) prototype$_3$.

and Fig. 21(c), respectively. It can be emphasized here that all the reflection coefficients are literally at worst around −9.5 dB. This means that the double both LP- and HP-NGD topology under study is susceptible to operate with less attenuation loss and good access matching.

C. STATE-OF-THE-ART COMPARISON OF NGD SPECIFICATIONS

Despite the progress of research interest on NGD circuit design, many efforts are still needed to increase its design familiarity compared to other classical electronic circuit design.

The main novelty of the present research work is more understandable with state-of-the-art comparison of NGD specifications. Therefore, Table 3 addresses the main differences of the proposed work compared to what was done in the literature [33]–[47]. Different topologies of two- [33]–[44], three- [45], [47] and four- [46] port circuits are discussed.

The main new contribution of the NGD engineering research present work is described as follows:

- The design of three-port NGD topology with only RC-network.
- The possibility to operate under double NGD function, the LP-NGD between port①-port② transmission and HP-NGD between port②-port③ transmission.
- Possibility to operate at both low and high frequencies (LF and HF).

TABLE 3. State of the art comparison of NGD specifications.

References	Design theory	Number of ports	NGD-type function	Operating frequency bands
[33-34,39]	Yes	2	Simple BP-NGD	LF and HF more than ten GHz
[35-37]	Yes		Simple BP-NGD	Only LF less than ten MHz
[34,39-41]	Yes		Simple LP-NGD	LF and HF more than ten GHz
[36-38]	Yes		Simple LP-NGD	Only LF less than ten MHz
[42,44]	Yes		Simple HP-NGD	LF and HF more than ten GHz
[43]	Yes		Simple HP-NGD	Only LF less than GHz
[45]	Yes	3	Simple LP-NGD	Only LF less than GHz
[46]	Yes	3	Simple BP-NGD	LF and HF more than ten GHz
[47]	Yes	4	Simple BP-NGD	Only LF less than GHz
Proposed work	Yes	3	Double LP- and HP-NGD	LF and HF more than ten GHz

VII. CONCLUSION

An original investigation on Tee-shaped passive topology operating with three-port circuit is developed.

The basic definition of parameters allowing to specify the LP- and HP-NGD function is described. The modelling of the Tee-shaped topology with 3-D S-matrix is established. The S-matrix study leads to the LP- and HP-NGD analyses. The original implementation of both double LP- and HP-NGD aspects is initiated in the first time. The existence condition of LP-NGD aspect from one branch of the Tee-circuit is proposed. Also, the existence condition of HP-NGD aspect through another branch of the Tee-circuit is expressed. The synthesis equations enabling to determine the resistor and capacitor elements are formulated.

The verification of the theoretical approach is performed with MATLAB® computation of the developed S-parameter model. Simulation was also run with commercial simulation tool. A three-port circuit comprised by SMD resistor and capacitor components is designed, implemented and tested. Then, measurements were realized in RF frequency band. As expected, the obtained results confirm outstandingly the validity of the double LP- and HP-NGD aspects. Moreover, calculated model, simulations and measurements in good agreement are presented.

REFERENCES

[1] R. Ho, K. W. Mai, and M. A. Horowitz, "The future of wires," *Proc. IEEE*, vol. 89, no. 4, pp. 490–504, Apr. 2001.
[2] D. K. Sharma, B. K. Kaushik, and R. K. Sharma, "VLSI interconnects and their testing: Prospects and challenges ahead," *J. Eng., Des. Technol.*, vol. 9, no. 1, pp. 63–84, Mar. 2011.
[3] M. A. Sayed and E. Y. A. Maksoud, "Interconnect synthesis in high speed digital VLSI routing," *Int. J. Open Problems Compt. Math.*, vol. 2, no. 3, pp. 383–415, Sep. 2009.
[4] C.-W. A. Tsao and C.-K. Koh, "A clock tree router for general skew constraints," *J. ACM TODAES*, vol. 7, no. 3, pp. 359–379, 2002.
[5] M. Qungang, Y. Yintang, L. Yuejin, and J. Xinzhang, "Optimal cascade lumped model of deep submicron on-chip interconnect with distributed parameters," *Microelectron. Eng.*, vol. 77, nos. 3–4, pp. 310–318, Apr. 2005.
[6] X.-C. Li, J.-F. Mao, and M. Tang, "High-speed clock tree simulation method based on moment matching," in *Proc. Prog. Electromagn. Res. Symp.*, Hangzhou, China, Aug. 2005, pp. 178–181.
[7] V. L. Chi, "Salphasic distribution of clock signals for synchronous systems," *IEEE Trans. Comput.*, vol. 43, no. 5, pp. 597–602, May 1994.
[8] X.-C. Li, J.-F. Mao, H.-F. Huang, and Y. Liu, "Global interconnect width and spacing optimization for latency, bandwidth and power dissipation," *IEEE Trans. Electron Devices*, vol. 52, no. 10, pp. 2272–2279, Oct. 2005.
[9] J. L. Wyatt, Jr., and Q. Yu, "Signal delay in RC meshes, trees and lines," in *Proc. IEEE ICAD*, Nov. 1984, pp. 15–17.
[10] P. K. Chan and M. D. F. Schlag, "Bounds on signal delay in RC mesh networks," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 8, no. 6, pp. 581–589, Jun. 1989.
[11] D. Standley and J. L. Wyatt, Jr., "Improved signal delay bounds for RC tree networks," in *VLSI Memo*. Cambridge, MA, USA: MIT, May 1986, nos. 86–317.
[12] N. Jain, V. Prasad, and A. Bhattacharyya, "Delay-time sensitivity in linear RC tree," *IEEE Trans. Circuits Syst.*, vol. CS-34, no. 4, pp. 443–445, Apr. 1987.
[13] A.-C. Deng and Y.-C. Shiau, "Generic linear RC delay modeling for digital CMOS circuits," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 9, no. 4, pp. 367–376, Apr. 1990.
[14] L. P. P. P. van Ginneken, "Buffer placement in distributed RC-tree networks for minimal Elmore delay," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 1990, pp. 865–868.
[15] R. Gupta, B. Tutuianu, and L. T. Pileggi, "The Elmore delay as a bound for RC trees with generalized input signals," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 16, no. 1, pp. 95–104, Jan. 1997.
[16] L. Vandenberghe, S. Boyd, and A. El Gamal, "Optimizing dominant time constant in RC circuits," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 17, no. 2, pp. 110–125, Feb. 1998.
[17] C. A. Marinov and A. Rubio, "The energy bounds in RC circuits," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 46, no. 7, pp. 869–871, Jul. 1999.
[18] K. T. Tang and E. G. Friedman, "Delay and noise estimation of CMOS logic gates driving coupled resistive–capacitive interconnections," *Integr. VLSI J.*, vol. 29, no. 2, pp. 131–165, Sep. 2000.
[19] C. V. Kashyap, C. J. Alpert, F. Liu, and A. Devgan, "Closed-form expressions for extending step delay and slew metrics to ramp inputs for RC trees," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 23, no. 4, pp. 509–516, Apr. 2004.
[20] A. B. Kahng and S. Muddu, "An analytical delay model for RLC interconnects," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 16, no. 12, pp. 1507–1514, Dec. 1997.
[21] Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Equivalent Elmore delay for RLC trees," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 19, no. 1, pp. 83–97, Jan. 2000.
[22] S.-P. Sim, S. Krishnan, D. M. Petranovic, N. D. Arora, K. Lee, and C. Y. Yang, "A unified RLC model for high-speed on-chip interconnects," *IEEE Trans. Electron Devices*, vol. 50, no. 6, pp. 1501–1510, Jun. 2003.
[23] A. Nieuwoudt, J. Kawa, and Y. Massoud, "Crosstalk-induced delay, noise, and interconnect planarization implications of fill metal in nanoscale process technology," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 3, pp. 378–391, Mar. 2010.
[24] M. A. El-Moursy and E. G. Friedman, "Exponentially tapered H-tree clock distribution networks," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 8, pp. 971–975, Aug. 2005.

[25] Y. Yutaka, A. Hideharu, K. Michihiro, J. Akiya, and A. Kenichiro, "Fat H-tree: An interconnection network for reconfigurable processor array," *J. IEICE Trans. Inf. Syst.*, vol. 89, no. 9, pp. 1923–1934, 2006.
[26] J. Rosenfeld and E. G. Friedman, "Design methodology for global resonant H-tree clock distribution networks," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 2, pp. 135–148, Feb. 2007.
[27] I. Chanodia and D. Velenis, "Parameter variations and crosstalk noise effects on high performance H-tree clock distribution networks," *Analog Integr. Circuits Signal Process.*, vol. 56, pp. 13–21, Mar. 2008.
[28] W.-K. Loo, K.-S. Tan, and Y.-K. Teh, "A study and design of CMOS H-tree clock distribution network in system-on-chip," in *Proc. 8th IEEE Int. Conf. ASIC*, Changsha, China, Oct. 2009, pp. 411–414.
[29] B. Ravelo, "Behavioral model of symmetrical multi-level T-tree interconnects," *Prog. Electromagn. Res.*, vol. 41, pp. 23–50, 2012.
[30] B. Ravelo, O. Maurice, and S. Lalléchère, "Asymmetrical 1:2 Y-tree interconnects modelling with Kron–Branin formalism," *Electron. Lett.*, vol. 52, no. 14, pp. 1215–1216, Jul. 2016.
[31] B. Ravelo and O. Maurice, "Kron–Branin modeling of Y-Y-tree interconnects for the pcb signal integrity analysis," *IEEE Trans. Electromagn. Compat.*, vol. 59, no. 2, pp. 411–419, Apr. 2017.
[32] C. J. Alpert, A. Devgan, and S. T. Quay, "Buffer insertion for noise and delay optimization," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 18, no. 11, pp. 1633–1645, Nov. 1999.
[33] K.-P. Ahn, R. Ishikawa, and K. Honjo, "Group delay equalized UWB InGaP/GaAs HBT MMIC amplifier using negative group delay circuits," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 9, pp. 2139–2147, Sep. 2009.
[34] B. Ravelo, S. Lalléchère, A. Thakur, A. Saini, and P. Thakur, "Theory and circuit modeling of baseband and modulated signal delay compensations with low- and band-pass NGD effects," *AEU-Int. J. Electron. Commun.*, vol. 70, no. 9, pp. 1122–1127, Sep. 2016.
[35] M. W. Mitchell and R. Y. Chiao, "Negative group delay and 'fronts' in a causal system: An experiment with very low frequency bandpass amplifiers," *Phys. Lett. A*, vol. 230, nos. 3–4, pp. 133–138, Jun. 1997.
[36] M. Kitano, T. Nakanishi, and K. Sugiyama, "Negative group delay and superluminal propagation: An electronic circuit approach," *IEEE J. Sel. Topics Quantum Electron.*, vol. 9, no. 1, pp. 43–51, Jan./Feb. 2003.
[37] Y. Meng, Z. Wang, S. Fang, T. Shao, and H. Liu, "A broadband switchless bi-directional amplifier with negative-group-delay matching circuits," *Electronics*, vol. 7, no. 9, pp. 1–11, Aug. 2018.
[38] M. T. Abuelma'atti and Z. J. Khalifa, "A new CFOA-based negative group delay cascadable circuit," *Anal. Integr. Circuits Signal Process.*, vol. 95, no. 2, pp. 351–355, May 2018.
[39] B. Ravelo, "Similitude between the NGD function and filter gain behaviours," *Int. J. Circuit Theory Appl.*, vol. 42, no. 10, pp. 1016–1032, Oct. 2014.
[40] B. Ravelo, "First-order low-pass negative group delay passive topology," *Electron. Lett.*, vol. 52, no. 2, pp. 124–126, Jan. 2016.
[41] R. Randriatsiferana, Y. Gan, F. Wan, W. Rahajandraibe, R. Vauché, N. M. Murad, and B. Ravelo, "Study and experimentation of a 6-dB attenuation low-pass NGD circuit," *Analog Integr. Circuits Signal Process.*, vol. 10, pp. 1–14, Apr. 2021.
[42] B. Ravelo, "High-pass negative group delay RC-network impedance," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 9, pp. 1052–1056, Sep. 2017.
[43] F. Wan, X. Huang, K. Gorshkov, B. Tishchuk, X. Hu, G. Chan, F. E. Sahoa, S. Baccar, M. Guerin, W. Rahajandraibe, and B. Ravelo, "High-pass NGD characterization of resistive-inductive network based low-frequency circuit," *COMPEL-Int. J. Comput. Math. Electr. Electron. Eng.*, vol. 40, no. 5, pp. 1032–1049, 2021.
[44] R. Yang, X. Zhou, S. Yazdani, E. Sambatra, F. Wan, S. Lalléchère, and B. Ravelo, "Analysis, design and experimentation of high-pass negative group delay lumped circuit," *Circuit World*, pp. 1–25, Aug. 2021.
[45] E. J. R. Sambatra, A. Jaomiary, S. Ngoho, S. S. Yazdani, N. M. Murad, G. Chan, and B. Ravelo, "Low-pass negative group delay modelling and experimentation with TRI-port resistorless passive cross-circuit," *Prog. Electromagn. Res. M*, vol. 108, pp. 39–51, 2022.
[46] F. Wan, Y. Liu, J. Nebhen, Z. Xu, G. Chan, S. Lalléchère, R. Vauche, W. Rahajandraibe, and B. Ravelo, "Bandpass negative group delay theory of fully capacitive Δ-network," *IEEE Access*, vol. 9, pp. 62430–62445, 2021.
[47] B. Ravelo, F. Wan, J. Nebhen, G. Chan, W. Rahajandraibe, and S. Lalléchère, "Bandpass NGD TAN of symmetric H-tree with resistorless lumped-network," *IEEE Access*, vol. 9, pp. 41383–41396, 2021.

HONGCHUAN JIA received the B.Sc. degree in communication engineering from the Nanjing University of Information Science and Technology, Nanjing, China, in 2021, where he is currently pursuing the M.S. degree. His research interests include abnormal wave propagation in dispersive media and microwave circuits.

FAYU WAN (Senior Member, IEEE) received the Ph.D. degree in electronic engineering from the University of Rouen, Rouen, France, in 2011. From 2011 to 2013, he was a Postdoctoral Fellow with the Electromagnetic Compatibility Laboratory, Missouri University of Science and Technology, Rolla. He is currently a Full Professor with the Nanjing University of Information Science and Technology, Nanjing, China. His current research interests include negative group delay circuits, electrostatic discharge, electromagnetic compatibility, and advanced RF measurement.

JAROSLAV FRNDA (Senior Member, IEEE) was born in Martin, Slovakia, in 1989. He received the M.Sc. and Ph.D. degrees from the Department of Telecommunications, VSB—Technical University of Ostrava, in 2013 and 2018, respectively. He is currently an Assistant Professor at the University of Žilina, Slovakia. He has authored or coauthored 21 SCI-E and eight ESCI articles in WoS. His research interests include quality of multimedia services in IP networks, data analysis, and machine learning algorithms.

MATHIEU GUERIN (Member, IEEE) received the Engineering degree in microelectronics and telecommunications from Polytech Marseille, in 2010, and the Ph.D. degree from the Aix Marseille University, in 2013. In 2010, he was a Research Master in integrated circuits design from the Aix Marseille University. He worked as a Technical Leader of the Analog and Radio-Frequency Design Team, IDEMIA-StarChip, for five years, and designed chips embedded in SIM cards and contactless bank cards with biometric recognition. In 2020, he joined Aix-Marseille University as an Assistant Professor and the CCSI Team, IM2NP Laboratory. His research interest includes design and synthesis of circuits in digital electronics. He is also working on methods of modeling and characterizing circuits in analog electronics.

WENCESLAS RAHAJANDRAIBE (Member, IEEE) received the B.Sc. degree in electrical engineering from Nice Sophia-Antipolis University, France, in 1996, the M.Sc. degree (Hons.) in electrical engineering from the Science Department, University of Montpellier, France, in 1998, and the Ph.D. degree in microelectronics form the University of Montpellier. In 1998, he joined the Microelectronics Department of Informatics, Robotics and Microelectronics Laboratory of Montpellier (LIRMM). In 2003, he joined the Microelectronic Department of Materials, Microelectronics and Nanoscience Laboratory of Provence (IM2NP), Marseille, France, where he was an Associate Professor. Since 2014, he has been a Professor at Aix Marseille University, where he heads the Integrated Circuit Design Group, IM2NP Laboratory. He is currently a Full Professor at Aix Marseille University. He is regularly involved to participate and to lead national and international research projects (ANR, H2020, and FP7 KIC-InnoEnergy). He directed and co-supervised 18 Ph.D. and 15 master's students. His research interests include AMS and RF circuit design from transistor to architectural level. His present research activity is focused on ultra-low-power circuit design for smart sensor interface and embedded electronic in bioelectronic and e-health applications, wireless systems, design technique, and architecture for multi-standard transceiver. He is the author or coauthor of 11 patents and more than 150 papers published in refereed journals and conferences. He is an expert for the ANR, the French Agency for Research. He has served on program committees for IEEE NEWCAS and ICECS. He has been and is a reviewer of contributions submitted to several IEEE conferences and journals, such as ISCAS, NEWCAS, MWSCAS, ESSCIRC, ESSDERC, RFIC, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, and *Electronics Letters* (IET).

PREETI THAKUR received the M.Phil. and Ph.D. degrees from Himachal Pradesh University, Shimla.

She is currently working as a Professor and the Head of the Physics Department, Amity University Haryana. She has published more than 100 research articles in national and international journals. She has supervised 66 master's and four Ph.D. students. She is invited by the Royal Academy of Engineering, U.K., to attend invited professors meet at Birmingham. She has several national and international collaborations and projects. She has filed 14 patents till date. She received the Gold Medal in electronics from HPU.

ATUL THAKUR received the M.Sc., M.Phil., and Ph.D. degrees from Himachal Pradesh University, Shimla. He held a postdoctorate training at the University of Brest, France, and the National Taiwan University, Taiwan. He is currently working as the Director with the Centre for Nanotechnology, Amity University Haryana. He has worked on various projects sponsored by DRDO, DAE, DST, and MNRE. He has published more than 100 international research papers and filed 15 patents. Recently, he has been awarded Newton Award from Royal Academy of Engineering, U.K.

BENOÎT AGNUS received the Ph.D. degree in microwave and millimeter wave engineering instrumentation and measurement techniques from the Laboratory of Physics of Interactions Waves Materials (''Physique d'Interaction Ondes Matières = PIOM''), University of Bordeaux 1, in 1994. He is currently the Director of the independent applied research enterprise ''Wave Conception.'' The enterprise is performing research in the areas of electromagnetism, plasmas, and multi-parametric servo systems. He pursued a 25-year career in industrial research and development (R&D) and published several scientific papers. His interests include electromagnetic waves, RF/microwave system modeling and post-processing, spatial or terrestrial communication instrumentation, plasma production and control, energy issues for system autonomy, embedded intelligence for the diagnosis and reconfiguration of complex systems, signal processing, and RF/microwave transceiver architectures.

BLAISE RAVELO (Member, IEEE) is currently a University Full Professor at NUIST, Nanjing, China. His research interests include multiphysics and electronics engineering. He lectures on circuit and system theory, science, technology, engineering and maths (STEM), and applied physics. He is a pioneer of the negative group delay (NGD) concept about $t < 0$ signal traveling in physical space. This extraordinary concept is potentially useful for anticipating and prediction all kind of information. He was the Research Director of 11 Ph.D. students (ten defended), postdoctorals, research engineers, and master internships. With U.S., Chinese, Indian, European, and African partners, he is actively involved and contributes on several international research projects (ANR, FUI, FP7, INTERREG, H2020, Euripides^2, and Eurostars). He is a member of *Electronics Letters* (IET)'s Editorial Board as a Circuit and System Subject Editor. He is a member of the Scientific Technical Committee of Advanced Electromagnetic Symposium (AES), in 2013, and IMOC2021. He is ranked in Top 2% world's scientists (2020–2021) by Stanford University, USA (https://elsevier.digitalcommonsdata.com/datasets/btchxktzyw/3). He has Google Scholar H-index (2022) = 24 and i10-index (2022) = 72. He is a member of research groups such as IEEE, URSI, GDR Ondes, and Radio Society, and (co)authors of more than 360 scientific research papers in new technologies published in international conference and journals. He is regularly invited to review papers submitted for publication to international journals (IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE ACCESS, *IET CDS*, and *IET MAP*) and books (Wiley and Intech Science).