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An Adaptive Multi-Resonant Current Controller for a Single-Phase Grid-Tied Converter With Grid Disturbance Rejection Capability

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ABSTRACT The grid-tied converters are always susceptible to abnormal grid disturbances, which are countered with the advanced current controllers. This paper presents an adaptive multi-resonant current controller (MRCC) in a current loop to maintain the converter synchronization with the grid under grid disturbance. The most critical disturbance like dc-offset, frequency variation, and harmonics in the grid voltage leads to current tracking performance degradation due to their non-adaptive nature. The modified second-order generalized integrator (MSOGI) based phase-locked loop (PLL) is proposed with grid frequency adaptability. The detailed analysis of the adaptive MRCC is presented with the dc-offset, frequency deviation, and harmonics in the grid voltage. The proposed MSOGI-PLL with an adaptive MRCC is tested under non-ideal grid conditions indicating the enhanced dynamic response over the non-adaptive methods. The efficacy of the frequency adaptive MRCC is tested on the laboratory prototype model of the single-phase GTC.

INDEX TERMS Phase-locked loop, grid-tied converters (GTCs), multi-resonant current controller (MRCC), unity power factor (UPF), modified second-order generalized integrator.

I. INTRODUCTION

A surge in the power supply demand and the shortage of thermal power has led to the foundation of the GTCs for the renewable energy system (RES) and the energy storage system (ESS). Single-phase GTCs find their potential application in the solar inverter, solar pump, solar heater, and uninterruptible power supply (UPS) [1], [2]. A detailed study on the different topologies of 1-φ GTCs for PV application is provided in [3]–[5]. There are two tasks performed by the inverter interfacing PV modules to the grid. The first one is the MPPT of the PV module, and the second is to inject sinusoidal current into the grid.

The bandwidth of the voltage control loop controls the transients of the dc-bus voltage. High bandwidth with a low value of the electrolytic capacitor controls the dc-bus voltage overshoot and undershoots during the load change. The ripple eliminator circuit is proposed to eliminate the dc-bus voltage ripple which replaces the bulky electrolytic capacitor [6], [7].

Single-phase GTCs suffer from the inherent problem of *2f* oscillation at the dc-bus and grid current harmonics at the grid side. In [8], a three-port converter is proposed. The third port is connected to an ESS via a power electronics converter. The idea is to regulate the dc-bus voltage while eliminating the dc-bus voltage ripple, and also reducing the size of the electrolytic capacitor. A voltage control loop based on the digital finite impulse response (FIR) filter is proposed in [9]. The FIR filters the second harmonic ripples of the dc-link voltage.

An adaptive PI controller has been implemented on the dc-bus voltage control loop to solve the problem of the *2f* oscillation of the dc-bus voltage and also grid current harmonics reduction [10]. The PI controller gains depend on the natural frequency (ω_n). The selection of ω_n depends upon the

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maximum value of the dc-bus voltage ripple and also the dc-bus voltage fluctuations during the load change. Double line frequency ripple power is a critical issue associated with 1-φ GTCs. This ripple power decreases the life span of the batteries, PV modules, and fuel cells [11], [12]. In [13], a model predictive control (MPC) has been implemented to control the power converter and drives. A current decoupling control scheme for the 1-φ GTC is discussed in [14]. In this scheme, the coupling terms between the q-axis and d-axis components are eliminated and a decoupling method is proposed to obtain a fast dynamic response of the converter.

Single-phase PLLs are crucial in synchronizing and controlling the GTCs. Several 1-φ PLLs and their performances are analyzed and discussed under the grid voltage distorted conditions [15]–[18]. In [19], a method is proposed to tune the bandwidth of the PLL appropriately and also the generated unit vectors have an acceptable limit of distortion. However, this technique has been implemented on the 3-φ PLL. The harmonics and dc-offset in V_g generate low-frequency oscillation in the estimated frequency and phase-angle. This results in the distorted unit vectors generated by the PLL. Hence, the reference current ($I*_{ref}$) of the current control loop also gets distorted. The current controller fails to track $I*_{ref}$ accurately in the presence of the dc-offset and harmonics in V_g. A notch filter-based approach is proposed in [20] to mitigate the dc-offset present in the input of the PLL. This approach uses an integrator to the PLL structure. A dc-offset rejection technique for 1-φ SRF-PLL is elaborated in [21]. An enhanced SOGI-PLL has been proposed to estimate the grid voltage θ_g and f_g when the V_g is contaminated with the dc-offset. An advanced 1-φ SOGI-PLL is proposed in [22] to estimate the grid voltage θ_g and f_g under polluted grid conditions including harmonics, dc-offset, and grid faults. In [23], slow frequency adaptation (SFA) of the orthogonal signal generator (OSG) is proposed to eliminate the influence of the OSG dynamics on the PLL loop gain. This is achieved by using an LPF in the frequency feedback loop to decouple the dynamics of SOGI-based OSG and SRF-PLL.

Proportional plus resonant (PR) controllers are widely used in the inner current control loop because of the reduced steady-state error and fast-tracking of the sinusoidal reference signal. The PR controller fails during the off-nominal grid frequency because the controller has been designed to track the reference signal at the fixed resonant frequency. The above-mentioned problem has been reported in [24]–[27]. This problem has been eradicated by modifying the PLL structure to immune against the grid frequency drift. The frequency adaptive selective harmonic control (FA-SHC) is proposed in [28] to eliminate the grid current harmonics under off-nominal grid-frequency variation from 50±0.50 Hz and 50±1.0 Hz. In [29], frequency-selective filters in the frequency locked loop (FLL) along with the PR controller are proposed to obtain the UPF operation at the grid side under grid frequency drift. However, the effect of polluted V_g with harmonics + dc-offset under off-nominal f_g on the dc-bus voltage is not presented in [28], [29]. In [30], adaptive

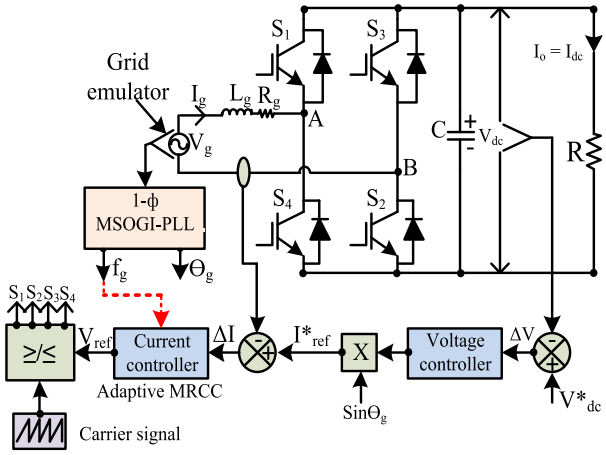

FIGURE 1. Schematic diagram of 1-φ grid-tied AC-DC converter and its control technique.

control for different grid impedances is achieved by implementing the impedance-phased dynamic control technique. In [30], a delay-based OSG has been used in the SRF-PLL that causes large in-loop phase delay and hence, limits the PLL bandwidth.

In this paper, a frequency adaptive MRCC has been designed to control 1-φ GTC efficiently. The frequency adaptive MRCC is implemented to reduce the harmonics of the grid current and achieve the UPF operation at the grid side under polluted grid conditions while meeting IEEE standard 1547 [31]. The MRCC performance is tested for dc-offset and 3^{rd}+ 5^{th} harmonic in the grid voltage under grid frequency fluctuation. The contributions in this paper are highlighted as follows:

1) An MSOGI-PLL is proposed to estimate θ_g and f_g accurately under off-nominal grid frequency along with the polluted grid conditions while complying with the power quality standard.
2) The adaptive MRCC has the capability to mitigate the lower-order harmonics from I_g in the presence of dc-offset and harmonics in V_g under nominal and off-nominal grid frequencies while maintaining the UPF operation at the grid side.

This manuscript is arranged in the following sections: The control technique adopted over 1-φ GTC is described in section II. The MSOGI-PLL analysis is presented in section III. The experimental results and conclusion are presented in sections IV and V respectively. The performances of adaptive controllers are mentioned in Table 3 considering different grid conditions.

II. CONTROL TECHNIQUE OF SINGLE-PHASE GRID-TIED CONVERTER

The control technique of a 1-φ GTC is shown in Fig. 1. The voltage and current control loop are cascaded [32].

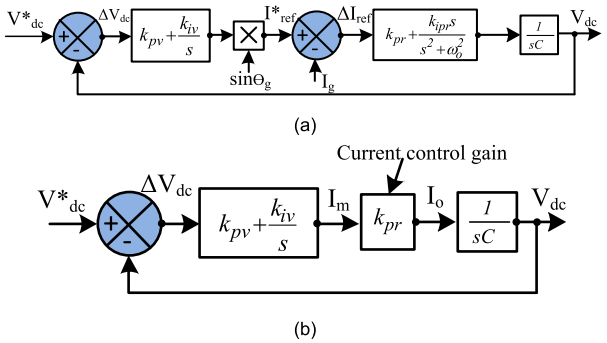

FIGURE 2. **(a) Closed-loop control diagram of the 1-φ GTC. (b) The simplified control diagram of the voltage control loop.**

The outer loop is the dc-bus voltage control loop to track V^*_{dc}. The inner loop is the current control loop to track I^*_{ref} generated by the voltage control loop [33]. The MRCC is implemented in the inner loop to eliminate the grid current harmonics. The MRCC has been tuned to resonate at the grid frequency for tracking I^*_{ref} perfectly under off-nominal grid frequency. The power converter is operated to achieve the UPF operation under polluted grid conditions.

A. DC-BUS VOLTAGE CONTROLLER

The schematic block diagram of the closed-loop control system of 1-φ GTC is shown in Fig. 2(a). The schematic control diagram is further simplified by considering the current controller gains equal to k_{pr} which is shown in Fig. 2(b). The transient and steady-state performance of the controller is enhanced by determining the appropriate values of the controller gains.

The open-loop transfer function of the unity feedback system shown in Fig. 2(b) is given in (1)

$$G(s) = \frac{k_{pv}k_{pr}s + k_{iv}k_{pr}}{s^2C} \tag{1}$$

The closed-loop transfer function of the voltage control loop shown in Fig. 2(b) is given in (2)

$$\frac{V_{dc}}{V^*_{dc}} = \frac{k_{pv}k_{pr}s + k_{iv}k_{pr}}{Cs^2 + k_{pv}k_{pr}s + k_{iv}k_{pr}} \tag{2}$$

The characteristic equation of the voltage control loop system is given in (3).

$$s^2 + \left(\frac{k_{pv}k_{pr}}{C}\right)s + \frac{k_{iv}k_{pr}}{C} = 0 \tag{3}$$

The roots of the characteristic equation given in (3) lie to the left half of the s-plane for k_{pv}, k_{iv}, and $k_{pr} > 0$. The power flow equation at the grid side is given in (4).

$$p_{ac}(t) = v_g(t) \times i_g(t) \tag{4}$$

The instantaneous values of the grid voltage and current are given in (5).

$$\begin{aligned} v_g(t) &= V_m sin(\omega t) \\ i_g(t) &= I_m sin(\omega t - \phi) \end{aligned} \tag{5}$$

where ϕ is the phase difference between $v_g(t)$ and $i_g(t)$. Substituting the value of $v_g(t)$ and $i_g(t)$ in equation (4) yields equation (6).

$$p_{ac}(t) = \frac{V_m I_m}{2}cos\phi - \frac{V_m I_m}{2}cos(2\omega t - \phi) \tag{6}$$

The ripple power in the dc-bus capacitor is given by (7)

$$p_c(t) = v_c(t) \times i_c(t) = \frac{V_m I_m}{2} \times cos(2\omega t) \tag{7}$$

The power flow equation at the load side is given in (8)

$$P_{dc} = V_{dc} \times I_{dc} \tag{8}$$

The losses occurred in the power electronics switches, dc-link capacitor, and grid inductor are not considered. The power balance equation is given in (9).

$$V_{dc} \times I_{dc} = \frac{V_m \times I_m}{2} \tag{9}$$

The current controller gain (k_{pr}) is determined using (9) and it is given by

$$\frac{I_{dc}}{I_m} = \frac{V_m}{2 \times V_{dc}} = k_{pr} \tag{10}$$

The characteristic equation of the second-order system given in (11) is compared to (3) to obtain the controller gains.

$$s^2 + 2\xi\omega_n s + \omega_n^2 = 0 \tag{11}$$

where ω_n and ζ are the natural frequency in rad/s and damping ratio respectively of the voltage control loop.

The controller gains are given in (12).

$$k_{pv} = \frac{2\xi\omega_n C}{k_{pr}} \text{ and } k_{iv} = \frac{C\omega_n^2}{k_{pr}} \tag{12}$$

where $\omega_n = 2\pi f_{bw}$; rad/s and f_{bw} is the bandwidth of the dc-bus voltage control loop in Hz.

The f_{bw} controls the dc-bus voltage fluctuation under the sudden change of load. Therefore, an appropriate value of f_{bw} is essential to control the dc-bus voltage fluctuation. A suitable value of damping ratio is required to evaluate the transient response of the system. The $\zeta > 1$ makes the system over-damped and has a poor dynamic response. The $\zeta = 0$ makes the system oscillatory. Hence, $\zeta = 0.707$ is preferred because the peak overshoot of the response is reduced. The PI controller gains of the dc-bus voltage control loop for different values of f_{bw} are mentioned in Table 1. The root locus plot of the voltage control loop is shown in Fig. 3(a). The root locus plot reveals that with an increase in the value of f_{bw}, the root locus is moving away from the imaginary axis. In Fig. 3(a), g1, g2, g3, g4, and g5 represent the root locus plot of the voltage control loop and their corresponding bandwidths are 5 Hz, 10 Hz, 15 Hz, 20 Hz, and 25 Hz respectively. The Bode plot of the open-loop transfer function of the unity feedback system represented by (1) is shown in Fig. 3(b). This figure reveals that the system is stable.

TABLE 1. pi controller parameters of the voltage control loop for different bandwidth.

f_{bw} (Hz)	k_{pv}	k_{iv}	k_{pr} (V/V)
5- g1	0.5847	13.1203	
10-g2	1.1694	52.481	
15-g3	1.7541	118.0823	0.3536
20-g4	2.3387	209.922	
25-g5	2.9234	328.0042	

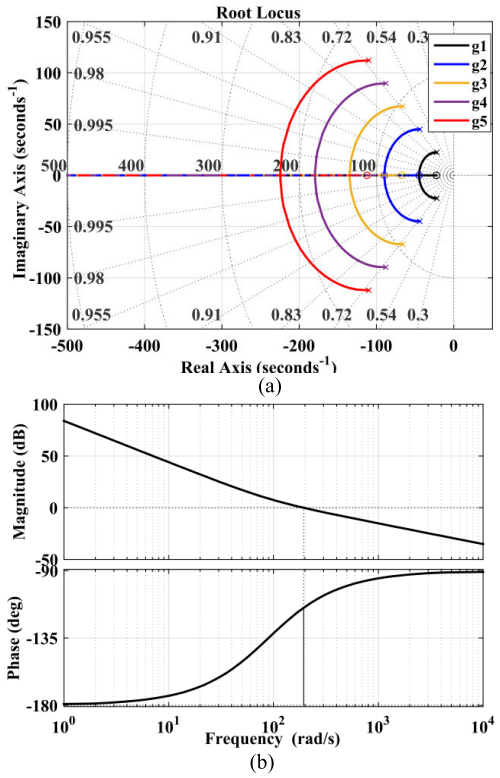

FIGURE 3. Voltage control loop. (a) Root locus plot for different values of f_{bw}. (b) Bode plot of the voltage control loop.

B. MULTI-RESONANT CURRENT CONTROLLER

The proportional + resonant (PR) controllers are stationary frame controllers and such controllers are very popular in 1-φ GTCs. However, the implementations of synchronous frame controllers are quite difficult because it involves the transformation of stationary-frame ac quantities to rotating-frame dc quantities and again back to stationary-frame to fire the power electronics switches after the completion of the controller action [34], [35]. The controller adaptability with f_g is difficult to achieve with PI and hysteresis controller. This causes the failures of these controllers to achieve the UPF operation under f_g drift. An adaptive resonant regulator is proposed in [36] and the performance of the control technique is tested under the nominal and off-nominal grid frequencies. However, the dc-offset rejection capability of the SOGI-FLL has not been considered in [36]. The PR controller can be made adaptive with f_g drift. This is possible by considering the resonating frequency (ω_o) of the PR controller same as

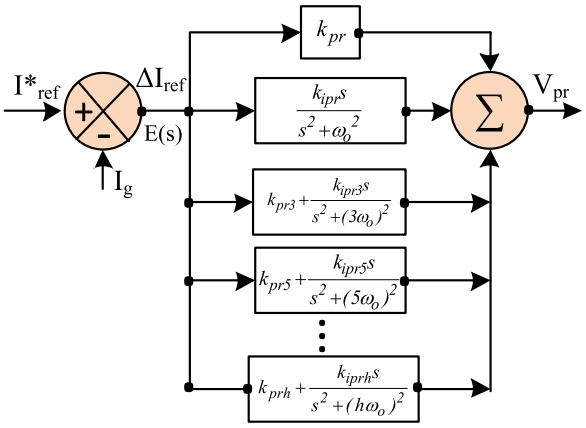

FIGURE 4. The block diagram of the MRCC.

the frequency estimated by a 1-φ PLL. The adaptive PR controller is capable to operate the GTC at UPF operation under f_g drift. The block diagram of the MRCC is shown in Fig. 4. There are a few distinct advantages of the MRCC over other linear controllers that are listed below.

1) The MRCC controller has a very high gain at the resonating frequency (ω_o) equal to f_g. Therefore, the tracking of $I*_{ref}$ is fast with zero steady-state error even under f_g drift.
2) The PR controller can be used as a filter to eliminate 3rd, 5th, …, 15th harmonic components from the grid current under the polluted grid conditions [36]–[38].
3) The proper selection of the proportional gains (k_{pr} and k_{prh}) and integral gains (k_{iprh}) determine the system gain and phase margin and also controller tracks I^*_{ref} with small steady-state error.

The transfer function of the MRCC for harmonic compensation is given in (13)

$$G_{prh}(s) = \sum_{h=3,5,7}^{n} \left(k_{prh} + \frac{k_{iprh} s}{s^2 + (h\omega_o)^2} \right) \tag{13}$$

The method to determine the resonant controller gains is discussed in [35], [39] and given in (14).

$$k_{prh} = L_{g\times} f_o \times h \text{ and } k_{iprh} = \frac{L_g (\omega_o h)^2}{\pi} \tag{14}$$

where $\omega_o = 2\pi f_o$; rad/s is the resonating frequency and $h = 3, 5, 7, \ldots$,n represents the harmonic components. The k_{pr} is given by (10). The k_{ipr} is obtained using (14) for $h = 1$.

The transfer function of the fundamental component and 3rd, 5th, and 7th harmonic components are given in (15).

$$G_1(s) = \frac{0.5s^2 + 314.2s + 4.935 \times 10^4}{s^2 + 9.87 \times 10^4}$$
$$G_3(s) = \frac{1.5s^2 + 2827s + 1.332 \times 10^6}{s^2 + 8.883 \times 10^5}$$
$$G_5(s) = \frac{2.5s^2 + 7854s + 6.169 \times 10^6}{s^2 + 2.467 \times 10^6}$$

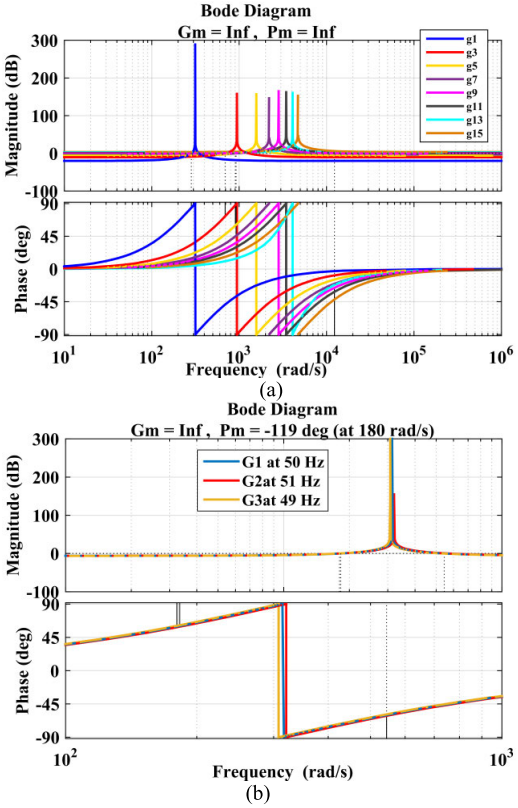

FIGURE 5. (a) Bode plot of MRCC for selective harmonic compensation of the I_g. (b) Bode plot of the current controller when the f_g drifts by 50±1 Hz.

$$G_7(s) = \frac{3.5s^2 + 1.539 \times 10^4 s + 1.693 \times 10^7}{s^2 + 4.836 \times 10^6} \tag{15}$$

The stability of the MRCC is presented through the Bode plot analysis that is presented in Fig. 5(a). The Bode plot shows that the MRCC has a very high gain at the resonating frequency equal to f_g. In Fig. 5(a), G_1, G_3, G_5, G_7, G_9, G_{11}, G_{13}, and G_{15} represent the Bode plot of the fundamental, 3rd, 5th, 7th, …, 15th harmonic components respectively. The fluctuation of the grid fundamental frequency by 50±1 Hz shifts the gain and phase margin of the controller that is shown in Fig. 5(b). The current controller fails to track I^*_{ref} under f_g drift and as a result, a small phase-shift is introduced between the grid voltage and current. However, this problem is overcome by considering the resonating frequency equal to the frequency estimated by the 1-φ MSOGI-PLL.

The error signal $E(s)$ is the input to the MRCC. The error signal given in (16) is determined by considering only the fundamental frequency of the grid voltage.

$$E(s) = \left(k_{pr} + \frac{k_{ipr}s}{s^2 + \omega_o^2}\right) V_{ref}(s) \tag{16}$$

where $V_{ref}(s)$ is the output of the PR controller. In time-domain, $v_{ref}(t)$ is given in (17).

$$v_{ref}(t) = V_{pr}\sin(\omega t) \tag{17}$$

Substituting the value of $V_{ref}(s)$ in (16) yields (18)

$$E(s) = \frac{k_{pr}s^2 + k_{ipr}s + k_{pr}\omega_o^2}{s^2 + \omega_o^2} \times \frac{V_{pr}\omega}{s^2 + \omega^2} \tag{18}$$

where ω is the grid frequency. The error is zero when $\omega = \omega_o$. Substituting $E(s)$ equals zero in (18) yields (19).

$$k_{pr}s^2 + k_{ipr}s + k_{pr}\omega_o^2 = 0 \tag{19}$$

The solution of (19) gives roots of $E(s)$ given in (20).

$$s_{1,2} = \frac{-k_{ipr}}{2k_{pr}} \pm j\sqrt{1 - \left(\frac{k_{ipr}}{2k_{pr}}\right)^2} \tag{20}$$

The roots of $E(s)$ give the location of zeros. The zeros are complex conjugate and lie to the left half of the s-plane. This also reveals that the current controller is stable under zero error conditions.

III. MODIFIED SOGI-PLL

The synchronization of power electronics converters with the grid is achieved through the PLL. The grid voltage θ_g and f_g estimation are achieved through the PLL. The transport-delay PLL (TD-PLL) is the most conventional approach to obtain the fictitious quadrature signal [16]. However, this method fails to extract θ_g and f_g accurately under the grid voltage disturbances. The quadrature signals are no longer 90^0 phase-shifted under the occurrence of grid frequency drift. The schematic block diagram of 1-φ MSOGI-PLL is shown in Fig. 6.

The MSOGI-PLL has immunity against f_g fluctuation and polluted grid conditions. A low-pass filter (LPF) is provided to eliminate the dc-offset from the V_g. The MSOGI-PLL is made frequency adaptive by subtracting the phase-offset error resulting from the grid frequency fluctuation from the estimated phase-angle and also multiplying the V_β-component with a magnitude factor (m_β) equals to (ω_g/ω_{fn}). The transfer functions of the orthogonal signals are given in (21) and (22) respectively.

$$G_\alpha(s) = \frac{V_\alpha(s)}{V_g(s)} = \frac{k\omega_{fn}s}{s^2 + k\omega_{fn}s + \omega_{fn}^2} \tag{21}$$

$$G'_\beta(s) = \frac{V'_\beta(s)}{V_g(s)} = \frac{k\omega_{fn}^2}{s^2 + k\omega_{fn}s + \omega_{fn}^2} \tag{22}$$

where ω_{fn} is the nominal fundamental frequency of the grid in rad/s, and k is the damping factor.

The Bode plot of $G_\alpha(s)$ and $G'_\beta(s)$ for $k = 1$ is shown in Fig. 7(a). The signals $V_\alpha(s)$ and $V'_\beta(s)$ are 90^0 phase-shifted and have the same magnitude at 50 Hz. The Bode plot analysis of $G_\alpha(s)$ and $G'_\beta(s)$ for different values of k are shown in Fig. 7(b) and (c) respectively.

The variation of k doesn't affect the steady-state performance of the PLL. However, the impact of k can be observed on the transient performance of the PLL. It can be seen from Fig. 7(b) and 7(c) that f_{bw} of $V_\alpha(s)$ and $V'_\beta(s)$ increases with an increase in the value of k. However, the filtering capability of

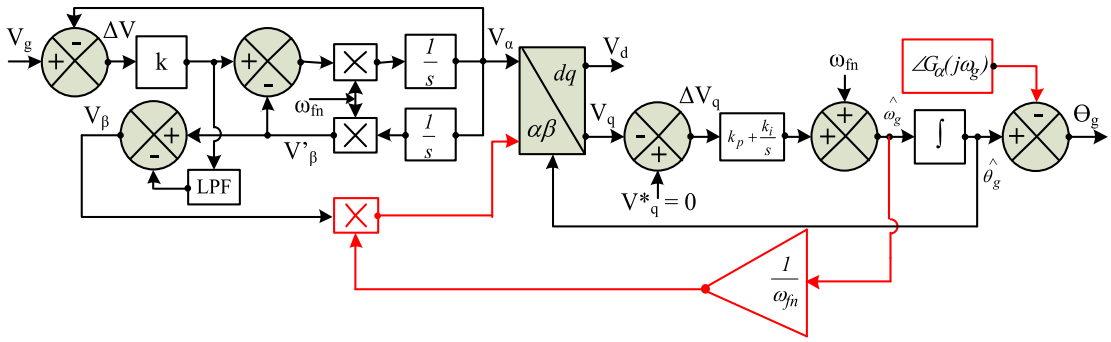

FIGURE 6. Schematic block diagram of 1-φ MSOGI-PLL.

the orthogonal signals decreases. Therefore, the appropriate value of k must be selected to obtain the optimum bandwidth and filtering effect.

A. DC-OFFSET REJECTION

The dc-offset gets injected in the PLL input because of the transformer's non-linearity, voltage sensors, and A/D conversion. The dc-offset at the PLL input generates oscillation in f_g and θ_g. The oscillation in the phase-angle generates the distorted reference current (I^*_{ref}) that affects the current controller performance of 1-φ GTCs and may also inject the dc-offset to the utility grid through the PV-fed GTCs. A low-pass filter (LPF) has been used to reject the dc-offset from the V_g in [40], [41]. An all-pass filter and type-3 filter have been used to eliminate the dc-offset in [42], [43]. However, the methods adopted in [40]–[42] fail under the grid frequency drift and the accurate extraction of f_g and θ_g is not possible. The MSOGI-PLL is implemented to serve the following tasks.

1) An LPF is used to remove the dc-offset from the PLL input as shown in Fig. 6. The lower-order harmonics are suppressed by the optimum selection of the damping factor (k).
2) The MSOGI-PLL accurately estimates the f_g and θ_g of the grid voltage under the grid frequency fluctuation. This is achieved by making the PLL adaptive to the grid frequency. A phase-offset error is generated due to the grid frequency fluctuation. The phase-offset error is subtracted from the estimated phase-angle to estimate the accurate grid phase-angle as shown in Fig. 6.
3) The magnitude of V_β changes due to the fluctuation in f_g. Therefore, V_β is multiplied by a magnitude factor (m_β) to suppress the change in the magnitude.

The transfer function of $G_\beta(s)$ having the dc-offset rejection capability is obtained using the block diagram reduction technique that is shown in Fig. 8(a) and 8(b).

The transfer function of the first-order LPF is given in (23).

$$T.F_{LPF} = \frac{1}{1 + sR_fC_f} \tag{23}$$

where $R_fC_f = \tau$ is the time constant in ms.

The transfer function of $G_\beta(s)$ given in (24) is obtained by substituting the value of $V'_\beta(s)$ from (22) and reducing the transfer function block of Fig. 8(b).

$$G_\beta(s) = \frac{V_\beta(s)}{V_g(s)} = \frac{-ks^2 + k\tau\omega_{fn}^2 s}{\tau s^3 + (1 + k\tau\omega_{fn})s^2 + (k\omega_{fn} + \tau\omega_{fn}^2)s + \omega_{fn}^2} \tag{24}$$

The Bode plot of $G_\beta(s)$ for different values of k is shown in Fig. 9. The $G_\beta(s)$ has band-pass filter (BPF) characteristics. The bandwidth of $G_\beta(s)$ increases with an increase in the value of k.

B. GRID-FREQUENCY ADAPTATION

The current controller fails to track I^*_{ref} generated by the dc-bus voltage controller perfectly under f_g drift. This generates a phase-shift between the V_g and I_g. The V_α and V_β are neither in-phase nor quadrature-phase with V_g because of the f_g fluctuation. This generates a phase-offset error in the output of the PLL. Therefore, it becomes necessary to make the PLL adaptive with f_g fluctuation. This is achieved by subtracting a phase-angle equivalent to the phase-offset error from the phase-angle estimated by the PLL as shown in Fig. 6. The calculation of the phase-offset error is mentioned below. At $s = j\hat{\omega}_g$

$$G_\alpha(j\hat{\omega}_g) = \frac{V_\alpha(j\omega_g)}{V_g(j\omega_g)} = \frac{j(k\omega_{fn}\hat{\omega}_g)}{\left(\omega_{fn}^2 - \hat{\omega}_g^2\right) + j\left(k\omega_{fn}\hat{\omega}_g\right)} \tag{25}$$

where $\hat{\omega}_g$ is the estimated grid frequency in rad/s. The magnitude of the $G_\alpha(j\omega_g)$ and $G'_\beta(j\omega_g)$ are given in (26) and (27) respectively.

$$\left|G_\alpha(j\hat{\omega}_g)\right| = \frac{k\omega_{fn}\hat{\omega}_g}{\sqrt{\left(\omega_{fn}^2 - \hat{\omega}_g^2\right)^2 + \left(k\omega_{fn}\hat{\omega}_g\right)^2}} \tag{26}$$

$$\left|G'_\beta(j\hat{\omega}_g)\right| = \frac{k\omega_{fn}^2}{\sqrt{\left(\omega_{fn}^2 - \hat{\omega}_g^2\right)^2 + \left(k\omega_{fn}\hat{\omega}_g\right)^2}} \tag{27}$$

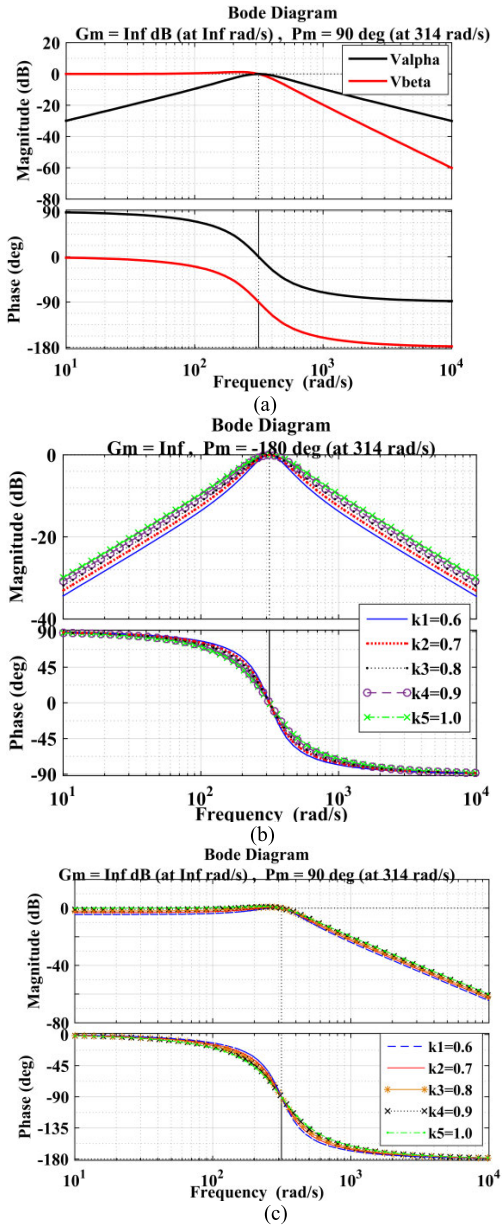

FIGURE 7. Bode plot analysis of the orthogonal signals for different values of k. $G_\alpha(s)$ and $G'_\beta(s)$ for $k = 1$. (b) $G_\alpha(s)$. (c) $G'_\beta(s)$.

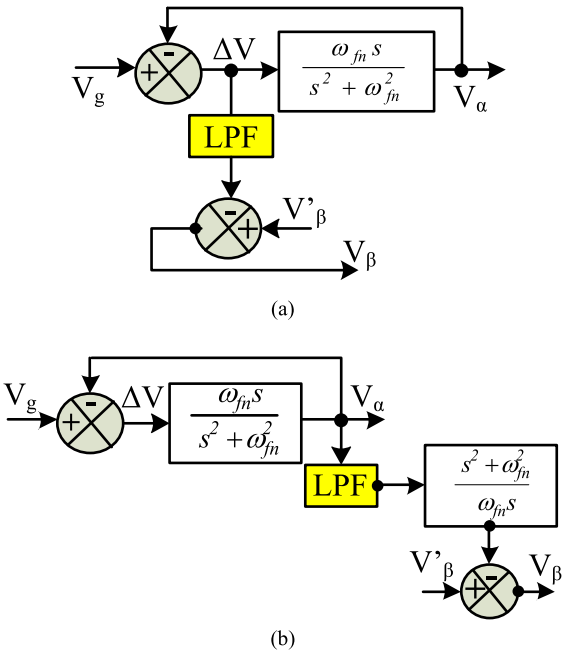

FIGURE 8. (a) Reduction of the outer feedback loop of the quadrature signal generation (QSG) block. (b) Shifting of take-off point to the right.

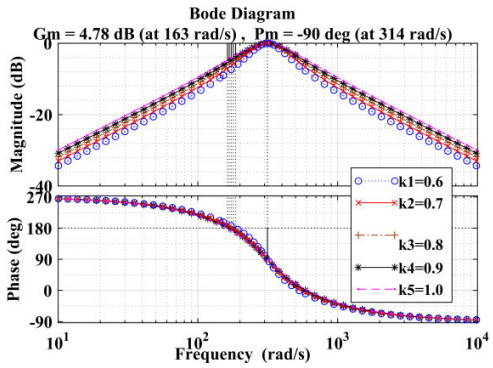

FIGURE 9. Bode plot analysis of $G_\beta(s)$ for different values of k.

The phase-offset error is obtained from the phase-angle of (25) and it is given in (28).

$$\angle G_\alpha(j\omega_g) = \frac{\pi}{2} - \tan^{-1}\left(\frac{k\omega_{fn}\hat{\omega}_g}{\omega_{fn}^2 - \hat{\omega}_g^2}\right) \tag{28}$$

In the presence of a small drift in f_g, the phase-offset error can be approximated in (29).

$$\angle G_\alpha(j\omega_g) = \frac{\omega_{fn}^2 - \hat{\omega}_g^2}{k\omega_{fn}\hat{\omega}_g} \tag{29}$$

where $(\omega_{fn} - \hat{\omega}_g)$ represents the drift in the angular grid frequency from the fundamental frequency in rad/s.

It is observed from (26) and (27) that the fluctuation in f_g changes the magnitude of the V_α and V'_β. The change in magnitude of the quadrature signal generates double frequency oscillation in the estimated f_g and θ_g. The double frequency oscillation in the PLL output is suppressed by multiplying V_β with a magnitude factor given in (30).

$$m_\beta = \frac{\hat{\omega}_g}{\omega_{fn}} \tag{30}$$

The magnitude factor (m_β) makes the V_β adaptive with the grid frequency. The magnitude of $G_\beta(j\omega_g)$ is given in (31).

$$|G_\beta(j\hat{\omega}_g)| = \frac{\sqrt{m_\beta^4 + \hat{\omega}_g^2\tau^2}}{\sqrt{\left(1 - m_\beta^2 - \tau m_\beta\hat{\omega}_g\right)^2 + \left(\begin{matrix} m_\beta + \tau\hat{\omega}_g - \\ m_\beta^2\hat{\omega}_g\tau \end{matrix}\right)^2}} \tag{31}$$

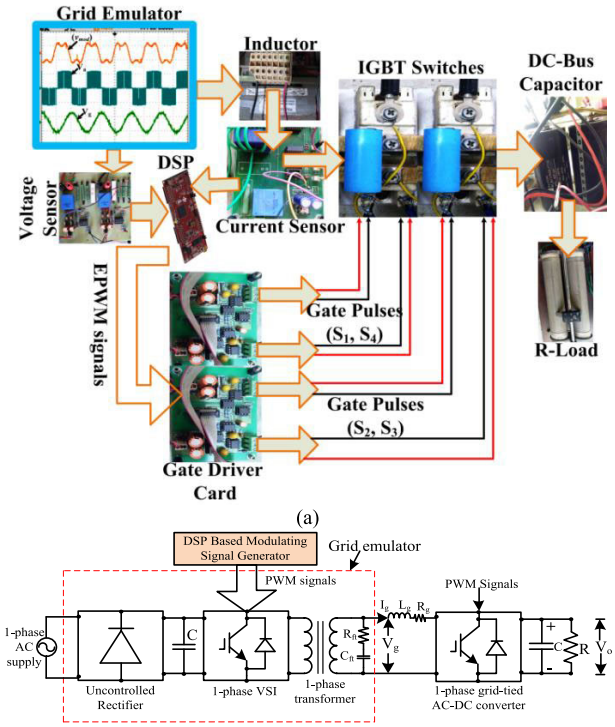

FIGURE 10. (a) Prototype model of 1-φ grid-tied AC-DC converter. (b) Schematic block diagram of 1-φ grid emulator.

TABLE 2. experimental parameters of the prototype model.

Parameters	Symbol	Value
Grid voltage	V_g	40 V, 50 Hz
Reference dc-bus voltage	V^*_{dc}	80 V
Grid inductance	L_g	10 mH
DC-bus capacitor	C	4700 µF
Load	Resistive	90Ω, 2A
Switching frequency	f_{sw}	4 kHz

IV. EXPERIMENTAL RESULTS AND DISCUSSION

A prototype model of a 1-φ GTC is developed in the laboratory as shown in Fig. 10(a). The emulator schematic diagram is shown in Fig. 10(b). The grid emulator is designed and fabricated in the laboratory. The grid emulator is comprised of a 1-φ voltage source inverter (VSI) fed 1-φ transformer.

The output voltage of the VSI fed transformer is polluted by injecting harmonics + dc-offset into the modulating signal used to fire the VSI switches. The harmonic components (3^{rd}+ 5^{th}harmonics) + dc-offset are injected into the fundamental component of the modulating signal to generate the resultant modulating signal (V_{mod}) through the DSP. The required modification in the V_{mod} is updated and implemented through the DSP algorithm. The modulating signal with harmonics and dc-offset is given in (32).

$$V_{\text{mod}} = m_a \times [\sin(\omega t) + 0.05 \times \sin(3\omega t) + 0.03 \times \sin(5\omega t)] + 0.05 \times V_{dc-offset} \quad (32)$$

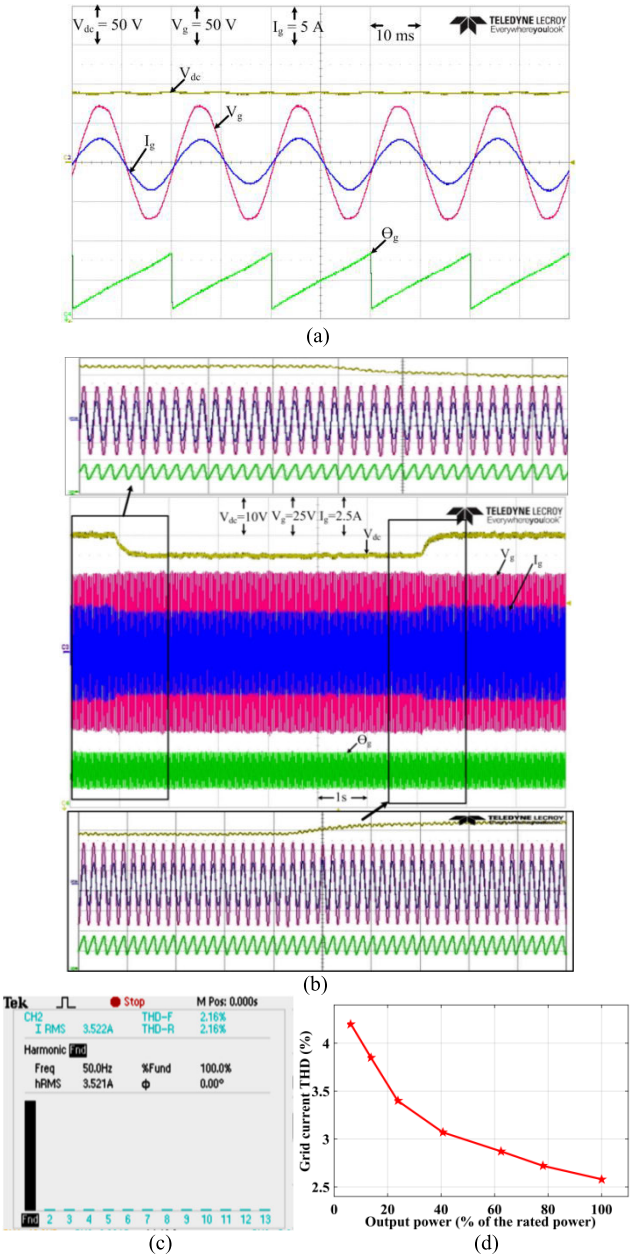

FIGURE 11. Performance of MRCC under ideal grid condition. (a) V_g, I_g, V_{dc}, and θ_g. (b) Step-decrease and increase of V_{dc}. (c) FFT of I_g. (d) Grid current THD vs output power (rated power: 200W).

where ω=$2\pi f$ is the angular frequency in rad/s, and f is the grid fundamental frequency i.e. 50 Hz. The amplitude modulation index (m_a) is given in (33).

$$m_a = \frac{\hat{V}_{\text{mod}}}{\hat{v}_{tri}} \quad (33)$$

where $\hat{V}_{\text{mod}}$ is the peak value of the modulating signal and $\hat{V}_{tri}$ is the peak value of the carrier signal.

The f_g drift is obtained by varying the fundamental frequency (f) of the modulating signal (V_{mod}). The V_{mod} is generated using the DSP by executing (32).

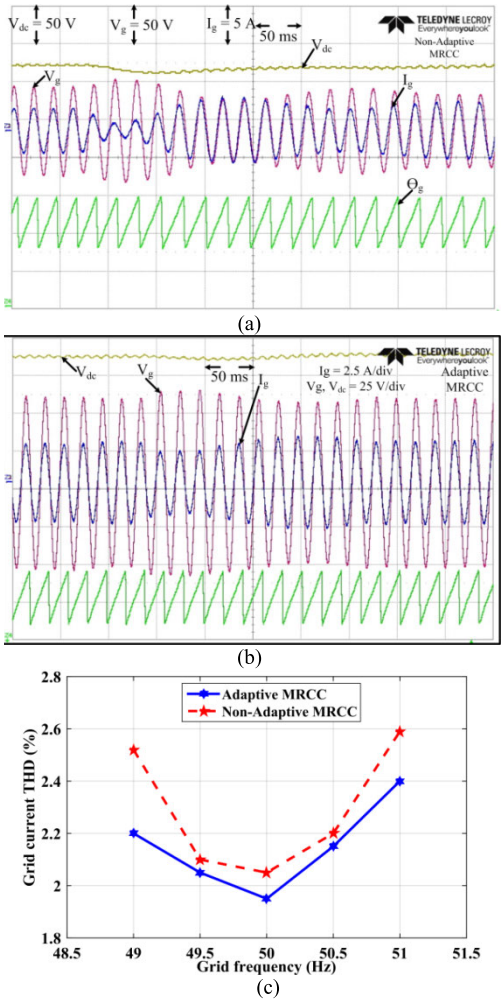

FIGURE 12. Step-change of f_g from 50 Hz-49 Hz. (a) Non-adaptive MRCC. (b) Adaptive MRCC. (c) Grid current THD vs fluctuation in the f_g.

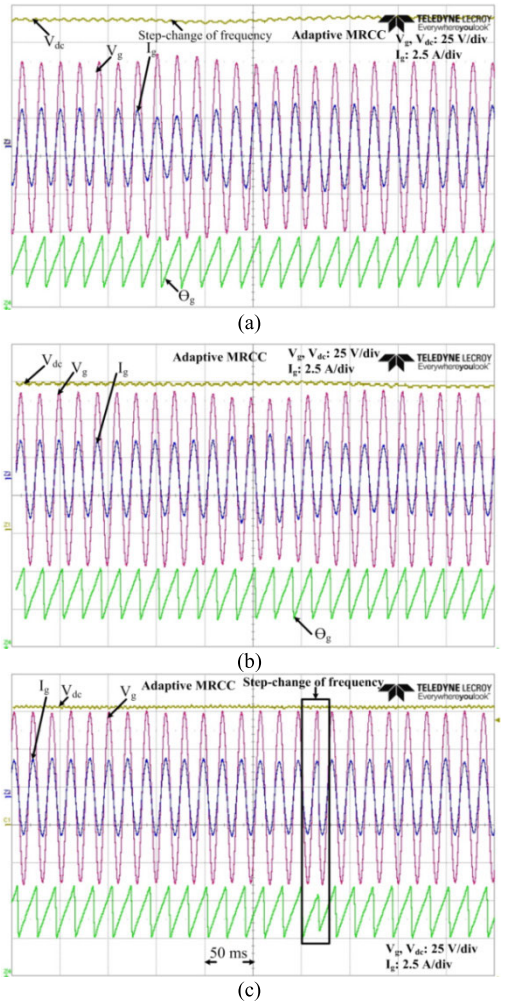

FIGURE 13. The V_g is contaminated with a 5% dc-offset. (a) Step-change of the f_g from 50 Hz - 49 Hz. (b) Step-change of the f_g from 50 Hz - 51 Hz. (c) Step-change of the f_g from 51 Hz - 50 Hz.

The experimental parameters are provided in Table 2. The GTC is operated under the ideal, as well as polluted grid conditions. The proposed control technique is implemented on the TMS320F28379D Delfino Launchpad. The sampling frequency of the voltage and current control loop is 5 kHz and 20 kHz respectively. The bilinear transformation is used to transform the s-domain function into the z-domain.

A. PERFORMANCE OF THE MRCC UNDER IDEAL GRID CONDITION

The experimental results of the ideal grid condition are shown in Fig. 11. The UPF operation at the grid side is shown in Fig. 11(a). The step-change of the dc-bus voltage is shown in Fig. 11(b). In Fig. 11(b), it has been shown that the UPF operation is maintained under the step-change of the dc-bus voltage. The FFT of I_g is shown in Fig. 11(c). The THD of I_g is 2.16% under ideal grid conditions. The grid current THD is plotted against the % of the output power of the converter for 50 Hz operation which is shown in Fig. 11(d).

B. PERFORMANCE OF ADAPTIVE MRCC UNDER NON-IDEAL GRID CONDITION

1) OFF-NOMINAL GRID FREQUENCY

The performance of the non-adaptive and adaptive MRCC under non-ideal grid conditions is shown in Fig. 12. The grid frequency is step-changed from 50 Hz – 49 Hz. In Fig. 12(a), it is shown that V_g and I_g are phase-shifted with the reduction in f_g and non-adaptive MRCC fails to maintain the UPF operation at the grid side. However, the adaptive MRCC follows the fluctuation in the grid frequency and UPF operation is maintained that is shown in Fig. 12(b). The THD of I_g is plotted against f_g fluctuation in Fig. 12(c). In Fig. 12(c), it is observed that an adaptive MRCC has improved performance under off-nominal grid frequency and has reduced grid current THD as compared to the non-adaptive MRCC. The MRCC is effectively reducing the current harmonics and also satisfying the IEEE standard 1547 [31].

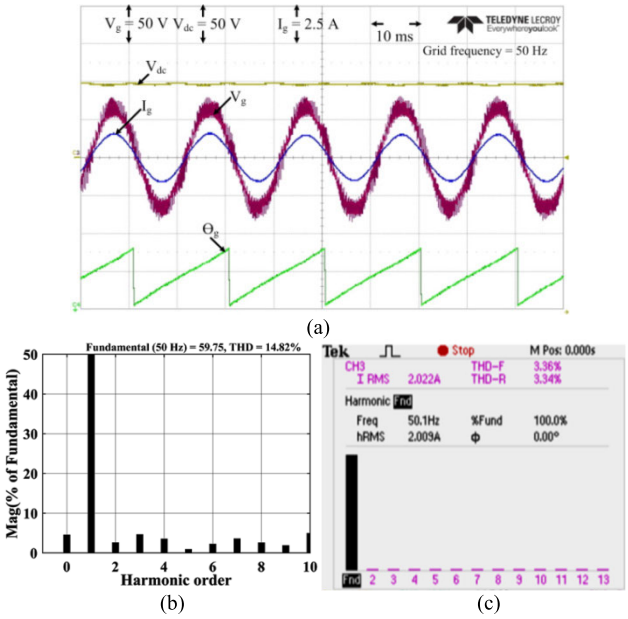

FIGURE 14. (a) V_g is contaminated with 3rd harmonic (5%) and dc-offset (5%). (b) FFT of V_g. (c) FFT of I_g.

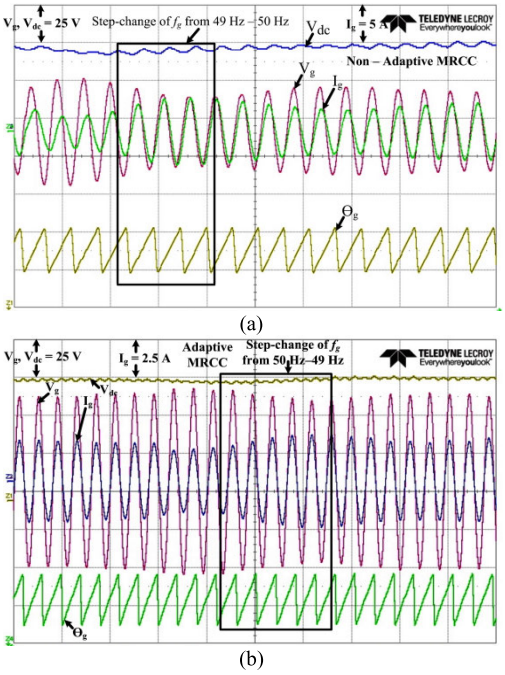

FIGURE 15. Step-change of the f_g from 50 Hz – 49 Hz. (a) Non-adaptive MRCC. (b) Adaptive MRCC.

2) DC-OFFSET UNDER GRID FREQUENCY FLUCTUATION

The V_g is contaminated by adding 5% dc-offset. The f_g is varied from 50 Hz – 49 Hz, 50 Hz – 51 Hz, and 51 Hz – 50 Hz. The effect of step-change of f_g on the V_{dc}, V_g, I_g, and θ_g is shown in Fig. 13. The adaptive MRCC is tracking the I^*_{ref} perfectly and UPF operation is maintained in the presence of dc-offset and fluctuation in the f_g.

3) THIRD-HARMONIC + DC-OFFSET UNDER GRID FREQUENCY FLUCTUATION

The V_g is contaminated with 3rd harmonic (5%) + dc-offset (5%). The MSOGI-PLL is accurately extracting f_g and θ_g from V_g in the presence of 3rd harmonic and dc-offset under the f_g fluctuation. The V_g, I_g, V_{dc}, and θ_g under polluted grid conditions at f_g equal to 50 Hz are shown in Fig. 14(a). The FFT of V_g and I_g under polluted grid conditions are shown in Fig. 14(b) and (c) respectively. The THD of V_g and I_g is 14.82% and 3.36% respectively.

The step-change of f_g from 50 Hz – 49 Hz under the polluted grid condition for non-adaptive and adaptive MRCC is presented in Fig. 15. The V_g is contaminated with 3rd harmonic (5%) and dc-offset (5%). In Fig. 15(a), it has been shown that the non-adaptive MRCC fails to track I^*_{ref} under the grid frequency fluctuation. As a result, the V_g and I_g are not in the same phase. However, the adaptive MRCC is perfectly tracking the I^*_{ref} under the f_g fluctuation as shown in Fig. 15(b).

The step-change of f_g from 50 Hz – 51 Hz under the polluted grid condition for non-adaptive and adaptive MRCC is shown in Fig. 16. The UPF operation is not maintained at the grid side under f_g fluctuation by implementing the non-adaptive MRCC that is shown in Fig. 16(a). However,

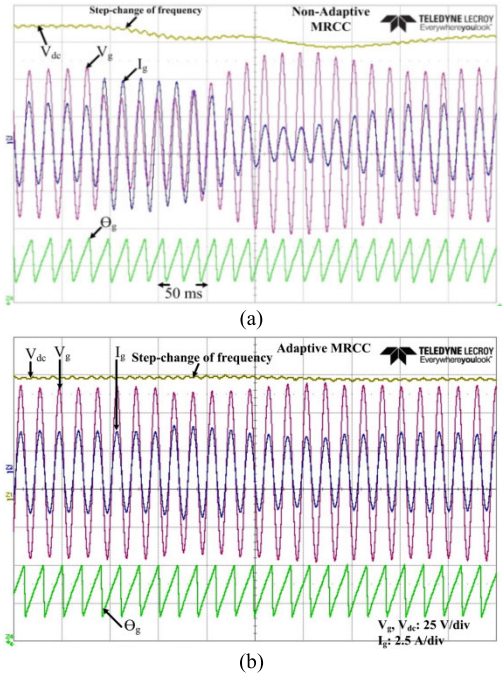

FIGURE 16. Step-change of the f_g from 50 Hz – 51 Hz. (a) Non-adaptive MRCC. (b) Adaptive MRCC.

the UPF operation is maintained at the grid side under the step-change of f_g by implementing the adaptive MRCC which is shown in Fig. 16(b).

4) 3rd+5th HARMONICS + DC OFFSET AT 50 HZ

The V_g is contaminated with 3rd (5%) + 5th (3%) harmonics and dc-offset (5%) at 50 Hz. The V_g, I_g, V_{dc}, and θ_g are shown

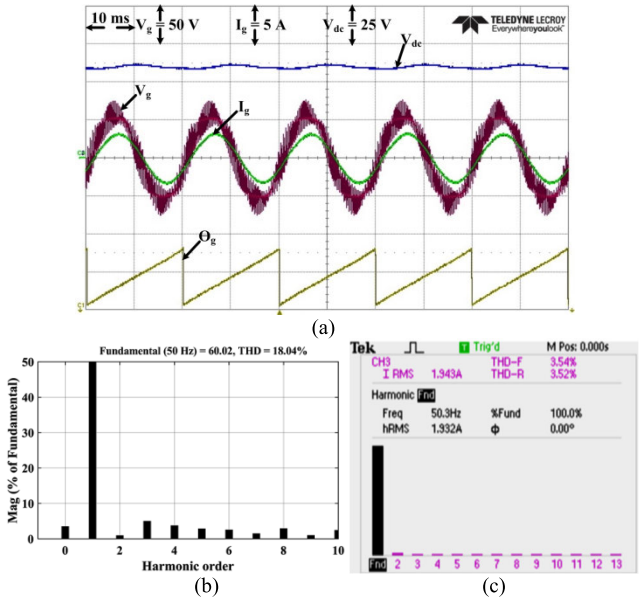

FIGURE 17. (a) V_g, I_g, V_{dc}, and θ_g. (b) FFT of V_g. (c) FFT of I_g.

TABLE 3. Comparative performance analysis of adaptive controllers.

Performance parameters	[10]	[24]	[25]	[28]	[29]	Proposed work
DC-bus voltage control	√	X	X	X	X	√
Grid current harmonic	4.3%	2.4%	Not specified	1.4 %	3.7%	2.16%
Frequency adaptive	X	(50± 0.5) Hz	(50±1) Hz, (50±3) Hz	(50± 1) Hz	(60± 1) Hz	(50±1) Hz
DC-offset + step-change frequency	X	X	X	X	X	DC-offset (5%) and (50±1) Hz
Harmonics + DC-offset + step-change frequency	X	X	X	X	√	3rd (5%) + 5th (3%) + DC-offset (5%)
Voltage sag	X	√	X	X	X	X
Adaptive PI for dc-bus voltage ripple reduction	√	X	X	X	X	X

in Fig. 17(a). The FFT of the V_g and I_g are shown in Fig. 17(b) and 17(c) respectively. The THD of V_g and I_g is 18.04% and 3.54% respectively.

Comparative performance analyses of the different adaptive controllers are mentioned in Table 3. In this table, different performance parameters are considered to analyze the performance of the adaptive controllers reported in the literature along with the proposed work.

V. CONCLUSION

The MSOGI-PLL has the capability to extract the grid voltage θ_g and f_g accurately under polluted grid conditions. The k_{pv} and k_{iv} are determined appropriately to enhance the steady-state and transient performance of the 1-φ GTC. The appropriate selection of the bandwidth of the voltage control loop controls the overshoot and undershoots of the dc-bus voltage. The frequency adaptive MRCC is implemented in the inner loop to eliminate the lower-order harmonics from I_g. This is achieved by properly selecting the bandwidth of the adaptive MRCC. The stability of the MRCC is analyzed through the Bode plot. The high gain of the MRCC ensures better tracking of I^*_{ref}. The MRCC is made frequency adaptive by resonating the controller at the frequency estimated by the MSOGI-PLL. The adaptive MRCC is capable to maintain the UPF operation at the grid side under polluted grid conditions and off-nominal grid frequency. The non-adaptive MRCC fails to maintain the UPF operation under the off-nominal grid frequency. The experimental results are presented to verify the controller performance under the ideal, as well as polluted grid conditions.

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