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Remote Synchronization of the Microgrid to the Utility Grid Without Access to Point of Common Coupling in the Presence of Disturbances

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ABSTRACT The article presents the method of remote micro-grid synchronization with the utility grid in the presence of voltage disturbances. The proposed algorithm and control devices synchronize different power systems on the basis of the instantaneous voltage phase angle in spite of voltage quality problems and without need of access to point of common coupling. In the presence of grid voltage disturbances, instantaneous grid voltage phase angle is estimated and transmitted remotely with a certain accuracy, which is varies in presence of disturbances of grid voltages or depends on the synchronization algorithm and data transmission rate. The paper focuses on the influence of voltage disturbances on the proposed remote synchronization strategy and the shape of the output current of the synchronized power converter on the micro-grid. The four types of grid voltage disturbances are presented: harmonics, one-phase sag, two-phase sag, and phase voltage jump. The final conclusions present the possibility of using the proposed remote synchronizations algorithm in micro-grid power converter applications in the presence of typical utility grid voltage disturbances.

INDEX TERMS Power converter remote synchronization, distributed generation, grid voltage disturbances, Ethernet and 4G data transmission, micro-grids, power system restoration.

I. INTRODUCTION

The concept of a micro-grid (MG) was introduced as a result of the increased demand for environment-friendly renewable sources and the need for energy generation in reliable and secure-based ways [1]. The first association responsible for this task was the consortium for electric reliability technology solutions [2]. In general, such MG is a small-scale power system or part of a utility grid (UG) that is made up of distributed generators such as wind turbines, fuel cells, photovoltaic panels, etc. Additionally, it can include flexible loads and energy storages that operate within clearly defined control strategies. That group of devices can be treated by the UG as controllable generators or loads [3], [4]. They are typically connected to the grid at one point, called the point of common coupling (PCC).

In normal operating conditions, the MG operates in grid-connected mode (in parallel with UG). In this case, the MG draws or supplies power to the UG, depending on the local generation and energy storage capacities or local load demands of the MG. The MG can be also operated in standalone mode (independently in an island mode) [5]– [8].

This possibility of operation is desirable in faults states, which can occur in the UG. The MG can be disconnected from UG and continue power delivery to consumers without long-term interruption. After the UG failure disappeared, there is a necessity to resynchronize MG with UG before reconnection [6]. The physical connection of both systems without synchronization is undesirable because that can lead to the flow of short circuit currents between the UG and MG.

To resolve the problem of MG to UG synchronization many methods were proposed. The most promising and research attractive group of methods is active synchronization which uses an additional control loop for faster and smoother transient states. For example, the solution presented in [9], [10] uses one of the energy sources which is responsible for the synchronization to the UG. All other power units are in droop control mode. Articles [11], [12] proposes an active synchronizing method that adopts the network-based control of multiple distributed generators. This was done with

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the use of the MG central controller. The MG central controller sends data independently to each distributed generator unit to correct the voltage and frequency offset to all controllable distributed generators. For better stability and reliability of the MG at synchronization articles [13]–[16] proposed the use of the droop control curves shifting. The idea is to shift the preset droop curves to change the operating frequency and voltage without changing the active/reactive power-sharing between sources. Article [17] proposes the distributed generators synchronization angle modification with the use of the sine function of the phase angle between both voltages to calculate the new angle value. The method presented in [18] is based on the combined use of different phase-locked loop (PLL) systems, to synchronize the phase angle and frequency of the MG with the UG. By means of the proposed PLLs, the MG central controller calculates the voltage signal, which is directly used by distributed generators. The signal is synchronized with the Global Positioning System (GPS) signal to synchronize zero-crossing voltage. Solutions presented in [19]–[24] use distributed synchronization methods. The solution presented in [25] adds the possibility to synchronize MG to different points of common coupling with the use of distributed synchronization. Unfortunately, the proposed method does not mention the problem of communication and demanded level of data transition rate. Furthermore, the above-mentioned group of active synchronization methods is not able to properly operate in fault states conditions of UG.

The problem of synchronization in presence of grid disturbance is resolved in different ways. Article [26] proposes that the local distribution source is responsible for removing harmonics from the micro-grid. Another solution presented in [27] proposed synchronizing not only to fundamental components but also harmonics, which minimalizes the instantaneous voltage differences. Article [28] presents the synchronization of the ship to shore. That method uses synchronization based on voltage harmonics to achieve smaller transient currents.

The main inconvenient of active synchronization is the necessity of taking measurements and communication directly on the PCC. In conventional active synchronization, voltages are measured from both sides of the three-phase breaker, and then the difference is calculated and sent to the MG controller. As a result, in any connection point, there is a need for a measurement device and dedicated connection. Also, an MG can be synchronized to the UG only if voltages are present on both sides of the three-phase breaker at the PCC. Article [29] presents the solution for such a problem, but the sample rate of phasor measurement unit is low which corresponds to slow synchronization. Also, there is no possibility of maintenance virtual synchronization, as the solution uses a slight frequency difference to calculate the switching moment of three-phase breaker. The remote synchronization strategy presented in [30] argues for the possibility to synchronize an MG with the UG even when measurements at the PCC are impractical or there is no connection with that point. Thus the dependence on measurements and even a connection with the PCC is removed. This adds desired flexibility and reliability to microgrids.

Article [30] which was published by the authors presents active remote synchronization method in the ideal situation when there are no disturbances on the MG or the UG side. Additionally, this article doesn't mention the problem of public communication media data transfer utilization. However, to represent a realistic scenario, it was necessary to carry out the research of the remote synchronization algorithm during the disturbance states and optimized conditions of data transfer rate. This paper investigates the use of the lastly proposed [30] remote synchronization method without access to PCC strategy in the situation of the presence of typical voltage disturbances. Furthermore, the researchers proposed introducing an improved solution based on data transfer optimization and a commonly known method of synchronization to provide the positive symmetrical voltage components which is SOGI-PLL (Second Order Generalized Filter) [31]. Proposed combination act as a low pass filter which is tuned for balance for fast response of UG transient states and immunity for harmonics disturbances. The main aim of this paper is to investigate the advanced synchronization algorithm such as SOGI-PLL, which will operate with the proposed remote synchronization strategy without accessible PCC. The proposed solution increases knowledge about active synchronization and also extends the capabilities of synchronization removing the necessity of access to PCC. Additionally, the proposed method allows for maintaining virtual synchronization even in presence of disturbances in UG based on rejection capabilities of signal disturbances.

In section II of this article, there is an extended analysis of the used synchronization strategy which is presented by authors before in [30]. The next section talks about the identification of instantaneous voltage parameters computation. Section IV presents an experimental test stand used to investigate the influence of disturbances on the synchronization method. The next part presents tests the influence of sending data rate on received the grid angle (theta). Section VI presents experimental research results for different disturbances. The final chapter offers conclusions based on performed laboratory tests.

II. BACKGROUND OF THE REMOTE SYNCHRONIZATION METHOD

Previously proposed by the authors in [30] remote synchronization utilized two devices: on the UG side there is a need for a synchronization data sender (SDS) and on the MG side a synchronization data controller (SDC). A diagram for the proposed solution is presented in fig. 1.

The SDS device measures voltage on the UG side. Next, with the use of the synchronization algorithm, it estimates voltage magnitude, frequency, and instantaneous phase angle. Synchronization algorithm on SDS device operates with 10 kHz frequency. Data packets are sent to the SDC device on the MG side with a 1 kHz frequency via Ethernet. As delays are crucial for the performance of the remote synchronization

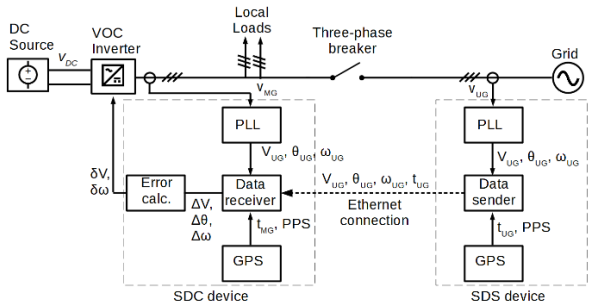
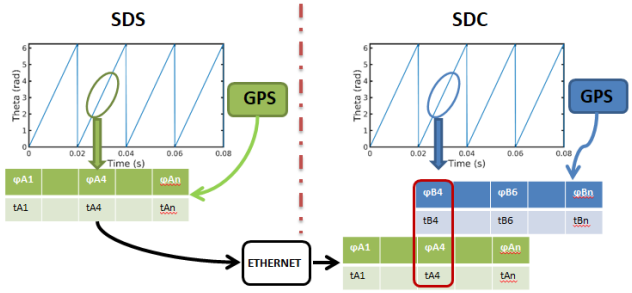


FIGURE 1. Diagram of an MG used in the presented solution. VOC – voltage oriented control inverter, SRF PLL – synchronous reference frame PLL, SDC – proposed synchronization data controller, SDS – proposed synchronization data sender.

method, User Datagram Protocol is used. The use of such protocol has the disadvantage of possible packet loss and reorder if Ethernet transmission disturbances occur. The reordering problem is resolved by discarding older packets, while packet loss causes slower performance of the solution fig. 2. The current implementation of the algorithm has constant coefficients, which causes that operate stable until maximum designed communication delays, but there is active research for dynamic coefficient use in situations when average delay changes. The transferred data consists of the magnitude of voltage, frequency, instantaneous phase angle, and current GPS timestamp. On the MG side, a receiving device collects samples of data and calculates the error signal. This solution provides a possibility to synchronize an MG with the UG even if there is a main three-phase breaker open between the MG and the UG.



$\Delta t < 10ms$	$\Delta t = tA1 - tB1$	$\Delta\varphi = \varphi A1 - \varphi B1$	$\delta\omega$
OK	5ms	+0.02	↓
OK	7ms	+0.01	↓
NO	30ms	+0.04	×
OK	4ms	-0.01	↑

FIGURE 2. Diagram of an algorithm used in the previously presented solution. SDC – proposed synchronization data controller, SDS – proposed synchronization data sender.

The proposed synchronization strategy uses data from both sides of UG and the MG. The SDC device receives UG side voltage parameters and with the use of the MG voltage parameters, calculates the difference of the voltage, frequency, and instantaneous phase angle. This is done by comparing historical data on SDC devices with data received from SDS devices. The algorithm discards data that is older than previously received or older than the threshold. Data from both sides are subtracted from each other and differences between both grids are computed. To ensure the correctness of computation, measurements on both devices are synchronized to the pulse per second signal from the GPS device. The time synchronization signal is obtained from high precision pulse per second GPS signal. GPS pulse per second signal has a frequency of only 1Hz, which causes that there is a need for a PLL to synchronize the GPS signal with the 10kHz measurements signal. The 10kHz measurements signal is also used for timestamp measurements.

Result differences between voltage parameters of the MG and the UG side are used to calculate voltage droop control parameters shift. If the voltage conditions are stable on the MG and the UG side and the magnitude of voltage, frequency, and phase angle are synchronized with each other, MG is ready to transition to grid-connected mode.

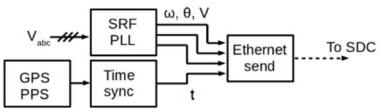


FIGURE 3. Schematic model of the proposed SDS device, GPS PPS – GPS pulse per second signal, SRF PLL – synchronous reference frame PLL.

Fig. 3 shows the proposed and developed SDS device. The synchronization module is responsible for collecting measurements, next the timestamps provided by a GPS receiver are added, and thus prepared data is sent by the Ethernet.

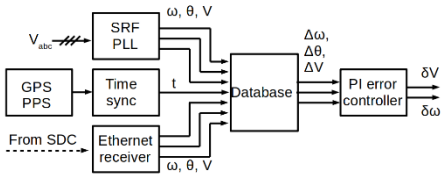


FIGURE 4. Schematic model of the proposed SDC device, GPS PPS – GPS pulse per second signal, SRF PLL – synchronous reference frame PLL.

Fig. 4 presents the SDC device algorithm. The SDC module is responsible for the calculation of the instantaneous parameters of the MG voltages and the acquisition of them in the SDC database. After data collection by SDC, the received information is aligned with time from the GPS and the output signal error is calculated with the use of two PI controllers. These controllers are presented with equations (1), (2):

$$\delta\omega = k_{p\omega}\Delta\omega + k_{p\varphi}\Delta\varphi + \int (k_{i\omega}\Delta\omega + k_{i\varphi}\Delta\varphi)dt \quad (1)$$

$$\delta V = k_{pV}\Delta V + \int (k_{iV}\Delta V)dt \quad (2)$$

where $k_{p\omega}$, $k_{p\varphi}$, k_{pV}, $k_{i\omega}$, $k_{i\varphi}$, and k_{iV} are the control parameters coefficients.

Eventually, calculated values are sent to the power converter droop control module [32]. The proposed remote synchronization method uses secondary level control to synchronize MG to the UG.

Both devices get voltage measurements and calculate voltage magnitude, frequency, and phase angle with the use of the Synchronous Reference Frame Phase Locked Loop (SRF PLL).

At the Lublin University of Technology, the research was conducted to investigate the parameters of the different synchronization methods [33], [34]. Table 1 presents selected results of these research.

TABLE 1. Compare of synchronization method at disturbances [33].

Method	Robustness on under-voltage	Robustness on frequency fluctuation	Robustness on harmonics
filtration αβ	No	No	No
SRF PLL	No	No	No
DDSRF PLL	Yes	Yes	Yes
DSOGI PLL	Partially	Yes	Yes
DSOGI-QSG-PSC-PLL	Yes	Yes	Yes

The latest research work [33] extends research synchronization algorithms in presence of harmonics, two-phase sags, and voltage phase jump. The conclusions presented in the article show that is the dual second order generalized integrator - quadrature-signals generator - positive-sequence calculator (DSOGI-QSG-PSC) and Decoupled Double Synchronous Reference Frame (DDSRF) PLL are more robust and immune on disturbances from the UG.

III. IDENTYFICATION OF THE INSTANTANEOUS PHASE VOLTAGE ANGLE

The synchronization of the MG to the UG requires precise identification of the instantaneous phase voltage angle of both systems. The synchronization angle determination causes no problem for an ideal power grid with a stable sinusoidal voltage shape. In most UG, such ideal operating conditions do not exist. The frequency of UG changes slightly, with power demands conditions. The voltage in the UG is distorted, by the non-linear loads, transient states caused by reconnection or disconnection of renewable energy sources, or single-phase loads in weak three-phase grids. In the presence of those mentioned problems, energy distribution operators decided that these microgeneration systems should meet the requirements of grid codes. The aim of these regulations is to reduce the possibilities of switching off sources of distributed generation in the case of transient states in the grid and the associated voltage drops. If such an abnormal grid condition occurs at a significant distance from PCC, the synchronization between MG and UG should still operate correctly (fig. 5). Thus, there is a need for accurate identification of the phase angle for a reliable synchronization process over a long distance, which allows for maintaining MG synchronization in the presence of disturbance on UG.

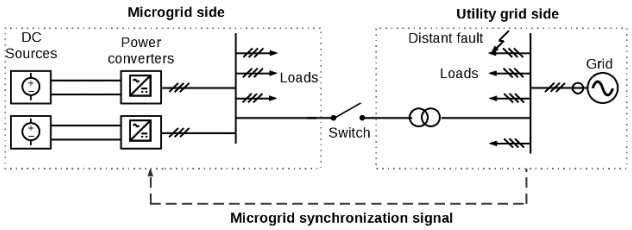


FIGURE 5. Synchronization of the MG to the UG with presence of distant fault in the UG.

Voltage in a three-phase system can be characterized as follows: instantaneous voltage (3) and the instantaneous synchronization angle θ is determined by the integral function (4) [35]:

$$v(t) = \begin{bmatrix} V_A \sin(\omega t + \varphi_A) \\ V_B \sin(\omega t + \varphi_B) \\ V_C \sin(\omega t + \varphi_C) \end{bmatrix} \tag{3}$$

$$\theta(t) = \int_0^T \omega dt \tag{4}$$

where: V_A, V_B, V_C – is a phase voltage magnitude, ω – pulsation of voltage, $\varphi_{A,}\ \varphi_{B,}\varphi_{C,}$ – is voltage phase.

Due to the periodicity of trigonometric functions, the $\theta(t)$ angle of ideal sinusoidal voltage takes a saw-tooth shape corresponding to the instantaneous phase angle. Fig. 6 presents voltage phase angle for positive phase order.

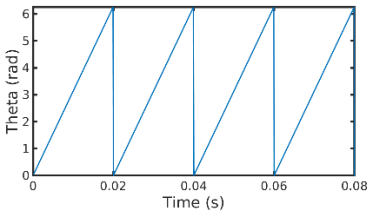


FIGURE 6. Interpretation of the grid synchronization angle specified for an ideal sinusoidal symmetrical voltage.

The classic synchronization method for three-phase systems is the SRF PLL algorithm, which is used to identify the instantaneous voltage phase angle in MG. The remote synchronization strategy based on GPS signal and SRF PLL was presented in previous article [30]. The scope of the author's work was a remote synchronization strategy without accessible PCC, which operates reliably for voltage stable conditions on the MG and the UG sides. For conducted test two different synchronization algorithm was used: previously used SRF PLL and more immune on disturbances DSOGI QSG PSC PLL which in this article will be called DSOGI PLL [31].

It is most commonly accepted that the synchronization algorithm should generate the ideal saw-tooth instantaneous phase angle, regardless of the type of disturbance. The key value for this investigation is the synchronization error δ which is the angle difference between the estimated grid angle

theta φ_{UG} and the ideal reference theta angle φ_{UGref}. For several discussed disturbances, an analysis of the synchronization error δ and its changes over time was performed. In the conclusion, the root means square error (rms_δ) of the synchronization error is calculated.

IV. EXPERIMENTAL TEST-STAND

To confirm the satisfactory operation of the proposed remote synchronization strategy operating with the UG under disturbances conditions, a laboratory test stand was set up, as shown in fig. 7.

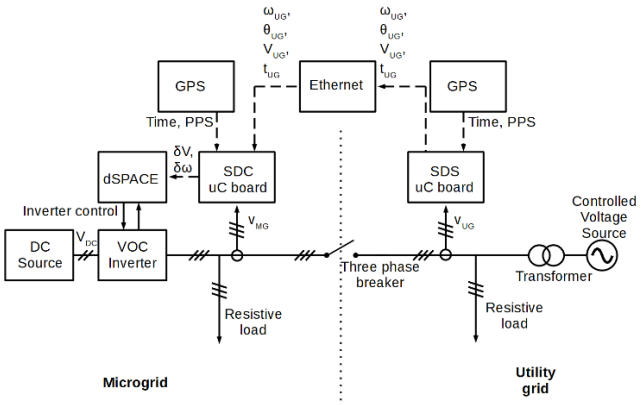


FIGURE 7. Experimental test stand schematic. μC board – microcontroller board.

The diagram could be divided into two separate functional modules: MG and UG galvanically isolated by a three-phase breaker. The MG was built based on resistive loads and an AC/DC power converter supplied by a DC source. The power converter and three-phase breaker were controlled by a dSPACE platform. The main control algorithm was a voltage-oriented control (VOC) with hierarchical control and droop control modules implemented. The SDC device uses its own local measurements, GPS signal, and data transferred from the SDS board by the Ethernet communication interface, to calculate the second control signal of hierarchical control. This signal is used to synchronize the MG to the UG.

At the right side of the three-phase breaker, there is a low voltage power transformer. The SDC device is taking measurements between the three-phase breaker and transformer on the UG side. Based on taken measurements and GPS timestamps, the SDS microcontroller board calculates the UG voltage parameters. Precalculated data is packed and sent to the SDC board by the Ethernet communication interface. As a voltage source, A Chroma 61512 source was used, which can produce the requested voltage waveform for UG. Table 2 presents parameters of test stand used in experiments.

The laboratory test stand is presented in Fig. 8. The MG side and the UG are not galvanically connected only by the Ethernet communication interface. The power converter was built-in IGBT technology in such a way to withstand 15x current overload during faults and synchronization tests. Additionally, the impedance between UG and MG was

TABLE 2. Parameters of the system used in the test stand.

Parameter	Value
Power converter	Two-level inverter
Power converter algorithm	Voltage Oriented Control with hierarchical control and droop control
Synchronization system	SRF PLL
Inverter output filter parameters	L = 1.83 mH C = 4.4 uF
Three-phase breaker	Moller DIL0M-G
DC source voltage	350V
DC bus capacitors	6000 uF
MG load	Resistive 33Ω per phase
GPS	SDC – uBlox NEO-6M SDS – uBlox NEO-7M
Ethernet communication interface	D-Link 100Mbps
Ethernet communication delay	5 – 10 ms
SDS, SDC	Tiva evaluation kit – LaunchPad EK-TM4C1294XL

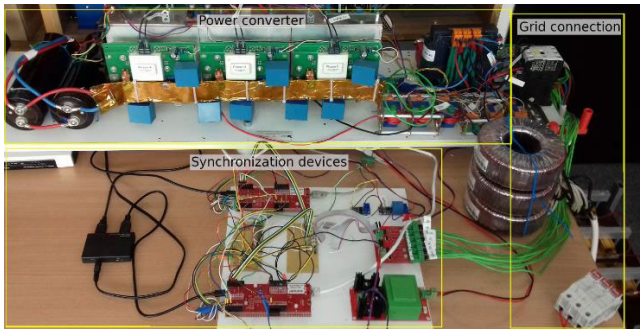


FIGURE 8. Picture of experimental test stand.

increased by the series inductance of the power transformer and oversized inverter filter. The laboratory tests were divided into four parts. By using the Chroma AC power source it was possible to generate four different types of disturbances and sags: the presence of higher harmonic below and above IEEE Std. 519-2014 standard, single-phase and two-phase sags. The main reason for these tests was to compare the performance of simple SRF PLL and SOGI-PLL advanced synchronization algorithms, operating in presented previously remote synchronization strategy without accessible PCC conditions, during the presence of the disturbances and sags. All used devices are within the laboratory. Used Ethernet connection used external IP and communicate by public Ethernet infrastructure.

V. INFLUENCE OF SENDING DATA RATE ON SYNCHRONIZATION STRATEGY

The first tests are related to the influence of packet sending data rate on the difference of the result theta angles for 10 kHz. For this test, the SRF PLL is used as a synchronization algorithm. The algorithm is chosen to test different distorted theta angles for typical voltage distortions that can be observed on the grid. Tests were performed for six different sending data rates: 5 kHz, 2.5 kHz, 1 kHz, 0.5 kHz, 0.25 kHz,

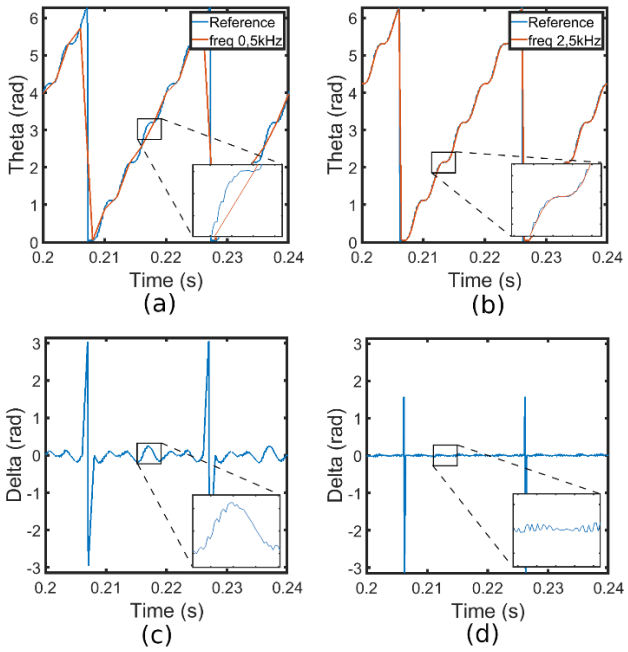


FIGURE 9. The impact of a different sending data rates on the result theta angle signal with presence of the higher harmonic THD 19%, (a), (b) – compare to reference theta angle for 0.5 kHz and 2.5 kHz of data rate, (c), (d) – difference between received theta angle to 10kHz reference theta angle for sending data rate of 0.5 kHz and 2.5 kHz.

and 0.1 kHz. For aforementioned sending data rates, four different distortions were measured: higher harmonic with THD of 6%, higher harmonic with THD of 19%, one phase sag, and two-phase sag.

Detailed results are presented for a few cases: 0.5 kHz and 2.5 kHz for higher harmonic with THD of 19% and two-phase sag.

A. PRESENCE OF HIGHER HARMONIC IN VOLTAGE ABOVE IEEE STD. 519-2014

For these results, it was assumed that non-linear load produces the level of harmonics distortion: 5th: 9.8%, 7th: 15.8%, 8th 2.16%. Fig. 9 presents results for tests with such distortions.

Fig. 9a and 9b present a difference between reference 10 kHz theta angle and corresponding theta angle received in data rate: (a) 0.5 kHz and (b) 2.5 kHz. Fig. 9 also presents the difference between the reference theta angle and received theta angle for (c) 0.5 kHz and (d) 2.5 kHz. The peaks indifference results are connected with discontinuity of theta angle. The region of discontinuity signal with higher frequency has more points than the low-frequency signal. This causes that on this region difference cannot be calculated correctly. The problem only occurs if a signal with a different data rate is compared. As both synchronization devices use the same data rate, the problem does not occur on real synchronization devices.

Provided results point out, that 2.5 kHz of theta angle sending data rate almost ideally represents reference theta angle on the theta angle continuous region. The maximum difference in this region is 0.05 radians. The results for 0.5 kHz of sending data rate points that results difference is much higher and has a maximum value of 0.25 radian.

B. TWO-PHASE SAG

For these results, it was assumed that the voltage magnitude of phase L2 and L3 is lowered to 50% of their nominal value. Moreover, the voltage phase angle difference between these lines is less than nominal and has a value of 40 degrees.

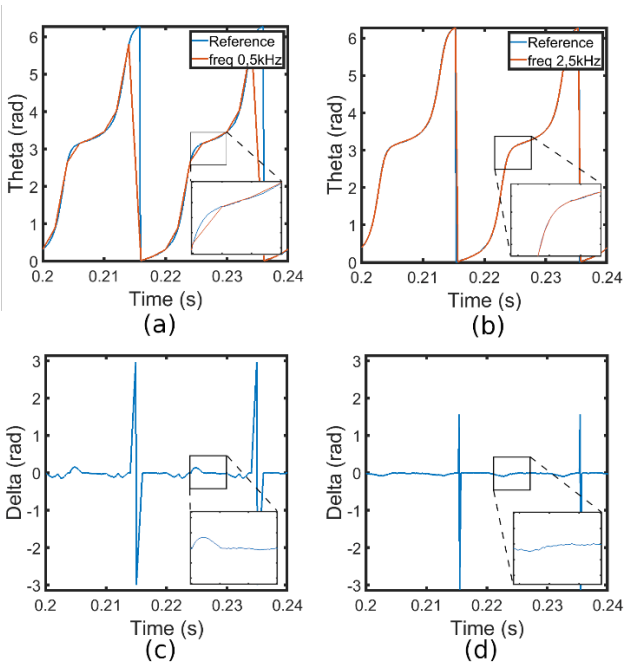


FIGURE 10. The impact of a different sending data rates on the result theta angle signal with presence of two-phase sag, (a), (b) – compare to reference theta angle for 0.5 kHz and 2.5 kHz of data rate, (c), (d) – difference between received theta angle to 10 kHz reference theta angle for sending data rate of (c) 0.5 kHz and (d) 2.5 kHz.

Fig. 10a and 10b present a difference between reference 10 kHz theta angle and corresponding theta angle received in data rate (a) 0.5 kHz and (b) 2.5 kHz. Fig. 10 also presents the difference between the reference theta angle and the received theta angle for (c) 0.5 kHz and (d) 2.5 kHz of data rate.

Provided results point out, that 2.5 kHz can also correctly represent theta angle for two-phase sag. The maximum difference in this region is 0.03 radians. The results for 0.5 kHz of sending data rate points that results difference is much higher and has a maximum value of 0.15 radian.

C. FIRST TEST CONCLUSIONS

For all tested results sending data rates and disturbances a root-mean-square (RMS) of the difference between reference theta angle and result theta angle. RMS is calculated for the

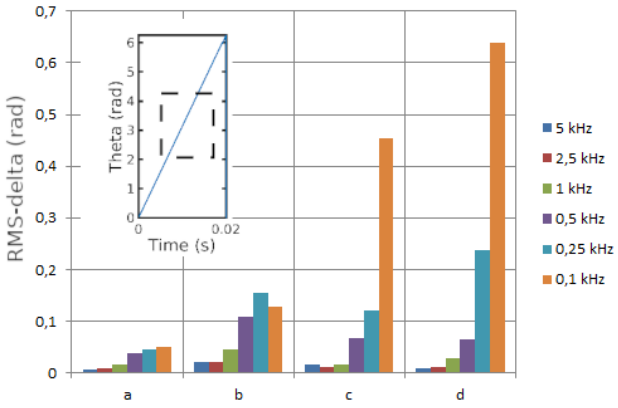


FIGURE 11. The impact of a different sending data rate on the result theta angle signal for different disturbances, (a) –higher harmonics with THD 6% (b) –higher harmonics with THD of 19%, (c) –one phase sag, (d) –two phase sag.

continuous region of theta angle difference signal between reference and measured theta angle.

Provided results, fig. 11, point out, that for higher data rates of theta angle sending, even highly distorted theta angle is not a problem. For lower data rates of theta angle sending received theta angle is deviates from reference theta angle. This deviation is higher if reference theta angle is more distorted with low frequency fluctuation.

As higher sending data rate causes more load on the Ethernet connection, a 1 kHz sending data rate is chosen as best compromise between performance and quality of remote synchronization method.

VI. USE OF DIFFERENT SYNCHRONIZATION ALGORITHM

The test was conducted with SRF PLL algorithms generating the grid angle on both the UG side and the MG side. The purpose of using SRF PLL on the UG site is to produce a distorted angle signal, which would then be transmitted to the MG side. Presented current waveforms show, that transmission of the distorted grid angle from the UG side to the MG side caused a large increase in THDi of the inverter operating on the MG side. In this case, it would be more beneficial to switch to an artificial grid angle and stop the synchronization between the MG and the UG.

A. PRESENCE OF HIGHER HARMONIC IN VOLTAGE BELOW IEEE STD. 519-2014

The first type of voltage distortion in UG is caused by current harmonics. harmonics are produced by nonlinear loads, but also by power electronics equipment. The first test was conducted for the level of voltage harmonics which did not exceed the limits of IEEE Std. 519-2014 standards. It was assumed that non-linear load produces the level of harmonics distortion: 5th: 3%, 7th: 2.5%, 11th 3.5% 13th: 3%.

The UG voltage distorted by the Chroma source was captured by the dSPACE A/D card and saved in a mat file. Fig. 12 presents a three-phase voltage waveform in the UG.

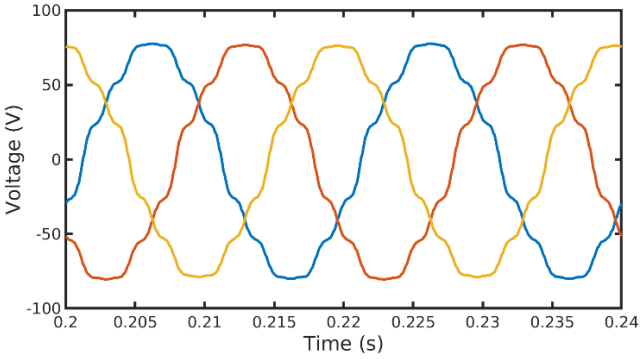


FIGURE 12. A waveform of UG voltage disturbed by Chroma source to the level of below of IEEE Std. 519-2014 standards.

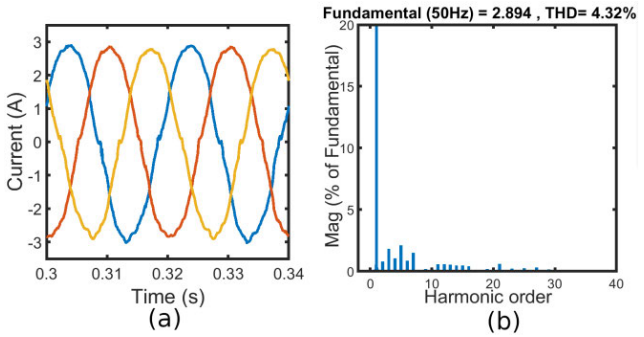


FIGURE 13. A waveform of MG current disturbed by power converter for synchronization signal with low level of harmonics.

Fig. 13 presents the power converter output current waveform during the distortion of synchronization signal by higher harmonics at level THD of 6%. For testing distorted synchronization signal, a SRF PLL was used as a synchronization algorithm. For this situation, the output current waveform is not distorted.

Fig. 14(a), (c) presents the synchronization angle received from the SDS and reconstructed from GPS time stamps and Ethernet data by the SDC microcontroller device. It is clear that the DSOGI PLL is more preferred to SRF PLL during the presence of higher harmonics. The use of this synchronization method introduces error, which finally will be transferred into the synchronization signal. Fig. 14(b), (d) represent the difference between reference synchronization angle and measured from SRF PLL and DSOGI PLL. Utilizing an algorithm with better filtration performance decreases the influence of higher harmonics on the synchronization signal.

B. PRESENCE OF HIGHER HARMONIC IN VOLTAGE ABOVE IEEE STD. 519-2014

The rise of the use of small power converters could cause the limits on harmonics on the distribution system could rise. For such conditions, a second test was performed with harmonics higher than those set in standard IEEE 519-2014. A controllable voltage source was used to produce the higher values of higher harmonics. It was assumed that non-linear

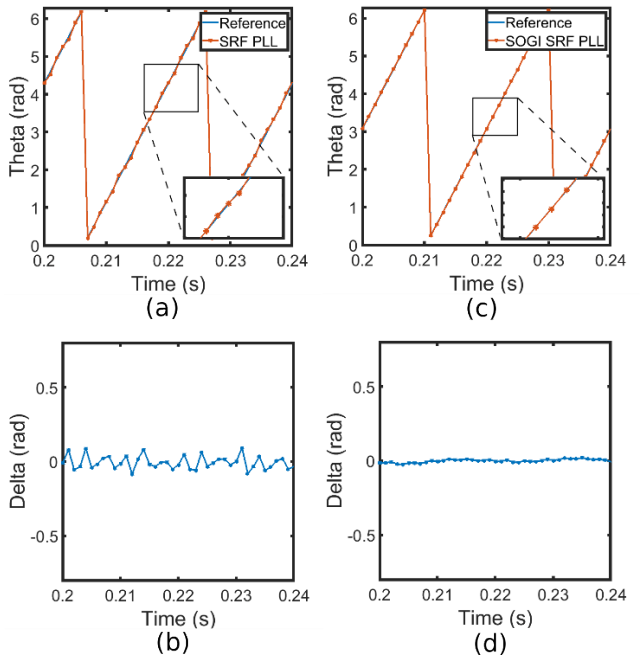


FIGURE 14. The influence of a higher harmonic below the standard IEEE Std. 519-2014b on remote synchronization tested devices for two cases: (a), (b) – SRF PLL, (c), (d) – DSOGI PLL, where: a) and c) is synchronization angles θ(t), b), d) synchronization errors δ(t) for tested algorithms.

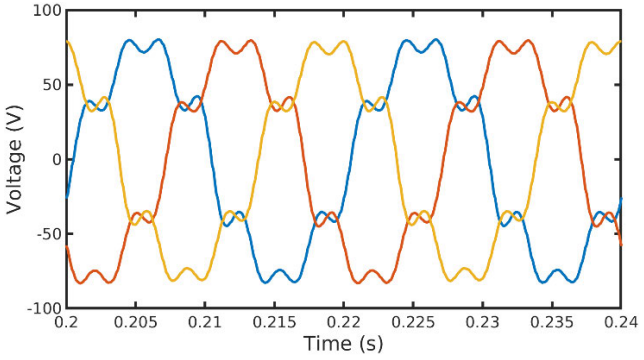


FIGURE 15. Used waveform to test presence of higher harmonic higher than in standards IEEE Std. 519-2014.

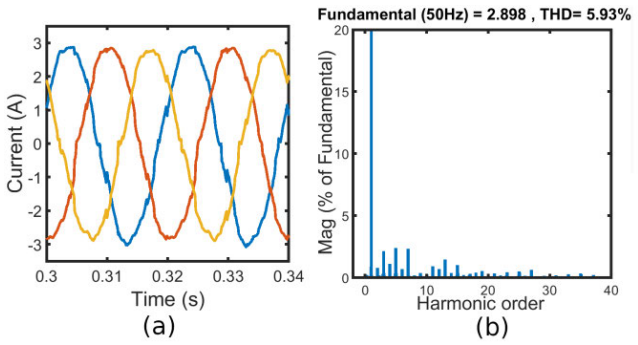


FIGURE 16. A waveform of MG current disturbed by power converter for synchronization signal with high level of harmonics.

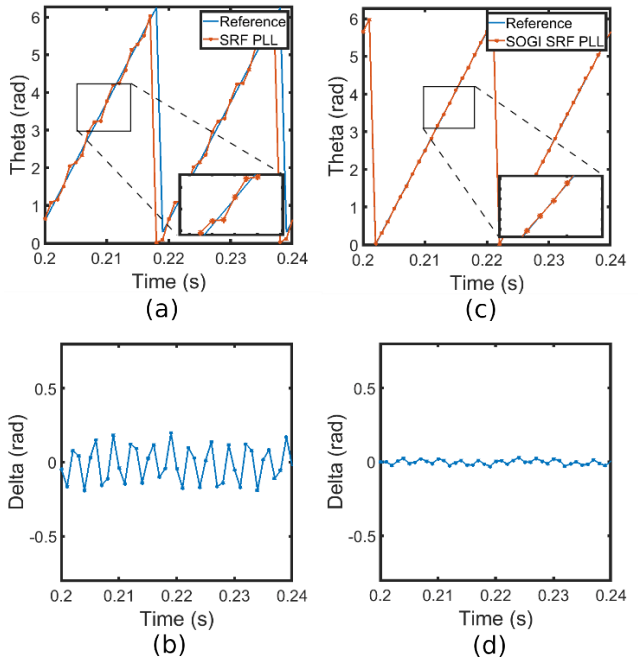


FIGURE 17. The impact of a higher harmonic, with harmonics higher than in standard IEEE Std. 519-2014, on the synchronization angle θ (t) (Theta angle(t) in the figure) and sync error δ(t) (delta(t) in the figure) using the following algorithms (a), (b) – SRF PLL, (c), (d) – DSOGI PLL.

load produces the level of harmonics distortion: 5th: 9.8%, 7th: 15.8%, 8th 2.16%.

Figure 15 presents a three-phase voltage waveform with a high presence of higher harmonics. Such voltage was connected to the UG of the synchronization test stand.

Fig. 16 presents the power converter output current waveform during the distortion of synchronization signal by higher harmonics at level THD of 19%. For this level of higher harmonics, the output current waveform is only slightly distorted. This is the result of signal filtration in the PI synchronization controller.

Fig. 17 (a) presents theta angle received from the SDS device when the SRF PLL algorithm was used, graphs (b) represent the difference between reference theta angle and SRF PLL. SRF PLL algorithm causes visible difference from reference theta angle in such condition. Fig. 17 (c) presents theta angle received from the SDS device when the DSOGI PLL algorithm was used, graphs (d) represent the difference between reference theta angle and DSOGI PLL. Theta angle produced by DSOGI PLL and reference theta angle ideally overlap each other. Graph (d) points out that the error of the DSOGI PLL synchronization method is almost 10 times smaller than using SRF PLL for tested conditions. The DSOGI PLL algorithm almost ideally estimates the synchronization angle.

Based on the results obtained from tests with higher harmonics, it can be stated that the DSOGI PLL synchronization algorithm determines the angle of synchronization with a high degree of accuracy even if there occurs a significant deformation of higher voltage harmonics.

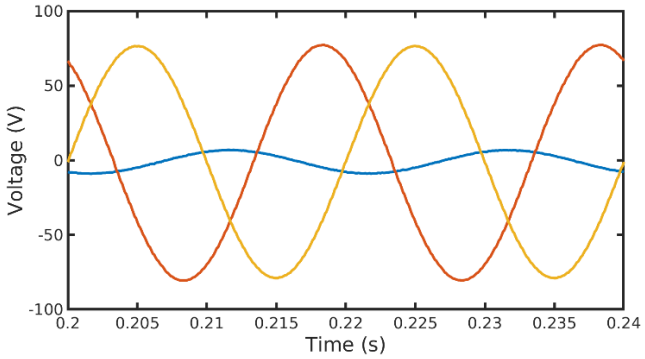


FIGURE 18. Used waveform to test one-phase voltage sag which causes go down of voltage magnitude to 10% of nominal magnitude in phase L1.

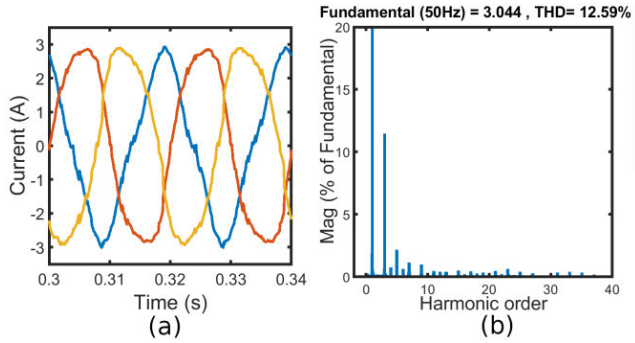


FIGURE 19. A waveform of MG current disturbed by power converter for synchronization signal with presence of distortion from one-phase sag.

The synchronization angle was best estimated by the DSOGI PLL algorithm, which showed the best results.

C. SINGLE-PHASE SAG

The single-phase sag happens during the connection of any line phase with a neutral line. This introduces negative sequence components in a three-phase voltage system, with which basic synchronization algorithms operate poorly. Fig. 18 presents a situation when such a condition occurs at a short distance from the device. The voltage magnitude of phase L1 is lowered to 10% of their nominal value.

Fig. 18 presents a three-phase voltage waveform for one phase sag in phase L1. For this type of transient sag, the operating conditions must survive for the time specified in the FRT codes of the grid operator. In the time required by these codes, the proposed device should operate without interruption. Such voltage was connected to the UG of the synchronization test stand.

Fig. 19 presents the power converter output current waveform during the distortion of synchronization signal by distant one-phase fault. For this type of disturbance, the output current waveform is slightly distorted. This points out that such a synchronization signal should not be used for MG synchronization. The use of such a distorted synchronization signal will cause distortion also in the MG.

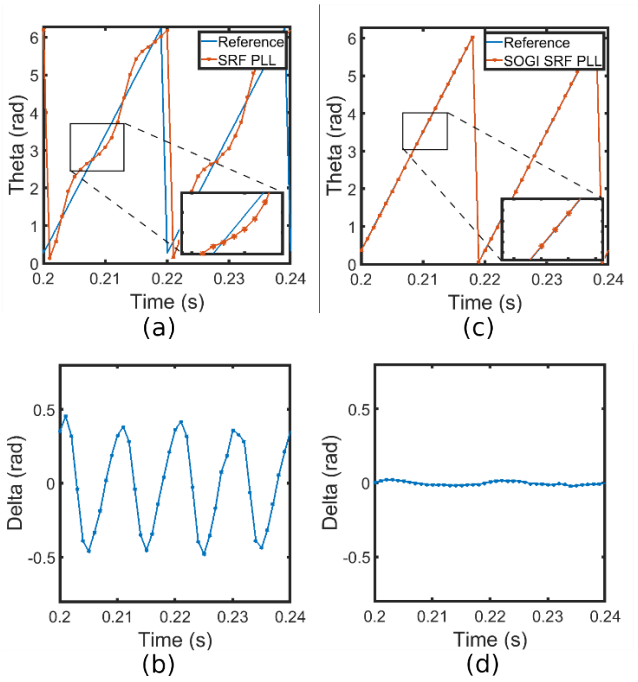


FIGURE 20. The impact of a single-phase sag on the synchronization angle on the synchronization angle θ (t) (Theta angle(t) in the figure) and sync error δ(t) (delta(t) in the figure) using the following algorithms (a), (b) – SRF PLL, (c), (d) – DSOGI PLL.

Fig. 20 (a) presents theta angle received from the SDS device when the SRF PLL algorithm was used, graphs (b) represent the difference between reference theta angle and SRF PLL. SRF PLL algorithm causes a big difference from reference theta angle in such conditions. Therefore, with single-phase sags, this algorithm cannot be used for such disturbances. Fig. 20 (c) presents theta angle received from the SDS device when the DSOGI PLL algorithm was used, graphs (d) represent the difference between reference theta angle and DSOGI PLL. DSOGI PLL algorithm extracts a positive sequence from the waveform, which causes ideal synchronization. Graph (d) points out that the error of the DSOGI PLL synchronization method is almost 20 times smaller than using SRF PLL for tested conditions. Theta angle produced by DSOGI PLL and reference theta angle ideally overlap each other. Therefore, with single-phase sags, this algorithm operates flawlessly for such disturbances.

D. TWO-PHASE SAG

The two-phase sag happens during the connection of any two phases. Fig. 21 presents a situation when such a condition occurs at a distance from the device. The voltage magnitude of phase L2 and L3 is lowered to 50% of their nominal value. Moreover, the voltage phase angle difference between these lines is less than nominal and has a value of 40 degrees.

Fig. 21 presents the three-phase voltage waveform for two-phase sag in phases L2 and L3. Such voltage was connected to the UG of the synchronization test stand.

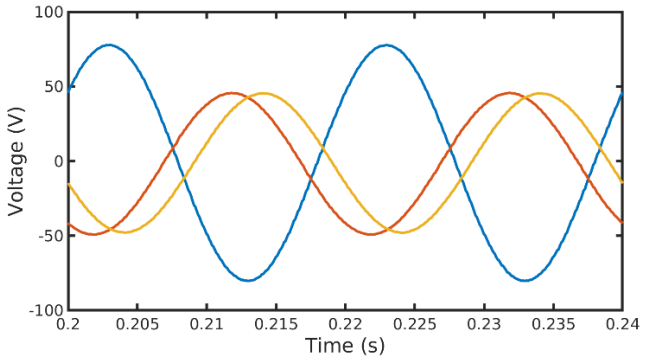


FIGURE 21. Used waveform to test a two-phase sag in phase L2 and L3.

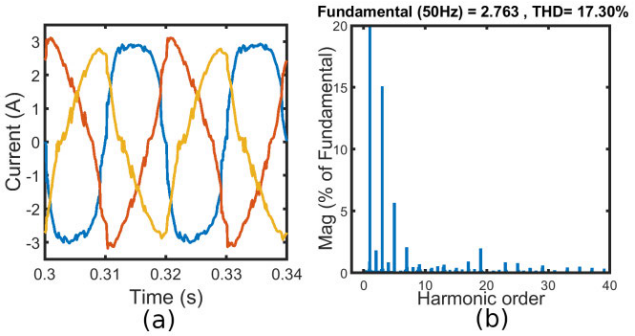


FIGURE 22. A waveform of MG current disturbed by power converter for synchronization signal with presence of distortions from two-phase sag.

Fig. 22 presents the power converter output current waveform during the distortion of synchronization signal by distant two-phase fault. For this type of disturbance, the output current waveform is distorted. This points out that such a synchronization signal should not be used for MG synchronization. The use of such a distorted synchronization signal will cause distortion also in the MG.

Fig. 23 (a) presents theta angle received from the SDS device when the SRF PLL algorithm was used, graphs (b) represent the difference between reference theta angle and SRF PLL. Similar to a single-phase sag, the use of the synchronization algorithm SRF PLL leads to a high value of synchronization errors. SRF PLL algorithm causes that difference between reference theta angle and estimated theta angle goes up to 0.7 radians in such condition. Therefore, with two-phase sags, this algorithm cannot be used.

Fig. 23 (c) presents theta angle received from the SDS device when the DSOGI PLL algorithm was used, graphs (d) represent the difference between reference theta angle and DSOGI PLL. In contrast, from the SRF PLL synchronization algorithm, the advanced DSOGI PLL algorithm overcomes two-phase sag very well. DSOGI PLL algorithm extracts a positive sequence from the waveform, which causes ideal synchronization. Theta angle produced by DSOGI PLL and reference theta angle ideally overlap each other. Graph (d) points out that the error of the DSOGI PLL synchronization method is almost 35 times smaller than using SRF PLL

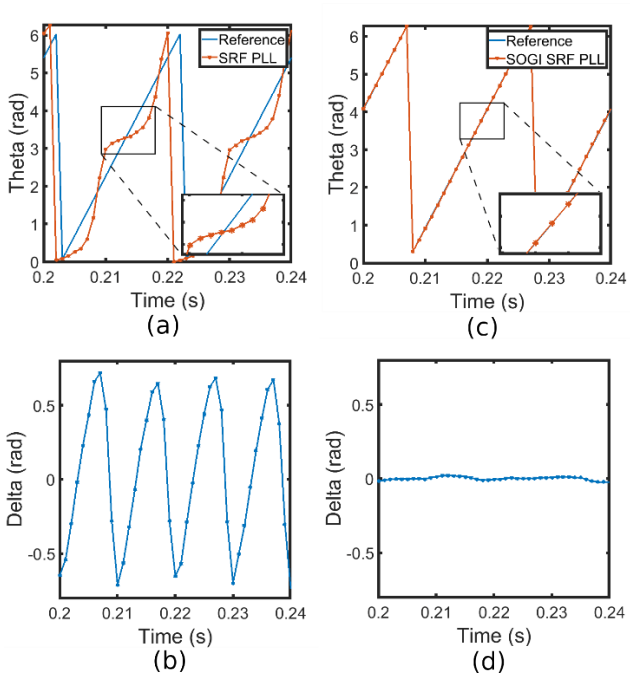


FIGURE 23. The impact of a two-phase sag on the synchronization angle on the synchronization angle θ (t) (Theta angle(t) in the figure) and sync error δ(t) (delta(t) in the figure) using the following algorithms (a), (b) – SRF PLL, (c), (d) – DSOGI PLL.

for tested conditions. Therefore, with two-phase sags, this algorithm operates flawlessly for such disturbances.

E. OPERATION OF PROPOSED SOLUTION IF PHASE JUMP OCCURS

A step-change in the phase angle can happen as a result of switching the power line. If the angle reaches several degrees, then this deviation can be caused by different parameters of the switched power line. If the angle is about 30 degrees or a multiple of this value, then the source of such a large jump is caused by a different group coupling the transformers supplying the lines. For example, switching from Dz6 to Dy5 is accompanied by a step-change in a three-phase voltage jump of 30 degrees. Also adding to the MG a big reactive load can cause a phase jump. The solution was tested for three different phase angle jumps 30, 60, and 90 degrees.

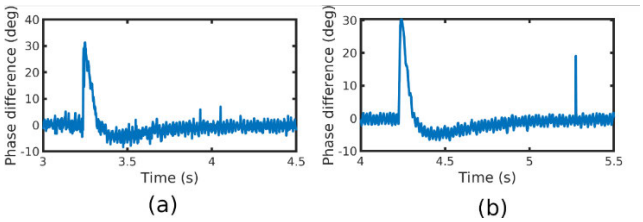


FIGURE 24. Voltage phase angle difference between the MG and the UG at phase jump 30 degrees for (a) SRF PLL, (b) DSOGI PLL.

Fig. 24-26 presents results for three-phase jumps with the use of classical SRF PLL and advanced DSOGI PLL. In both

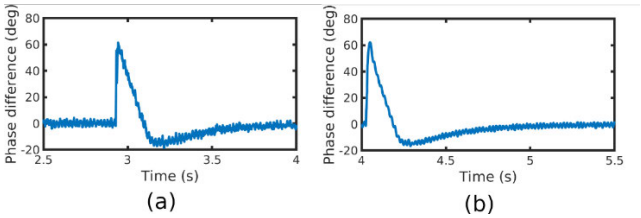


FIGURE 25. Voltage phase angle difference between the MG and the UG at phase jump 60 degrees for (a) SRF PLL, (b) DSOGI PLL.

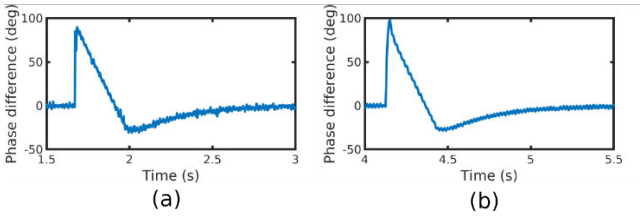


FIGURE 26. Voltage phase angle difference between the MG and the UG at phase jump 90 degrees for (a) SRF PLL, (b) DSOGI PLL.

TABLE 3. Time needed by proposed method to correct phase difference.

	Time to synchronize with use of SRF PLL [s]	Time to synchronize with use of DSOGI PLL [s]
30°	0.49	0.41
60°	0.791	0.77
90°	1.16	1.1

cases, we can see that after the phase jump, there is normal synchronization. It can be compared to the situation when synchronization starts at a different phase angle.

Table 3 presents the time needed by the proposed method to synchronize the MG to the UG after the phase angle jump. Synchronization time with the use of both methods is almost the same, which points that synchronization time mainly depends on the PI synchronization controller and delay time on communications and does not depend on the time of the synchronization algorithm. As MG synchronization time is higher than the setting time of both synchronization algorithms, both can be used.

F. SECOND TEST CONCLUSIONS

In order to compare the results presented in fig. 12 to 23, bar charts in fig. 27 show the rms(δ) errors for the considered distortion. In this graph, the blue bars indicate the SRF PLL algorithm whereas the red bars specify the DSOGI PLL algorithm.

Based on the presented results, it is clearly visible that if the DSOGI PLL algorithm is used in the previously proposed remote synchronization algorithm, the achieved results are very good. The worst condition for use of the SRF PLL synchronization algorithm occurs with asymmetrical voltage sags. Synchronization errors for this algorithm do not go down to zero, and the result rms error is significant.

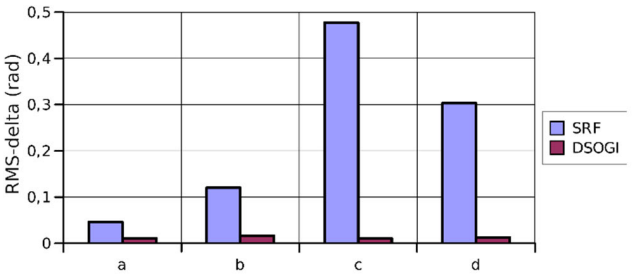


FIGURE 27. An value of the rms(δ) during an event as: a) higher harmonic disturbances within limits IEEE Std. 519-2014, b) higher harmonic disturbances above limits IEEE Std. 519-2014, c) two-phase sag, d) single-phase sag.

The analysis presented here is based on the difference between reference theta angle and estimated theta angle. From this, the delta (δ) and error root mean square rms(δ) are calculated. On its basis, it can be concluded that the DSOGI PLL synchronization algorithm is more suitable to use for instantaneous voltage parameters estimation in the previously presented remote synchronization method without accessible PCC. It operates correctly even with disturbances in the grid.

Presented power converter waveforms show that synchronization signal transferred from the UG side needs to be without any distortions, otherwise, the distortion would transfer to the MG side, despite not being galvanically connected. In a case, where the UG side grid angle signal is distorted, the MG should disable synchronization to the UG and switch to an internal grid angle signal.

VII. CONCLUSION

This paper presents the extension of the previously developed by authors remote synchronization strategy presented on [30]. The main achievement is to remove dependence on the PCC measurements. The proposed devices can be mounted in any connection point of the UG and the MG. Even in the case of more than one three-phase breaker between the MG and the UG. The proposed new active synchronization method which is based on remote synchronization was tested in situations when the voltage distortion is present in UG. The evaluation of proposed remote synchronization was based on the injection of typical disturbances such as voltage sags, phase jumps, two-phase short, and higher harmonics. For the purpose of determining the influence of synchronization algorithms, two different methods were taken to account. The first one was a simple and extremely fast SRF PLL and the second was DSOGI PLL, which is robust and based on the symmetrical components decomposition. The article presents also, that the issue of the quality of the synchronization signal and the impact of the overall performance of MG. The presented on paper results also show the influences of grid voltage disturbances on MG operation.

The presented results were performed on a physical model of a laboratory microgrid MG. The Source of voltage was created by using a power converter with VOC control and

hierarchical control. The synchronization signal was tested with wireless transmission and GPS time synchronization signals.

The conclusions show is 1 kHz of data rate is the optimal trade-off between quality of synchronization and the level of usage of the data transmission channel. The chosen data rate is sufficient to represent every distorted synchronization signal in case of the presence of typical grid voltage disturbance. Conclusions also show that the correctness of remote synchronization mainly depends on the disturbances immunity of the main synchronization algorithm.

The presented method and solution is the expansion of the potential of usage microgrids technology worldwide. Also allows for a smooth transition between stand-alone to grid-tide operation even in presence of typical grid voltage disturbances and the absence of availability of a PPC measurement point.

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