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A Biasing Approach to Design Ultra-Low-Power Standard-Cell-Based Analog Building Blocks for Nanometer SoCs

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ABSTRACT This paper presents an approach to design analog building blocks for nanometer systems on a chip (SoCs) that are based on digital standard-cells. The proposed approach guarantees that all the CMOS inverters, taken from a standard-cell library, operate with well-defined quiescent current and output voltage, thus allowing the implementation of analog circuits with good robustness against PVT variations. The approach is based on an Analog Body Bias Generator (ABBG) reusable block, similar to the ones adopted in digital applications to cope with process variations, and exploits the bulk terminals of both the p-channel and n-channel MOS transistors of the standard-cell inverter as current and voltage control inputs. The bulk voltages generated by the ABBG are routed to all the standard-cell inverters used for analog functions and allow to set the quiescent current of each cell to a multiple of a reference current and the static output voltage of each cell to half the supply voltage. The full custom design of the ABBG is presented, as well as the design flow to allow the automatic place and route of the proposed standard-cell based analog building blocks. We finally give an example of application trough the design of a fully synthesizable four-stage-gain low-power operational transconductance amplifier (OTA). Both the body bias generator and the OTA have been implemented in a 65-nm CMOS technology. The OTA nominal current consumption is 1.75 μA with 0.41-μA standard deviation. Good robustness against supply and temperature variations is also found.

INDEX TERMS Standard-cell analog circuits, body bias, low voltage, low power, four-stage OTA.

I. INTRODUCTION

Battery-operated or energy-harvested systems, such as biomedical implantable devices or sensor nodes for the Internet of Things (IoT), require the development of ultra-low-voltage, ultra-low-power CMOS Systems on Chip (SoCs) in which analog interface circuits are integrated together with the digital processing and communication cores [1]–[4].

In the conventional design flow of mixed-signal integrated circuits (MS ICs), the design and implementation of the analog building blocks is usually carried out manually by the analog designer who iterates several times each step of the flow to optimize performance and area figures of merit. In contrast, the digital section is synthesized using the standard-cell approach in a semi-custom design flow. This design flow is based on automated place and route and exploits standard (digital) cells from a library often supplied by the foundry and that have been designed to fulfill the design/electrical rule checks of the specific technology. Of course, this approach allows the design cycle to be strongly simplified and verification/test techniques to be easily implemented.

Nowadays, due to the continuous scaling of MOS feature size in the nanometer regime, the analog designer has to cope with new challenges in the simulation and implementation steps of the design flow. For example, lower supply voltages, poor scaling of analog properties of transistors, increased variability of electrical parameters and the added complexity of transistor structures, pose stringent requirements in terms of area, cost, and design effort, often requiring calibration

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and/or reprogrammable functions because computer simulations do not often match with the silicon results [5]. At this purpose, recent works have introduced the standard-cell approach also to analog circuit design. This allows to specify behavioral performance through a hardware description language (HDL) and to exploit a fully-automated (including place & route) design flow.

In this framework, standard-cell approaches have been exploited to design macroblocks such as phase-locked loops, stochastic analog-to-digital converters, and time-to-digital converters, [6]–[10], down to basic building blocks such as voltage comparators and operational amplifiers that in these solutions are based on inverter gates [11]–[15]. However, the main limitation of these latter solutions is related to the absence of a reliable control mechanism of the bias current of the inverter cell as well as of its static output voltage. This results in a high sensitivity of the overall circuits to process, voltage and temperature (PVT) variations and implies an ill controlled power dissipation, which is not tolerable in ultra-low-power applications.

In this paper, we introduce a novel technique to design ultra-low-voltage, ultra-low-power, standard-cell-based analog building blocks with well-defined quiescent conditions. The approach requires a standard-cell library which provides the accessibility of the body terminals as [16]–[20] and is based on an *Analog Body Bias Generator* (ABBG) block which allows to accurately set the quiescent current and the static output voltage of the digital standard-cells by driving the bulks of both p-channel and n-channel MOS transistors.

The biasing principle is described in Sec. II, whereas the proposed semi-custom design flow for analog circuits is outlined in Sec. III, together with the design of a fully synthesizable four-gain-stage operational transconductance amplifier (OTA). The design of a test chip in 65-nm CMOS including the body bias generator and the OTA together with the experimental and simulation results are then presented in Sec. IV, thus confirming the effectiveness of the biasing technique and the overall performance of the amplifier. Finally some conclusions are drawn in Sec. V.

II. BIASING APPROACH

The proposed biasing approach is based on the availability of the following building blocks either in a triple-well bulk or fully depleted silicon on insulator (FDSOI) CMOS process:

1) Conventional CMOS inverter standard-cells taken from the standard-cell library of the technology with the accessibility of the body terminals. The inverter cells, other than the input and output terminals, must have 4 power nets to be treated as global nets, namely, V_{DD_core}, V_{SS_core}, V_{bulkN}, and V_{bulkP}.

Fig. 1 illustrates the unitary inverter of a specific standard-cell library, denoted as *IVx1*, and that for our purposes is referred to as the "reference" one. W_{P_REF} and W_{N_REF} are the gate widths of M_P and M_N, i.e., the reference inverter PMOS and NMOS transistor, respectively.

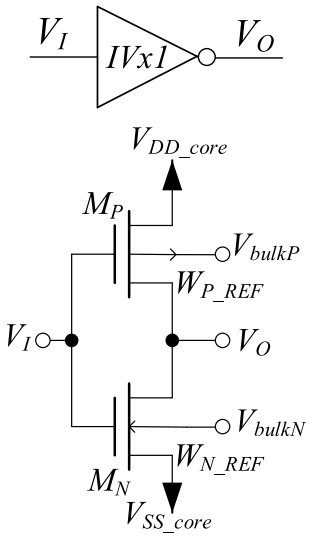

FIGURE 1. Unitary inverter, IVx1, from a standard-cell library. Transistor widths are W_{P_REF} and W_{N_REF}. L is the minimum allowed by the technology.

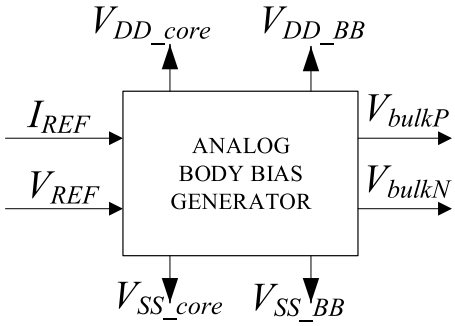

FIGURE 2. Block view of the proposed analog body bias generator.

In this library, a higher cell number, like e.g. *IVx4*, means that the widths of the cell are four times greater than those of *IVx1*. The above-mentioned power nets must be routable independently. This feature is available in almost all recent nanometer CMOS technologies, where adaptive body bias (ABB) and adaptive supply voltage scaling (ASV) are frequently utilized by digital designers to cope with PVT variations and to reduce the spread of maximum operating frequency and power consumption [21]–[29]. In these approaches, specific Body Bias Generators are exploited to provide forward body bias (FBB) or reverse body bias (RBB) for optimizing the speed/power consumption tradeoff. These blocks are typically designed following a full-custom approach as happens for the standard-cells in the digital libraries of a given technology. Once all the needed files are available, body bias generators can be exploited in semi-custom design flows where the synthesis and layout steps are performed by automatic synthesis and place & route.[1]

[1]CAD tools such as RTL Compiler (for synthesis) and Innovus (for place & route) are those typically used when referring to a Cadence design flow.

2) A new Body Bias Generator reusable block specifically tailored for analog standard-cell-based circuits. The aim of this block is to provide bias voltages, V_{bulkN} and V_{bulkP}, to the inverter standard-cells used in the analog domain to ensure:

a. A well-defined DC output voltage for each standard-cell;
b. A well-defined DC current for each standard-cell.

The proposed Analog Body Bias Generator (ABBG) block is depicted in Fig. 2 and is designed by following a full custom approach. In addition to V_{DD_core} and V_{SS_core}, the block needs two further (positive and negative) body bias supply voltages, V_{DD_BB} and V_{SS_BB}, because the standard-cells may require body voltages that extend beyond the core supply rail. In SoC environment both thicker oxide transistors and higher supply voltage dedicated to I/O and peripheral blocks are always available and in the following we exploit thicker oxide I/O MOS devices and the I/O supply rail for the proposed ABBG. However, if the I/O supply rail is not available or not suited for a specific design, V_{DD_BB} and V_{SS_BB} can be generated by ad hoc charge pump circuits.

Once designed, the ABBG will be used as an ordinary reusable standard-cell library element. At this purpose, the abstract view needed for automatic place & route has to be developed as will be discussed in the following section. The block takes as two inputs 1) the stable reference current I_{REF}, from which the DC current of the standard-cell is derived, and 2) the stable reference voltage V_{REF} equal to half the core supply voltage, that is used to set the output DC voltage of the standard-cells. The current reference can be generated from integrated bandgap references easily available in a SoC context, whereas V_{REF} is derived from the core power supply and can be easily implemented through a voltage divider and a buffer amplifier. Usually, $V_{REF} = (V_{DD\_core}+V_{SS\_core})/2$, is chosen for symmetric input and output swing.

The proposed ABBG is based on a previous replica biasing solution, developed by the authors, which allows the quiescent current of a MOS device to be accurately set through its body terminal [30]–[32]. In the present case, we apply the technique to both MOS transistors forming the inverter stage.

The simplified transistor-level schematic of the ABBG is shown in Fig. 3, where two feedback loops force the quiescent currents and output voltages of two reference transistors, M_{P_BB} and M_{N_BB}, that will be used to bias the reference inverter in Fig. 1. The gates of both the reference transistors are set to V_{REF}. Then, referring to Fig. 3a for the p-channel side, the error amplifier, A_P, sets the drain of M_{P_BB} to V_{REF} (thanks to the input virtual short) and produces the body voltage, V_{bulkP}, required to set its quiescent current to I_{REF}.

A similar working principle characterizes the dual circuit in Fig. 3b for the n-channel side which generates control voltage V_{bulkN}.

Observe now that the gate widths of M_{P_BB} and M_{N_BB} are chosen equal to W_{N_REF} and W_{P_REF}, i.e., the gate widths of the reference inverter *IVx1* in Fig. 1. Being $V_{IN} = V_{REF}$ in quiescent conditions, then transistors M_P and M_{P_BB} (M_N and M_{N_BB}) share the same nominal dimensions and the same gate, source, and body voltages (for ideally infinite gain of the error amplifiers).

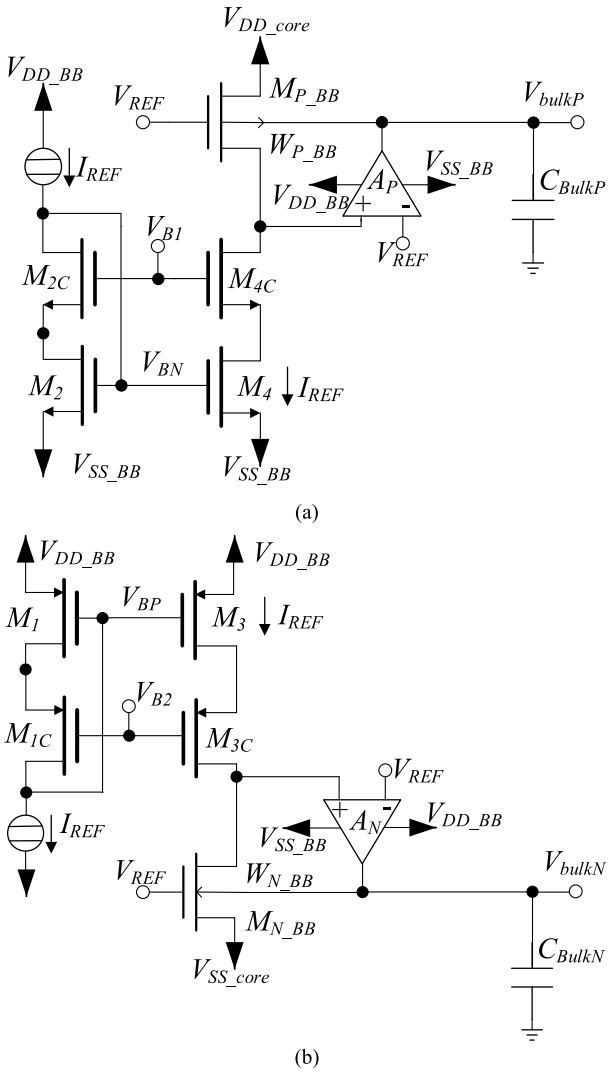

FIGURE 3. Simplified schematic diagram of the ABBG: V_{bulkP} generation subcircuit (a), V_{bulkN} generation subcircuit (b).

Therefore, we get in these ideal conditions that V_O and the quiescent current in the reference inverter *IVx1* (in Fig. 1) are respectively equal to V_{REF} and I_{REF}. It must be remarked that V_{bulkN} and V_{bulkP} of the ABBG track any PVT variation through the sensing transistors M_{P_BB} and M_{N_BB} and are able to guarantee the prescribed voltage and current quiescent conditions. These bulk voltages are connected to the global nets so that V_{bulkN} and V_{bulkP} are routed to all the standard-cells used for analog design. Through this replica bias approach, each standard-cell will mirror a multiple of I_{REF} according to its gate width ratio, therefore cell *IVx4*, for instance, will have a quiescent current of $4I_{REF}$ and the same DC output voltage V_{REF}.

The two error amplifiers A_P and A_N are implemented through the topology illustrated in Fig. 4. It is a conventional

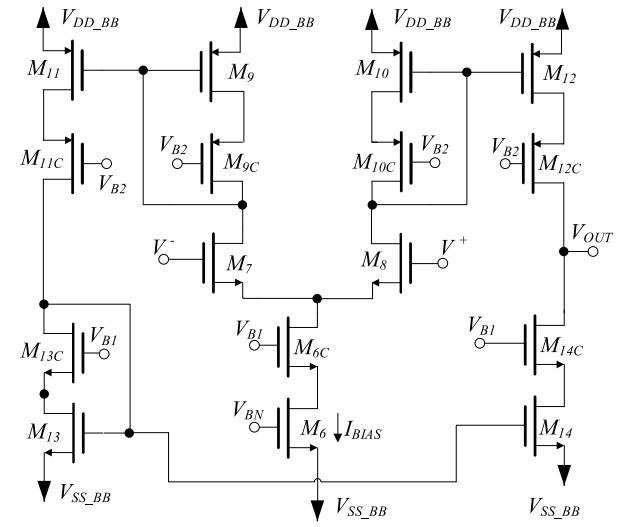

FIGURE 4. Schematic diagram of the error amplifiers in the ABBG.

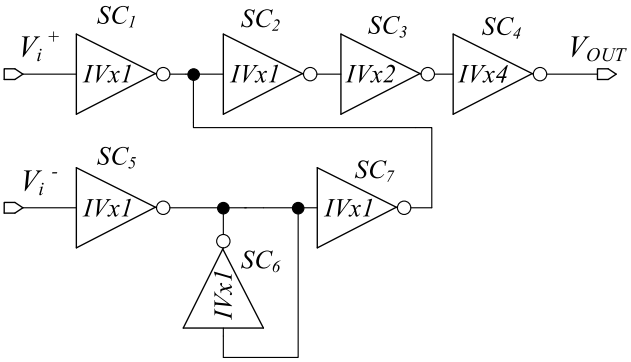

FIGURE 5. Schematic of the proposed inverter based 4-stage OTA.

single-stage high-gain, low-voltage cascode amplifier. Due to the static function of the amplifiers (they are used to set quiescent parameters), they are required to provide neither large bandwidth nor large common-mode input range. Two small output capacitors, C_{BulkP} and C_{bulkN}, are sufficient to stabilize the two loop gains by dominant-pole compensation.

III. SEMI-CUSTOM DESIGN FLOW FOR ANALOG CIRCUITS AND EXAMPLE OF APPLICATION

A. SEMI-CUSTOM DESIGN FLOW

After the full custom design and layout of the ABGG have been completed, the views needed for the automatic place and route flow can be derived. In particular, layout information such as size, pin names, pin positions and routing blockages can be incorporated into the library exchange format (.LEF) file which can be automatically generated through an abstract generator tool starting from the layout view. A Verilog (.v) file of the ABBG module which contains only the module interface pins can be easily written following the Verilog syntax. Now the ABBG can be instantiated via Verilog code together with all the standard-cells used to implement analog functions on a mixed-signal SoC, thus building the full netlist of the analog section.

It has to be noted that, in the proposed design approach, the customized design effort related to ABBG implementation is a "one time" effort, required only to build the library containing the ABBG similarly as what happens to build the standard-cell library containing the standard-cells or the body bias generator libraries used to cope with PVT variations in digital circuits. Once designed, the ABBG can be used as an ordinary reusable standard-cell library element for several SoCs. The full custom design and library implementation of the ABBG can be carried out by the IC manufacturer and the ABBG library distributed together with the standard-cell library as happens for body bias generator libraries used for digital circuits [21]–[28].

In the following subsections we will illustrate the application of the methodology through an example: the design of a four-stage OTA. Without loss of generality, we refer, for the design example in this section, to a 28-nm FDSOI CMOS technology. This technology provides standard-cell libraries with accessibility to the bulk terminal of both PMOS and NMOS devices through suitable Welltap cells. This feature is typically available even on conventional triple-well CMOS technologies with feature size lower than 90-nm.

In the proposed approach all the standard-cells exploited to implement analog functions have the bulk connections driven by the ABBG. This means that we have two big local substrates (one including all the standard-cells exploited for analog design, and the other including all the standard-cells used for digital design) that can be biased by different voltages. The substrate voltage of the analog section is driven by the ABBG, whereas the bulk connections of standard-cells in the digital section will have a different substrate voltage (which could be driven by a conventional BBG for digital circuits) and this is allowed by recent technologies and supported by recent tools for automatic place and route under the multi-supply voltage flow.

To allow the usage of more than one ABBG with different bulk voltages, isolated bulk connections for both NMOS and PMOS transistors in each standard-cell are required. This is allowed, for example in the 28-nm FDSOI CMOS process from STMicroelectronics (which we used in the example in section III) which provides an additional library in which the standard-cells have isolated bulk connections for both NMOS and PMOS transistors. Obviously the standard-cells in this library occupy a larger area footprint than the standard-cells in the conventional library.

B. EXAMPLE OF APPLICATION: 4-STAGE OTA

In this subsection we will discuss an example application of the proposed semi-custom design flow for analog circuits in the implementation of a fully synthesizable OTA whose cell-level schematic is illustrated in Fig. 5.

We remark that this OTA is chosen only as an illustrative example and that virtually all the topologies based on inverter cells can take advantage of the proposed ABBG and biasing approach. Nevertheless, since the OTA topology is partially new, we will briefly explain its operating principle below.

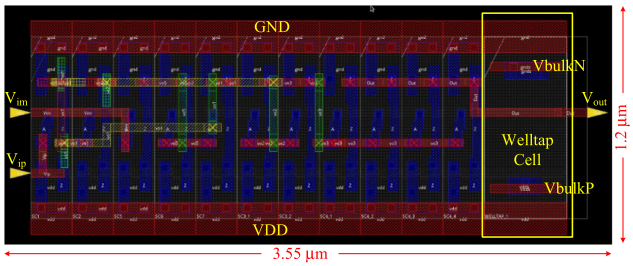

FIGURE 6. Layout of the OTA in Fig. 5 generated through automatic place and route by using the Cadence Innovus tool (28-nm FDSOI CMOS technology).

It is well known that under small signal conditions the generic *i-th* inverter provides a voltage gain, A_{vi}, given by the product of its transconductance, g_{mi}, and its output resistance, r_{oi}.

$$A_{vi} = g_{mi} r_{oi} \tag{1}$$

where g_{mi} is the sum of the transconductances of the PMOS and NMOS transistors of the inverter (in the quiescent conditions), and r_{oi} is the parallel of the output resistances of the same transistors. Low bias current requirements imply MOSFETs operating in the subthreshold region, with low transconductances and consequently low gains. Four stages are therefore required to achieve an acceptable OTA DC gain. We assume, in our example, that the last two inverter stages, SC_3 and SC_4, have increasing scale factors, $\times 2$ and $\times 4$, respectively, to increase the driving capability of the OTA, in a similar way we find in a tapered buffer. This also means that their transconductances are 2 and 4 times greater than that of the unitary inverter, respectively. All the other inverters in the first and second stage are nominally equal to the unitary one. The differential to single-ended conversion required by a differential-input OTA is made up of two paths. The path driven by V_i^+ is simply a single inverter, SC_1, whereas the path driven by V_i^- is the cascade of three inverters, SC_5-SC_7, the second of which, SC_6, has the input and output tight together. This inverter, under small signals and in absence of any mismatch, is equivalent to a resistance $1/g_{m6} = 1/g_{m1}$, being g_{m1} the transconductance of the unitary inverter.

As a result, the cascade of inverters SC_5 and SC_6 provides a unitary inverting gain so that the small-signal voltage at the input of the second-stage inverter, SC_2, is

$$g_{m1} \left(r_{o1} \parallel r_{o7}\right) \left(V_i^- - V_i^+\right) \tag{2}$$

To ensure closed loop stability, frequency compensation is provided by adding a Miller capacitor, C_C, from the input of SC_2 to the output of SC_4, resulting in a compensation scheme which is referred to as the Single Miller Capacitor (SMC) [33]–[47]. It has to be noted that capacitors are usually not available in conventional standard-cell libraries adopted in a semi-custom design flow. Therefore, a library of capacitors with all the relevant files has to be derived, starting from the layout cell of the compensation capacitor, by using an approach similar to the one adopted in [6] to implement a capacitors bank for standard-cell based analog filters.

Further details on the OTA design and performance analysis are outside the aim of this work and will be given in a forthcoming publication.

The schematic of the OTA in Fig. 5 has been described in structural Verilog language by instantiating minimum sized inverters taken from the standard-cell library for the *IVx1* cells and using multiple instances in parallel to implement the *IVx2* and *IVx4* cells, and the obtained Verilog netlist is reported in the APPENDIX.

The Verilog netlist has been imported in the Cadence Innovus environment, together with all the technology files needed in the conventional place and route flow usually adopted for digital circuits. A conventional place and route flow (without timing constraints) including design import, floorplanning, place, and routing has then been carried out exploiting the same scripts conventionally adopted to implement digital circuits. These scripts can be easily ported to different technologies by just changing the paths to library files and the name of the standard-cells. The automatically generated layout of the OTA for the 28-nm process is illustrated in Fig. 6, where the Welltap cell needed to access the bulk nets V_{bulkN} and V_{bulkP} on automatically routable layers is highlighted in yellow color. The size of the OTA including the Welltap cell is as low as $3.55\mu m \times 1.2\mu m$ in the 28-nm FDSOI process. It has to be noted that, in a SoC environment, an arbitrary number of analog building blocks implemented by following the above approach can be instantiated. The V_{bulkN} and V_{bulkP} pins of all these analog circuits can be driven by just one ABBG, which allows to accurately set the quiescent current and the static output voltage of all the standard-cells utilized.

IV. TEST CHIP DESIGN AND VALIDATION RESULTS

To provide experimental validation of the proposed biasing approach we designed and fabricated the circuits in Figs. 3, 4, and 5 in a 65-nm triple-well CMOS process supplied by STMicroelectronics. The microphotograph of the 65-nm test chip (which contains also other test circuits which are out of the aim of this work) is reported in Fig. 7. The figure shows also a detailed screenshot of the layout where the four-stage OTA, the compensation capacitor C_C and the ABBG are highlighted. The OTA area occupation is 25 μm $\times$ 8 μm, the area of the compensation capacitor C_C is 12.7 μm $\times$ 8 μm whereas the area of the whole test circuit (including the OTA, the compensation capacitor C_C and the ABBG) is about 48 μm $\times$ 18 μm. The 2.5-V I/O supply rail was exploited for the ABBG implemented with the thicker oxide transistors. Table 1 summarizes transistors dimensions (all with the 280-nm minimum channel length) and bias currents.

The power supply for the standard-cells was set to 0.5 V and transistors dimensions (all with minimum channel length of 65 nm) of the standard-cells composing the OTA and their bias currents are summarized in Table 2. Compensation capacitor C_C was set to 0.5 pF. Preliminarily, the auxiliary amplifiers, A_P and A_N, which are realized as two instances of the same architecture in Fig. 4, were simulated. The DC gain

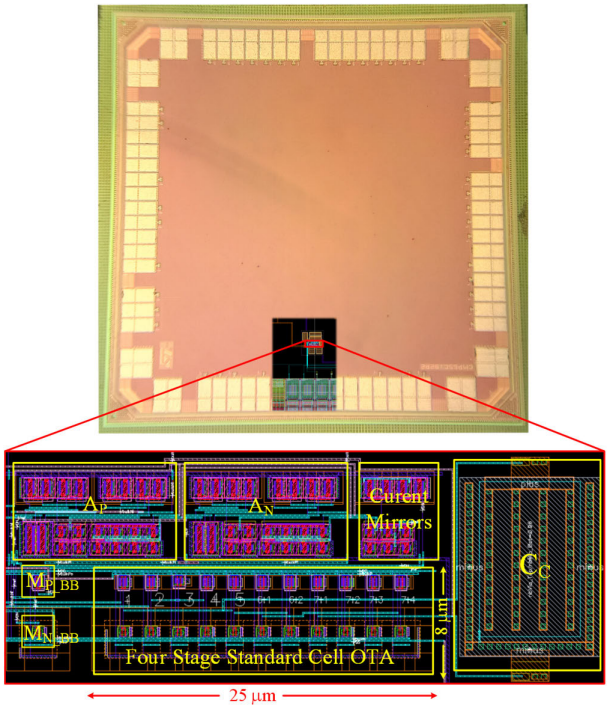

FIGURE 7. Microphotograph of the 65nm test chip and detail of the layout including the four stage OTA, the compensation capacitor Cc and the ABBG circuits.

TABLE 1. Transistors dimensions and bias settings of the Body Bias Generator in Figs. 3-4 (L = 280nm).

Device	W (µm)	Ibias (nA)
M1, M1C, M3,M3C	1	150
M2, M2C, M4,M4C	0.5	150
M6, M6C	0.5	400
M7, M8	2	200
M9, M9C, M10,M10C	1	200
M11, M11C, M12,M12C	1	200
M13, M13C, M14,M14C	0.5	200

TABLE 2. Transistors dimensions and bias settings of the standard-cell based four-stage OTA(L = 65nm).

	Wp (µm)	Wn (µm)	Ibias (nA)	Vin_dc (V)	Vout_dc (V)
1st stage	1.4	0.7	150	0.25	0.25
2nd stage	1.4	0.7	150	0.25	0.25
3rd stage	2x1.4	2x0.7	300	0.25	0.25
4th stage	4x1.4	4x0.7	600	0.25	0.25

was 64 dB, providing sufficient closed-loop accuracy for our aims.

Then, the effectiveness of the biasing approach was tested by evaluating the statistical distribution of the bias current I_{bias} and static output voltage V_O for two instances of the unitary inverter. The first instance has been simulated with V_{bulkP} and V_{bulkN} tied to the positive (0.5 V) and negative (0 V) core supply voltages as usual, and is denoted in the following as "*no ABBG*", whereas the second instance has been tested with V_{bulkP} and V_{bulkN} driven by the proposed ABBG cell, in which I_{REF} and V_{REF} have been set to 150-nA and 250-mV respectively, and is denoted as "*with ABBG*".

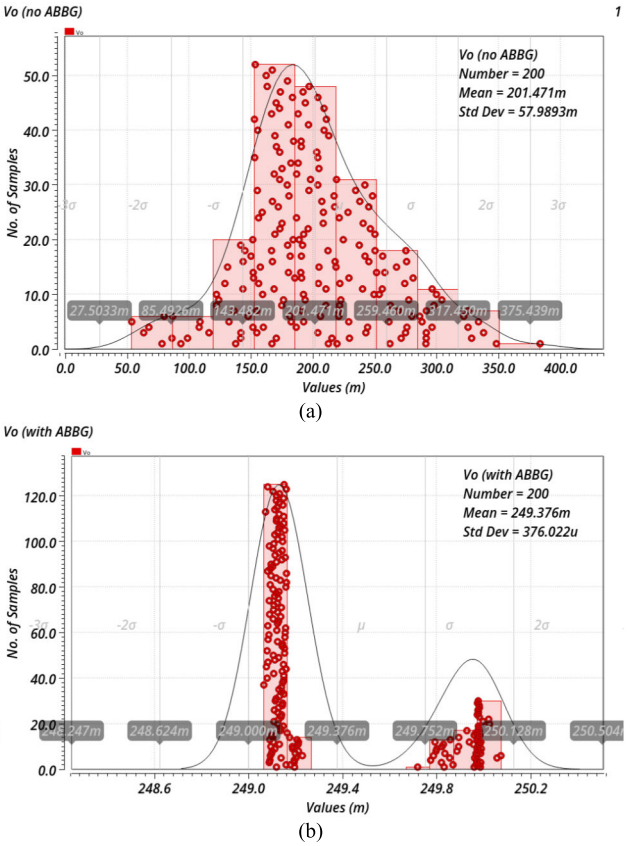

FIGURE 8. Statistical distribution of the static output voltage Vo of the unitary inverter with no ABBG (a) and with ABBG (b).

TABLE 3. Monte carlo simulation results.

Param	Mean	StdDev	Unit
A_0	69.3	7.13	dB
GBW	6.85	2.08	MHz
m_φ	62.1	14.8	Deg.
V_{os}	2.7	19.2	mV
I_{TOT}	1.75	0.41	µA
SR^+	1.48	0.25	V/µs
SR^-	1.53	0.34	V/µs

TABLE 4. Effect of supply voltage and temperature variations.

Parameter						Unit
V_{DD}-V_{SS}	0.45	0.5	0.55	0.5	0.5	V
T	27	27	27	-20	110	°C
A_0	67.9	69.6	70.6	69.4	68.1	dB
GBW	6.65	6.99	7.21	7.58	5.87	MHz
m_φ	61.2	62.8	64.0	61.1	63.2	Deg.
V_{os}	2.2	2.5	2.7	2.1	4.0	mV
I_{TOT}	1.750	1.751	1.752	1.752	1.782	µA
SR^+	1.35	1.72	1.75	1.72	1.55	V/µs
SR^-	1.6	1.69	1.8	1.8	1.45	V/µs

The histograms of the static output voltage V_O for the unitary inverter with "*no ABBG*" and for the one "*with ABBG*" are reported in Fig. 8a and Fig. 8b respectively.

The mean value of V_O *with ABBG* is 249.4 mV with a standard deviation of only 0.4 mV showing how the proposed

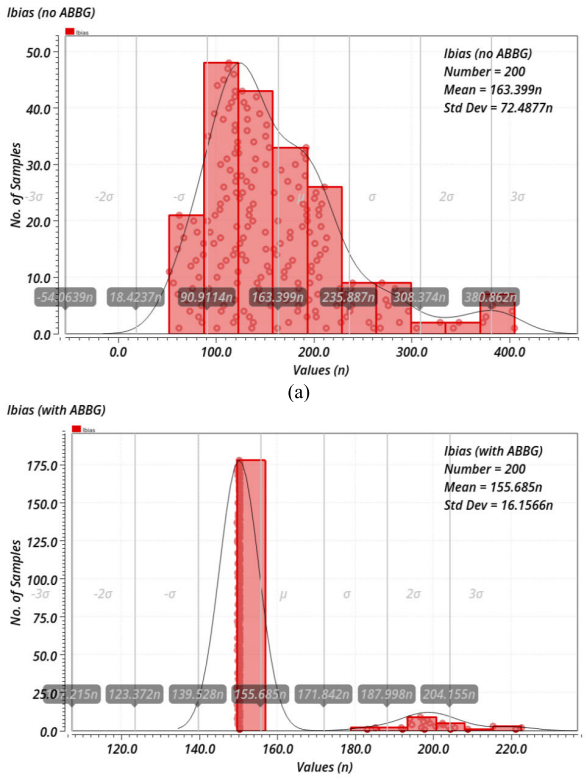

FIGURE 9. Statistical distribution of the bias current I_{bias} of the unitary inverter with no ABBG (a) and with ABBG (b).

biasing strategy allows an excellent capability to set V_O under process variations. The histograms of the bias current, I_{bias}, for the unitary inverter with "*no ABBG*" and for the one "*with ABBG*" are illustrated in Fig. 9a and Fig. 9b, respectively. The mean value of I_{bias} *with ABBG* is 155.7 nA, with a standard deviation of about 16 nA. It is evident that distributions in Fig. 8b and Fig. 9b are not normal. This is probably due to the fact that in some process cases (i.e. Monte Carlo runs) the output of the *ABBG* saturates and the loop partially loses its efficacy. By looking at Fig. 8b, it is evident that this saturation effect is very limited: the static output voltage is always between 249mV and 250mV in all the iterations. A similar effect is present also in Fig. 9b. In this case, the *ABBG* saturation results in higher variation of the bias current for a limited number of extreme process cases. A yield better than 90% for what concerns the accuracy of the bias current is however guaranteed by the proposed technique and implementation.

Table 3 shows mean values and standard deviations of some OTA parameters extracted from 1000 Monte Carlo iterations (process + mismatch). It is seen that the total OTA quiescent current, I_{TOT}, is well-defined with standard deviation as low as 0.41 μA with mean value equal to 1.75 μA. The input equivalent offset is 2.7 mV with standard deviation of 19.2 mV.

The same OTA parameters are also evaluated under different supply and temperature values, as summarized in Table 4. In conclusion, a reasonably good robustness against PVT variations is found.

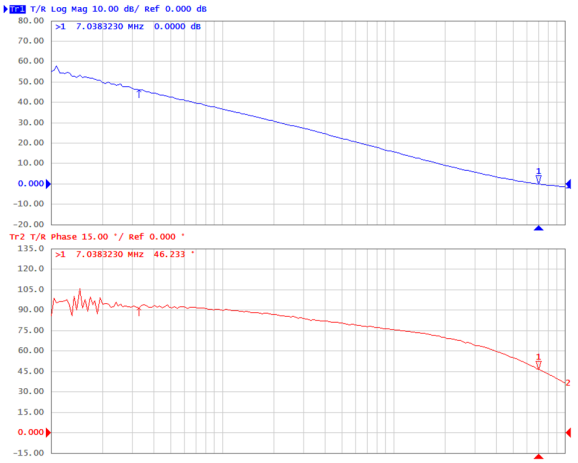

FIGURE 10. Measured frequency response of the implemented standard-cell based OTA.

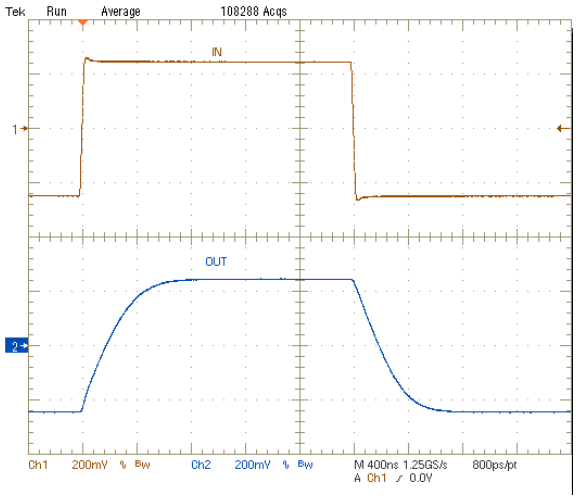

FIGURE 11. Measured time response of the OTA in unity gain non-inverting configuration for a 500mV input pulse.

V. CONCLUSION

The known solutions aimed at implementing analog building blocks starting from digital standard-cell libraries usually lack of suitable control over the quiescent operating point. This exposes the same solutions to large performance variations under PVT changes. This paper presented a biasing technique through the development of and Analog Body Bias Generator, that seems a viable solution towards the design of standard-cell-based analog circuits with well-defined quiescent current ad output voltage. As an example of application, a four-stage fully synthesizable OTA operating under 0.5-V supply was designed in a 65-nm CMOS process and experimentally validated, showing accurate bias point and good stability of its performance parameters.

APPENDIX A
VERILOG NETLIST OF THE STANDARD-CELL OTA IN FIGURE 5

```
module sc_ota(
      input Vip,
      input Vim,
      output Out);
```

```
wire vo1;
wire vo2;
wire vo3;
wire vo5;
IVX4 SC1(.A(Vip),.Z(vo1));
IVX4 SC2(.A(vo1),.Z(vo2));
IVX4 SC3_1(.A(vo2),.Z(vo3));
IVX4 SC3_2(.A(vo2),.Z(vo3));
IVX4 SC4_1(.A(vo3),.Z(Out));
IVX4 SC4_2(.A(vo3),.Z(Out));
IVX4 SC4_3(.A(vo3),.Z(Out));
IVX4 SC4_4(.A(vo3),.Z(Out));
IVX4 SC5(.A(Vim),.Z(vo5));
IVX4 SC6(.A(vo5),.Z(vo5));
IVX4 SC7(.A(vo5),.Z(vo1));
endmodule
```

REFERENCES

[1] A. P. Chandrakasan, N. Verma, and D. C. Daly, "Ultralow-power electronics for biomedical applications," *Annu. Rev. Biomed. Eng.*, vol. 10, no. 1, pp. 247–274, Aug. 2008.

[2] A. Tabesh and L. G. Fréchette, "A low-power stand-alone adaptive circuit for harvesting energy from a piezoelectric micropower generator," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 840–849, Mar. 2010.

[3] M. Alioto, *Enabling the Internet of Things: From Integrated Circuits to Integrated Systems*. Springer 2017.

[4] C. S. Abella, S. Bonina, A. Cucuccio, S. D'Angelo, G. Giustolisi, A. D. Grasso, A. Imbruglia, G. S. Mauro, G. A. M. Nastasi, G. Palumbo, and S. Pennisi, "Autonomous energy-efficient wireless sensor network platform for home/office automation," *IEEE Sensors J.*, vol. 19, no. 9, pp. 3501–3512, May 2019.

[5] X. Jiang, N. P. Ramachandran, D. W. Kang, C. K. Chen, M. Rutherford, Y. Cong, and D. Chang, "Digitally-assisted analog and analog-assisted digital design techniques for a 28 nm mobile system-on-chip," in *Proc. 40th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 475–478.

[6] J. Liu, B. Park, M. Guzman, A. Fahmy, T. Kim, and N. Maghari, "A fully synthesized 77-dB SFDR reprogrammable SRMC filter using digital standard cells," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 6, pp. 1126–1138, Jun. 2018.

[7] S. M. Newton and P. R. Kinget, "A 4th-order analog continuous-time filter designed using standard cells and automatic digital logic design tools," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2016, pp. 297–300.

[8] Y. Guo, J. Jin, X. Liu, and J. Zhou, "An inverter-based continuous time sigma delta ADC with latency-free DAC calibration," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 11, pp. 3630–3642, Nov. 2020.

[9] O. Aiello, P. Crovetti, and M. Alioto, "Standard cell-based ultra-compact DACs in 40-nm CMOS," *IEEE Access*, vol. 7, pp. 126479–126488, 2019.

[10] O. Aiello, P. Crovetti, and M. Alioto, "Fully synthesizable low-area digital-to-analog converter with graceful degradation and dynamic power-resolution scaling," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 8, pp. 2865–2875, Aug. 2019.

[11] P. S. Crovetti, "A digital-based analog differential circuit," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 12, pp. 3107–3116, Dec. 2013.

[12] F. Michel and M. S. J. Steyaert, "A 250 mV 7.5 μW 61 dB SNDR SC $\Delta\Sigma$ modulator using near-threshold-voltage-biased inverter amplifiers in 130 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 709–721, Mar. 2012.

[13] F. M. Yaul and A. P. Chandrakasan, "A noise-efficient 36 nV/$\sqrt{}$Hz chopper amplifier using an inverter-based 0.2-V supply input stage," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 3032–3042, Nov. 2017.

[14] P. Wang and T. Ytterdal, "A 54- μW inverter-based low-noise single-ended to differential VGA for second harmonic ultrasound probes in 65-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 7, pp. 623–627, Jul. 2016.

[15] K. A. Ng and Y. P. Xu, "A low-power, high CMRR neural amplifier system employing CMOS inverter-based OTAs with CMFB through supply rails," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 724–737, Mar. 2016.

[16] D. Golanski and P. Fonteneau, "First demonstration of a full 28 nm high-K/metal gate circuit transfer from Bulk to UTBB FDSOI technology through hybrid integration," in *Proc. Symp. VLSI Circuits*, Jun. 2013, pp. 124–125.

[17] R. Carter, J. Mazurier, L. Pirro, and J. U. Sachse, "22 nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications," in *IEDM Tech. Dig.*, Dec. 2016, pp. 1–4.

[18] A. Quelen, G. Pillonnet, P. Flatresse, and E. Beigné, "A 2.5μW 0.0067 mm^2 automatic back-biasing compensation unit achieving 50% leakage reduction in FDSOI 28 nm over 0.35-to-1V V_{DD} range," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 304–306.

[19] M. Blagojevic, M. Cochet, B. Keller, P. Flatresse, A. Vladimirescu, and B. Nikolic, "A fast, flexible, positive and negative adaptive body-bias generator in 28 nm FDSOI," in *Proc. IEEE Symp. VLSI Circuits (VLSI-Circuits)*, Jun. 2016, pp. 1–2.

[20] S. Hoppner, H. Eisenreich, D. Walter, A. Scharfe, A. Oefelein, F. Schraut, J. Schreiter, T. Riedel, H. Bauer, R. Niebsch, S. Scherzer, T. Hocker, S. Scholze, S. Henker, M. Nossmann, U. Hensel, and H. Prengel, "Adaptive body bias aware implementation for ultra-low-voltage designs in 22 FDX technology," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 10, pp. 2159–2163, Oct. 2020.

[21] A. Siddiqi, N. Jain, and M. Rashed, "Back-bias generator for post-fabrication threshold voltage tuning applications in 22 nm FD-SOI process," in *Proc. 19th Int. Symp. Quality Electron. Design (ISQED)*, Mar. 2018, pp. 268–273.

[22] N. Kamae, A. Tsuchiya, and H. Onodera, "A body bias generator compatible with cell-based design flow for within-die variability compensation," in *Proc. IEEE Asian Solid State Circuits Conf. (A-SSCC)*, Nov. 2012, pp. 389–392.

[23] J. W. Tschanz, J. T. Kao, S. G. Narendra, R. Nair, D. A. Antoniadis, A. P. Chandrakasan, and V. De, "Adaptive body bias for reducing impacts of die-to-die and within-die parameter variations on microprocessor frequency and leakage," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1396–1402, Nov. 2002.

[24] S. H. Tang, D. Somasekhar, J. W. Tschanz, and V. K. De, "Wide-range local bias generator for body bias grid," U.S. Patent 6 784 722, Apr. 15, 2004.

[25] M. Meijer, J. P. de Gyvez, B. Kup, B. van Uden, P. Bastiaansen, M. Lammers, and M. Vertregt, "A forward body bias generator for digital CMOS circuits with supply voltage scaling," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2010, pp. 2482–2485.

[26] S. Perisetty, "Integrated circuits with adjustable body bias and power supply circuitry," U.S. Patent 7 675 317, Mar. 9, 2010.

[27] N. Kamae, A. K. M. Mahfuzul Islam, A. Tsuchiya, and H. Onodera, "A body bias generator with wide supply-range down to threshold voltage for within-die variability compensation," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2014, pp. 53–56.

[28] N. Kamae, A. Tsuchiya, and H. Onodera, "An area effective forward/reverse body bias generator for within-die variability compensation," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2011, pp. 217–220.

[29] D. Ruscio, F. Centurelli, P. Monsurro, and A. Trifiletti, "Reconfigurable low voltage inverter-based sample-and-hold amplifier," in *Proc. 13th Conf. Ph.D. Res. Microelectron. Electron. (PRIME)*, Jun. 2017, pp. 133–136.

[30] P. Monsurró, G. Scotti, A. Trifiletti, and S. Pennisi, "Biasing technique via bulk terminal for minimum supply CMOS amplifiers," *Electron. Lett.*, vol. 41, no. 14, pp. 779–780, Jul. 2005.

[31] P. Monsurró, S. Pennisi, G. Scotti, and A. Trifiletti, "Exploiting the body of MOS devices for high performance analog design," *IEEE Circuits Syst. Mag.*, vol. 11, no. 4, pp. 8–23, 4th Quart., 2011.

[32] A. Ballo, S. Pennisi, and G. Scotti, "0.5 V CMOS inverter-based transconductance amplifier with quiescent current control," *J. Low Power Electron. Appl.*, vol. 11, no. 4, p. 37, Dec. 2021.

[33] K. N. Leung, P. K. T. Mok, W.-H. Ki, and J. K. O. Sin, "Three-stage large capacitive load amplifier with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 221–230, Feb. 2000.

[34] X. Fan, C. Mishra, and E. Sánchez-Sinencio, "Single Miller capacitor frequency compensation technique for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 584–592, Mar. 2005.

[35] S. O. Cannizzaro, A. D. Grasso, G. Palumbo, and S. Pennisi, "Single Miller capacitor frequency compensation with nulling resistor for three-stage amplifiers," *Int. J. Circuit Theory Appl.*, vol. 36, no. 7, pp. 825–837, Oct. 2008.

[36] S. Guo and H. Lee, "Single-capacitor active-feedback compensation for small-capacitive-load three-stage amplifiers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 10, pp. 758–762, Oct. 2009.
[37] X. Peng, W. Sansen, L. Hou, J. Wang, and W. Wu, "Impedance adapting compensation for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 445–451, Feb. 2011.
[38] S. Guo and H. Lee, "Dual active-capacitive-feedback compensation for low-power large-capacitive-load three-stage amplifiers," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 452–464, Feb. 2011.
[39] S. S. Chong and P. K. Chan, "Cross feedforward cascode compensation for low-power three-stage amplifier with large capacitive load," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2227–2234, Sep. 2012.
[40] Z. Yan, P. I. Mak, M. K. Law, and R. P. Martins, "Ultra-area-efficient three-stage amplifier using current buffer Miller compensation and parallel compensation," *Electron. Lett.*, vol. 48, no. 11, pp. 624–626, May 2012.
[41] L. Zhang, Z. Chang, Y. Wang, and Z. Yu, "Current-reuse single Miller feedforward compensation for multi-stage amplifiers," *Electron. Lett.*, vol. 49, no. 2, pp. 94–96, Jan. 2013.
[42] Z. Yan, P.-I. Mak, M.-K. Lau, and R. P. Martins, "A 0.016-mm^2 144-μ W three-stage amplifier capable of driving 1-to-15 nF capacitive load with >0.95-MHz GBW," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 527–540, Feb. 2013.
[43] M. Tan and W.-H. Ki, "A cascode Miller-compensated three-stage amplifier with local impedance attenuation for optimized complex-pole control," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 440–449, Feb. 2015.
[44] A. D. Grasso, G. Palumbo, and S. Pennisi, "High-performance four-stage CMOS OTA suitable for large capacitive loads," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 10, pp. 2476–2487, Oct. 2015.
[45] D. Marano, A. D. Grasso, G. Palumbo, and S. Pennisi, "Optimized active single-Miller capacitor compensation with inner half-feedforward stage for very high-load three-stage OTAs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 9, pp. 1349–1359, Sep. 2016.
[46] W. Qu, S. Singh, Y. Lee, Y. S. Son, and G. H. Cho, "Design-oriented analysis for Miller compensation and its application to multistage amplifier design," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 517–527, Feb. 2017.
[47] A. D. Grasso, D. Marano, G. Palumbo, and S. Pennisi, "High-performance three-stage single-Miller CMOS OTA with no upper limit of C_L," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 11, pp. 1529–1533, Nov. 2018.

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