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Transformerless Quadruple High Step-Up DC/DC Converter Using Coupled Inductors

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ABSTRACT This paper proposes a high voltage step-up DC/DC converter by combining a coupled inductor and a voltage multiplier rectifier. The input side of the proposed converter operates in an interleaved manner with two coupled inductors connected in parallel, and the output side is composed of a voltage multiplier rectifier where two voltage doubler rectifiers are merged in series. By changing the turns ratio of the coupled inductor of the proposed converter, the voltage gain can be increased, and additional voltage gain can be obtained by combining it with a voltage multiplier rectifier. Due to the passive lossless clamping performance of the proposed method, it is possible to recycle the leakage inductance energy of the coupled inductor and voltage stress reduction can be achieved along with zero current turn–ON and turn–OFF of switches and diodes. Finally, this paper evaluates the effectiveness and practicality of the proposed method by operating a prototype circuit with an input voltage of 20V, an output voltage of 400V, and an output power of 320W. The maximum efficiency of the proposed converter is 97.2% and the efficiency at maximum power is 94.1%.

INDEX TERMS DC/DC converter, high step-up, coupled inductor, voltage multiplier rectifier.

I. INTRODUCTION

Today, global energy (coal, oil) is rapidly depleting, and due to the effects of global warming, many countries are concentrating on research on solar, wind, and fuel cell energy [1]–[5]. In general, these renewable energies belong to low-voltage and high-current power supplies, which require a high step-up converter in the front-end stage circuit of the application [6]. The high step-up DC/DC converter requires high power density and efficiency as well as high voltage gain. The conventional boost converters are widely used due to high efficiency and simple structure. When the voltage gain of the conventional boost converter increases, the parasitic resistance component limits the voltage gain and causes serious loss [7]. In high output voltage applications, high voltage stress on switches and diodes deteriorates device performance, causing severe hard switching losses, conduction losses, and reverse recovery issues [8]–[10]. Therefore, in high step-up DC/DC applications, voltage stress must be spread across the devices by reducing the duty cycle and using devices with low voltage stress.

The isolated fly-back DC/DC converter is a commonly used topology with a simple structure that can increases voltage gain and has electrically insulating performance. The voltage stress of the semiconductor device is usually high due to the leakage inductance of the transformer. Several methods to recycle the leakage inductance energy of a transformer and to lower the voltage stress of a semiconductor device have been proposed in the literature [11], [12]. Nevertheless, the isolated fly-back DC/DC converter requires a large transformer to obtain a high voltage gain, and there is a problem in that the conduction loss increases by flowing a large input current and current ripple through a single switch. Interleaved DC/DC converters have been proposed for high power and high efficiency applications, which can reduce the input current ripple and overall size of the system. The interleaved coupled inductor DC/DC converter not only has the advantages of interleaved technology, but also recycles the leakage inductor energy of the coupled inductor to the output side and achieves a high voltage gain by using the turns ratio [13]–[18].

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The derivation procedure of the proposed high step-up converter is shown in Fig. 1, and the three technologies are merged. Fig. 1(a) depicts a boost converter with conventional interleaved technology, which reduces the input current ripple and increases the effective switching frequency [19]. It features easy equipment selection, good transient response, easy thermal management and low conduction losses. Fig. 1(b) illustrates a high step-up converter that combines a flyback converter with a coupled inductor and an output-side stacked type [20]. It is possible to increase the voltage gain and efficiency of the coupled inductor by using the turns ratio and leakage inductance energy. However, high step-up converters have large input current ripple under increasing conduction losses and they are not suitable for high power applications. Fig. 1(c) shows a voltage multiplier rectifier (VMR) composed of a diode and a capacitor [21]. The VMR can double the voltage gain and it reduces the voltage stress of the diode and the voltage of the capacitor by one-half. Also, quadrupler type voltage rectifiers are being studied by increasing the VMR by an even multiple. However, excessive doubling of the VMR leads to the problems of increased power loss, cost, and circuit size.

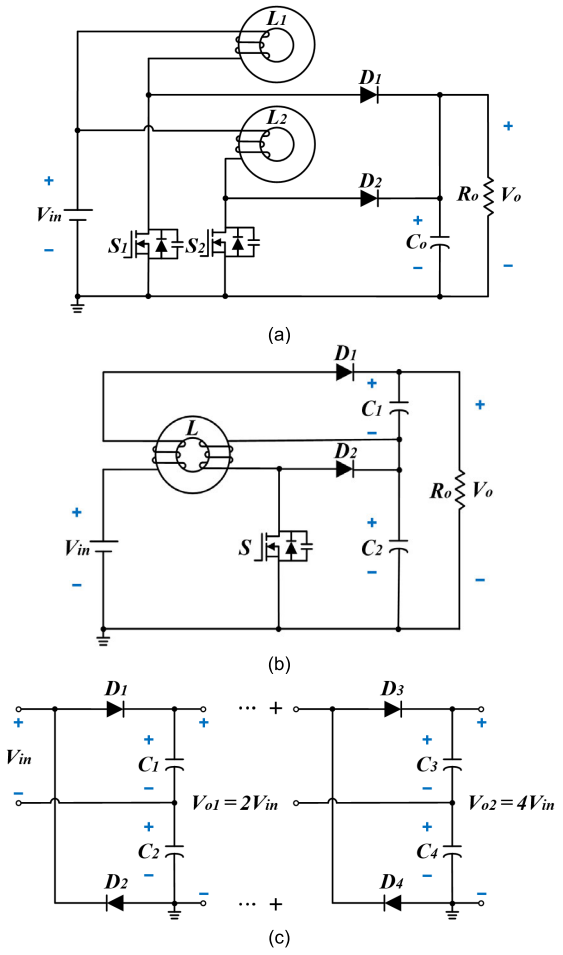

FIGURE 1. Derivation of the proposed high step-up DC/DC converter. (a) Interleaved boost converter [19]. (b) Stacked coupled inductor boost converter [20]. (c) Voltage multiplier rectifier [21].

In transformerless DC/DC converters, voltage gain can be increased by combining voltage multiplier cells (VMC) [22]–[24]. In addition, a voltage gain may be increased by increasing the number of VMC, and voltage stress of a semiconductor device may be reduced through voltage clamping performance. However, the higher the number of VMC, the higher the number of components, the complexity of the circuit configuration, and the overall cost of the converter. In addition, this type of converter still has problems with hard switching of semiconductor devices.

A high step-up converter that combines a coupled inductor and VMC not only achieves a high voltage gain, but also extends the additional voltage gain by increasing the turns ratio [25]–[29]. The magnetizing inductor of a coupled inductor is charged when the power switch is in the ON state, and the stored energy supplies the circuit when the switch is in the OFF state. In addition, the leakage inductor of the coupled inductor can greatly reduce the switching loss and solve the reverse current recovery problem by implementing Zero Current Switching (ZCS) turn–ON of the power MOSFETs and ZCS turn–OFF of the diodes.

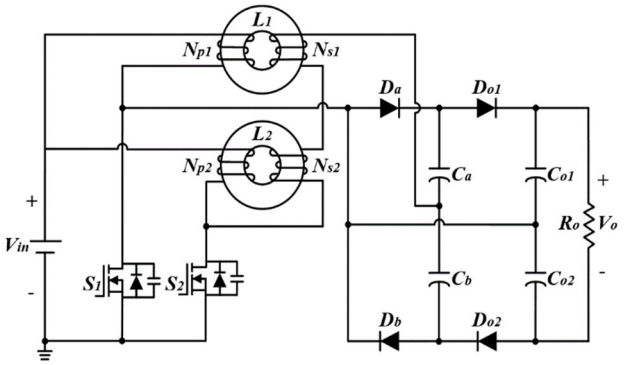

FIGURE 2. Proposed high step-up DC/DC converter.

This paper proposes a transformerless type high step-up DC/DC converter based on the interleaved method on the input side and the stack method on the output. The interleaved method can reduce the input current ripple while increasing the power level, and the stack method has the advantage of increasing the voltage gain through charging or discharging in mode. Fig. 2 portrays the circuit configuration of the proposed high step-up converter. On the input side, two coupled inductor methods are connected in parallel, and the output side is connected with a quadrupler method in which two voltage multiplier rectifiers are connected in series. The coupled inductor method can effectively use the core and increase the voltage gain by increasing the turns ratio. The quadrupler lossless clamping performance is combined with the coupled inductor, and the leakage inductor can realize ZCS turn–ON of power MOSFETs and ZCS turn–OFF of diodes, and lower the voltage stress of switches and diodes by clamping the voltage.

With the construction of this paper, the operating principle is described in Section II, and steady-state performance

analysis is performed in Section III. Design considerations and simulation and experimental results are provided in Section IV. Conclusions are given in Section V.

II. OPERATING PRINCIPLES OF THE PROPOSED HIGH-STEP DC/DC CONVERTER

Fig. 3 shows the equivalent circuit diagram of the proposed high step-up converter. Fig. 4 illustrates the input and output voltage/current of the proposed circuit as well as the switch and diode current directions (V_{in}, I_{in}, V_o, I_o, i_{S1}, i_{S2}, i_{Da}, i_{Db}, i_{Do1}, i_{Do2}). The coupled inductors (L_1, L_2) are connected in parallel with the input side, and they are divided into magnetizing inductors (L_{m1}, L_{m2}), leakage inductors (L_{k1}, L_{k2}, L_s), primary windings (N_{p1}, N_{p2}), and secondary windings (N_{s1}, N_{s2}). The quadrupler VMR consists of diodes (D_a, D_b, D_{o1}, D_{o2}) and capacitors (C_a, C_b, C_{o1}, C_{o2}), which are connected in series with the output side.

The proposed high step-up converter operates in continuous conduction mode (CCM) and the leakage inductance has a value greater than zero. The duty cycle (D) of the switches is greater than 0.5 and are interleaved with a 180 degree phase shift. In addition, the following conditions were used to simplify the circuit operation principle.1) The resistance component of active and passive elements is ignored and the parasitic capacitance of the switches (S_1, S_2) is considered. 2) The capacitors (C_a, C_b, C_{o1}, C_{o2}) are large enough. Therefore, the capacitor voltage is considered constant over the switching period (T_s). 3) The leakage inductors (L_{k1}, L_{k2}, L_s), of the coupled inductors (L_1, L_2) are considered with the turns ratio $N = N_{p1}/N_{s1} = N_{p2}/N_{s2}$.

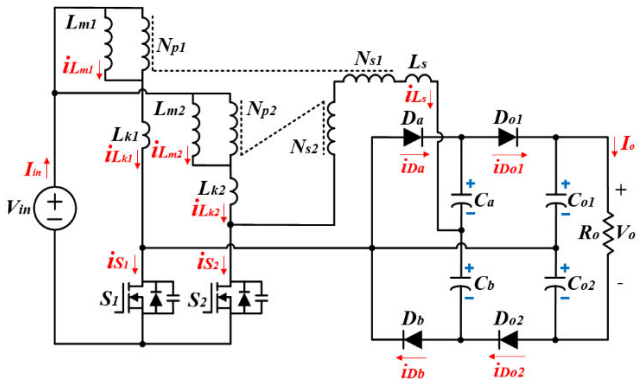

FIGURE 3. Equivalent circuit of proposed high step-up converter.

1) Mode 1 [$t_0 - t_1$]: At $t = t_0$, the switch (S_2) remains ON and the switch (S_1) is turned–ON. The diodes (D_a, D_{o2}) remain reverse-biased, as illustrated in Fig. 5(a). The primary side leakage inductor (L_{k1}, L_{k2}) of the coupled inductors (L_1, L_2) increases or decreases, and the secondary side leakage inductor (L_s) decreases. The current in the primary side leakage inductor (L_{k1}) is gradually increased so that the switch (S_1) current is zero current switch turned–ON. The diodes (D_a, D_{o2}) current can alleviate the reverse recovery problem because the current of the secondary side leakage inductor (L_s) is linearly reduced. This mode ends when the secondary side leakage inductor (L_s) current gradually decreases to zero.

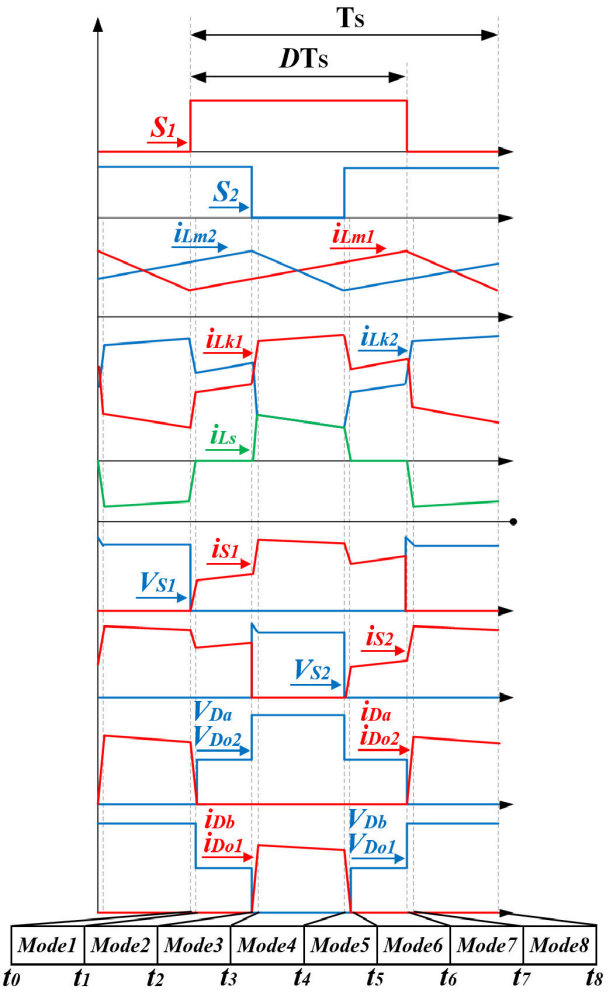

FIGURE 4. Key waveforms by voltage and current of the proposed high step-up converter, [$L_{k1} = L_{k2} > 0$].

2) Mode 2 [$t_1 - t_2$]: At $t = t_1$, this mode is started. The switches (S_1, S_2) are ON-state and the diodes (D_a, D_b, D_{o1}, D_{o2}) are in reverse bias state, as described in Fig. 5(b). In this mode, since the secondary side of the coupled inductors (L_1, L_2) are connected in the opposite direction, the energy is not transferred the current of the magnetizing inductor, leakage inductor, and switches (S_1, S_2) increases linearly with the input voltage (V_{in}). Also, the voltage of each diode is equal to the clamping voltage charged in each capacitor.

$$i_{Lm1}(t) = i_{Lk1}(t) = i_{S1}(t) = I_{Lm1}(t_1) + \frac{V_{in}}{L_1}(t - t_1) \quad (1)$$

$$i_{Lm2}(t) = i_{Lk2}(t) = i_{S2}(t) = I_{Lm2}(t_1) + \frac{V_{in}}{L_2}(t - t_1) \quad (2)$$

$$V_{Da} = V_{Db} = V_{Do1} = V_{Do2} = V_{Ca} = V_{Cb},$$
$$V_{Co1} = V_{Co2} = V_o. \quad (3)$$

3) Mode 3 [$t_2 - t_3$]: At $t = t_2$, this mode started. The switch (S_2) is turned–ON and the diodes (D_b, D_{o1}) are changed to a

forward bias state as illustrated in Fig. 5(c). The energy of the magnetizing inductor (L_{m1}) is continuously supplied by the input voltage (V_{in}), and the stored energy in the magnetizing inductor (L_{m2}) gradually decreases through three paths. The first path is $L_{m2} \rightarrow L_{k2} \rightarrow S_2$, which releases energy into the parasitic capacitor of the switch (S_2). The second and third paths are $L_{m2} \rightarrow L_{k2} \rightarrow N_{s2} \rightarrow N_{s1} \rightarrow L_s \rightarrow C_a \rightarrow D_{o1} \rightarrow C_{o1}$ and $L_{m2} \rightarrow L_{k2} \rightarrow N_{S2} \rightarrow N_{s1} \rightarrow L_s \rightarrow C_b \rightarrow D_b$. Along the two paths, the energy is charged in parallel to the capacitors (C_{o1}, C_b), respectively.

$$i_{S1}(t) = i_{Lm1}(t) + i_{Ls}(t) + i_{Db}(t) + i_{Do1}(t) \tag{4}$$
$$i_{Lk1}(t) = i_{Lm1}(t) + i_{Ls}(t), \quad V_{Da} = V_{Do2} = V_{Co2}. \tag{5}$$

4) Mode 4 [$t_3 - t_4$]: At $t = t_3$, this mode is started. The switch (S_1) is ON and the switch (S_2) is OFF, as given in Fig. 5(d). The primary and secondary sides of the coupled inductor (L_2) and the secondary side of the coupled inductor (L_1) are connected in series with the input voltage (V_{in}) to charge the capacitors (C_b, C_{o1}). Therefore, the currents of the diode (D_{o1}) including the primary side leakage inductor (L_{k2}) and the secondary side leakage inductor (L_s) of the coupled inductor gradually decrease.

5) Mode 5 [$t_4 - t_5$]: At $t = t_4$, the switch (S_1) remains ON and the switch (S_2) is turned–ON. The diodes (D_a, D_{Do2}) remain reverse-biased, as depicted in Fig. 5(e). The primary side leakage inductor (L_{k1}, L_{k2}) of the coupled inductors (L_1, L_2) increases or decreases, and the secondary side leakage inductor (L_s) decreases. The current in the primary side leakage inductor (L_{k2}) is gradually increased so that the switch (S_2) current is zero current switch turned–ON. The diode current can alleviate the reverse recovery problem because the current of the secondary side leakage inductor (L_s) is linearly reduced. This mode ends when the leakage inductor (L_s) current gradually decreases to zero.

6) Mode 6 [$t_5 - t_6$]: At $t = t_5$, the switches (S_1, S_2) are ON and the diodes (D_a, D_b, D_{o1}, D_{o2}) are reverse biased. This mode operates the same as *Mode 2* and it is sketched in Fig. 5(b).

7) Mode 7 [$t_6 - t_7$]: At $t = t_6$, this mode started. The switch (S_1) is turned–OFF and the diodes (D_a, D_{o2}) are changed to a forward bias state as given in Fig. 5(f). The energy of the magnetizing inductor (L_{m1}) is stored by the input voltage (V_{in}), and the energy in the magnetizing inductor (L_{m2}) diminishes through three paths. The first path is $L_{m1} \rightarrow L_{k1} \rightarrow S_1$, which releases energy into the parasitic capacitor of the switch (S_1). The second and third paths are $L_{m1} \rightarrow L_{k1} \rightarrow D_a \rightarrow C_a \rightarrow L_s \rightarrow N_{s1} \rightarrow N_{s2} \rightarrow S_2$ and $L_{m1} \rightarrow L_{k1} \rightarrow C_{o2} \rightarrow D_{o2} \rightarrow C_b \rightarrow L_s \rightarrow N_{s1} \rightarrow N_{s2} \rightarrow S_2$. Along the two paths, the energy is charged in parallel to the capacitors (C_a, C_{o2}).

$$i_{S2}(t) = i_{Lm2}(t) - i_{Ls}(t) + i_{Da}(t) + i_{Do2}(t) \tag{6}$$
$$i_{Lk2}(t) = i_{Lm2}(t) - i_{Ls}(t), \quad V_{Db} = V_{Do1} = V_{Co1}. \tag{7}$$

8) Mode 8 [$t_7 - t_8$]: At $t = t_7$, this mode is started. The switch (S_2) is ON and the switch (S_1) is OFF, as shown in Fig. 5(g). The primary and secondary sides of the coupled inductor (L_1) and the secondary side of the coupled inductor (L_2) are connected in series with the input voltage (V_{in}) to charge the capacitors (C_a, C_{o2}). Therefore, the currents of the diode (D_{o2}) including the primary side leakage inductor (L_{k1}) and the secondary side leakage inductor (L_s) of the coupled inductor gradually decrease.

III. STEADY-STATE PERFORMANCE ANALYSIS OF THE PROPOSED HIGH STEP-UP DC/DC CONVERTER

A. HIGH STEP-UP GAIN

In this chapter, the steady-state analysis (*Mode 1*, *Mode 2*, *Mode 3*, *Mode 4*) is simplified by ignoring the leakage inducor ($L_{k1} = L_{k2} = L_s \approx 0$) of the proposed converter, and these key waveforms are depicted in Fig. 6. In addition, since *Mode 1* and *Mode 3* have the same operating mode, the current flow is as illustrated in Fig. 7. The period in which the switches (S_1, S_2) are ON is represented by the primary (N_{p1}, N_{p2}) and secondary (N_{s1}, N_{s2}) voltages of the coupled inductors.

$$\frac{L_{m1}}{L_{m1} + L_{k1}} V_{in} = \frac{L_{m2}}{L_{m2} + L_{k2}} V_{in} = kV_{in} \tag{8}$$
$$V_{Lk1}^{Mode1,3} = V_{Lk2}^{Mode1,3} = (1-k)V_{in} \tag{9}$$
$$V_{Np1}^{Mode1,3} = V_{Np2}^{Mode1,3} = kV_{in} \tag{10}$$
$$V_{Ns1}^{Mode1,3} = V_{Ns2}^{Mode1,3} = kNV_{in}. \tag{11}$$

By applying voltage-second balance, the primary (N_{p1}, N_{p2}) and secondary (N_{s1}, N_{s2}) voltages of the coupled inductors can be obtained in the period when the switches (S_1, S_2) are OFF, as given in Fig. 7(a).

$$\int_0^{DT_s} V_{Lk1}^{Mode1} dt + \int_{DT_s}^{T_s} V_{Lk1}^{Mode4} dt = 0 \tag{12}$$
$$\int_0^{DT_s} V_{Np1}^{Mode1} dt + \int_{DT_s}^{T_s} V_{Np1}^{Mode4} dt = 0 \tag{13}$$
$$\int_0^{DT_s} V_{Ns1}^{Mode1} dt + \int_{DT_s}^{T_s} V_{Ns1}^{Mode4} dt = 0 \tag{14}$$
$$V_{Lk1}^{Mode4} = V_{Lk2}^{Mode1} = -\frac{(1-k)D}{1-D} V_{in} \tag{15}$$
$$V_{Np1}^{Mode4} = V_{Np2}^{Mode2} = -\frac{kD}{1-D} V_{in} \tag{16}$$
$$V_{Ns1}^{Mode4} = V_{Ns2}^{Mode2} = -\frac{kND}{1-D} V_{in}. \tag{17}$$

Fig. 7(b) shows that the capacitor (C_b) is charged via $V_{in} - N_{p2} - N_{s2} - N_{s1} - C_b$. And the followings can be obtained

$$V_{Cb} = V_{in} - V_{Np2}^{Mode2} - V_{Lk2}^{Mode2} - V_{Ns2}^{Mode2} + V_{Ns1}^{Mode2} \tag{18}$$
$$V_{Cb} = \frac{1+kN}{1-D} V_{in}. \tag{19}$$

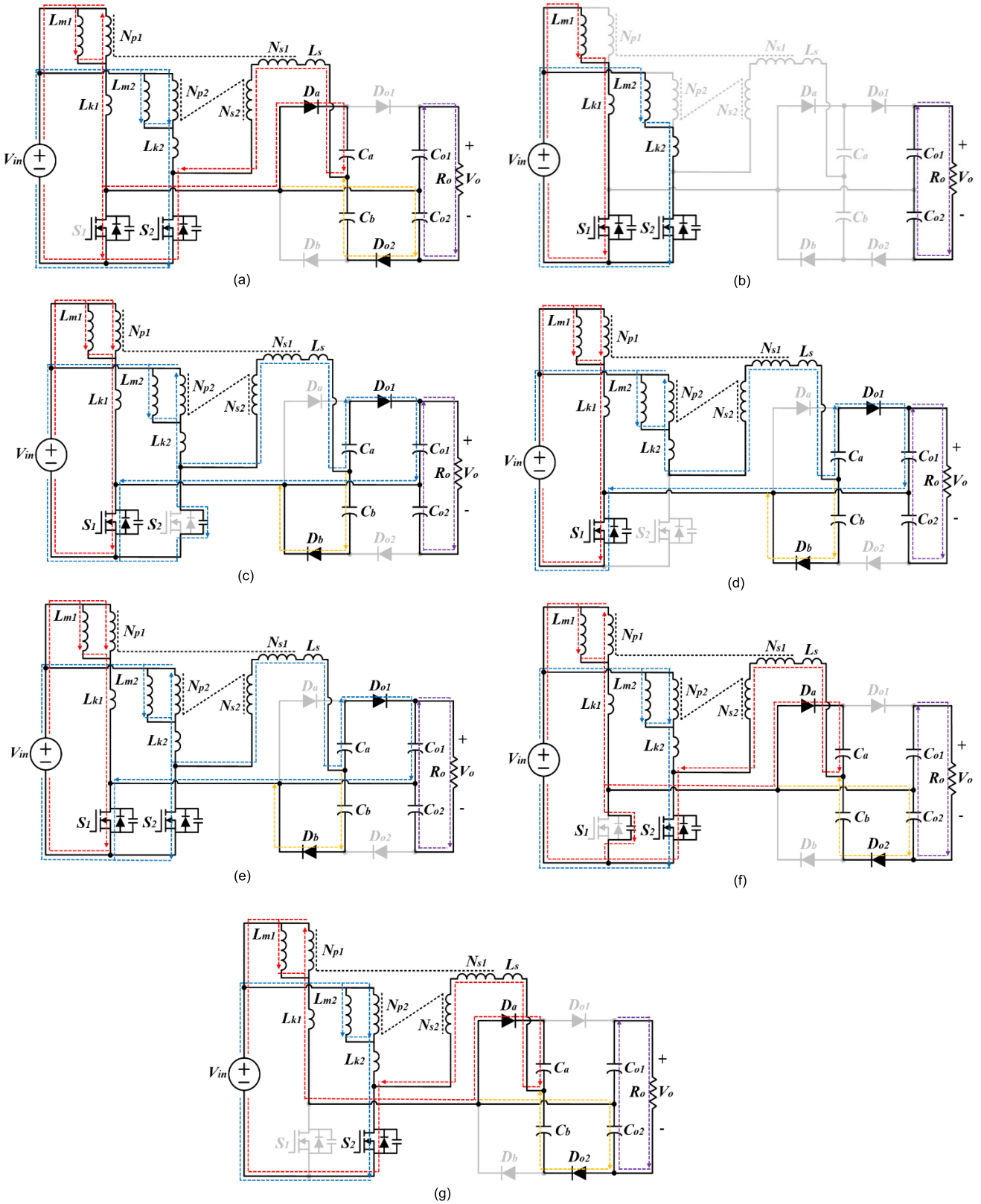

FIGURE 5. Operating mode by current flow of the proposed high step-up converter, [$L_{k1} = L_{k2} > 0$]. (a) *Mode 1*. (b) *Mode 2*. *Mode 6*. (c) *Mode 3*. (d) *Mode 4*. (e) *Mode 5*. (f) *Mode 7*. (g) *Mode 8*.

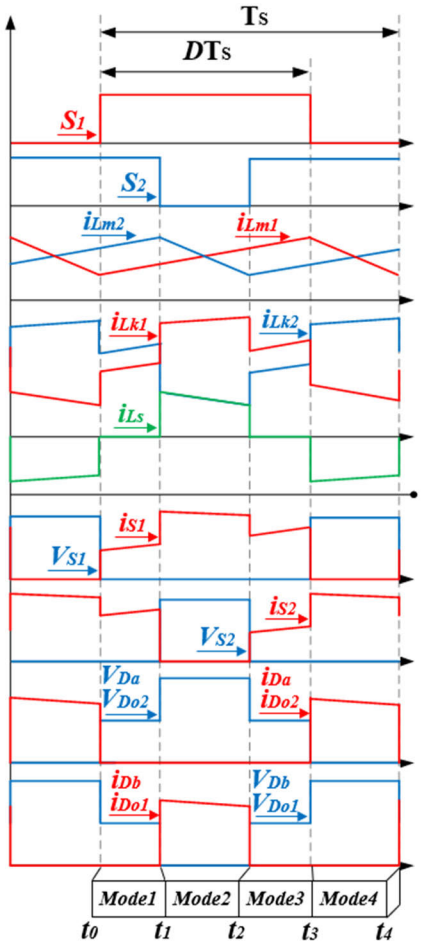

FIGURE 6. Key waveforms by voltage and current of the proposed high step-up converter, [$L_{k1} = L_{k2} \approx 0$].

Fig. 7(c) implies that the capacitor (C_a) is charged via $V_{in} - N_{p1} - N_{s1} - N_{s2} - C_a$ and the following equations are satisfied

$$V_{Ca} = V_{in} - V_{Np1}^{Mode4} - V_{Lk1}^{Mode4} - V_{Ns1}^{Mode4} + V_{Ns2}^{Mode4} \quad (20)$$

$$V_{Ca} = V_{Cb} = \frac{1 + kN}{1 - D} V_{in}. \quad (21)$$

The charged power of the two series-connected capacitors (C_{o1}, C_{o2}) is discharged through the load resistor (R_o) on the output side. Thus, the followings can be easily derived:

$$V_{Co1} = V_{in} - V_{Np2}^{Mode2} - V_{Lk2}^{Mode2} - V_{Ns2}^{Mode2} + V_{Ns1}^{Mode2} + V_{Cb} \quad (22)$$

$$V_{Co2} = V_{in} - V_{Np1}^{Mode4} - V_{Lk1}^{Mode4} - V_{Ns1}^{Mode4} + V_{Ns2}^{Mode4} + V_{Ca} \quad (23)$$

$$V_{Co1} = V_{Co2} = \frac{2 + 2kN}{1 - D} V_{in} \quad (24)$$

$$V_o = V_{Co1} + V_{Co2} = \frac{4 + 4kN}{1 - D} V_{in}. \quad (25)$$

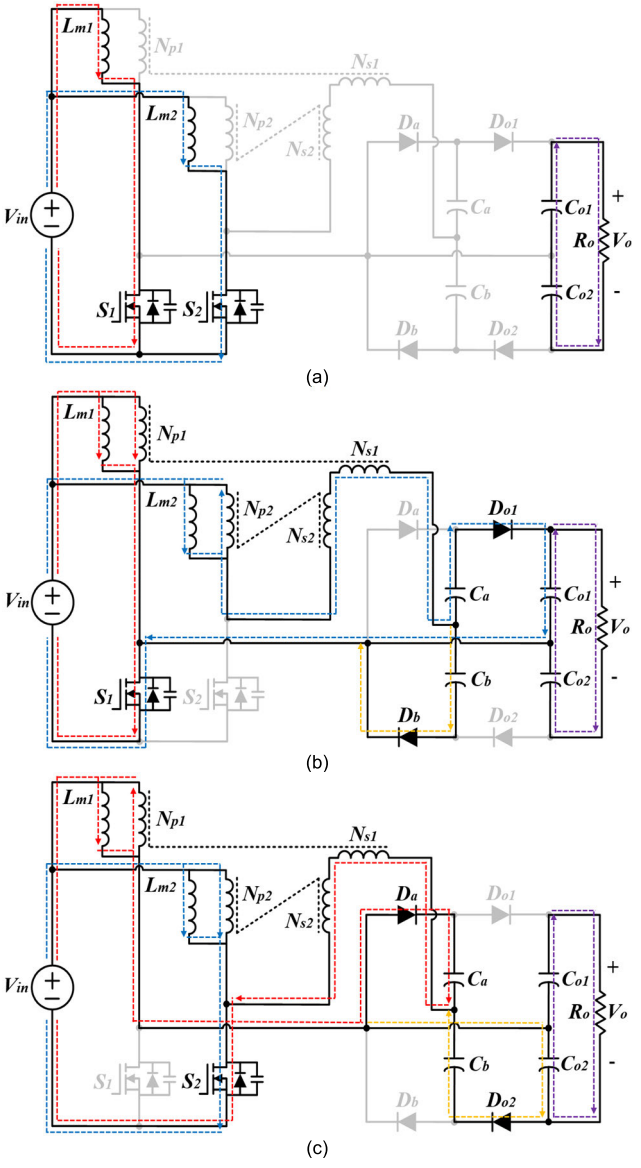

FIGURE 7. Operating mode by current flow of the proposed high step-up converter, [$L_{k1} = L_{k2} \approx 0$]. (a) *Mode 1. Mode 3.* (b) *Mode 2.* (c) *Mode 4.*

After all, the voltage gain (M) of the proposed converter can be represented as follows:

$$\therefore M = \frac{V_o}{V_{in}} = \frac{4 + 4kN}{1 - D} = \frac{4 + 4N}{1 - D}\Big|_{k=1}. \quad (26)$$

Fig. 8 depicts the proposed high step-up voltage gain (M) according to (26). It should be noted that the proposed high step-up converter can obtain twenty times higher voltage gain (M) when $D = 0.6$ and $N = 1$, and higher voltage gain (M) can be obtained by increasing turns ratio (N).

B. VOLTAGE STRESS

The voltage stress of the switches (S_1, S_2) is low compared to the output voltage (V_o), and it becomes even lower when the turns ratio (N) of the coupled inductors is increased.

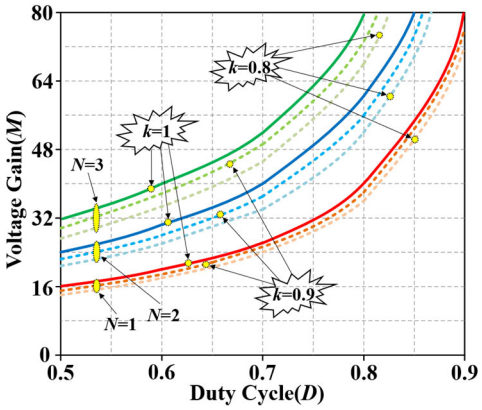

FIGURE 8. High step-up voltage gain (*M*) vs Duty cycle (*D*) and Turns ratio (*N*), [$k = 0.8 \sim 1$].

The proposed converter has a characteristic that the voltage stress of the switches (S_1, S_2) is lowered when the voltage gain (M) is increased.

$$V_{S1} = V_{S2} = \frac{1}{1-D} V_{in} = \frac{1}{4+4N} V_o. \tag{27}$$

The voltage stress of the diodes (D_a, D_b, D_{o1}, D_{o2}) is maintained at half the output voltage (V_o) regardless of the turns ratio (N).

$$V_{Da} = V_{Db} = V_{Do1} = V_{Do2} = V_{Ca} + V_{Cb} = \frac{2+2N}{4+4N} V_o = \frac{V_o}{2}. \tag{28}$$

Fig. 9 depicts voltage stress characteristics for semiconductor devices according to (27) and (28). The low voltage stress of these devices can reduce conduction loss and thus it is possible to improve operating performance by selecting a semiconductor device with low ON-resistance and low rated voltage.

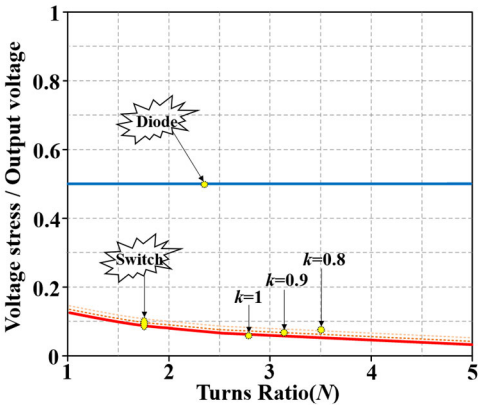

FIGURE 9. Voltage stress/Output voltage vs. Turns ratio (*N*), [$k = 0.8 \sim 1$].

C. KEY CIRCUIT PERFORMANCE COMPARISON

Table 1 compares the proposed high step-up converter with similar converters [30]–[32] in various aspects. The proposed high step-up converter has the same number of elements or up to 63% less than the comparable converters. The number of switches is two less compared to the compared converter. If the number of switches is large, the operation circuit configuration becomes complicated and the size and price increase due to the added gate driver and PCB layout.

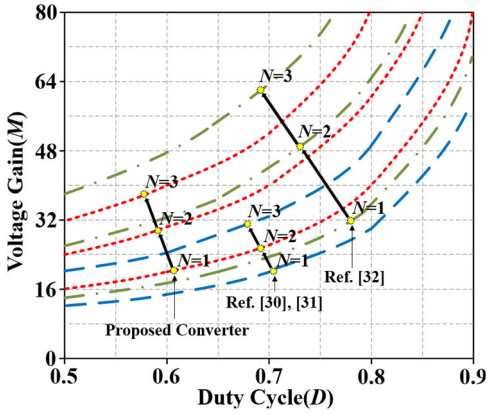

FIGURE 10. Voltage gain (*M*) vs. Duty cycle (*D*) and Turns ratio (*N*) comparison between the proposed high step-up converter and similar converters [30]–[32], [$k = 1$].

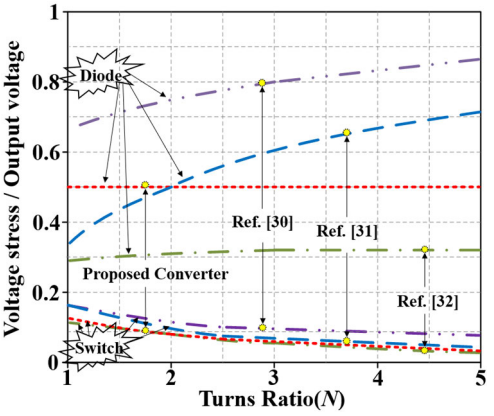

FIGURE 11. Voltage stresses/Output voltage vs. Turns ratio (*N*) comparison between the proposed high step-up converter and similar converters [30]–[32], [$k = 1$].

Fig. 10 illuminates the voltage gain (M) according to duty cycle (D) and turns ratio (N). The proposed high step-up converter has a voltage gain (M) of up to 62.5% [$N = 3$] higher than those of [30] and [31] while 15.7% [$N = 3$] lower than that of [32]. Fig. 11 illustrates the voltage stress according to the turns ratio (N). Compared to [31], the proposed converter achieves 24% reduction in switch voltage stress. The diode voltage stress of the proposed method is 24% less than that of [31] while 44% greater than that of [32]. It should be noted that the proposed high step-up converter yields a high voltage gain without increasing the number of turns ratio (N), and the circuit configuration is simple because the number of active and passive elements is small.

TABLE 1. Performance comparison of high step-up DC/DC converters.

Topologies	Nu. of Sw.	Nu. of Di.	Nu. of Co.	Nu. of Ca.	Voltage gain	Voltage Stress Sw.	Voltage Stress Di.	Duty Limit	Frequency/ Ma. Power	Frequency/ Ma. Power	Efficiency
Proposed Converter	2	4	2	4	$\frac{4+4N}{1-D}$	$\frac{1}{4+4N}V_o$	$\frac{1}{2}V_o$	$0.5 \le D$	20V/400V	$50kHz$/ $320W$	94.1%
Ref. [22]	2	4	2	4	$\frac{4+2N}{1-D}$	$\frac{1}{4+2N}V_o$	$\frac{1+N}{2+N}V_o$	$0.5 \le D$	20V/400V	$50kHz$/ $320W$	94.8%
Ref. [23]	2	6	2	6	$\frac{4+2N}{1-D}$	$\frac{1}{2+4N}V_o$	$\frac{N}{2+N}V_o$	$0.5 \le D$	20V/400V	$100kHz$/ $400W$	95.2%
Ref. [24]	4	6	2	7	$\frac{1+6N}{1-D}$	$\frac{1}{1+6N}V_o$	$\frac{2N}{1+6N}V_o$	$0.1 \le D$	59V/900V	$42kHz$/ $400W$	95.4%

TABLE 2. Components and parameters of the prototype.

Components	Parameters
Output Power(P_{out})	$320W$
Input→Output Voltage(V_{in}→V_{out})	20→400V
Input→Output Current(I_{in}→I_{out})	16→0.8A
Load Resistance(R_o)	500Ω
Switching Frequency(f_s)	$50kHz$
Switches(S_1, S_2)	IRF200P222
Diodes(D_a, D_b, D_{o1}, D_{o2})	RF1501
Capacitors(C_a, C_b, C_{o1}, C_{o2})	$100\mu F$
Coupled Inductors(L_1, L_2)	CS468125
Turns Ratio(N)	1(24:24)
DSP	TMS320F28335

IV. SIMULATION AND EXPERIMENTAL VERIFICATION

In this section, related parts are designed to implement the proposed converter, and simulation and experimental verification are conducted based on the design data. The design specifications of the proposed high step-up converter are given in Table 2.

A. DESIGN CONSIDERATIONS

Based on the parameters in Table 2, the MOSFETs are selected through the design within the rated voltage of the switches (S_1, S_2).

$$V_{S1} = V_{S2} = \frac{V_o}{4+4N} = \frac{400}{4+4\times 1} = 50V. \quad (29)$$

The above equation (29) is the voltage stress value of the switches (S_1, S_2) based on the voltage gain (M), but in Section II (*Mode 3*, *Mode 7*), the voltage spike problem of the switches (S_1, S_2) occurs through the resonance phenomenon of the leakage inductors (L_{k1}, L_{k2}) and parasitic capacitors [6], [33]. Therefore, a simple snubber network of switches (S_1, S_2) is added and designed as 200V.

The diodes (D_a, D_b, D_{o1}, D_{o2}) are not affected by the turns ratio (N). From (28) the following can be obtained

$$V_{Da} = V_{Db} = V_{Do1} = V_{Do2} = \frac{V_o}{2} = \frac{400}{2} = 200V. \quad (30)$$

The diode voltages are set as 300V with a safety margin by referring to (30).

The coupled inductors operate at continuous conduction mode (CCM) and the duty cycle (D) is assumed to be 0.5 or more.

$$N = \frac{M(1-D)-4}{4} = \frac{20(1-0.6)-4}{4} = 1. \quad (31)$$

The input current (I_{in}) and current ripple ($\Delta i_L = \Delta i_{L1} = \Delta i_{L2}$) rate are applied to the magnetizing inductance ($L_m = L_{m1} = L_{m2}$) values of the coupled inductors.

$$I_{L1} = I_{L2} = \frac{I_{in}}{2} = 8A \quad (32)$$

$$\Delta i_L = I_{L1\_30\%} = I_{L2\_30\%} = \frac{I_{in}}{2}\times 0.3 = \frac{16}{2}\times 0.3 = 2.4A \quad (33)$$

$$L_m \ge \frac{V_{in}D}{\Delta i_L f_s} = \frac{20\times 0.6}{2.4\times 50\times 10^3} = 100\mu H. \quad (34)$$

From the above equations, the minimum bound of the magnetizing inductance (L_m) can be obtained as $100\mu H$. Fig. 12 depicts the applied toroidal core.

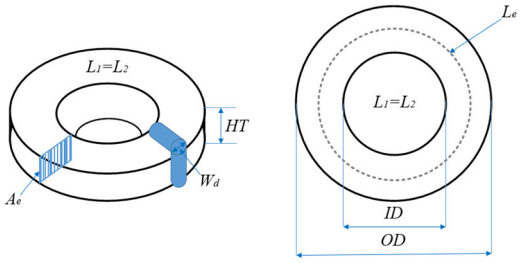

FIGURE 12. The toroidal core of the coupled inductors (L_1, L_2).

The turns ratio (N) can be calculated from the normal inductance (A_L) and magnetizing inductance (L_m) of the core.

$$L_m = A_L \cdot N^2 \rightarrow N = \sqrt{\frac{L_m}{A_L}} = 24Turns. \quad (35)$$

The area and volume can be obtained through the length of the core, and a coupled inductor is designed with a Litz wire.

This is detailed in Table 3.

$$L_e = \frac{\pi\,(OD - ID)}{\ln\left(\frac{OD}{ID}\right)} = 116mm,$$
$$A_e = \frac{HT \cdot (OD - ID)}{2} = 137mm,$$
$$V_e = L_e \cdot A_e = 15945mm^2,$$
$$W_a = \pi \cdot \left(\frac{W_a}{2}\right)^2 = 3.14mm^2,$$
$$T_w = 2N \cdot \left(\frac{OD - ID}{2} + HT + 2W_d\right) = 1356mm. \quad (36)$$

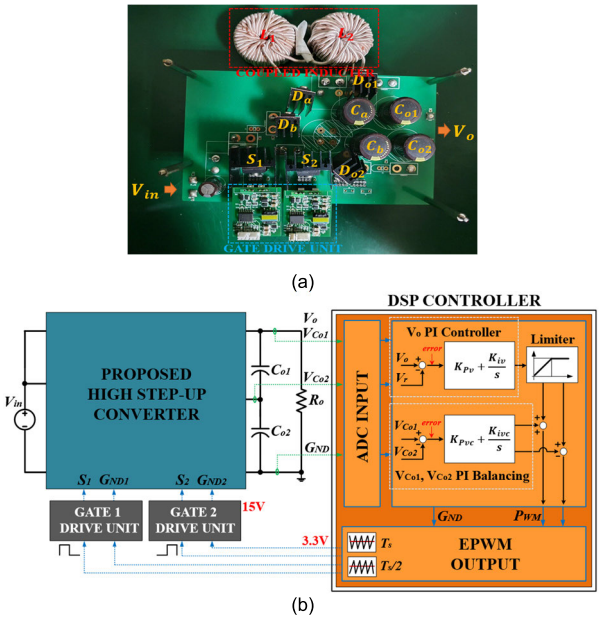

FIGURE 13. Experimental data of the proposed non-isolated high step-up DC/DC converter. (a) Hardware. (b) Controller block diagram.

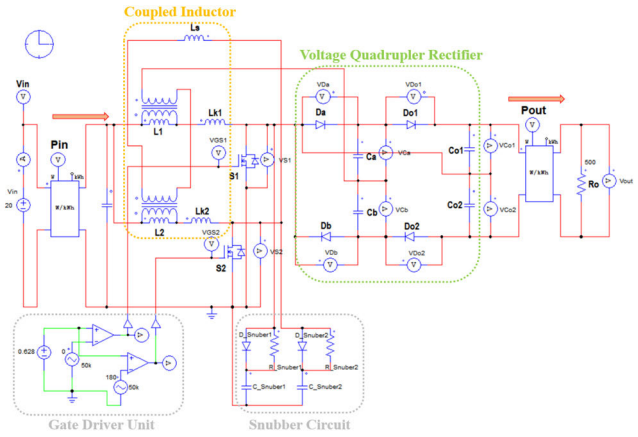

FIGURE 14. PSIM simulation schematic of the proposed high step-up converter.

The values of the capacitors (C_a, C_b) are obtained through the ratio of the current ($I_{Ca} = I_{Cb}$) and the ripple voltage

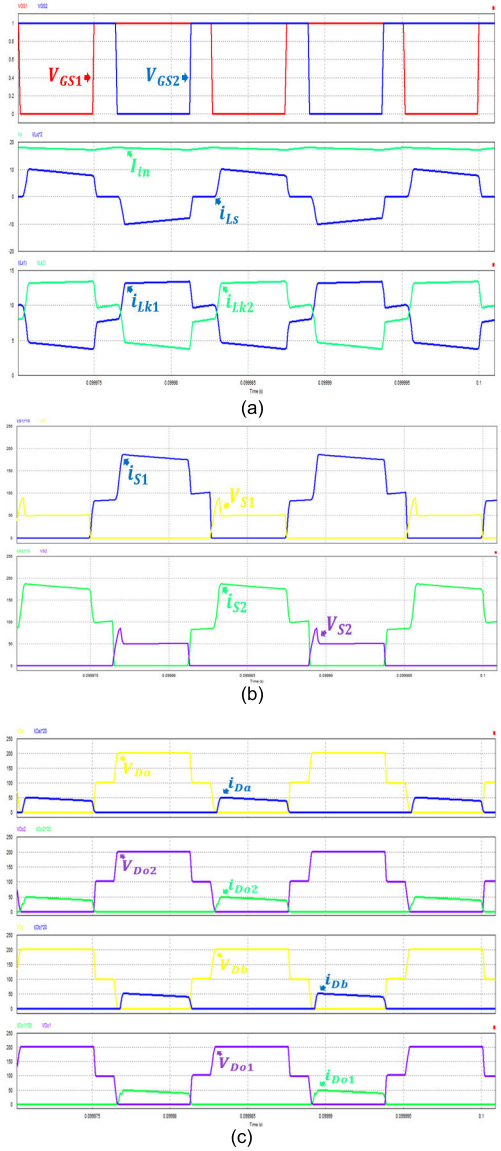

FIGURE 15. Simulation waveforms (V_{in} = 20V, R_o = 500Ω). (a) V_{GS1}, V_{GS2}, I_{in}, i_{Ls}, i_{Lk1}, i_{Lk2}. (b) V_{S1}, V_{S2}, i_{S1}, i_{S2}. (c) V_{Da}, V_{Do2}, V_{Db}, V_{Do1}, i_{Da}, i_{Do2}, i_{Db}, i_{Do1}.

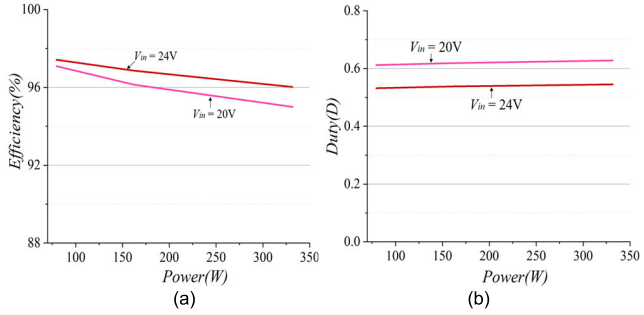

FIGURE 16. Simulation results of the proposed high step-up converter. (a) Efficiency (%) vs. Power (W). (b) Dudy (D) vs. Power (W).

($\Delta V_{Ca} = \Delta V_{Cb}$) value during the duty cycle (1-D) period.

$$I_{Ca} = I_{Cb} = \frac{I_L}{4} \quad (37)$$

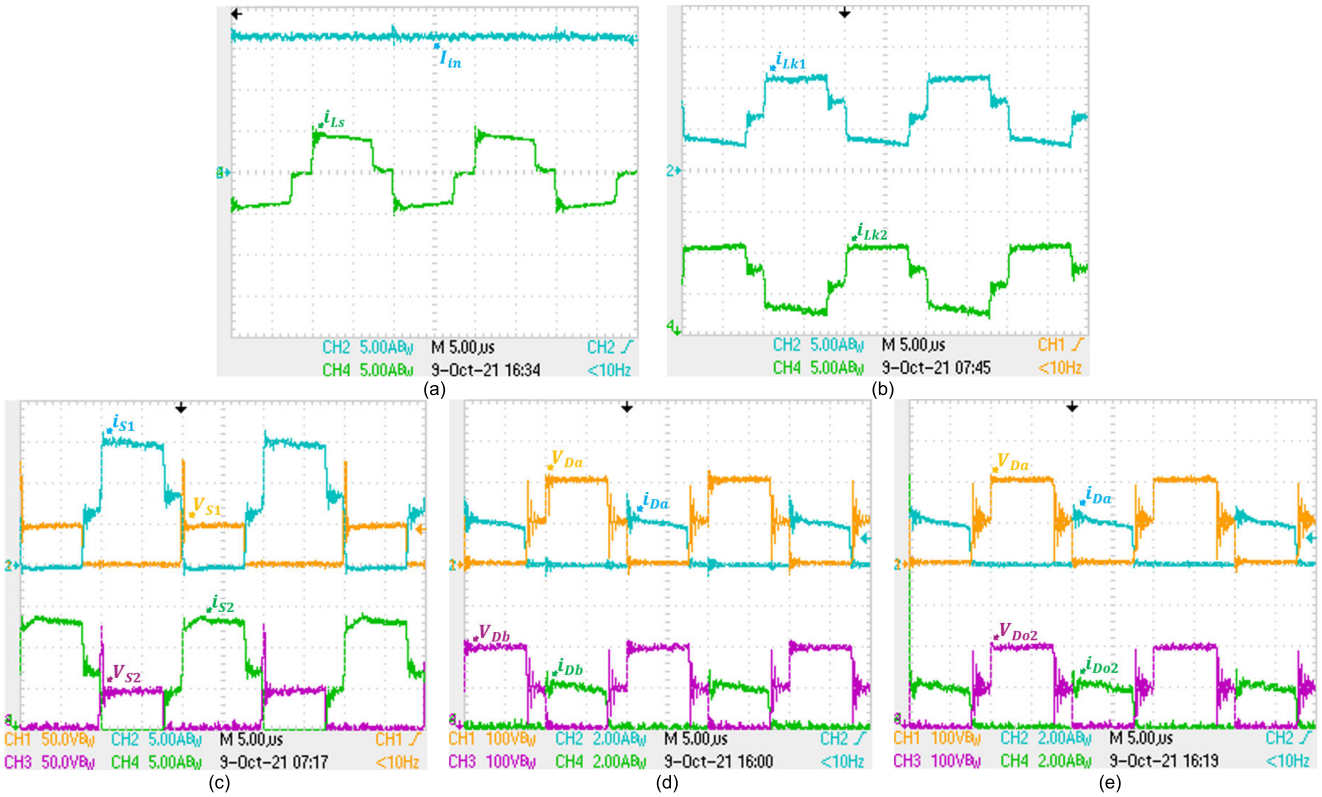

FIGURE 17. Experimental waveforms (V_{in} = 20V, R_o = 500Ω). (a) I_{in}, i_{Ls}. (b) i_{Lk1}, i_{Lk2}. (c) V_{S1}, V_{S2}, i_{S1}, i_{S2}. (d) V_{Da}, V_{Db}, i_{Da}, i_{Db}. (e) V_{Da}, V_{Do2}, i_{Da}, i_{Do2}.

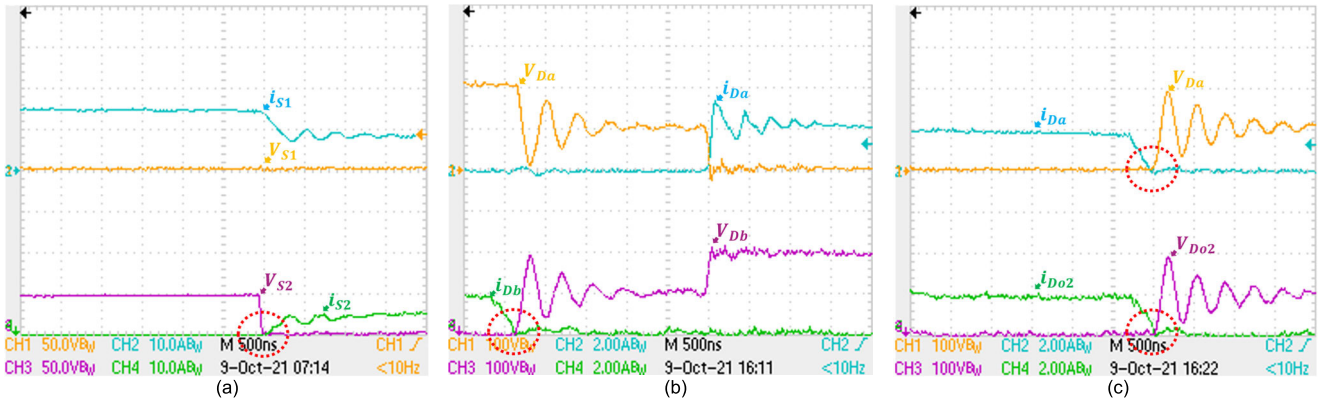

FIGURE 18. Detailed experimental waveforms (V_{in} = 20V, R_o = 500Ω). (a) V_{S1}, V_{S2}, i_{S1}, i_{S2}. (b) V_{Da}, V_{Db}, i_{Da}, i_{Db}, (c) V_{Da}, V_{Do2}, i_{Da}, i_{Do2}.

$$C_a = C_b \geq \frac{I_{Ca}(1-D)}{\Delta V_{Ca\_2\%}} T_s = \frac{1.875 \times 0.4 \times 0.00002}{100 \times 0.02} = 7.5\mu F. \quad (38)$$

The values of the capacitors (C_{o1}, C_{o2}) connected in series to the output side are obtained through the ratio of the output current (I_o) and the ripple voltage ($\Delta V_{Co1} = \Delta V_{Co2}$) value during the duty cycle (D) period.

$$C_{o1} = C_{o2} \geq \frac{I_o D}{\Delta V_{Co1\_1\%}} T_s = \frac{0.8 \times 0.6 \times 0.00002}{200 \times 0.02} = 4.8\mu F. \quad (39)$$

The minimum capacitance in the steady state is obtained through the power (P_o), duty cycle (D), and ripple ratios including the capacitor voltage and current of (38) and (39). The proposed high step-up converter was designed as $100\mu F$ considering the rate of change (ripple, D).

B. SIMULATION AND EXPERIMENTATION

Table 4 shows detailed values for the components of the proposed high step-up converter. In order to measure the exact

TABLE 3. Detailed data of toroidal cores.

Part No.		CS468
A_L	Nominal inductance	$178nH/N^2$
N	Turns ratio	24Turns
OD	Outside diameter of core	46.74mm
ID	Inside diameter of core	28.7mm
HT	Height of core	15.24mm
L_e	Magnetic path length	11.63mm
A_e	Effective cross section area	$134mm^2$
V_e	Effective core volume	$1558mm^3$
W_d	Wire diameter	2mm
W_a	Wire Area	$3.14\ mm^2$
T_w	Total wire	1356mm

effect of efficiency and duty cycle (D), the data are applied to simulation data including the resistance component of each device.

TABLE 4. Components and value of the prototype.

Components	Value	
IRF200P222 (S_1, S_2)	V_{DSS} (Drain-source breakdown voltage)	200V
	$R_{DS(ON)}$ (Drain-source ON-resistance)	5.3mΩ
RF1501 (D_a, D_b, D_{o1}, D_{o2})	V_R (Reverse voltage)	300V
	V_F (Forward voltage)	1.35V
CS468125 (L_1, L_2)	L_{m1}, L_{m2} (Magnetizing inductance)	101.18μH 101.72μH
	L_{k1}, L_{k2} (Primary side leakage inductance)	1.67μH 1.72μH
	L_s (secondary side leakage inductance)	3.59 μH

Fig. 13(a) shows the hardware picture of the proposed non-isolated high step-up DC/DC converter, and toroidal-type coupled inductors (L_1, L_2), VMR (D_a, D_b, D_{o1}, D_{o2}, C_a, C_b, C_{o1}, C_{o2}), and switches (S_1, S_2) are indicated. Fig. 13(b) depicts the proposed high step-up converter and DSP control block diagram. The DSP used TMS320F28335 and coded the program using CCS 3.3 version to generate output voltage sensing (ADC INPUT) and two PWM signals. The frequency of the switching waveform is set to 50kHz, and PWM signals are applied to MOSFTEs through EPWM modules and insulated gate drives.

Fig. 14 shows the schematic diagram of the proposed high step-up converter simulation based on a coupled inductor and a voltage quadrupler rectifier. In order to operate in the interleaved method, the switches (S_1, S_2) of the gate driver are delayed by 180 degrees and the duty cycle (D) is set to 0.6 or more. Fig. 15 (a) depicts the current simulation waveforms of the input and leakage inductors as well as the voltage of the gates. Also, Fig. 15 (b) and 15 (c) illustrate the voltage and current simulation waveforms of switches (S_1, S_2) and diodes (D_a, D_b, D_{o1}, D_{o2}), respectively.

Fig. 16 (a) and 16(b) illustrate the measured efficiency and duty cycle (D) when the input voltage (V_{in}) is 20V or 24V according to power (W). The maximum efficiency is 97.32% at the input voltage of 24V and 80W, and the minimum efficiency was 95.03% at the input voltage (V_{in}) of 20V and 330W. Theoretically, when the input voltage (V_{in}) is 20V, the duty cycle (D) is 0.6, and when the input voltage (V_{in}) is 24V, the duty cycle (D) is 0.58.

Fig. 17 portrays the experimental waveforms of the proposed high step-up converter based on Table 1, Table 2, and simulation. Fig. 17(a) and Fig. 17(b) shows the current waveforms of the input, secondary side leakage inductor, and primary side leakage inductor. The proposed method has a small input current ripple due to the interleaved operation, which is helpful for the lifetime of the renewable energy system. Fig. 17(c) illuminates the voltage and current waveforms of the switches (S_1, S_2), and the voltage stress is observed to be only 50V. Fig. 17(d) and Fig. 17(e) depicts the voltage and current waveforms of diodes (D_a, D_b, D_{o1}, D_{o2}), and the voltage stress is 200V, which is the same as the theoretical and simulation results.

Fig. 18(a), Fig. 18(b), and Fig. 18(c) illustrate detailed waveforms of the switch and diodes, which imply that the switch (S_2) shows zero current turn–ON and the diodes (D_a, D_b, D_{o2}) give zero current turn–OFF performance. Therefore, the semiconductor devices of the proposed converter can reduce the switching loss along with conduction loss, which allows the advantage of using a power switch with a low rated voltage and low on-resistance.

Fig. 19 compares and depicts the simulation and experimental data of the proposed high step-up converter, and the average values of the measured experimental data are 95.39% (V_{in}:20V) and 96.32% (V_{in}:24V), confirming the high efficiency characteristics.

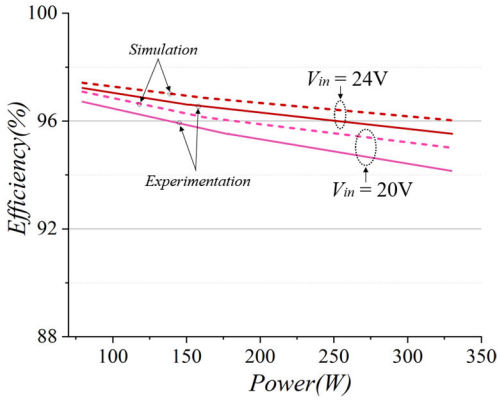

FIGURE 19. Simulation and experimental efficiency curves of the proposed high step-up converter (V_{in} = 20V, 24V, R_o = 500Ω, P_o = 320W).

V. CONCLUSION

This paper proposed a transformerless type DC/DC converter with high voltage gain by combining coupled inductor and

quadrupler technology. The proposed high step-up converter is very efficient because it not only obtains additional voltage gain through the turns ratio of the coupled inductor, but also recycles the energy in the leakage inductor to the output side. In the proposed converter, the stacked voltage quadrature technology on the output side can be combined with a coupled inductor to increase efficiency by enabling the selection of semiconductor devices that trap low rated voltages and On-resistance of switches and diodes through lossless clamp-performance. However, as demonstrated by steady-state analysis, leakage inductors of coupled inductors cause switching losses due to voltage spikes when the switch is turned OFF. Therefore, a passive clamp circuit may be needed to clamp the voltage level of the switches. The operating principle of the proposed converter and high efficiency characteristics of up to 94.1% [320W] were confirmed through simulation and experimental results. Therefore, the proposed high step-up DC/DC converter is expected to show good performance in fuel cells and solar electricity-based power conversion systems that require high voltage gain.

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