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Advanced System Analysis and Survey on the GPS Receiver Front End

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ABSTRACT A fully integrated GPS receiver system can enable unique system capabilities by synthesizing both receiver front end and baseband on the same chip, leading to lower area overhead and higher integration. A survey on the GPS receiver system that focuses on front end design is presented in the paper. The first section discusses the various global navigation satellite system (GNSS), followed by the GPS working section. Afterwards, the paper discusses the previous works on the GPS receiver front end design. It provides a detailed survey and classification of various receiver architecture, including the LNA, mixer, filter, and ADC topologies. Besides, several image rejection techniques are presented for more than 50 GPS receivers. The various performance parameters of the GPS receiver front end in the literature are presented with the graphical view in the state-of-the-art discussion section. This literature survey provides the most extensive compilation to date of the various topologies, techniques and explains their implementation in the GPS receiver system. A new figure of merit that includes all the system parameters is proposed. The FOM can be an excellent reference to enhance the research work in the field of GPS receivers. In the end, the paper describes the possible research scope and challenges associated with the design of the GPS receiver front end.

INDEX TERMS Global navigation satellite system (GNSS), image rejection, RF front end, sensitivity, spurious free dynamic range (SFDR), wireless communication.

I. INTRODUCTION

This paper presents a detailed description of the global positioning system (GPS) receiver front end. The GPS is a satellite navigation system that provides necessary information on the user's absolute position, time, and velocity. As per the federal communication commissions (FCC) regulations, every cellular device should determine the location with better than 100 m accuracy [1]. Therefore, to achieve this objective, low-cost solutions and higher-level integration are required, demanding fewer external components [2]. Radio receivers for the GPS signal reception were traditionally implemented using bipolar technology because of the demanding noise and sensitivity performance in the multipath environment. With the advancement of the CMOS technology node, the CMOS GPS receivers are mostly preferred for such applications [3]. At present, the global navigation satellite system (GNSS) include fully operational GPS of the United States and GLONASS from Russia as well as developing global and regional navigation satellite system, namely Europe's Galileo, China's Compass/Beidou, India's Indian regional navigation satellite system (IRNSS) and Japan's quasi-zenith satellite system (QZSS).

The applications of the GPS receivers span many areas, which demand higher sensitivity. The GPS receivers have also been considered for aircraft navigation which helps flight in the rugged terrain and also assists the proper landing of flights. This saves millions of dollars. The GPS is used for marine navigation, sports, and hiking [4], [5]. These applications can be successfully achieved only if the GPS receivers provide accurate position and speed information. This is possible with high sensitivity receiver in a multi path environment. With proper circuit design and multi-band multi GNSS receivers, higher sensitivity can be achieved. Recently, in order to overcome this limit, the GPS modernization plan involves the addition of an extra band that enhances tracking performance in the multipath environment [6].

This paper compiles, classifies, and discusses the previous work on the GPS receiver front end most comprehensively to date and provides many non-simulation references to give a

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complete picture. This paper will describe the GNSS receiver front end design from the LNA to the mixer, filter until ADC design. This paper also presents a novel comparative study of demonstrated GPS receiver systems over several measurement scenarios [1]–[3], [6]–[37], [38]–[47]. Their sensitivity, image rejection ratio (IMRR), noise figure (NF), and gain are analysed concerning power dissipation and publication date. The combination of various performance metrics is proposed into a new figure of merit (FOM) for the GPS receiver systems. It can propel innovative research towards demonstrating systems with increased performance at lower power dissipation and hopefully expedite the inclusion of multiple bands and multiple GNSS into the future GPS receivers. Section II provides an overview of the GNSS, highlighting details of the same and gives a summary of the working principles of the GPS. In contrast, Sections III-IV discuss the GPS receiver system-level design and various sub-blocks of the receiver front end. The system survey results are presented in Section V, and the conclusion is derived in Section VI.

II. GNSS OVERVIEW AND WORKING

The GPS is the GNSS launched by the US military in the early 1970s. In the initial stages, the use of GPS was limited to the US military. Later on, it was made available for civilian use across all the countries. The satellites which were launched in the early development stage provide service only in a single L1 band. Subsequently, the L2 band was added. Currently, the satellites which are in orbits offer service in three bands L1 (1575.42 MHz), L2 (1227.6 MHz), and L5 (1176.45MHz). The GPS provides two types of services: precise positioning system (PPS) and standard positioning system (SPS). The other GNSS are Galileo from Europe, GLONASS from Russia, Beidou from China, QZSS from Japan, and IRNSS from India. Fig. 1 gives a complete idea about the frequency spread of the various GNSS bands. L1 and L5 bands are the most used frequency bands among all GNSS. However, most of the commercial GPS receivers offer service only in the L1 band. Table 1 gives an idea about the number of satellites in each GNSS system, satellite orbit, supported frequency band, multiplexing scheme, and modulation techniques used in the various GNSS. The CDMA technique is used in all the GNSS systems except the GLONASS. Though an FDMA technique is used in GLONASS; however, it will support CDMA to enhance its compatibility and interoperability with other GNSS systems in the future. All the GNSS systems use the BPSK, and some of them use the QPSK modulation technique. A new modulation scheme binary offset carrier (BOC) is planned to be used soon. The different GNSS have the satellite location at different heights and elevation angles to provide adequate coverage in their respective countries throughout their revolution period.

The GPS consists of the satellite system in the medium earth orbit (MEO), the GPS receivers in the user system, and the augmentation system, including satellite-based and ground-based augmentation systems. There should be at least four or more satellites in outlook from any point at any time to determine the user's correct location. However, in urban areas, the signal strength at the receiver is very weak due to multiple reflections from tall buildings. Therefore, to ensure good signal strength even in densely populated areas, the count of satellites in orbit has been increased, and at the same time, more frequency bands like L1, L2, and L5 are used for transmission. It ensures good signal strength even in substantial interference from the strong signal falling in the same band and also cancels the ionospheric interference.

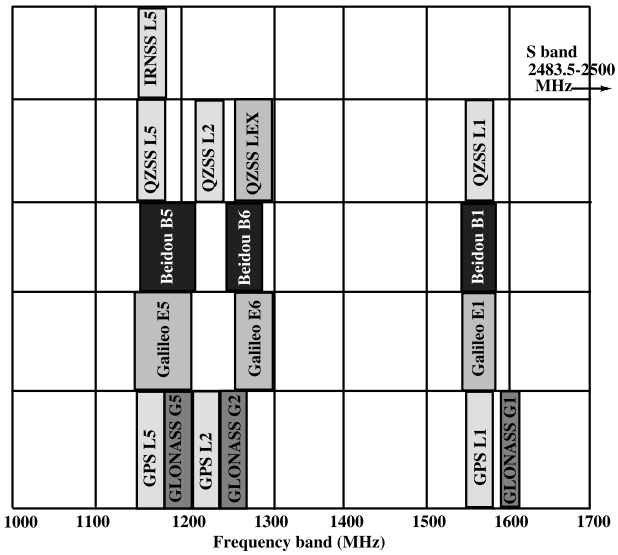

FIGURE 1. Frequency band spectrum of the existing GNSS bands.

Direct Sequence Spread Spectrum (DSSS), BPSK modulation, and CDMA multiplexing scheme are used for GPS applications. The navigation data transmitted by the satellite contains information about the satellite location (ephemerides) and time of transmission [48]. Every satellite has a unique pseudo-random (PRN) code. For example, the GPS L1 band has a data rate of 50 bps, the carrier signal frequency is 1575.42 MHZ (L1), and the PRN code has a chipping rate of 1.023 Mbps for civilian use and 10.23 Mbps for military purposes. The carrier signal is modulated with the data signal, which is a digital signal in the form of 1s and 0s. This modulated carrier signal is further modulated with the PRN Code as depicted in Fig. 2. Fig. 3 presents the frequency domain plot for the final modulated signal. In the frequency domain, the modulated signal has the maximum amplitude around zero frequency. The modulated signal is then transmitted through the channel and suffers attenuation; thus, the very weak signal is received at the receiver antenna. The signal is amplified and downconverted by the receiver front end. Later on, the signal is demodulated at the baseband portion to obtain the data signal. The despreading process in the receiver is successful only if the PRN code is perfectly synchronized with the received one.

III. SYSTEM LEVEL DESIGN OF GPS RECEIVER

A systematic approach for designing the GPS receiver front end is discussed in this section. The overall specification of the entire receiver is evaluated by using the wireless standards [49]. The minimum signal power received at the antenna is −130 dBm and -133 dBm for GPS L1 and L2 band, respectively. The basic requirements of the GPS receiver include the gain dynamic range, noise performance, IMRR, phase noise of the oscillator, filter bandwidth, and the ADC resolution. The various performance parameters, along with gain and noise budget for the GPS L1 band, are described in detail in [6]. The parameters are defined by considering minimum power consumption, maximum gain, higher linearity, and minimum NF. Besides, the bit error rate (BER) is one of the performance parameters in digital communication. The BER is the ratio of the no of error bits divided by the total no of bits received. SNR is the carrier to noise ratio (C/No) per unit bandwidth. There is a relation between SNR, C/No, and Eb/No [11]:

$$\frac{C}{No} = \left(\frac{S}{N}\right) B = \left(\frac{Eb}{No}\right) Rb \tag{1}$$

where S and N are signal and noise power respectively in a specified bandwidth, B is the noise equivalent bandwidth which is equal to the bandwidth of the narrowest of all the filters used in the receiver front end, and Rb is the bit rate. For the GPS receiver front end, the signal's bandwidth is 2 MHz for the civilian GPS signal; therefore, the filter with 2-3 MHz cut-off is required. The bit rate is 50 bps and 25 bps for the GPS L1 and L5 band, respectively. A conventional iterative method based on a literature survey or the technique based on power coefficients can be used to specify the sub-block specifications [49]. The basic system level parameters such as sensitivity, IIP3, SFDR, and NF are evaluated using the formula available in literatures [49], [50]. The above parameters are used to define the block level specification such as gain, NF, IIP3. The design can be verified through system level modelling using MATLAB tool and Veriloga models initially, followed by transistor level implementation of each block to achieve the overall system performance with minimum power consumption.

IV. GPS RECEIVER FRONT END ARCHITECTURE

This section contains a detailed explanation of the various GPS receiver front end architectures and their sub-blocks. Fig. 4 illustrates the classification of each sub-block in the GPS receiver front end architecture in the form of a tree diagram. The most commonly used receiver front end architecture for GPS applications are low-IF, zero-IF, and heterodyne. The heterodyne architecture used to be the choice for GNSS receiver architecture before the introduction of the low-IF topology due to its performance. However, once the low-IF receiver came into existence, it became the first choice of the circuit designers as it helps to achieve both integration and performance [50]. From the pie-chart shown in Fig. 5, 88.9% of the GPS receiver front ends surveyed in the literature have

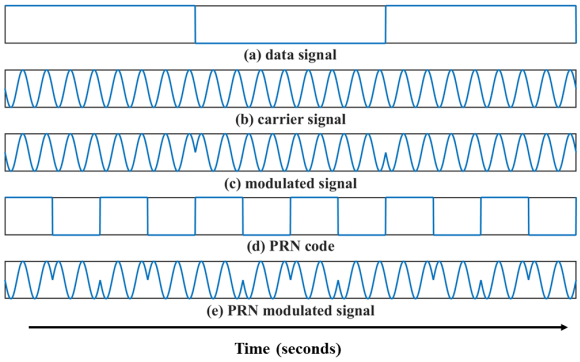

FIGURE 2. Time plot of the data signal, carrier signal, the carrier BPSK modulated with the data, PRN code, PRN code modulated on the data modulated carrier [51].

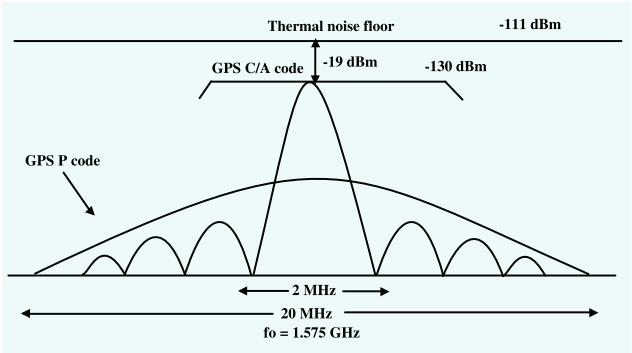

FIGURE 3. Frequency domain waveform (GPS L1 C/A code and P-Code Spectrum) [6].

used low-IF architecture while 7.4% of them have used zero-IF architecture. However, 3.7% of them have used heterodyne architecture. The low-IF architecture is often preferred because most of the GPS coarse acquisition (C/A) code signal energy lies at the mid-frequency, as shown in Fig. 3. However, [1], [28], [29] have used heterodyne architecture. The zero-IF architecture has been used in [9] and [30]. However, there is a possibility to extensively use the zero-IF architecture for GPS application in the future if the challenges like DC offsets, mixer second-order non-linear effects, and flicker noise are taken care of while designing the various sub-blocks. This will help to achieve the highly integrated solution for various standards like GPS, CDMA on a single chip with optimized die area and performance. It offers the advantage of higher integration due to the block reuse for several modes and the flexible frequency planning. It leads to a reduction in chip area and design cost [9]. The front end linearity is not an issue in the single-mode GPS receivers as their signal power is low [8]. In multi-mode receivers, the linearity of the GPS signal becomes crucial in the presence of cellular jammer signals [7]. This problem can be tackled through BPF before the LNA, LC tank load in the LNA, and the mixer.

In the low-IF architecture, the IF frequency is equivalent to the bandwidth of the signal. This architecture is a compromise between the heterodyne and homodyne; therefore, it will

TABLE 1. Parameters of the different GNSS.

	GPS (USA)	Glonass (Russia)	QZSS (Japan)	Beidou (China)	Galileo (Europe)	IRNSS (India)
No of satellites	31	24	1 (7)	14	3 (30)	2(7)
Satellite Orbit	MEO	MEO	4 GSO, 3 GEO (Currently 1)	5 GEO,5 GSO, 4 MEO	MEO	3 GEO, 4 GSO
Frequency band	L1,L2,L5,GPS-3(future)	L1,L2,L3, GLONASS-K(future)	L1,L2,L5 (Similar to GPS,LEX (Galileo E6)	B1,B2,B3(not civilian use),Beidou-3 (future)	E1,E5,E6	L5,S
Multiplexing	CDMA	FDMA (CDMA in GLONASS-K)	CDMA	CDMA	CDMA	CDMA
Modulation	BPSK, GPS-3(BOC)	BPSK, GLONASS-K(BOC)	BPSK	BPSK, QPSK	E1(BOC) ,BPSK	BPSK

Note: values in the bracket denotes the future plan

combine the benefits of both. It has a high level of integration, and at the same time, it is free from DC offset, and flicker noise [52]. The problem of the image is solved using two downconversion paths. A low Q BPF can be used in a low-IF receiver similar to the low pass filter (LPF) in the case of a zero-IF receiver [50]. The low-IF architecture can be further classified into single, dual, and triple downconversion architecture. Generally, a single downconversion architecture [2], [7], [8], [10]–[13] is preferred, however [3], [6] have used double downconversion architecture, and [28] has used triple downconversion architecture. The dual downconversion low-IF architecture with non-zero IF is depicted in Fig. 6. In single downconversion, the entire gain is divided among a few stages, leading to instability. However, in dual downconversion architecture, the gain is divided among several stages, such as two mixer stages and filter blocks, and LO is well isolated from RF [26]. The dual downconversion needs two stages of IF, therefore offering the higher image rejection and minimizing flicker noise [26]. However, the double and triple conversion architecture involves more blocks and more power consumption, thus comparatively complex design. Therefore, the single downconversion is preferred over the double and triple downconversion.

Depending on the number of GNSS bands supported, the receivers can be categorized into single, dual, and multi-band receivers. The single band receivers support either the L1, L2, or L5 band of single GNSS or multiple GNSS; therefore, the circuit is simple. Dual band receivers provide support for any two bands of either the single or the multiple GNSS. The circuit of the dual band receivers is comparatively complex and needs appropriate frequency planning. The correct choice of the local oscillator frequency leads to the reuse of LO frequency, thus, reducing the number of oscillators required. The detailed frequency planning is discussed in section V-A. The multi band receivers provide support for multiple GNSS bands. It needs two frequency synthesizers which further increases the complexity. However, the GNSS receivers, which are equipped to receive various GNSS bands, can calibrate the ionosphere's error and make the required correction [2]. It helps to enhance the receiver's preciseness and sensitivity to a greater extent.

A. FREQUENCY PLANNING

The frequency planning is a prerequisite for the receiver design. The image rejection requirement can be relaxed very much using proper frequency planning [6]. It allows to share the required components like frequency synthesizers which further reduces area overhead and increases the level of integration. The single low noise frequency synthesizer that can provide LO signals for L1, L2, L5, and S bands is proposed in this paper [53]. In various literature, different sort of frequency planning scheme is discussed. These schemes can be categorized as follows:

1) SINGLE BAND DUAL DOWNCONVERSION OF LOW-IF

In the case of the single downconversion architecture, a lower value of IF leads to poor LO-RF isolation. This problem is tackled using double downconversion architecture. The choice of the low-IF removes RF or LO feedthrough from the IF signal, and the noise bandwidth of the first stage is also reduced in case of dual downconversion [26]. Two possible frequency schemes having different LO frequencies are shown in Fig. 7. The preferred scheme is selected by using the switch. The first IF frequency is selected such that the same frequency synthesizer can be used to generate the second LO as well that reduces the complexity of the chip [26].

2) DUAL BAND DUAL DOWNCONVERSION OF LOW-IF

This scheme supports two frequency bands of either the same or different GNSS. There are two options in this frequency scheme which is depicted in Fig. 8. In Fig. 8(a), any one of the two L1/L2 bands can be received at one time, or both the bands can be received through a single chain; however, the NF is deteriorated by 3 dB. As shown in Fig. 8(b), a separate path is available for both L1 and L2 signals' simultaneous reception. With the correct frequency planning, all the

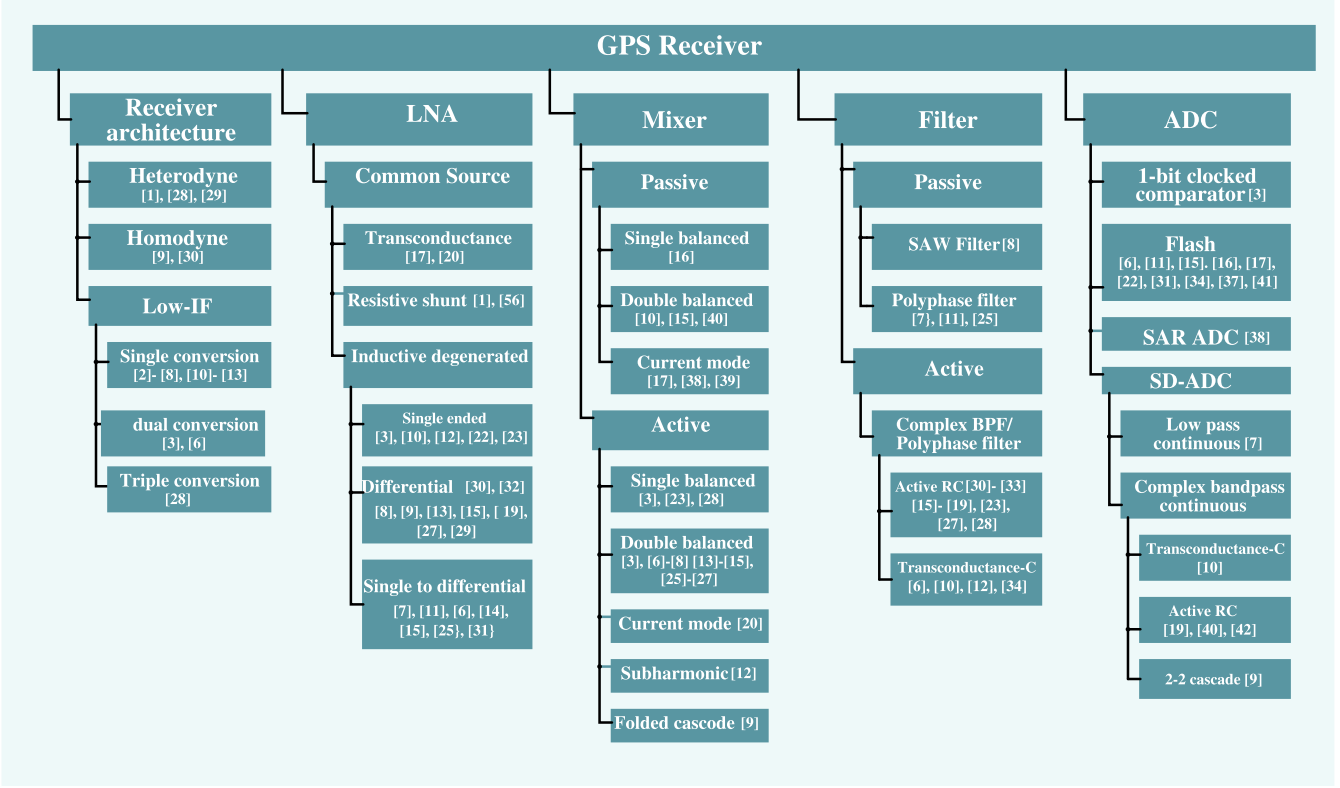

FIGURE 4. Tree diagram showing the entire GPS receiver front end classifications.

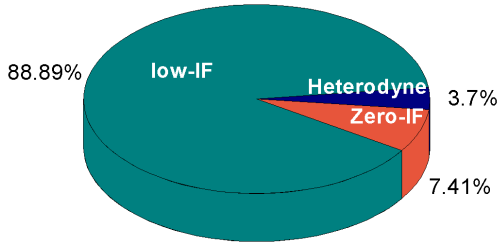

FIGURE 5. Pie-chart showing GPS receiver architecture distribution.

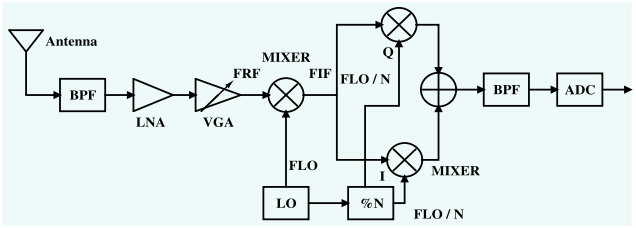

FIGURE 6. Low-IF architecture [52].

signals can be generated from a single frequency synthesizer. The first LO is chosen to be equidistant from both the L1 and L2 frequencies. Therefore, the image signal lies within the GPS band (alternate or self), leading to a non-stringent image rejection requirement [6]. The second LO can also be generated from the same synthesizer through the use of a divider block. It helps to reduce the number of synthesizers and achieves good performance. Therefore, it demonstrates the significance of frequency planning in the image rejection.

3) MULTI BAND SINGLE DOWNCONVERSION OF LOW-IF

In the case of a multi band single downconversion, the multiple GNSS bands can be received simultaneously. The GNSS receiver can receive any two signals from GPS/Galileo/GLONASS/Beidou systems concurrently. As shown in Fig. 9, the GNSS signals present either in the same band (i.e., 1.6 GHz, 1.2 GHz) or in the different bands (i.e., 1.6 GHz and 1.2 GHz) are processed concurrently. If the bandwidth of two GNSS signals are different, two separate image rejection filters are used. Otherwise, a single image rejection filter of either 2 or 10 MHz bandwidth is enough. The LNA, matching network, and a single antenna can be shared between two GNSS signals in the same band. The flexible frequency planning with two frequency synthesizers can support different operating modes [33].

B. OFF-CHIP COMPONENTS

The CMOS process is the most commonly used technology for GPS receivers [10]–[25]. However, [26] has used bipolar technology and [8], [9], [30] have used the BiCMOS technology. The GPS receiver front end has used off-chip components such as the SAW filter for image rejection [8],

the external balun for single to differential (S2D) conversion, and other impedance matching networks for minimizing the NF and improving the sensitivity [9], [15], [17]. The SAW filter has high Q and sharp filter characteristics, but it adds to the insertion loss, and a driver circuit is also required, which increases the power dissipation of the circuit. Due to lower frequencies, the GPS receiver LNA needs higher high Q off-chip inductor values for input matching. Therefore, the on-chip inductors are introduced to deal with the issue, however, at the cost of the area and lower Q. The narrow band mixer first receiver architecture with optimized noise performance can be adopted for the GPS receiver front end since it will deal with both area and external component issues simultaneously.

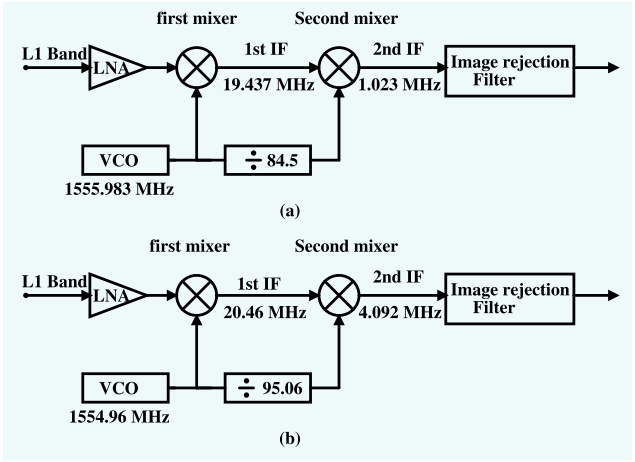

FIGURE 7. Single band dual downconversion frequency plan (a) Approach I. (b) Approach II [26].

C. LNA

The LNA is the first building block of the receiver. It receives the signal with poor strength from the antenna and amplifies it with little noise addition. Fig.10 shows the pie-chart of the various LNA topology distribution used in the GPS receiver. It is observed from the pie-chart that 21.74% of the literature have used single ended common source (CS) topology; however, 34.78% have used differential CS, and the other 34.78% have used single to differential CS. 4.35% of the GPS receivers have used resistive shunt, and the other 4.35% have used transconductance LNA topology. Therefore, 90% of the GPS receivers have used single ended, differential, and single to differential CS inductive degenerated LNA topologies. All these topologies are narrowband due to narrowband input matching and LC tank load. The various Q enhancement techniques such as spiral geometry and AI-based layout optimization techniques are adopted for maximizing Q, which helps to achieve higher gain, better selectivity, and lower NF. The LNA topologies are described below:

1) INDUCTIVE DEGENERATED SINGLE ENDED LNA

It receives the single ended RF input signal and gives a single ended signal at the output, as depicted in Fig. 11(a) [54], [55].

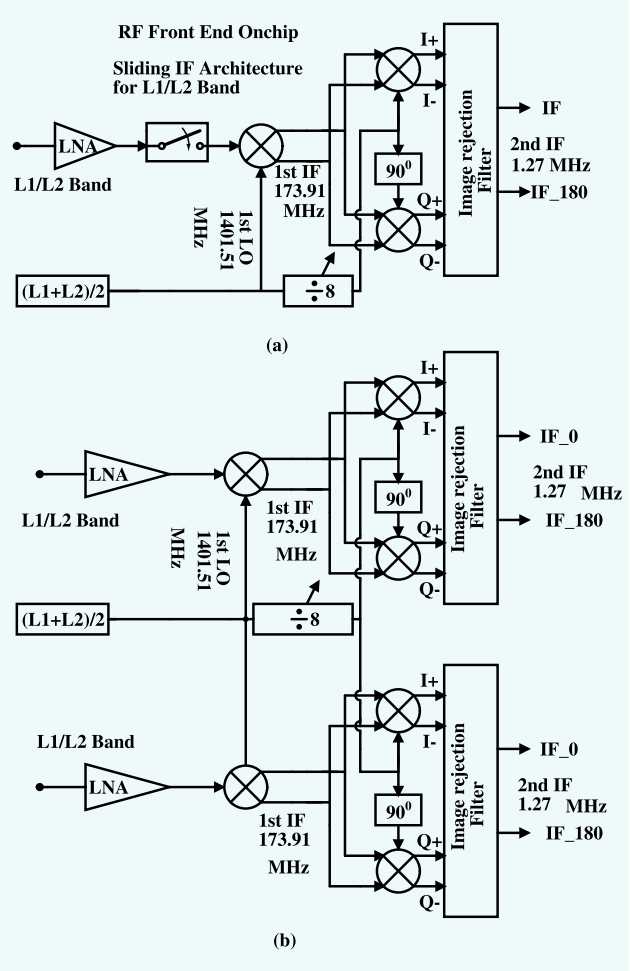

FIGURE 8. Dual band dual downconversion frequency plan (a) Single chain L1/L2 selectable receiver. (b) Dual chain with separate L1 and L2 receiver [6].

The primary issue with this topology is that a double balanced mixer is mostly used after LNA, requiring differential input. Thus, we need one extra circuit to convert the single ended output from the LNA to the differential to feed it to the mixer. The single ended LNA also suffers from the substrate noise.

2) INDUCTIVE DEGENERATED DIFFERENTIAL LNA

The differential LNA topology is depicted in Fig. 11(b), which needs extra balun at the input side to feed into its differential inputs. Therefore, this increases the NF and also occupies a large area. However, the circuit is immune to the substrate noise and provides a differential output that can be used directly in the double balanced mixer. The differential LNA can achieve similar noise performance at twice the power dissipation of single ended version [29].

3) INDUCTIVE DEGENERATED SINGLE TO DIFFERENTIAL LNA

Fig. 11(c) shows single to differential conversion LNA. This LNA exploits the benefit of both the single ended and the differential topologies. It offers 6 dB extra gain compared to single ended and has less area overhead than differential.

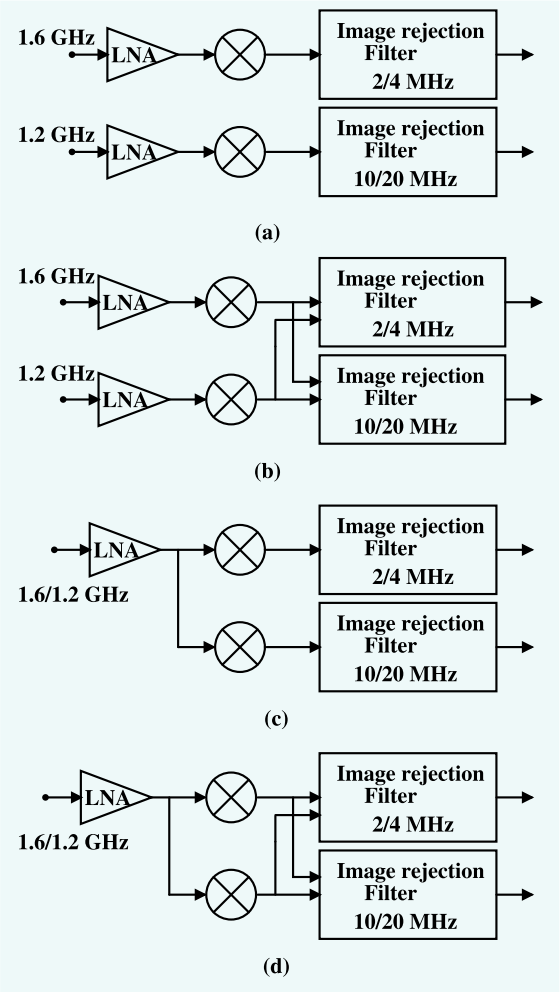

FIGURE 9. Multiband dual downconversion frequency plan of the GNSS signals in (a) different bands with separate filters. (b) different band with the same filter. (c) the same band with separate filters. (d) the same band with the same filter [33].

The circuit is immune to the substrate noise. However, the circuit suffers from amplitude and phase mismatch at high frequency due to parasitics. Therefore, it is always challenging to design completely single ended to differential conversion circuits.

4) RESISTIVE SHUNT FEEDBACK LNA

Fig. 11(d) shows resistive shunt feedback LNA [56], [57]. This LNA provides wide band input matching, and it is also free from inductors. It helps to achieve the desired performance at very low power dissipation. However, it suffers from a high noise figure and requires high quality band select filter.

D. VARIABLE GAIN AMPLIFIER (VGA)

The VGAs are the circuits used to adapt the gain of the entire receiver chain as per the strength of the incoming signal at the antenna. It helps to avoid the saturation of the transistors and achieve an optimum signal level at the ADC input [2]. Variable gain can be achieved through various circuits like a combination of VGA and automatic gain control (AGC)

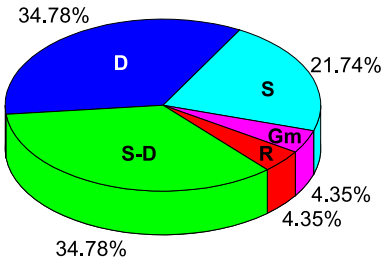

FIGURE 10. Pie-chart showing LNA topology distribution S-single ended, D-differential,S-D-single to differential, R- resistive shunt and Gm - transconductence LNA.

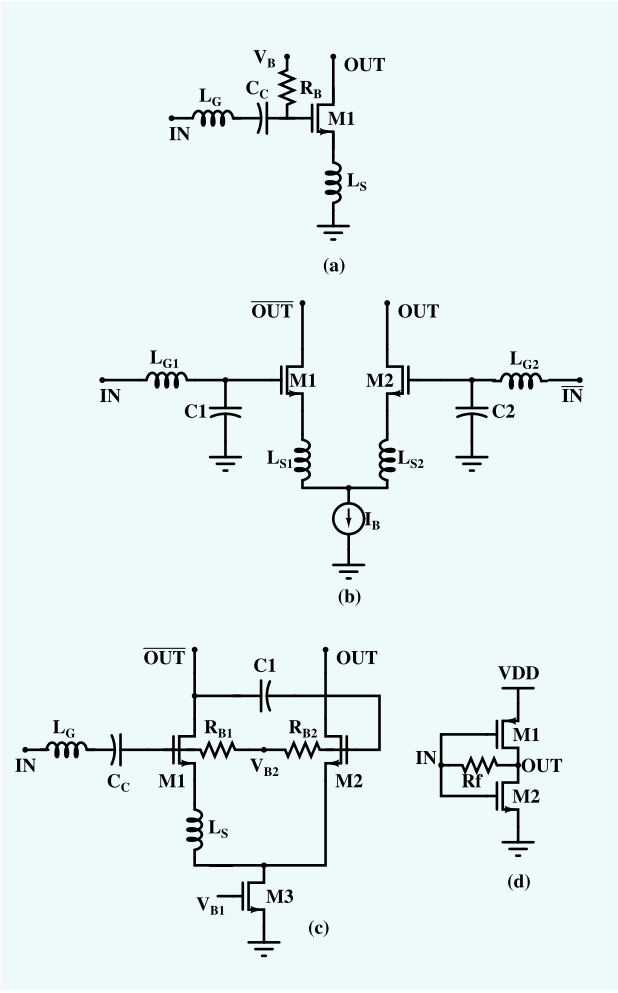

FIGURE 11. The LNA topologies. (a) Single ended LNA [3]. (b) Differential LNA [13]. (c) Single to differential LNA [7]. (d) Resistive shunt [57].

loop, programmable gain amplifier (PGA) [17], [32], variable gain complex filter [6], [57] variable gain LNA, dual gain LNA, etc. In the AGC loop, the gain of the VGA is automatically controlled by monitoring the output of the ADC [11]. Fig. 12(a) depicts variable gain LNA that achieves the variable gain through load resistance variation. The Fig. 12(b) depicts the dual gain LNA topology that sets either V_{HI} or V_{LO} depending upon the control voltage. Dual gain LNA helps to adapt the use of active and passive antennas in the GPS [17].

The Fig. 12(c) shows the another architecture of variable gain LNA that helps to achieve gain variability by controlling the bias point of the transistor. Based on the survey, achieving linear programmable gain is easier in the baseband portion of the receiver compared to the receiver front end.

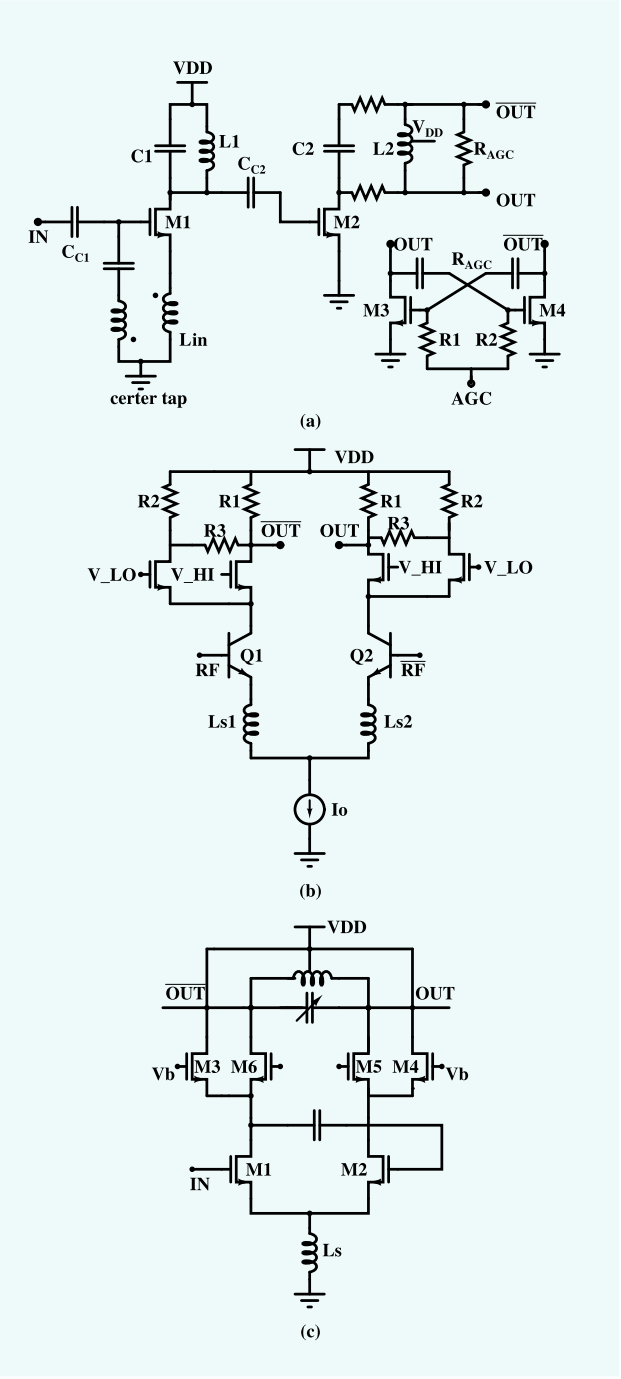

FIGURE 12. The VGA architectures. (a) Variable Gain LNA: Architecture I [22]. (b) Dual gain LNA [8]. (c)Variable gain LNA: Architecture II [17].

E. MIXER

The mixer receives the radio frequency (RF) from the LNA, LO from the VCO, and performs frequency translation to produce an intermediate frequency (IF) [58]. As shown in Fig. 4, the mixer given in the literature can be broadly categorized into active and passive. Based on single ended and differential RF input, it can further be divided into single balanced and double balanced. The active mixers can also be classified as current mode, sub-harmonic, and folded cascode mixers. The mixer architecture choice depends on the GPS receiver specifications, such as the targeted gain, noise figure, linearity, and power dissipation. Due to its higher linearity characteristics and lower power consumption, the passive mixer is used for GPS application [15], [16]. Therefore, the passive mixers are an excellent choice for ultra-low power specifications. Fig. 13(a) depicts the passive mixer, which offers better performance in terms of flicker noise as transistors are biased in the triode region and have less area overhead [14]. The active mixer offers higher conversion gain at the cost of higher power dissipation and occupies comparatively more area. Fig. 13(b) depicts a single balanced active mixer that offers low LO-RF isolation compared to the double balanced active mixer that is shown in Fig. 13(c). The doubled balanced active mixer is the most widely used mixer topology in the GPS receivers. Many literatures have adopted several techniques to improve power dissipation, flicker noise, and linearity performance in the conventional Gilbert cell mixers.

In [13], on-chip load, along with the current reuse technique adopted in the Gilbert cell mixer, helps to achieve the performance at lower power dissipation. However, [6] has used the current bleeding technique to achieve higher gain at lower supply voltage and lower flicker noise due to reduction in dc current [11]. As the gilbert mixer has more stacked transistor that reduces the overdrive voltage, removal of tail current improves linearity. Fig. 13(d) demonstrates the folded cascode mixer that provides higher voltage headroom to transistors and also allows to choose different currents for input transistors and switching core [9]. The folded cascode mixer improves the linearity, however, at the cost of adding an extra inductor that increases the chip area. The subharmonic mixer is illustrated in Fig. 13(e). The required LO signals in the subharmonic mixer are just half of that needed in the Gilbert cell mixer. Thus, in the case of the subharmonic mixer, the frequency synthesizer design for dual band operation becomes easier as both LO frequencies come closer in value [12].

F. IMAGE REJECTION USING FILTER

The filter is a significant section in the receiver design. The filter discards higher frequencies and selects the desired one providing image rejection. The paper discusses the circuit level methods that include the filters followed by their implementation in system-level design (hartley or weaver receiver architecture) to observe the overall performance. Most of the receivers have exploited hartley architecture, while some have used weaver architecture [21], [25]. The GPS receivers have an added advantage due to P-code which guarantees no signal in the 10 MHz range on both sides; thus, image rejection constraint is not stringent. Some literature has used

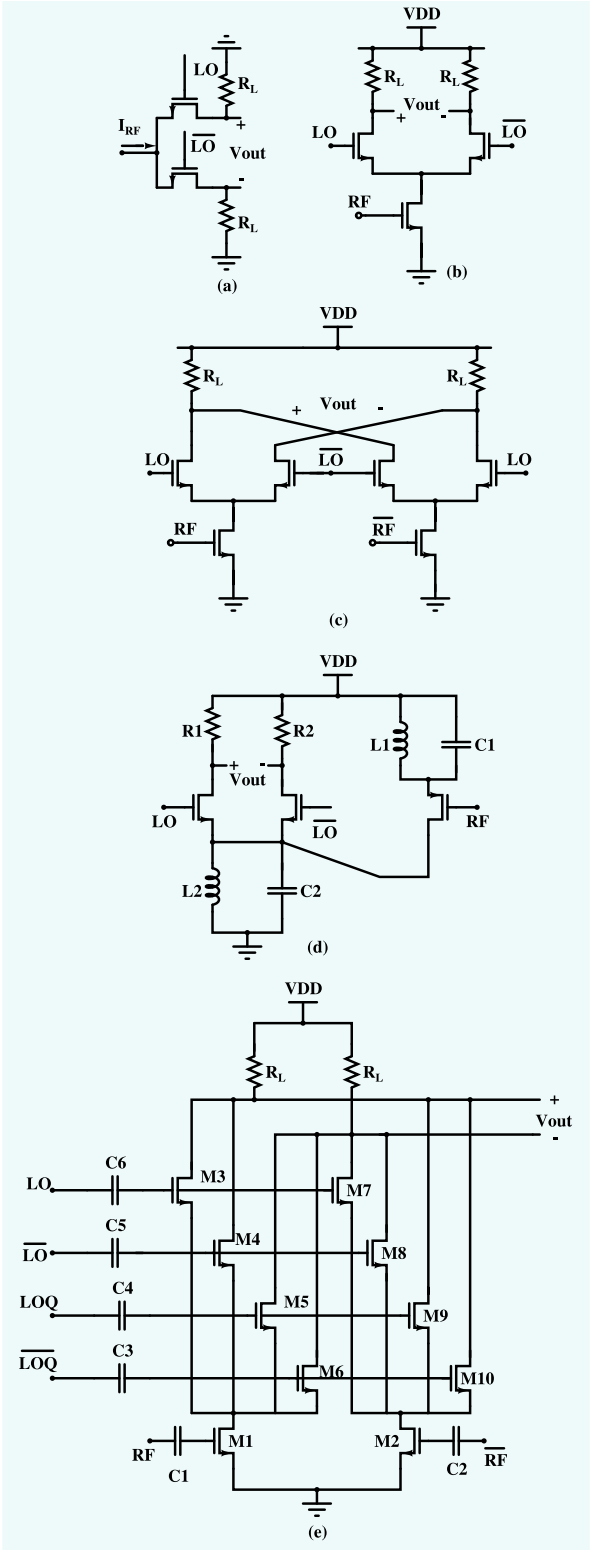

FIGURE 13. The mixer topologies. (a) Passive current mode mixer [17]. (b) Single balanced active mixer [52]. (c) Double balanced active mixer [11]. (d) Folded cascode mixer [22]. (e) Subharmonic mixer [12].

the BPF after antenna to attenuate adjacent channel interference [3]. After surveying several literatures, the filters used in the GPS receivers can be classified into active and passive filters. The passive filters include the SAW filter and passive polyphase filter (PPF). However, the active filters include complex bandpass filters (CBPF). The digital assisted IQ calibration (DAIQC) technique is further used for improving the image rejection. The CBPF is the most commonly used for image rejection [3], [15]–[17], [59]. However, [7], [11] have used PPF. In the literature [23], [27] a combination of the CBPF and PPF is used. It will help to improve image rejection and increase the voltage gain of the entire circuit. The image rejection technique can be implemented in both the analog and digital domains. The various filters used for image rejection can be classified as:

1) POLYPHASE FILTER

The polyphase filters can be divided into two categories, the first is passive RC, and the second is active polyphase filters (APF). The PPF includes passive components like R, and C. Fig. 14(a) depicts the third-order PPF. The amplitude of the image frequency is reduced around the pole frequency introduced by the PPF. It gives the narrow-band rejection. The number of cascaded stages determines the bandwidth and image rejection ratio. The multistage filter suffers from loss as each stage loads the previous stage. The loading is overcome by using an interstage buffer. However, the buffer boosts the signal strength at the cost of higher power dissipation and chip area. Cascading N number of stages reduces the sensitivity towards component mismatch, process variation and provides improved image rejection. They offer limited maximum operating frequency. The active polyphase filters involve active components like Op-amp and transconductor. The active polyphase filter has the advantage of a small chip area, high gain, and high image rejection compared to their passive counterparts. The polyphase filter provides a good IMRR by using Op-amp circuits. Extra buffer circuits are not required. However, the circuit is comparatively complex; it offers a higher operating frequency range. The third-order PPF provides more than 30 dB image rejection, even with 20% RC variation [11].

2) CBPF

The CBPF can be based on either Gm-C or the active RC approach. Active RC based CBPF provides improved linearity performance than the Gm-C approach [16] however, Gm-C based filter dissipates less power compared to the active RC-based. Fig. 14(b) and Fig. 14(c) demonstrate the CBPF based on the Gm-C and active RC approach, respectively. The image rejection is deteriorated due to the I/Q mismatch caused by the component imparity in various filter topologies. To achieve higher image rejection, various topologies have been adopted. In [6] variable gain complex filter based on Gm-C technique is used to achieve the image rejection up to 20 dB along with variable gain, and [16] has used CBPF implemented with the help of a biquadratic unit cell to achieve image rejection of 23 dB. However, [15] has adopted an active complex polyphase filter, which is fifth-order active-RC leapfrog type LPF and, achieved wideband

image rejection up to 30 dB. While [17] has used active sixth-order Chebyshev CBPF, which is realized using two real LPFs and provides image rejection up to 39.1 dB and variable gain also.

3) DAIQC

Fig. 14(d) depicts the DAIQC technique, which involves IQ calibration to reduce the component mismatch. Ideally, the amplitudes of the I and Q signals are equal with 90° phase shift. However, in actual circuits, there exists some β and ϕ mismatch in the amplitude and phase of the I and Q signals. The solution for this mismatch is to perform the calibration for cancelling out the errors. The digital IQ calibration technique reduces the mismatch between I and Q branches, thus improving the IMRR up to 50 dB [25], [32], [33], [60].

G. ADC

ADC block is used after the image rejection filter in the GPS receiver chain. The ADC converts the incoming analog signal into digital in order to process in the baseband. A typical 103 dB cascaded gain before the ADC is required in the receiver to get up to 400 mV full-scale range input of the ADC [32]. The 1-bit ADC used to be the choice for low cost receivers; however, we prefer to have multi-bit ADC for improved SNR performance. The sampling rate of the ADC in the low-IF receiver is limited by the bandwidth of the signal not the highest frequency component present in the signal. Based on the literature survey, the ADC used for the GPS receiver include 1-bit clocked comparator [3], [8], 2-4 bit charge pump-based ADC (Flash ADC) [6], [11], [15]–[17], [22], [31], [33] and several variants of sigma-delta ADC (SDADC) [7], [9], [10], [19], [41]–[44]. While [38] has used 9-bit SAR ADC. A wide dynamic range 1-bit clocked comparator helps to reduce power consumption by eliminating the AGC loop. The 1-bit ADC is the simplest one in terms of architecture; however, it leads to SNR degradation is depicted in Fig. 15(a). The flash ADC has been implemented in 50% of GPS receiver front ends. This ADC gives better SNR performance compared to the 1-bit. The basic charge pump-based 2-bit flash ADC architecture is represented in Fig. 15(b). The GPS receivers with ADC of lower resolution and dynamic range employee automatic gain control (AGC) loop to enhance the overall dynamic range of the system. However, a low pass continuous-time passive SDADC has achieved up to 40 dB dynamic range with oversampling ratio (OSR) of 16 and 1-bit local ADC [7]. A high-resolution ADCs help in DC offset cancellation in the digital domain [9]. In the case of multi-mode receivers, the dynamic range reduces with increased bandwidth.

The SDADC can be broadly categorized into discrete and continuous time counterparts. Since the power reduction is an important constraint for the GPS receivers, continuous-time (CT) architecture is preferred over discrete-time (DT) architecture due to reduced Op-amp requirements and inherent anti-aliasing. The continuous time SDADC can further be divided into low pass SDADC and bandpass SDADC.

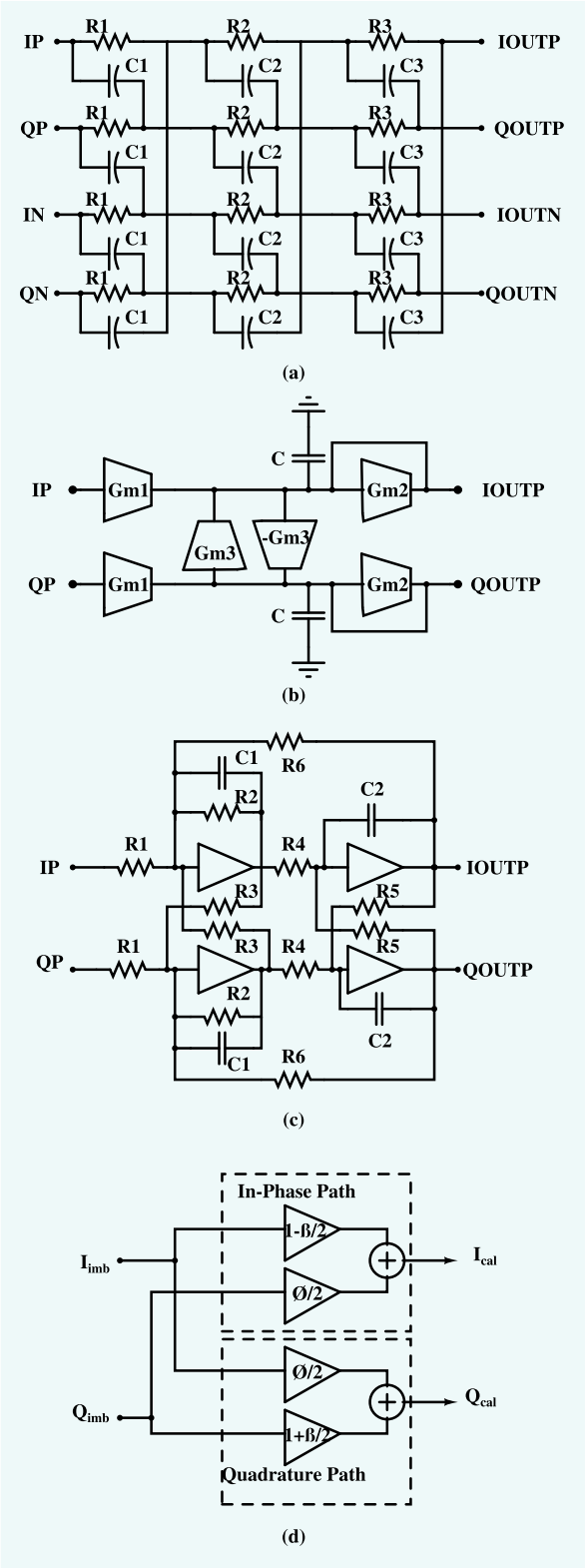

FIGURE 14. The image rejection filter topologies. (a) The third-order Polyphase filter [11]. (b) CBPF based on Gm-C [6]. (c) CBPF based on Active RC [16]. (d) Digital IQ calibration [33].

The bandpass SDADC is preferred over the low pass SDADC due to its lower OSR requirement to achieve the same SNR. The architecture of the bandpass SDADC can also

be categorised into quadrature and non-quadrature topology. The quadrature SDADC differs from a low pass counterpart in terms of the complex bandpass loop filter [10]. The quadrature architecture is preferred over non-quadrature as it reduces the number of Op-amps and provides higher image rejection [19]. In [6], 1-bit 2-2 cascade SDADC topology has achieved 66 dB of dynamic range. However, [10] has used quadrature continuous SDADC based on Gm-C implementation to achieve 62 dB of dynamic range with 14.2 mW power dissipation. While in [19] the 2nd-order CT SDADC with resistive DAC feedback achieves 65 dB dynamic range and dissipates only 4.2 mW power. Fig. 15(c) shows the basic block diagram of SDADC. A more detailed description of SDADC design for GPS application can be found in [19].

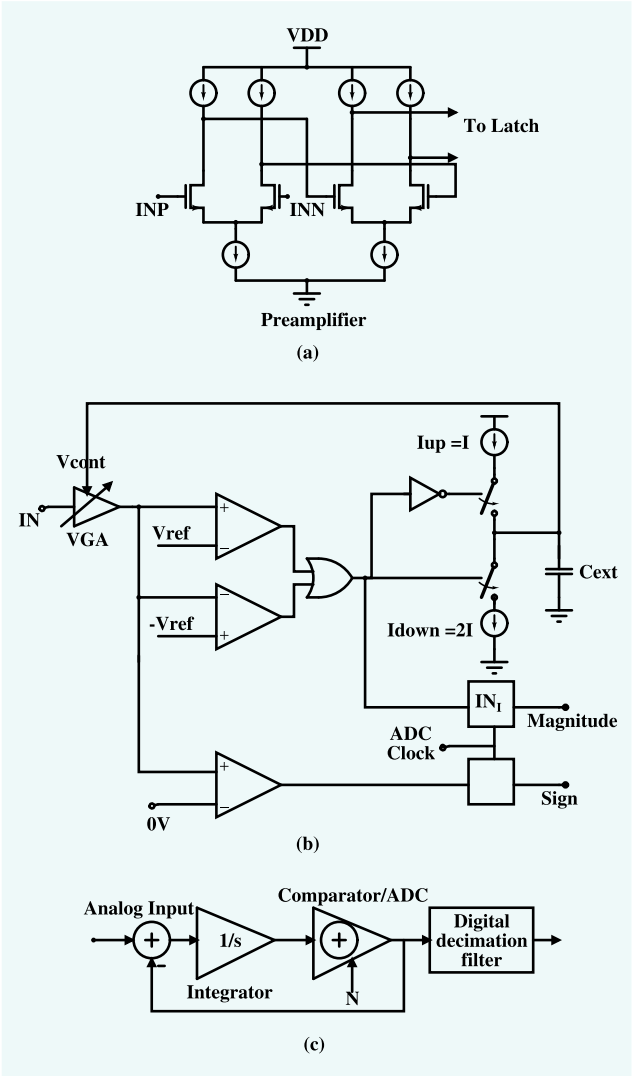

FIGURE 15. The ADC topologies. (a) 1-bit clocked comparator (b) 2-bit ADC [6]. (c) Sigma delta ADC [52].

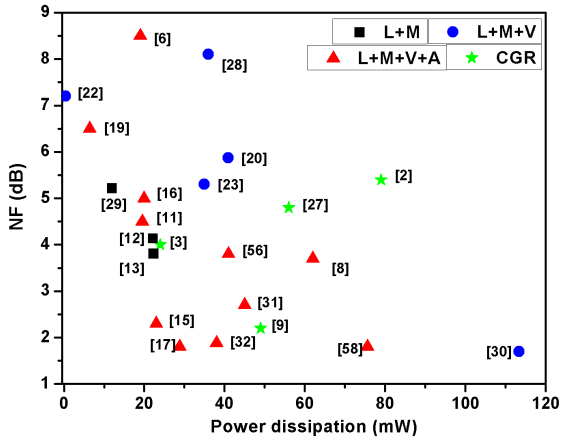

FIGURE 16. The NF versus power dissipation for the surveyed papers.

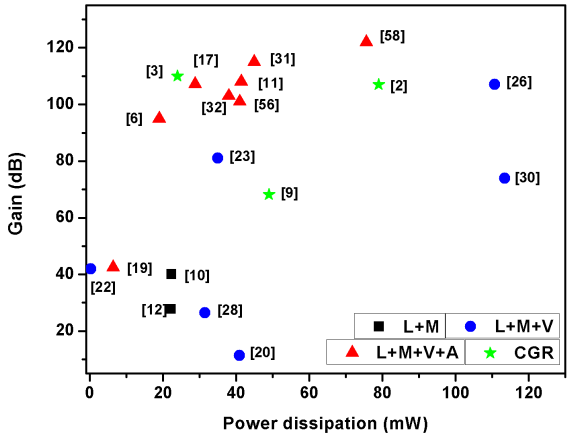

FIGURE 17. The gain versus power dissipation for the surveyed papers.

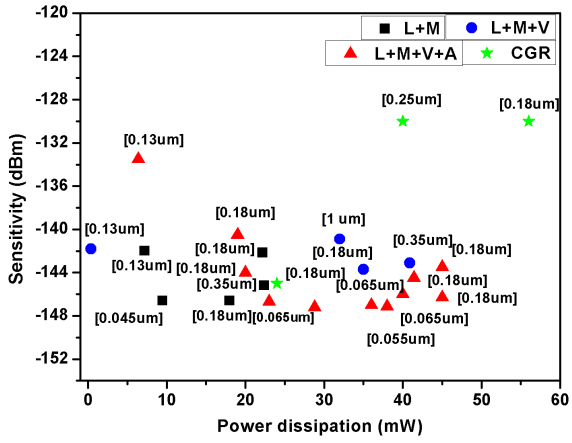

FIGURE 18. Sensitivity for reported power dissipation and technology node of surveyed GNSS systems.

V. STATE OF THE ART DISCUSSION

This section presents the result of detailed research on the GPS receiver front end. Based on the density of the blocks present in the RF front end, the published literature of the GPS receiver front ends can be categorized as L+M (LNA+Mixer), L+M+V (LNA+Mixer+VCO), L+M+V+A (LNA+Mixer+VCO and ADC), and complete

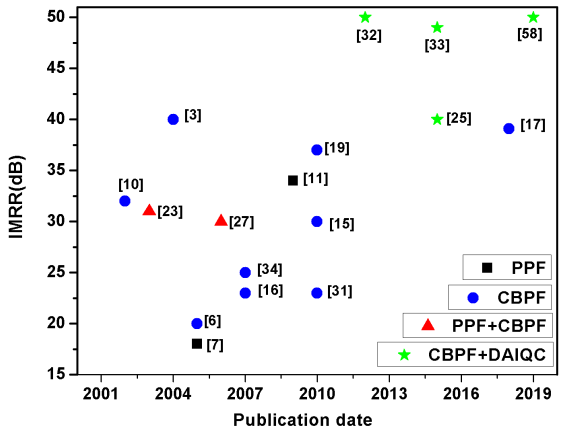

FIGURE 19. Image rejection ratio reported by publication date for surveyed GNSS systems that utilized various Image rejection technique spanning over PPF, CBPF, DAIQC.

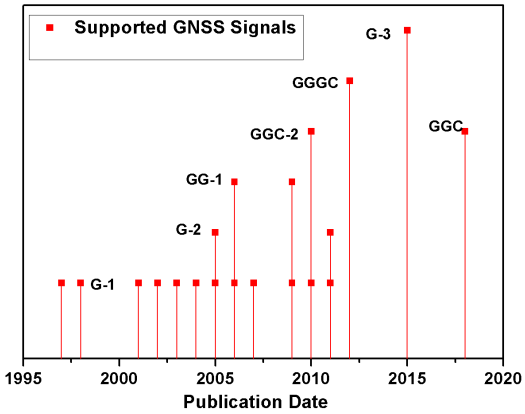

FIGURE 20. The supported GNSS signal versus publication date.

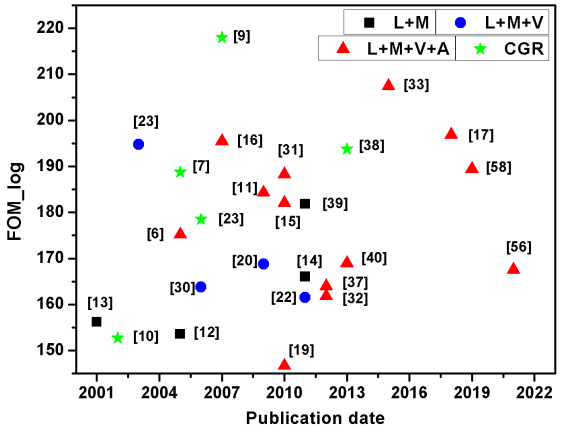

FIGURE 21. Figure of merit versus publication date for surveyed papers of various categories L+M, L+M+V, L+M+V+A, CGR.

GPS receiver (CGR). The GPS receivers have important parameters such as sensitivity, image rejection, and power dissipation. In order to achieve better sensitivity, the NF of the system should be minimum, and the gain should be maximum. The LNA is a critical block in determining the NF of the entire receiver system. In the literatures, the LNA gain ranges between 15 to 30.4 dB, and NF varies from 0.8 to 7 dB while consuming 3–21 mW power from 1–3 V supply voltage.

Fig. 16 presents the plot of the total NF of entire receiver systems versus power dissipation according to the abbreviated domains. This graph clearly illustrates that the maximum work done is on the entire RF front end (L+M+V+A). This graph shows that it is possible to achieve good NF at the cost of higher power dissipation and vice-versa. An optimized performance can be obtained by trading off both the performance parameters. The minimum achieved NF is around 1.7 dB at the cost of 113 mW power dissipation [30]. [22] has tried to reduce the power dissipation and make ultra-low power GPS receiver front end with power dissipation of 0.352 mW; however, at the cost of NF of 7.2 dB. [6], [28] have poor noise performance due to lack of noise optimization.

Fig. 17 presents system survey results for the gain of the entire receiver versus power dissipation with respect to various categories. The maximum gain achieved for the L+M category is 40 dB [10]. The maximum gain achieved by the receivers of type L+M+V [26], and CGR [2] are in the same range of 100 dB; however, [26] has used dual downconversion; therefore, more number of blocks and more gain, however, at the cost of higher power dissipation. While the maximum gain achieved in the L+M+V+A category is 122 dB [60]. The graph depicts that the most of the work that belongs to either the L+M+V+A or CGR category has achieved the gain between 90-120 dB with power dissipation ranging between 20-50 mW. [17] has achieved 1.7 dB NF at the cost of only 29 mW power dissipation due to improved flicker noise performance and lower power dissipation of passive mixer using 180 nm CMOS process. The extra circuitry of TIA is added to compensate for lower gain due to the passive mixer.

Fig. 18 depicts the sensitivity versus power dissipation curve with regards to the various categories and technology nodes. It is observed from the graph that most of the work done in the GPS receiver design is in a technology node of either 0.18 μm and 0.13 μm, and the power dissipation is between 20 mW to 50 mW. [17] achieved the sensitivity of -147.2 dBm with the power dissipation of 28.8 mW in the L+M+V+A category, and the technology node used for design is 0.18 μm. For the sake of representation, -165 dBm sensitivity data is omitted from the Fig. 18; however, it is mentioned in Table 2. The best achieved sensitivity to date for GPS receivers is -165 dBm through optimization in the baseband. Fig. 16, Fig. 17, and Fig. 18 together demonstrate the higher the gain, the better is the noise figure and the sensitivity of the GNSS system.

The IMRR is another critical constraint in the GPS receiver design as it mostly uses the low-IF receiver architecture. Fig. 19 demonstrates the IMRR achieved using different image rejection techniques used in the literature versus publication date. The graph depicts the minimum image rejection

TABLE 2. Performance summary of the state-of-the-art GNSS receivers of last 20 years.

Reference	Chip NF(dB)	Gain (dB)	IIP3 (dBm)	IMRR (dB)	Sensitivity (dBm)	Power (mW)	FOM_1 (in log)	FOM_2 (in log)	Category	Receiver architecture	Year of Publication
[56]	3.8	101	-42	28	-145.2	41	152.3	NA	L+M+V+A	low-IF	2021
[58]	1.8	122	-30	50	-147.2	75.6	152.3	NA	L+M+V+A	low-IF	2019
[17]	1.8	107.2	-19.325	39.1	-147.2	28.8	195	214.6	L+M+V+A	low-IF	2018
[25]	7	NA	NA	40	-142	7.2	NA	NA	L+M	low-IF	2015
[33]	2	122	-15	49	-147	36	205.4	229.9	L+M+V+A	low-IF	2015
[40]	3	60	-21	43	-146	40	165.9	187.4	L+M+V+A	low-IF	2013
[38]	2.1	78	-8	33	-146.9	26	191.6	208.1	CGR	low-IF	2013
[37]	2.7	110	-48	28	-143.5	45	161.2	175.2	L+M+V+A	low-IF	2012
[32]	1.88	103	-51	50	-147.12	38	159.9	184.9	L+M+V+A	low-IF/Zero-IF	2012
[14]	2.4	68	-32	NA	-146.6	18	163.6	NA	L+M	low-IF	2011
[22]	7.2	42	-35.8	6	-141.8	0.352	154.3	157.3	L+M+V	low-IF	2011
[39]	2.4	37	-3.5	NA	-146.6	9.49	179.4	NA	L+M	low-IF	2011
[47]	NA	NA	-5	40	-165 [c]	18	NA	NA	CGR	low-IF	2011
[31]	2.7	115	-29	23	-146.3	45	185.5	197	L+M+V+A	low-IF	2010
[15]	2.3	48	-5	30	-146.7	23	179.7	194.7	L+M+V+A	low-IF	2010
[19]	6.5	42.5	-30	37	-133.5	6.4	140.6	158.6	L+M+V+A	low-IF	2010
[20]	5.87	11.4	6.1	NA	-143.13	40.9	162.9	NA	L+M+V	low-IF	2009
[11]	4.5	108	-28[b]	34	-144.5	41.4	179.8	196.8	L+M+V+A	low-IF	2009
[45]	3.2	NA	NA	40	-165[c]	19.5	NA	NA	CGR	low-IF	2009
[44]	NA	42.5	NA	NA	NA	7.2	NA	NA	L+M+V+A	low-IF	2009
[9]	2.2	68.2	24	NA	-146.8	49	215.7	NA	CGR	Zero-IF	2007
[16]	5	65	2	23	-144	20	190.4	201.9	L+M+V+A	low-IF	2007
[34]	4.3	112	-65	25	-144.7	12	150.6	163.1	L+M+A	low-IF	2007
[27]	4.8	92	-10	30	-130[c]	56	173.7	188.7	CGR	low-IF	2006
[30]	1.7	74	-30	NA	-147.3	113.4	162	NA	L+M+V	Zero-IF	2006
[8]	3.7	103	NA	40	-152[c]	62	NA	NA	L+M+V+A	low-IF	2006
[7]	2	38	5	18	-154[c]	84	186.7	195.7	CGR	low-IF	2005
[12]	4.13	27.7	-19	NA	-142.16	22.2	146.7	NA	L+M	low-IF	2005
[6]	8.5	95	-30	16	-140.5	19	166.7	174.7	L+M+V+A	low-IF	2005
[3]	4	110	NA	40	-145	24	NA	NA	CGR	low-IF	2004
[23]	5.3	81	-4	31	-143.7	35	189.4	204.9	L+M+V	low-IF	2003
[10]	1.5[a]	29.5[a]	-6[a]	32	-130	40	151.2	167.2	CGR	low-IF	2002
[13]	3.8	40	-25.5	NA	-145.2	22.4	152.3	NA	L+M	low-IF	2001

a=Only LNA, b= LNA + Mixer, c = sensitivity values are already given in literatures.

achieved is around 18 dB by using the 2nd order PPF [7] while the image rejection of 34 dB is reached by using the 3rd order PPF [11]. Based on the survey provided in Fig. 19, the higher order CBPF has achieved more than 40 dB of IMRR [3], [17], [19]. Therefore, the CBPF is the preferred filter for the GPS front end. The Fig. 19 clearly depicts that trend has moved from the use of standalone CBPF to the use of DAIQC along with CBPF for better image rejection. The maximum achieved image rejection is 50 dB by using DAIQC besides CBPF [51].

Another approach to achieve higher accuracy in the GPS reception is to incorporate multi band multi GNSS receiver system along with the several circuit level optimization techniques. It provides enhanced sensitivity over a single band single GNSS counterpart. Fig. 20 demonstrates the supported GNSS signals versus publication date. The abbreviation G denotes the GPS, GG denotes both GPS and Galileo, GGC denotes the GPS, Galileo, Compass, and GGGC denotes the band of GPS, Galileo, Glonass, and Compass. The digits 1, 2, and 3 indicate L1, L1 & L2, and L1, L2 & L5 bands of the corresponding GNSS. It is pretty clear from the graph that the trend has now shifted from single to double and multiple bands GNSS receiver. Therefore, it can be concluded that the GNSS receiver design is mainly focused on the multi band multi GNSS in the future.

Based on the literature study, useful FOMs for the GPS receiver can be derived combining the performance parameters which help to stimulate the growth for upcoming designs and is stated as:

$$\text{FOM}_1 = 10log\frac{(\text{Gain} * \text{linearity})}{(\text{power} * \text{Sensitivity})} \tag{2}$$

$$\text{FOM}_2 = 10log\frac{(\text{Gain} * \text{linearity} * \text{IMRR})}{(\text{power} * \text{Sensitivity})} \tag{3}$$

where all the parameters are converted into the linear scale. In order to bring uniformity in the sensitivity values, the formula used for calculation of the sensitivity in the Table 2 is given by [11]:

$$Sensitivity = \left(\frac{E_b}{N_o}\right)_{\min} dB + 10\log R_b[dB - Hz] + N_o\left[\frac{dBm}{Hz}\right] + NF[dB] \tag{4}$$

The calculation is based on the assumption that a minimum Eb/No of 8 dB is required at the correlator, Rb is 50 bps for the L1 band, and No equals to −174 dBm/Hz. Fig. 21 depicts FOM_1 of the state-of-the-art GNSS receivers of the last 20 years versus publication date according to the abbreviated domains. Table 2 provides detailed performance parameters and FOMs of the state-of-the-art GNSS receivers of the last 20 years. The optimum choice for the performance parameters of the entire GNSS receiver can be estimated from the graphical analysis of the existing state-of-the-art. The gain can be chosen more than 100 dB, and the noise figure can be around 2-3 dB with the IIP3 requirement of −10 to −15 dBm. While, the sensitivity requirement can be around −145 dBm with total power dissipation of 20-50 mW, and FOM can be around 205 dB in log scale as per the literature survey.

VI. CONCLUSION

In this paper, a detailed and comprehensive survey has been done on the performance requirements of the GNSS receiver system that includes gain, noise, sensitivity, linearity, and the IMRR. Incorporating image rejection schemes along with the appropriate frequency planning and the right choice of block architecture helps to enhance the performance matrix of the GPS receiver front ends in the congested spectrum. Based on the literature survey, it is observed that more than 88% of the GPS receiver front end uses low-IF receiver architecture as most of the GPS signal energy lies at the centre frequency. This paper described several topologies of LNA, mixer, filter, ADC used in the GPS receivers and organized them into several categories. The promises of the GPS receiver of exact user localization can be achieved if the designers successfully remove image interference through multiple image rejection techniques. Various techniques such as polyphase filters, CBPF, and DAIQC are used to improve the IMRR in the low-IF receiver. The best image rejection performance achieved until now is 50 dB using the DAIQC technique besides CBPF [32]. Due to the very weak signal received from the satellite, the GPS receiver should achieve higher sensitivity. The highest sensitivity achieved till now is −165 dBm by optimizing the baseband architecture for correlation efficiency [45]. Although, the most commonly used receiver architectures, sub-blocks topologies used for the GPS receiver application are described in this review work, the reader can explore the new receiver architectures such as the mixer first receiver architecture with optimized performance, multi-band multi GNSS receiver, active inductor approach to minimize the areas and having tunability, improved on-chip inductor Q performance and new sub blocks topologies for the performance improvement of the GPS receiver. It is still a challenging task to achieve the optimized performance, including the support of multiple bands of GNSS on a single chip. Moreover, the paper proposed a novel FOM combining all these system parameters and will be an excellent reference used in the future.

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