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Wide Power Dynamic Range CMOS RF-DC **Rectifier for RF Energy Harvesting System: A Review**

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ABSTRACT This article investigates the latest research outcomes on the wide power dynamic range (PDR) CMOS RF-DC rectifier for on-chip radio frequency energy harvesting (RFEH) system as a viable approach to extend the high power conversion efficiency (PCE) operating range which is limited by the varying nature of the available far-field RF power. The significance of enhancing the rectifier's PDR is that it offers a more reliable operation of RFEH in real-life applications. Therefore, this review seeks to navigate the research and development focus of the RFEH system towards extending the PDR of the CMOS RF-DC rectifier by providing analysis of the effect of state-of-the-art PDR extension techniques and their design tradeoffs. The review encapsulates the transmission of the RF power, a brief overview of the RFEH front-end circuit, and a comprehensive review of the CMOS rectifier design focusing on PDR. At the end of this article, we discuss the future design aspects to address the limitation of the RFEH system. Recent research shows that extending the rectifier's PDR will enhance the overall performance of the RFEH system.

INDEX TERMS CMOS rectifier, power conversion efficiency (PCE), power dynamic range (PDR), RF energy harvesting, RF power transmission.

I. INTRODUCTION

In the era of industrial revolution 4.0 (IR4.0), there has been an exponential rise in the number of users of low-powered electronic devices to cope with the demand for Internet of Everything (IoE) [1] applications such as healthcare monitoring, industrial monitoring, wearables, edge computing, smart cities, etc. [2]–[5]. The increasing energy demand in the form of batteries used to power these portable devices is unsustainable due to their maintenance constraints and high replacement costs. Not to mention that the constant use of highly flammable batteries poses safety concerns [6] and also causes pollutions to the environment at its disposal [7]. As an alternative solution, prominent research works [8]–[12] has been carried out on radio frequency (RF) based wireless power transmission or RF energy harvesting (RFEH) for its potential as an alternative energy source for powering

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portable low-power devices such as biomedical implants, radio frequency identification device (RFID) and wireless sensor nodes (WSNs) enabling the IoE applications.

The portability, flexibility and scalability advantages from using the RFEH system in CMOS technology for large scale deployment of WSNs portray it as a preferred solution over other ambient energy sources. Nevertheless, challenges remain in designing a highly efficient RFEH system. As a core front-end circuit in the RFEH system, an RF-DC rectifier plays a vital role in converting the harvested power from the RF input to a usable DC output, as shown in Fig. 1 whereby the RF energy harvester front-end circuit consists of a receive antenna, an impedance matching network and a RF-DC rectifier. Therefore, improving the efficiency of the RF-DC rectifier will significantly enhance the overall performance of the RFEH system.

To increase the DC output, the RF-DC rectifier usually consists of a cascade of multiple stages. Each stage rectifies the RF input and feeds its DC voltage into the subsequent



FIGURE 1. Block diagram of RF energy harvester front-end circuit.

stages, resulting in voltage multiplication. The final rectifier output DC voltage (V_{ROUT}) is proportional to the number of optimized cascaded stages. Conventional diode-based rectifier such as Dickson rectifier [13] suffers from poor sensitivity and low power conversion efficiency (PCE) at low input power level due to its high dropout voltage, especially in multistage configuration. On the other hand, a cross-coupled differential-drive (CCDD) rectifier [14], which has achieved improvement in sensitivity and higher peak PCE compared to the Dickson rectifier, is widely adopted for its performance to be used in the RFEH system. However, a reverse leakage current is generated in the CCDD rectifier as the rectifying crosscoupled transistor conducts in the reverse direction when the DC output voltage is higher than the RF input signal in every negative cycle, resulting in a limited power dynamic range (PDR). The PDR is described as the RF input power range whereby the rectifier is operating at a high PCE. This reverse leakage current becomes severe as the DC output voltage of the CCDD rectifier increases and thus further degrading the PCE and the PDR in a multistage configuration.

Several design architectures and circuit techniques have been explored in [15]-[17] to improve the sensitivity and the peak PCE of the rectifier. Yet, there is only a handful of research work aims to achieve a wider PDR in rectifier design to perpetuate the RFEH performance in an actual environment where the power density of the available RF power varies dynamically with the change of transmitted power during the RF transmission between the transmit antenna and the receive antenna. The heterogeneous nature of the RF power during transmission is mainly due to the nonuniform deployment of RF facilities [18] and obstacles disturbance [19] which result in variable harvested RF input power range. Hence, the consensus approach is to fill the research gap through a comprehensive review of CMOS RF-DC rectifiers focusing on PDR to enhance the overall performance of the RFEH system.

This article not only provides an overview of the RFEH front-end circuit which consists of the antenna, the impedance matching network and the rectifier but also deep-diving into the review of the latest research progress achieved in the practical extended PDR design and development of the CMOS RF-DC rectifier over the years. In section II, the review covers the transmission of the RF power. Section III provides a brief overview of the RFEH front-end circuit. Section IV presents a comprehensive review of wide PDR RF-DC rectifier circuits. Section V explores the future design aspects that contribute to a more efficient RFEH system. Section VI concludes this review article.

II. RF TRANSMISSION

In RF-based wireless power transmission, electrical power is firstly converted into RF energy before being transmitted over a distance through a free space medium. This transmitted RF energy is then received and converted back into electrical power at the receiving end. Depending on the propagation distance, the electromagnetic signal can be utilized for near-field and far-field applications. Fraunhofer distance provides the limit between near-field and far-field [20]. Typically, the power is transferred through magnetic coupling between coils of wire at a short range distance in near-field applications, whereas in far-field applications, the power is transferred by harvesting the energy from the ambient electromagnetic radiation propagating over a long range distance between the transmit antenna and receive antenna. By using the Friis transmission equation [21], the input power received by the receive antenna can be calculated as:

$$P_R = \frac{P_T G_T G_R c^2}{(4\pi D f)^2} \tag{1}$$

where P_R is the received power, P_T is the transmitted power, G_T is the antenna gain of the transmit antenna, G_R is the antenna gain of the receive antenna, c is the speed of light, f is the frequency of the RF wave and D is the RF transmission distance between the transmit antenna and the receive antenna. According to the equation in (1), it is important to note that P_R is inversely proportional to D^2 and the relationship can be shown in Fig. 2. In reference to the simulation work reported in [22], the power density curve observed in Fig. 2 is correlated with the Friis transmission equation in (1)whereby the received power is much higher in the near-field than far-field segregated by the Fraunhofer distance [20]. As such, the power density of the received power is proven to be varied dynamically with the transmission distance. Hence, it is clear that extending the PDR of the rectifier will offer a higher degree of portability and flexibility for the RF energy harvester in an actual IoE application.

Theoretically, more RF power could be harvested at lower frequencies. However, the strength of signals from different RF bands can be inconsistent in distinct locations around the world, resulting in the different available magnitude of the power density due to the nonuniform deployment of RF facilities [18] and blocking obstacles [19] such as buildings and mountains. The measurement of the power density can be conducted through RF surveys [23]–[27] to investigate the spectrum of available RF bands which are suitable for energy harvesting. From the RF surveys conducted as shown in Table 1, it has been concluded that GSM900 and GSM1800 are the two most reliable ultra-high-frequency (UHF) bands applicable for energy harvesting as these

TABLE 1. Measured power density of RF bands in different locations.

Ref.	RF Band (Freq.)	Average Power	Peak Power		
[24] ^a	Digital TV (470 – 610 MHz)	0.89 nW/cm ²	460 nW/cm ²		
	GSM900 (800 - 915 MHz)	36 nW/cm ²	1930 nW/cm ²		
	GSM1800 (1.805 – 1.88 GHz)	84 nW/cm ²	6390 nW/cm ²		
	3G (2.11 – 2.17 GHz)	12 nW/cm ²	240 nW/cm ²		
	WiFi (2.4 – 2.5 GHz)	0.18 nW/cm ²	6 nW/cm ²		
[25] ^b	CDMA800 (810 – 870 MHz)	-40/-34 dBm	-38.99/-30 dBm		
	GSM900 (935 – 960 MHz)	-50/-56 dBm	-45/-52 dBm		
	GSM1800 (1.805 – 1.85 GHz)	-55/-48 dBm	-54.9/-39 dBm		
	CDMA2000 (2.11 – 2.15 GHz)	-59/-55 dBm	-55/-45 dBm		
	TD-LTE / WiFi (2.32 – 2.575 GHz)	-70/-65 dBm	-61/-60 dBm		
	GSM900	-34.9/-26.65	-22.66/-7.65		
	(880 – 960 MHz)	dBm	dBm		
	GSM1800	-45.53/-15.66	-27.56/-1.29		
	(1.71 – 1.88 GHz)	dBm	dBm		
[26]°	UMTS	-43.27/-13.33	-29.09/-10.65		
[20]	(1.92 – 2.2 GHz)	dBm	dBm		
	WiMax	-48.53/-31.48	-41.40/-27.04		
	(2.3 – 2.39 GHz)	dBm	dBm		
	WiFi	-43.19/-24.8	-29.92/-15.56		
	(2.4 – 2.5 GHz)	dBm	dBm		
[27] ^d	GSM900 (925 – 960 MHz)	n.a.	-22.5 dBm		
	GSM1800 (1.805 – 1.88 GHz)	n.a.	-17.8 dBm		
	3G (2.11 – 2.23 GHz)	n.a.	-23 dBm		
	WiFi (2.39 – 2.4 GHz)	n.a.	-25.6 dBm		
	LTE (2.5 – 2.7 GHz)	n.a.	-26.5 dBm		
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^aLondon Underground stations, UK; ^bShunde shopping center/ residential area, China; ^cKedah and Perlis (semi-urban area)/ Penang (urban area), Malaysia; ^dMultimedia University, Selangor, Malaysia

UHF bands have the highest measured power density in the actual urban environment from the wide adoption in communication activities such as television broadcasts, wireless LAN, Bluetooth and mobile phones, making it practical to be adopted for the RFEH system. Nonetheless, the choice of frequency in designing the RFEH system should be suitable for the dedicated application and location. For instance, GSM900 and GSM1800 can be selected for outdoor or suburban IoE applications such as smart agriculture, whereas UMTS and WiFi can be considered for indoor or urban IoE applications such as smart homes based on the availability and reliability of the RF power density. This has set the specification in designing the RF energy harvester front-end circuit.

III. RFEH FRONT-END CIRCUIT

The three main components in an RF energy harvester frontend circuit are the receive antenna, impedance matching network and RF-DC rectifier. As the incident RF input is



FIGURE 2. Power density curve of RF energy harvesting system [22].



FIGURE 3. Power flow of RF energy harvester front-end circuit.

harvested by the receive antenna, the received power is sensed through an impedance matching circuit in order to achieve maximum power transfer. Subsequently, the RF-DC rectifier converts the matched RF power to DC at the output load. For illustration, this power flow of the RF energy harvester frontend circuit is shown in Fig 3 which takes into account the efficiencies and the losses of the front-end circuit during the conversion of the input RF power to the output DC power. The overall performance of the RF energy harvester front-end circuit can be represented by:

$$\eta_{FRONT} = \frac{P_{DC}}{P_R} = \eta_{IMN} \cdot \eta_{REC}$$
(2)

where η_{FRONT} is the overall efficiency of the RF energy harvester front-end circuit, P_{DC} is the output DC power, P_R is the received power, η_{IMN} is the efficiency of the impedance matching circuit, η_{REC} is the efficiency of the RF-DC rectifier. This is where the effort of improving the efficiency of the impedance matching circuit and the rectifier, benefits the overall performance of the RFEH system. To estimate the DC output for the overall RFEH system, η_{IMN} is considered to be 50% at maximum power transfer [28] and η_{REC} ranges from 25% to 86% depending on the rectifier design, which is summarized in Table 3 and will be discussed later in section IV. The end-to-end efficiency of the power flow from the receive antenna to the DC load, as exhibited in Fig. 3, can be calculated by multiplying η_{IMN} and η_{REC} shown in (2),

 TABLE 2. Comparison of the recently published works on compact antennas.

Ref.	Freq. (GHz)	Size (mm ²)	Measured Gain
[29] ^g	2.45	24.9 x 8.6	0.8 dBi @ 2.45 GHz
[30] ^a	2/2.5/3.5	120 x 120	9.2 dBi @ 3.5 GHz
[31] ^a	2.0 - 3.1	50 x 35	3 dBi @ 3.1 GHz
[32] ^a	0.9	130 x 130	5.6 dBi @ 900 MHz
[33] ^b	2.45	35 x 35	-1.6 dBi @ 2.45 GHz
[34] ^b	2.15 - 2.9	43.6 x 18.5	2.2 dBi @ 2.45 GHz
[35]°	0.85/1.81/2.4	160 x 160	4.82 dBi @ 2.4 GHz
[36] ^d	0.95/1.74/2.42	220 x 220	7.6 dBi @ 2.42 GHz
[37] ^e	1.8	45 x 45	3 dBi @ 1.8 GHz
[38] ^e	0.915/0.945	49.18 x 49.18	1.3 dBi @ 915/945 MHz
[39] ^f	2.3 - 2.63	190.5 x 26	8.7 dBi @ 2.63 GHz
[40] ^g	2.45	30 x 18	5.6 dBi @ 2.45 GHz
[41] ^h	2.3 - 4.1	40 x 38	6.3 dBi @ 3 GHz
[42] ^h	2.4/3.8/5.6	24 x 19	3.73 dBi @ 5.6 GHz

^aslotted/slitted antenna; ^bfractal antenna; ^cbow-tie antenna; ^dfork-shaped antenna; ^eloop antenna; ^fquasi-Yagi antenna; ^gcoplanar waveguide-fed antenna; ^basymmetric coplanar strip-fed antenna

and the resulting end-to-end efficiency is ranged from 12.5% to 43%.

A. ANTENNA

Since the early days of radio engineering, the standard of 50 Ω antenna has been used in RF applications as a compromise between low loss and power handling for coaxial cables [43]. A receive antenna is an essential component in the RFEH system as it can intercept the ambient RF power to generate an electrical signal at its terminal. The peak input voltage generated by the receive antenna can be calculated by [44]:

$$V_{ANT} = \sqrt{8 \times R_{ANT} \times P_R} \tag{3}$$

where V_{ANT} is the peak input voltage at the receive antenna, R_{ANT} is the radiation resistance of the receive antenna and P_R is the received power in (1). This peak input voltage is usually very low and needed to be rectified and multiplied by an increased RF-DC rectifier stage. Among the antennas, patch antennas or printed antennas are preferred due to their compact size, low fabrication cost and ease of integration with the RF-DC rectifier [29]. In the perspective of antenna design, some design techniques have been investigated towards the miniaturization of the antenna for RFEH system which includes creating slots/slits on antenna [30]–[32], employing fractal geometry on antenna [33], [34], bow-tie antenna [35], forked-shaped antenna [36], utilizing the compact loop antenna [37], [38], adopting the compact quasi-Yagi antenna [39] and also implementing different feeding structures such as coplanar waveguide [29], [40] and asymmetric coplanar strip [41], [42].

In [30], the proposed triple-band antenna is realized by etching two rectangular slot loops connected in the ground plane with a dimension of 120 mm \times 120 mm, achieving a measured gain of 7, 5.5, and 9.2 dBi at the frequencies of 2, 2.5 and 3.5 GHz respectively. By combining the annular slot radiation patch and the newly slotted ground plane, the

50 mm \times 35 mm slotted antenna in [31] has achieved a peak gain of 3 dBi at 3.1 GHz. An octagonal-shaped patch antenna with eight tapered slits is designed in [32]. The proposed 130 mm \times 130 mm tapered-slit patch antenna is able to provide a circular polarized wide-angle beam with a gain of 5.6 dBi at 900 MHz for the RFEH system.

Apart from creating slots/slits on the antenna, a compact antenna is developed in [33] with a dimension of 35 mm \times 35 mm based on the fractal geometry of Koch curve. Despite the compact size, the antenna has a measured gain of -1.61 dBi at 2.45 GHz due to high loss tangent of the low-cost substrate used for fabrication. On the basis of fractal geometry, a novel broadband antenna is introduced in [34] by etching fractal slot on the antenna patch. With a broad operating range of 2.15 - 2.9 GHz, the gain of the antenna with a size of 43.6 mm \times 18.5 mm is reported to be around 2.2 dBi at 2.45 GHz. The advantage of employing fractal geometry on the antenna over a slotted structure is in the compactness achieved. Nevertheless, the planar structure naturally has a more complex design and lower reported antenna gain. Alternatively, higher antenna gain of 4.82 dBi and 7.6 dBi can be achieved by trading off the compactness of the antenna using bow-tie antenna [35] and fork-shaped antenna [36] respectively.

On the other hand, a compact loop antenna for RFEH at GSM1800 band is presented in [37] with a measured peak gain of 3 dBi. To harvest RF energy from different directions, a dual-band loop antenna array is developed in [38] with a compact size of 49.18 mm \times 49.18 mm per antenna element. The dual-band compact loop antennas have a gain of 1.3 dBi at 915 and 945 MHz, respectively. Furthermore, the reported work in [39] has proposed a novel quasi-Yagi antenna array with an effective area of 190.5 mm \times 26 mm. A high gain of 8 – 8.7 dBi from 2.3 to 2.63 GHz is realized by adopting a collinear antenna and employing a few collinear parasitic strips. At the cost of narrower frequency bandwidth, the proposed design can further offer a compact size by reducing the size of patches and the distance between parasitic strips and the collinear antenna. Thus, there is a positive correlation between the antenna's effective area and its operating frequency bandwidth.

In addition, antennas with different feeding structures are also being explored for smaller overall footprint. In [29], a rectangular patch antenna with two etched U-shaped slots benefited from a symmetric coplanar feeding structure to achieve an overall dimension of 24.9 mm \times 8.6 mm. However, its measured peak gain is only 0.8 dBi at 2.45 GHz. At the same frequency, another work in [40] has demonstrated a higher peak gain of 5.6 dBi using a novel 30 mm \times 18 mm coplanar waveguide-fed antenna with a rectangular tuning stub. An alternative approach is taken in [41] by proposing an antenna feeding technique using a metal-backed asymmetrical coplanar waveguide. The overall dimension of the proposed structure is 40 mm \times 38 mm with two inverted L-shaped strips placed at the microstrip line of the asymmetric coplanar waveguide. Measured at the operating frequency of 2.3 to 4.1 GHz, the peak gain is observed to be 6.3 dBi with a substrate-size reflector. Besides that, a compact grounded asymmetric coplanar strip-fed flexible antenna is presented in [42] backed by a flexible polyamide substrate with a dimension of 24 mm \times 19 mm. The reported antenna radiates unidirectionally with a peak gain of 3.73 dBi at 5.6 GHz. In spite of the higher gain compared to the coplanar waveguide-fed antennas, the downside of the asymmetric coplanar strip-fed antennas is that the design may suffer from asymmetric radiation patterns [29].

The performance of the recently published works on compact antennas for the RFEH system is summarized in Table 2. Within the selected operating frequency, the tradeoff between the antenna size and the antenna gain is apparent. Upon the integration to the rectifier, the high gain of the antenna will elevate the performance of the RFEH system in terms of sensitivity. Still, the designed antenna should be compact for better cost-effective and practical use. The compactness of the antenna is realized by selecting higher frequency bands as the higher the frequency, the shorter the wavelength and the smaller the antenna. However, this will come at the expense of utilizing frequency bands with lower RF power density compared to GSM900 and GSM1800 such as UMTS and WiFi. Therefore, these tradeoffs have to be factored in to obtain the optimized antenna performance and practicality. Although there are other published works on broadband antenna [45]-[47] that are able to simultaneously harvest more RF power from a wide frequency band, these reported antennas are relatively bulky and are not feasible to be embedded ubiquitously into portable devices, especially WSNs.

B. IMPEDANCE MATCHING CIRCUIT

The complication occurs as the diodes or transistors used in the rectifier are nonlinear devices, resulting in a highly varying rectifier impedance dependent on the frequency [48], [49]. Due to the wide variation of the rectifier impedance, it is a challenge to match the 50 Ω antenna to the RF-DC rectifier. Impedance discontinuity between the antenna and the rectifier causes some of the electrical signal to be reflected, as illustrated in Fig. 5(a). The amount of signal reflected can be modeled using the reflection coefficient equation given by [50]:

$$\Gamma = \frac{Z_{REC} - Z^*_{ANT}}{Z_{REC} + Z^*_{ANT}} \tag{4}$$

where Γ is the reflection coefficient, $Z_{REC} = R_{REC} + X_{REC}$ is the rectifier impedance and Z^*_{ANT} is the complex conjugate of the antenna impedance, $Z_{ANT} = R_{ANT} + X_{ANT}$. To ensure maximum power transfer and minimum signal reflection, an impedance matching circuit is needed to be designed specifically between the receive antenna and the RF-DC rectifier to match the antenna impedance and the rectifier impedance [53], [54]. The efficiency of the impedance matching circuit can be determined as the ratio of the incident power from the receive antenna and the power delivered to the



FIGURE 4. Impedance matching circuit topologies. (a)-(d) L-matching. (e) High-pass PI-type. (f) Low-pass PI-type. (g) High-pass T-type. (h) Low-pass T-type. (i) Transformer matching [51], [52].

RF-DC rectifier as given by [10]:

$$\eta_{IMN} = \frac{P_R - P_{REFLECT}}{P_R} = \frac{P_{REC}}{P_R} \tag{5}$$

where η_{IMN} is the efficiency of the impedance matching circuit, $P_{REFLECT}$ is the power reflected during transmission, P_{REC} is the power delivered to the rectifier and P_R is the incident power from the antenna.

The commonly used impedance matching circuit in the RFEH system is the L-matching network [55]–[59], with different configurations of inductor and capacitor in an L-shape relative to the load impedance at the desired frequency as

shown in Fig. 4(a)-(d). When the antenna impedance, Z_{ANT} is larger than the rectifier impedance, Z_{REC} , the L-matching network is configured as shown in Fig. 4(a) and Fig. 4(b) to transform the load impedance upward from Z_{REC} to Z_{ANT} . As for the downward impedance transformation, the L-matching network is connected as exhibited in Fig. 4(c) and Fig. 4(d). Both configurations in Fig. 4(a) and Fig. 4(d) are low-pass L-match, whereas Fig. 4(b) and Fig. 4(c) represent high-pass L-match. The quality factor or Q-factor of the inductor in the impedance matching circuit is an important design parameter as it is positively correlated to the passive voltage gain, which will affect the sensitivity of the rectifier. The relationship between the Q-factor and the voltage gain can be expressed as [56]:

$$\frac{V_{RIN}}{V_{ANT}} = \frac{1}{2}\sqrt{1+Q^2} \tag{6}$$

where V_{RIN} is the input of the rectifier, V_{ANT} is the peak input voltage at the receive antenna and Q is the Q-factor of the inductor.

From characterizing both the impedance matching network and the rectifier circuit, optimization can be achieved by choosing the optimum values for the design parameters [56]. To obtain a higher Q-factor, off-chip components are used in the impedance matching circuit design [58] to improve the performance of the rectifier for variable input power. Despite the improvement in sensitivity from the passive voltage gain, the use of bulky off-chip matching elements has imposed a disadvantage in terms of the form factor and flexibility relative to the on-chip matching network design [56], [57]. A comparative study has been conducted in [59] to examine the limit and tradeoffs for both on-chip and off-chip matching networks in the RFEH system.

To enable energy harvesting from different RF inputs, parallel-connected matching networks have been developed in [60] to harvest from two frequencies simultaneously by combining two different rectifier circuits. Alternatively, the dual-band RFEH operation is achieved in [61] with the proposed band-pass and band-stop filters for providing zeros and poles to pass and stop signals. By employing the Integrated-Passive Device technology, the matching networks and filters have low power loss and high Q-factor. Apart from that, novel dual-band matching networks were designed using a T-type network [62] and a PI-type network [63] for dual-band RFEH systems at 915 MHz and 2.45 GHz. In [62], the dual-band matching network is assembled using a single-stage T-type network with only three segments of the transmission line to reduce the design complexity and form factor. On the other hand, the PI-type network in [63] is reported as a sub-network to match a pair of conjugate impedances from two arbitrary frequency-dependent impedances for realizing dual-band RFEH.

Some reported work in [51], [52] utilizes a transformerbased impedance matching circuit as represented in Fig. 4(i) to provide additional voltage boosting for the rectifier while simultaneously working as a matching circuit. However, there is a tradeoff between the power transfer and the transmission efficiency in reference to the maximum power transfer theorem mentioned in [28]. At the maximum power transfer condition, the efficiency of the impedance matching circuit will be capped at 50%. Increasing the power to the rectifier will lead to a decline in the efficiency of the impedance matching circuit. Therefore, the optimization between the power transfer and the efficiency of the impedance matching circuit has reached a bottleneck for the performance of the RFEH system. As such, there has been an increase in research interest focusing on the performance of the RFEH system.

C. RF-DC RECTIFIER

As a core component in the RFEH front-end circuit, the RF-DC rectifier is used for voltage rectification and voltage multiplication from RF energy into DC energy. Due to the low power density of the harvested RF energy, the power delivered to the rectifier has to be rectified and multiplied to provide sufficient DC power to the output load. The performance of the rectifier can be evaluated based on the following aspects:

1) SENSITIVITY

The sensitivity of the rectifier is defined as the minimum input power required to generate a DC output of 1 V at desired output load. It is an important metric to ensure that the RFEH system is activated and able to work reliably in an actual environment. The expression for the sensitivity of the rectifier is given by [64]:

$$P_{dBm} = 10\log_{10}(P_{mW})$$
(7)

where P_{dBm} is the sensitivity of the rectifier expressed in dBm and P_{mW} is the power received by the rectifier expressed in milliwatts.

2) POWER CONVERSION EFFICIENCY (PCE)

The PCE of the rectifier is defined as the ratio of the DC output power to the RF power received by the rectifier which is determined by:

$$\eta_{REC} = \frac{P_{DC}}{P_{REC}} \tag{8}$$

where η_{REC} is the PCE of the rectifier, P_{DC} is the output DC and P_{REC} is the RF power received by the rectifier. The RF power received by the rectifier can be calculated in an equation as given by [65]:

$$P_{REC} = P_R - P_{REFLECT} = P_R \left(1 - |S_{11}|^2 \right)$$
(9)

where $|S_{11}|^2 = |\Gamma|^2$ is the power reflection coefficient. The PCE measures the ability of the rectifier to convert RF power to DC power and it is highly dependent on the rectifier circuit design.

3) POWER DYNAMIC RANGE (PDR)

The PDR of the rectifier is defined as the range of input power at which the rectifier maintains its PCE above 20% [66]. Based on the definition, the relationship between PDR and PCE of the rectifier can be expressed as:

$$PDR(dB) = \{100\% \ge \eta_{REC} \ge 20\%\}$$
(10)

where η_{REC} is the PCE of the rectifier and dB is the unit of measurement for PDR in decibel. Maintaining a wide PDR in the rectifier performance improves the reliability of the RFEH system in an RF environment with varying power densities. In the later section, the latest research progress on wide PDR rectifiers for the RFEH system will be reviewed.

4) FIGURE OF MERIT (FoM)

To provide a comprehensive evaluation between different PDR extension techniques, a FoM is formulated to better reflect the performance of the wide PDR rectifiers after deriving it from the equation reported in [67], [68]. The RF-DC rectifier's FoM can be re-expressed as:

$$FoM = \frac{PCE \times PDR}{N} \log_{10} \left(\frac{f}{f_0}\right) \tag{11}$$

where FoM is the rectifier's figure of merit, N is the total number of rectifier stages, f is the frequency of operation and $f_0 = 5$ MHz is the frequency normalization factor to uniformly evaluate the performance of the state-of-the-art rectifiers which operate at different frequencies [67], [68].

The essential take in designing the rectifier using CMOS technology is to understand the characteristics and behavior of the transistor during operation to provide an approach on how to improve the performance of the rectifier. In RFEH, the transistor usually conducts in a weak inversion region whereby the gate-to-source voltage is below or near the threshold voltage of the transistor. This subthreshold conduction of the transistor can be modeled in the equation given by [69]:

$$I_D = \mu_n C_{OX} V_T^2 \frac{W}{L} e^{\left(\frac{V_{GS} - V_{TH}}{nV_T}\right)} \left\{ 1 - e^{\left(-\frac{V_{DS}}{V_T}\right)} \right\}$$
(12)

where I_D is the drain current of the transistor, μ_n is the carrier mobility of NMOS transistor, C_{OX} is the oxide capacitance per unit area, W is the channel width, L is the channel length, n is the slope factor, V_{TH} is the threshold voltage, V_{GS} is the gate-to-source voltage, V_{DS} is the drain-to-source voltage and V_T is the thermal voltage.

As shown in Fig. 5(a), the Dickson rectifier [13] and the CCDD rectifier [14] are the two main rectifier topologies used in the RFEH system. Since the RF input power density is typically very low, multiple stages of rectifier are cascaded to attain a higher usable DC output voltage. Each stage rectifies the RF input (V_{RIN}) and feeds its DC output voltage (V_{ROUT}) into the subsequent stages, resulting in voltage multiplication from one stage to the next. The final output voltage (V_{DC}) of the rectifier, as shown in Fig. 1, is proportional to



FIGURE 5. Single stage RF-DC rectifier topology. (a) Dickson [13]. (b) cross-coupled differential-drive (CCDD) [14].

the number of the cascaded stages, N and is evaluated by $V_{DC} = NV_{ROUT}$ [70].

Even though the Dickson rectifier has been commonly adopted for generating higher output voltages, the rectifier suffers from poor sensitivity and PCE during low voltage operation, especially in multistage configuration. Referring to (12), the performance of the rectifier can be improved through boosting V_{GS} or reducing V_{TH} . The proposed threshold voltage compensation scheme in [57], [71]–[74] enhanced the sensitivity of the rectifier by applying an additional bias voltage between the gate and the drain terminals of the transistor to reduce the voltage drop. However, the tradeoff arises when the reverse leakage occurs in the compensation scheme. This limits the efficiency of the rectifier as some of the power flows back to the source. To reduce the reverse leakage, an adaptive or hybrid threshold compensation scheme is proposed in [16], [75]-[77] to optimally increase the forward conduction by increasing the voltage compensation during the forward bias condition and decreasing the voltage compensation during the reverse bias condition of the transistor, hence, improving the sensitivity and PCE of the rectifier. Apart from that, various other methods are also reported to reduce the threshold voltage of the transistor, such as self-body-biasing techniques [15], [78]-[80], tunable threshold design [81] and implementation of zerothreshold transistors [82].

Alternatively, a CCDD rectifier is adopted for low voltage operation to achieve relatively better sensitivity and PCE by



FIGURE 6. Wide PDR RF-DC rectifier architectures. (a) Reconfigurable rectifier [91]. (b) Self-biasing technique in CCDD rectifier [17].

applying the differential RF input across the four rectifying transistors, as shown in Fig. 5(b). Nevertheless, the CCDD rectifier design has been bottlenecked by the presence of reverse leakage current, which degrades its PCE at high RF input, causing narrow PDR. Worse still, the reverse leakage can be more severe in a multistage configuration whereby the output voltage is much higher than the incoming input voltage. The performance optimization between the reverse leakage and the number of stages of the CCDD rectifier to provide sufficient output voltage has been a design challenge in the RFEH system. Several reverse leakage reduction techniques are introduced to reduce the effect of reverse leakage. In [83], the issue of reverse leakage is addressed by using a complementary MOS diode at the last stage of the rectifier. The utilization of thick-oxide MOSFET as a rectifying device to reduce the leakage current is shown in [84]. Improvement in the PCE can also be made through complementing the bootstrapping approach [85], [86] and the threshold voltage cancellation scheme [87], [88] in the rectifier design. A selfbiased design is proposed in [89] by utilizing two feedback resistors between the transistor gate and the output, which lowers the driving voltage of the rectifying transistors when the output voltage is higher than the input voltage. Reducing the detrimental effect of the reverse leakage can significantly

increase the operation range of the RFEH system. In the next section, state-of-the-art circuit enhancement techniques that can further extend the PDR of the rectifier will be reviewed and discussed.

IV. WIDE POWER DYNAMIC RANGE RFEH RECTIFIER

To ensure the RFEH system operates efficiently in a highly dynamic RF environment, many research works have been carried out to extend the PDR of the CMOS RF-DC rectifier while achieving a high PCE and good sensitivity. As reported in [66], five-stage CCDD rectifiers are connected in a dualpath structure with adaptive control that achieves a PDR of 11 dB by using a common-gate input comparator to switch the path with some power overhead. By optimizing the width of transistors differently for the low power path and the high power path, the system is able to maintain high PCE for a wide range. Another work in [90] integrates a dual-input rectifier scheme with Dickson and CCDD topology to harvest energy from two individual energy sources. By selecting the path of high PCE using a logic control circuit, the proposed work manages to extend the PDR of the rectifier to 26 dB.

Besides that, a reconfigurable rectifier presented in [91] operates at a wide PDR through a series path during low power operation and a parallel path during high power operation by adaptively switching between the series path and the parallel path to maximize the operating range of the RFEH system as represented in Fig. 6(a). Further improvement has been accomplished in [92]-[94] by reconfiguring multiple rectifier stages depending on the input power conditions to determine the optimal rectifier stages for improving the PDR. The implementation of one-two-four-eight-stage configurations for the reconfigurable rectifier in [94] manages to achieve a PDR of 10 dB in a fully integrated system with a matching network, rectifier, power management circuitry and storage capability. A wide PDR RFEH system of 13 dB with an effective maximum power point tracking (MPPT) power efficiency above 72% is designed in [92] with an optimized reconfigurable two-three-four-six-twelve stage rectifier. The work in [93] proposed a reconfigurable one-two-four-eight stage rectifier with optimal loading point determination showcasing a PDR of 14 dB. A more complex reconfigurable differential rectifier with a cross-connection transistor in a threshold voltage compensation scheme is proposed in [95]. The work in [96] has presented a bidirectional class-DE circuit that can be reconfigured as a rectifier or an oscillator where the rectifier is reported to have a PDR of 19 dB using the proposed architecture. Moreover, the work in [65], [97] have proposed another method of reconfiguring the rectifier by transitioning the type of rectifier from configuring the gate connection of each transistor which allows the PCE of the rectifier to be attained even with the increasing number of stages at varying input power condition.

Apart from the reconfigurable mechanism, self-biasing techniques have been proposed in [17], [89], [98], [99] to extend the range of input power for multistage CCDD rectifier. The operating principle is to adaptively control the

conduction of the rectifying transistors during high input power operation when the reverse leakage becomes severe. This is executed by applying DC self-bias from the output voltage to the rectifying PMOS gates of the CCDD rectifier using feedback resistors [89] or a feedback network [98] to detect the output voltage and limit the reverse leakage in the presence of high input power, thus improving the PCE and extending the PDR of the rectifier.

The substitution of the feedback resistors with feedback diode-connected transistors is realized in [17], which are positioned to be reverse-biased for the RF input and forward-biased for the DC output to provide a variable resistance for DC voltage depending on the RF input while limiting the passage of the RF signal from the input to the output as shown in Fig. 6(b). A similar diode-connected gate-biasing scheme is proposed in [99] to reduce the reverse leakage current with the addition of self-body-biasing scheme that lowers the turn-on voltage of the transistor in the rectifier. Another work in [100] utilizes a dual-mode nested feedback circuit to perform the self-biasing technique. By enhancing the conductivity of the rectifier at low power while reducing the reverse leakage at high power, the PDR of the rectifier will be extended.

An optimized voltage compensation scheme that is proposed in [101] exhibits a PDR of 10.5 dB using three different implementations of the rectifiers with different auxiliary circuits to generate the optimum compensation voltage. Through calculations and simulations, the desired optimum compensation voltage is generated by utilizing minimal auxiliary transistors operating in the subthreshold region to reduce the power consumption of the auxiliary circuits. In [102], a novel threshold voltage compensation technique is proposed by exploiting both dynamic and static self-compensation to allow rectifier operation of high PCE and high sensitivity over a input power range of 8 dB. A twostage CCDD rectifier with DC-boosted gate bias is presented in [103] which enables the rectifier to operate in subthreshold region, achieving a peak PCE of 73.6% and a PDR of 15 dB. The auxiliary gate bias also manages to reduce the reverse leakage current by constraining the positive gate voltage during off state.

Another work in [104] has performed parasitic-aware RFEH system design through the proposed RFEH global reverse analysis and modeling to optimize the size of the matching network, predict the PCE and determine the MPPT regulation ratio. At 2.45 GHz, the proposed design achieved 48.3% peak PCE at -3 dBm incident RF power and 11 dB of wide incident power range. Other than that, a resistance compression is used in [105] to minimize the rectifier's sensitivity for the variation in the input power and the rectifier load. Fabricated in 180 nm, the proposed design also provides a regulated voltage of 1 V with a sensitivity of -16 dBm and a peak PCE of 47.1% while maintaining a wide PDR of 16 dB at 2.4 GHz. The performances of the state-of-the-art wide PDR CMOS rectifier for RFEH system are summarized in Table 3.

The rectifier operating frequency bands reported in the recently published works are mostly in the UHF bands. This coincides with the aforementioned RF surveys as discussed in Section II to ensure a reliable operation of the RFEH system. Still, the design of the RFEH system should be subjected to the availability of the frequency range depending on the desired application and location. For example, lower frequencies are more practical for suburban IoE applications, whereas higher frequencies are better suited for urban applications. The effect of the frequency that will influence the performance of the rectifier is manifested at a higher frequency due to the higher switching loss, tapering off the rectifier's PCE and PDR as the switching loss increases. It is important to take note that different PDR extension techniques have shown different merit in their performances depending on the capability of offsetting the tradeoffs in the rectifier design. While all of the reconfigurable Dickon rectifier designs [91]-[94] are able to achieve a wide PDR of more than 10 dB, they are confronted with a limitation in reaching higher peak PCE due to its significant drawback in the dropout voltage. On the other hand, the implementation of the self-biasing technique in CCDD rectifier [17], [89], [98] has manifested a tradeoff in reducing the reverse leakage and hindering the forward conduction concurrently during high input power operation. Moreover, the power that is partially consumed by the usage of the reference path and adaptive control circuit in the dual-path rectifier [66] has been compromising the achievable PCE in order to extend the PDR of the rectifier. These tradeoffs have to be taken into consideration when designing the circuit architecture to optimize the performance of the rectifier.

Another consideration to keep in mind is that the performance of the rectifier changes with the transistor size and output load. Depending on the CMOS process and type of transistor used, an optimum transistor sizing ratio can be determined through iterative simulation and the sizing ratio of the PMOS transistor is generally larger than the sizing ratio of the NMOS transistor due to the higher electron mobility in NMOS transistor [106]. Changing the output load will lead to a shift in the PCE curve and output voltage as investigated in [102]. Generally, the PCE curve will shift to the right as the load decreases and the optimum peak PCE and PDR can be acquired after sweeping for multiple load values. The load affects the performance of the rectifier with respect to the output voltage by obeying Ohm's Law. Hence, a suitable output load is chosen with the intention to obtain a high peak PCE, a wide PDR and a good sensitivity in delivering sufficient voltage required for the desired application.

Although there are many alternative methods to extend the PDR of the rectifier as reported in [107]–[112], these enhancement techniques, which are realized from using discrete components rather than integrated circuits, are not included in this review because the scope of this review is focused on the implementation of CMOS technology which has a leading edge in terms of the form factor, scalability and flexibility in designing the RFEH system for low power applications. Not to mention that the threshold voltage of the transistor could be reduced by using an advanced CMOS technology node which has a shorter transistor channel length and lowers power consumption. Consequently, this will further improve the performance of the rectifier but with an increase in fabrication costs and tend to be more exposed to reverse leakages as the tradeoff.

The test bench for RF characterization may vary depending on the operating frequencies and the performance parameters. Generally, the device under test (DUT), namely the RFEH circuit is tested using the on-chip wafer probing or is embedded within a test fixture via the printed circuit board (PCB) to enable the characterization through the test equipment such as the vector network analyzer (VNA). To measure the frequency-dependent input scattering parameters (S-parameters), the VNA injects RF into one port and measures the RF reflected from that port. However, the quality and the accuracy of the measured S-parameters can be affected by the discontinuities introduced in the on-chip probes and test fixtures, especially at high frequencies [113]. These measurement errors can be mathematically removed by performing proper calibration and de-embedding process.

The typical measurement setup reported in the published works consists of a VNA, RF signal generator, oscilloscope and a digital multimeter. For on-chip measurements conducted in [17], [89], [94], [96], [99], [100], a wafer probing is adopted for on-chip characterization. Upon sweeping a wide range of RF input with the output load at the operating frequency, the corresponding output voltage and S-parameters are measured using on-chip probing. The de-embedding process for the on-chip measurement is accomplished by setting the reference plane to be at the on-chip pads of the rectifier input and the calibration is done at the probe tips. The net RF input power delivered to the rectifier after considering the reflection and transmission losses can be derived from the equation in [17], [100]:

$$P_{REC} = P_{source} - 10\log|S_{11}|^2$$
(13)

where P_{REC} (dBm) is the net RF input power delivered to the rectifier, Psource (dBm) is the RF power generated from the signal generator, and S_{11} is the S-parameter of the rectifier input measured using the VNA. Alternatively, chip on board (CoB) based measurement is reported in [65], [66], [91]–[93], [95], [97], [101]–[105]. In CoB measurement setup, off-chip components can be interconnected on PCB such as antenna [92], impedance matching circuit [91], [95], [101] or additional control pins [65], [66], [97] depending on the characterization condition of the proposed design. Similarly, calibration is undertaken at the connection terminals of the test fixture whereby the reference plane is shifted to the ports of the test fixture. De-embedding is performed to compensate for the effects of the test fixture used in the measurement up to the DUT connection point. 2x Thru de-embedding is an example of a popular de-embedding methodology used for CoB measurement due to its accuracy and simplicity [114]. By modeling the test fixture, the effects of the fixture are subtracted from the measurement results through de-embedding and the net input power is determined by referring to the equation in (13) which can be expressed as:

$$P_{REC} = P_{source} - L_{insertion} - 10 \log |S_{11}|^2$$
(14)

where P_{REC} (dBm) is the net RF input power delivered to the rectifier, P_{source} (dBm) is the RF power generated from the signal generator, $L_{insertion}$ (dB) is the insertion loss and S_{11} is the S-parameter of the rectifier input measured using the VNA.

As of recently reported work, the proposed designs which can extend the PDR of the rectifier for more than 20 dB are reported in [90], [100]. The adoption of both Dickson and CCDD rectifiers in the dual-input design [90] helps to outperform other reported works by leveraging the advantages of both of the rectifiers. Similarly, the outperformance of the dual-mode nested rectifier design in [100] compared to the other published works is dedicated to the adaption of the self-biasing technique whereby the conductivity of the rectifier during low power operation is enhanced while reducing the reverse leakage current during high power operation by dynamically biasing the rectifying transistors using a dualmode nested feedback circuit. In terms of the rectifier's FoM, the dual-mode nested design in [100] also has the highest FoM among the other recently published designs. Although the higher FoM may imply greater merit in the rectifier PDR extension techniques, it hardly reflects the suitability and practicality of the RFEH system design due to the highly varied output load range and the availability of the selected frequency for RFEH depending on the IoE applications. Therefore, it is difficult to use FoM for benchmarking and comparing the performance of the rectifier fairly. As for the performance benchmark, the proposed rectifier must be able to simultaneously achieve high peak PCE, good sensitivity and wide PDR. Some viewpoints are put forward on the RFEH design further outlook in the next section.

V. RFEH DESIGN FURTHER OUTLOOK

Although many state-of-the-art rectifier's PDR extension techniques have been reviewed and discussed in this article, designers should also consider other design aspects which can also contribute to the overall performance improvement of the RFEH system.

To improve the sensitivity, an antenna-rectifier co-design has been proposed in [83], [115]–[120] to reduce the minimum input RF power required in generating the targeted output voltage. This is achieved by resonating the antenna inductance and the rectifier input capacitance to boost the input signal into a larger voltage swing at the input of the rectifier [83], [116]. Fig. 7(a) illustrates a simplified diagram of the antenna-rectifier co-design. The elimination of the impedance matching network in the proposed antennarectifier co-design reduces the circuit complexity and costs while improving the sensitivity, thereby extending the range of operation and PDR of the RFEH system. An optimized

Ref.	Tech. (nm)	Freq. (MHz)	Rectifier Topology	Ν	PDR Extension Technique	Output Load	VDC	Sensitivity at 1 V	Peak PCE	PDR (dB)	FoM *
[17] ^b	180	900	CCDD	1	Double-sided self-biasing	100 kΩ	1.3 V	-18.2 dBm	66% @ -18.5 dBm	13.5	20.1
[65]°	350	13.56	CCDD	1	Reconfigurable	500 Ω	2.2 V	3 dBm	82% @ 3 dbm	12	4.2
[66]°	65	900	CCDD	5	Dual-path	147 kΩ	2.8 V	-17.7 dBm for $\infty \Omega$	36.5% @ -10 dBm	11	1.8
[89] ^b	180	433	CCDD	1	Self-biasing	100 kΩ	1.6 V	-17 dBm	51.5% @ -18 dBm	14	14
[90] ^a	65	953	Dickson/ CCDD	4/4	Dual-input	150 kΩ	5.5 V	-20.6 dBm for 100 kΩ	47.87% @ -19 dBm	25	6.8
[91]°	180	902	Dickson	2	Reconfigurable	200 kΩ	4 V	-20.2 dBm for 1 MΩ	33% @ -8 dBm	13	4.8
[92]°	180	915	Dickson	2-3- 4-6- 12	Reconfigurable	10 kΩ	2.2 V	-17.8 dBm for 1 MΩ	34.4% @ 1.3 dBm	13	0.8
[93]°	130	820	Dickson	1-2- 4-8	Reconfigurable	$4.7 \ \mathrm{k}\Omega$	1 V	-3 dBm	39% @ -5 dBm	14	1.5
[94] ^b	180	915	Dickson	1-2- 4-8	Reconfigurable	1 MΩ	1.8 V	-14.8 dBm	25% @ -5 dBm	10	0.7
[95]°	130	868	CCDD	2	Reconfigurable	n.a.	2 V	-21 dBm @ 2V	60% @ -8 dBm	19	12.8
[96] ^b	65	5750	Class-DE	1	Bidirectional	400 Ω	n.a.	-10 dBm	52% @ 5 dBm	19	30.2
[97]°	350	13.56	CCDD	2-3	Reconfigurable	2 kΩ	5 V	3 dBm	76% @ 7 dBm	15	1.6
[98] ^b	180	1000	CCDD	1	Self-biasing	100 kΩ	1.5 V	-18 dBm	65% @ -21 dBm	17	25.4
[99] ^b	130	900	CCDD	3	Self-body- biasing	100 kΩ	2.4 V	-18.7 dBm	80.3% @ -17 dBm	14.5	8.8
[100] ^b	65	433	CCDD	1	Dual-mode nested	100 kΩ	1.1 V	-19.2 dBm	86% @ -20 dBm	26	43.3
[101]°	130	896	Dickson	4	Optimum voltage compensation	1 MΩ	6.5 V	-22 dBm	51% @ -11 dBm	10.5	3
[102]°	130	915	CCDD	10	Threshold voltage compensation	450 kΩ	3 V	-29 dBm for 100 MΩ	42.4% @ -16 dBm	8	0.8
[103]°	65	2450	CCDD	2	DC-boosted gate bias	13.8 kΩ	2.9 V	-12 dBm for $\infty \Omega$	73.6% @ -6 dBm	15	14.8
[104]°	65	2450	CCDD	1	MPPT, modeling and parasitic aware	n.a.	1 V	-17.1 dBm @ 0.4V	48.3% @ -3 dBm	11	14.3
[105]°	180	2400	CCDD	3	Resistance compression	5 kΩ	1 V	-16 dBm for $\infty \Omega$	47.1% @ -6 dBm	16	6.7

TABLE 3. Performance summary and comparison of recently published works on wide PDR RFEH rectifier.

^aSimulation; ^bOn-chip measurement; ^cCoB measurement; ^{*}Calculated using equation (11)



FIGURE 7. Simplified block diagram of RFEH design further outlook. (a) Antenna-rectifier co-design [116], [120]. (b) Integration of PMU with MPPT [132]. (c) RF combiner in multiband RFEH system [121]. (d) DC combiner in multiband RFEH system [121].

design methodology is critical to ensure the antenna-rectifier co-design is integrated and matched perfectly to avoid any loss.

To fully utilize the available ambient RF energy for harvesting, numerous research work has been carried out on wideband or multiband ambient RFEH systems [49], [60], [121]-[126] to overcome the limitation of narrowband RFEH. It is evident from the RF surveys that there are a few different frequency bands that have shown promising power density depending on the harvest location. As more power is harvested from these frequency bands, the efficiency of the RFEH system can be relatively better. RF combiner and DC combiner are the two circuit architectures that are used for multiband RFEH as shown in Fig. 7(c) and Fig. 7(d), respectively. An investigation has been made in [121] to discuss their advantages and disadvantages for multiband RFEH. Nevertheless, when designing a multiband RFEH system, suitable circuit architecture is chosen based on their desired applications for reliable operation and high efficiency with the selection criterion such as frequency, transistor's threshold voltage, design tradeoffs, etc.

Apart from that, a power management unit (PMU) can be integrated into the RFEH system to regulate and manage the output voltage of the rectifier. Voltage regulator [127], [128] is included in the PMU to smooth the rectified voltage fluctuations caused by the varying RF input power density. If the rectifier output voltage is too low for the desired application, it can be boosted using a low-startup DC-DC converter [129]–[131] in the PMU to generate a usable output voltage. To ensure that the power is being harvested at maximum efficiency, an MPPT circuit is implemented in [132] to control the switching frequency of the DC-DC converter and the configuration of the impedance matching network for optimizing the performance of the RFEH system, as shown in Fig. 7(b). Lastly, a storage element can also be integrated into PMU to store the harvested power.

VI. CONCLUSION

This article has presented a review of the recent research progress of the CMOS RF-DC rectifier for RFEH system based on its PDR performance. The review covers the transmission of the RF power to provide an understanding of the varying nature of the available ambient RF power. An overview of the RFEH front-end circuit is included to discuss the characteristics of each of the main circuit components with their design consideration, challenge, and limitation. The performances of prior state-of-the-art wide PDR CMOS rectifiers are summarized and compared to investigate the development of the circuit design techniques. A section on the RFEH design further outlook has also been presented to explore other design aspects which contribute to the overall performance enhancement of the RFEH system. In addition, the de-embedding process to accurately measure the designed rectifiers is explained. To endure a high PCE over a wide range of RF input power densities, the PDR extension technique for the CMOS RF-DC rectifier has been the recent research interest and direction to enable power autonomous ubiquitous devices in IoE applications.

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