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A Versatile SoC/SiP Sensor Interface for Industrial Applications: Implementation Challenges

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ABSTRACT We present in this paper design considerations and implementation challenges of a proposed versatile SoC/SiP sensor interface intended for industrial applications. The proposed interface involves high-voltage circuits such as class-D power amplifiers, gate drivers, level shifters, and electrical isolators. Also, it includes low-voltage blocks like programmable gain amplifiers and ADCs. In addition, DC-to-DC converters are used to supply the various building blocks of the projected sensor interface. The key challenges for implementing each block are discussed in this paper. Also, the technological aspects to support the proposed SoC/SiP solution are given. Moreover, the different available packaging technologies to implement the intended SiP solution are discussed in addition to the thermal aspects associated with the system packaging.

INDEX TERMS Industrial applications, sensor interface, versatility, system-on-chip (SoC), system-in-package (SiP), thermal management.

I. INTRODUCTION

Sensor interfaces are key circuits in many industrial applications such as automotive, robotics, industrial control, and aerospace. They are required to provide reliable high current and voltage to many industrial sensors and actuators and to read feedback signals for further processing. Their reliability, safety, and efficiency are important factors and these properties depend on their internal blocks. In addition, cost, size, weight and power (CoSWaP) are important factors that should be considered for optimization. Moreover, these interfaces are connected to different loads and sensors that typically have their own current and voltage requirements. Therefore, the sensor interfaces should be adjusted for different needs. Redundancy and lack of versatility/flexibility motivate interfaces' manufacturers to look for ways to reduce CoSWaP by shrinking the size of components and making sensor systems more flexible. This helps to ease maintenance and gain economic benefits.

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System-on-chip (SoC) and system-in-package (SiP) are strong candidates to reduce the CoSWaP of electronic systems and allow versatility, flexibility, and reconfigurability. In SiP, separate chips are packaged together into a system with a very small form factor using a common two-dimensional (2-D) or three-dimensional (3-D) substrate. It is suitable for integration of systems combining different fabrication processes, where meeting all specifications with a single chip is difficult or too expensive. Therefore, a SoC can be part of a SiP solution. Several sensor interface solutions for industrial applications were presented in the literature. In [1], [2] an interface chip for eddy current displacement sensors was reported. This interface includes an oscillator to generate a high-frequency carrier signal, where eddy current displacement modulates the carrier amplitude. A peak detector-based amplitude modulation circuit was used to demodulate the carrier signal. An off-chip analog-to-digital converter was also used to digitize the measured signal for further processing. This interface presents only readout circuits with off-chip ADC. Also, it does not allow any type of versatility.

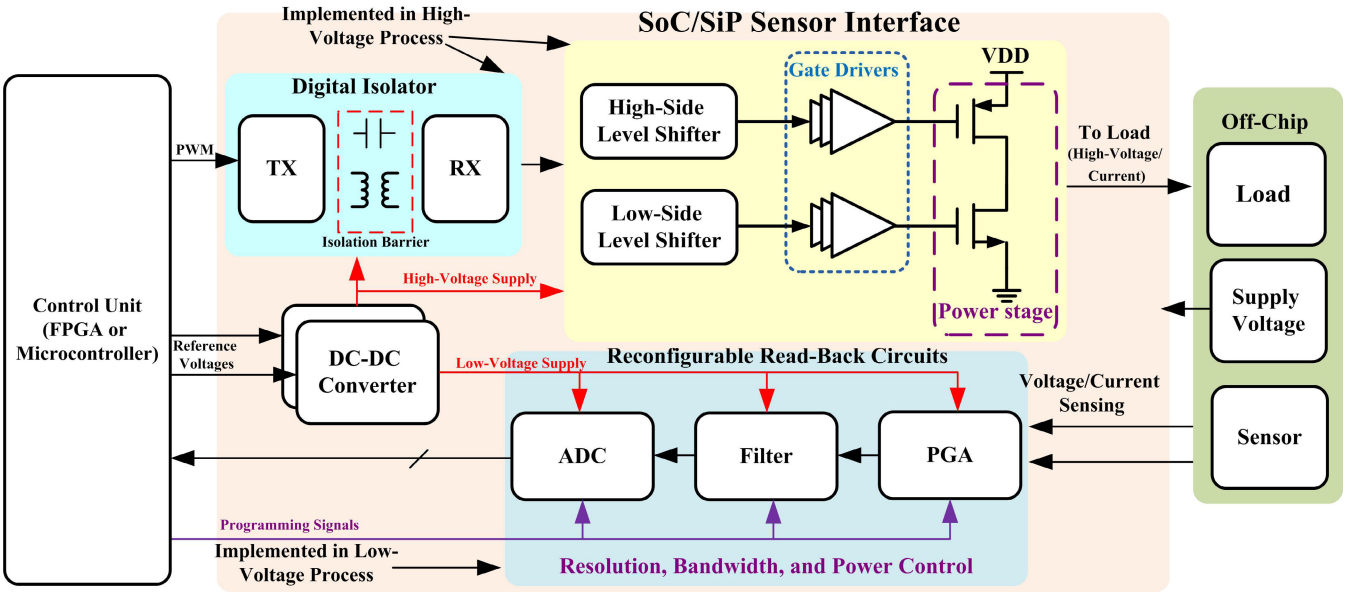


FIGURE 1. Block diagram of the proposed versatile SoC/SiP sensor interface.

Another sensor interface was presented in [3] for angle measurements in industrial applications. In this interface chip, the measured signal is firstly applied to a programmable instrumentation amplifier. Then, the amplifier output is converted to digital form using an integrated ADC. Also, this interface topology includes an internal voltage regulator that allows using non-regulated supply voltages from external supply sources. Although this interface allows programmable features, it deals only with low-voltage and low-power applications. Moreover, several interfaces for resistive and/or capacitive sensors were reported [4]–[7]. These interfaces are suitable for low-power applications such as multi-sensor microsystems. An ultra-low-power, wide dynamic range interface circuit for capacitive and resistive sensors is reported in [5]. This interface was implemented as a switched-capacitor circuit using programmable capacitors to achieve high configurability.

In this paper, we present implementation challenges and possible solutions that relate to SoC/SiP based sensor interfaces intended for industrial applications. To address these challenges, several existing techniques and methods can be used to implement the various system's sub-blocks and circuits. Moreover, packaging and thermal issues that relate to SoC/SiP implementation are carefully covered.

The rest of the paper is organized as follows: Section II introduces the proposed versatile SoC/SiP based sensor interface and outlines the methodology adopted to implement it. Section III discusses design considerations of each building block of the proposed interface. In Section IV, several technological challenges associated with the proposed design are identified. Section V explores various packaging techniques that could be adopted for the intended SiP integration. Thermal aspects associated with the SiP integration are discussed in Section VI, where thermal modeling of various packaging approaches is presented in addition to the on-chip thermal monitoring techniques. The main findings and considerations of this work are summarized in Section VII.

II. PROPOSED VERSATILE SoC/SiP SENSOR INTERFACE

A. SYSTEM OVERVIEW

Figure 1 shows the general block diagram of the proposed versatile SoC/SiP sensor interface [8]. It aims to support different loads and sensors with different specifications. Some of specifications may need to be configurable or programmable such as bandwidth, resolution, excitation current/voltage, etc. The sensor interface's building blocks are divided into two main categories: high-voltage blocks (HVBs) and low-voltage blocks (LVBs). HVBs include power electronics such as class-D amplifiers (including gate drivers and level shifters), digital isolators, and DC-to-DC converters. These blocks involve power transistors that operate at high voltage levels (up to 120 V). Thus, a high-voltage process must be used to implement these blocks. On the other hand, LVBs are mainly the read-back circuits, which involve programmable gain amplifiers (PGAs), filters, and data converters. They operate with nominal voltage ratings (up to 3.3 V), and thus low-voltage processes can be used to integrate these blocks. Each command sent to the sensors is initiated from the control unit implemented either with a field-programmable gate array (FPGA) or a microcontroller. In addition, the control unit monitors the feedback system to perform the required loop tuning. Also, an integrated controller can be used to perform fast loop tuning.

TABLE 1. Performance comparison of high-voltage and high-power class-D power amplifiers.

References	JSSC 2003 [9]	JSSC 2004 [10]	ISSCC 2006 [11]	ISSCC 2009 [12]	JSSC 2012 [13]	JSSC 2014 [14]	JSSC 2015 [15]	JSSC 2016 [16]	JSSC 2017 [17]
Process	BCD SOI	0.6 μ m BCD	0.4 μm/1.8 μm BiCMOS	BCD SOI	0.35/3 μm HV CMOS	0.14 μ m BCD SOI	0.14 μ m BCD SOI	0.18 μm BiC-MOS	0.14 μ m BCD SOI
Supply voltage (V)	60	20	50	85	18	80	80	24	25
Max. output power/ch.	100 W	20 W	240 W	460 W	13 W	45 VA	45 W	70 W	80 W
Efficiency @ Max. output power (%)	90	89	NA	90	88	94	91	90	90
Load	4 Ω	8 Ω	4 Ω	8 Ω	8 Ω	23 μF + 1.6 Ω	12 Ω	22 μF + 4 Ω	40 Ω
THD+N (%)	0.017	0.01	<0.1	10	<0.7	0.03	NA	0.03	10
Dynamic range (dB)	103	NA	NA	NA	84	NA	NA	108	115
Dead time (ns)	70	20	NA	NA	15	100	100	NA	
Die size (mm^2)	22	12	NA	NA	48.9	6.324	8.5	13.4	NA

B. IMPLEMENTATION METHODOLOGY

The methodology adopted to implement the targeted sensor interface involves five steps: modeling, implementation, chip integration, validation, and system level packaging.

1) MODELING

The sensor interface must be behaviorally modeled to examine the effects of circuit imperfections on the overall performance, to inspect the interaction of different modules, and to optimize different control and design parameters that can be adjusted to meet the target specifications. MATLAB® and Simulink® will be used to take advantage of the short simulation time they offer for system design as compared to circuit or physical level simulations. Verilog-A/AMS will also be used as a bridge between behavioral simulations and circuit implementations.

2) TRANSISTOR-LEVEL IMPLEMENTATION

After verifying the system behaviour through modeling, all analog building blocks will be implemented at the transistor level with a proper silicon process, and their performances will be verified with simulations using different process, voltage and temperature (PVT) sets of parameters. The Cadence® Virtuoso® custom design platform will be used for this phase of the design.

3) LAYOUT AND SoC INTEGRATION

Physical implementation of the building blocks in the target system will be performed and as a step in that direction, their post-layout simulations will allow examining the effects of parasitics and physical imperfections such as mismatches on the performance of each building block. Then, the final design of the various modules in the target system will be submitted for fabrication.

4) EXPERIMENTAL VALIDATION

Each fabricated chip will be wirebonded inside a package. The latter will be soldered to a custom printed circuit board (PCB) to facilitate the experimental characterization. Various tests and measurements must be performed to validate and characterize experimentally the performance of each integrated building block as well as the functionality of the fabricated SoC module.

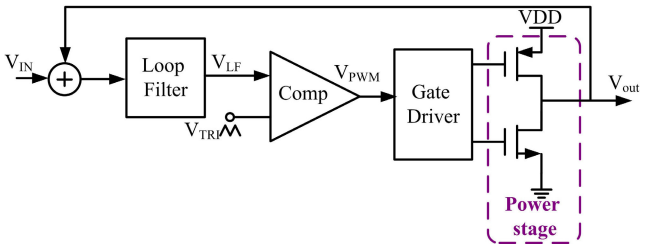


FIGURE 2. Conventional closed-loop class-D amplifier.

5) SiP INTEGRATION

A proper multi-chip packaging technology will be adopted to implement the projected SiP-based sensor interface. SiP enables using dies fabricated with different manufacturing technologies in different parts of the system that have conflicting requirements such as voltage range, isolation for signal integrity and for protection against transient surges, integration density and finally pure performance provided by fine pitch technologies. It is generally recognized that trying to satisfy a wide range of contradictory requirements with a single monolithic integrated circuit tends to be impractical or very costly which militates for multi-dies SiP solutions. The resulting modules will thus integrate high and low-voltage chips in a single package. This SiP prototype will be experimentally validated to ensure its functionality and the compatibility of its various constituents (IP modules, packaged ICs or chips on board; various possible options will be investigated).

III. SENSOR INTERFACE BUILDING BLOCKS

In the following subsections, we present the role, design considerations, and implementation challenges of each

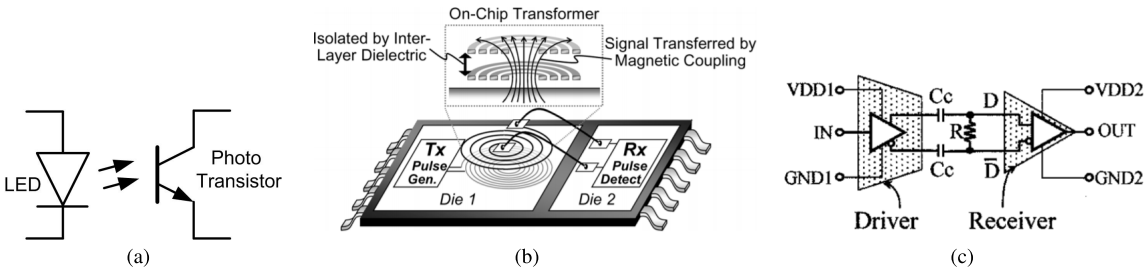


FIGURE 3. Isolation techniques (a) Optocoupler, (b) On-chip-transformer [18], and (c) Capacitive isolation [19].

building block of the proposed interface. Also, a quick review is conducted to show the most recent reported progress for each block.

A. CLASS-D POWER AMPLIFIER

The power amplifier in the proposed interface is used to provide proper current or voltage waveforms to excite external actuators. A class-D configuration was chosen to implement the amplifier as it offers a better efficiency compared to other classes. Our goal is to implement a versatile power amplifier to provide a configurable waveform. Thus, a high-voltage high-power class-D amplifiers are required. Their specification, requirements, and structure are similar to class-D amplifiers for audio applications.

However, one of the research challenges is to improve the amplifier's immunity against power supply bounce to avoid performance degradation. To obtain the desired immunity, internally regulated floating supply voltages, variable driving strength for the gate drivers and efficient two-step level-up shifter are some possible solutions [14].

Another issue is that during the ON/OFF transition of the active devices (forming the power stage), there is a short period of time when both PMOS and NMOS transistors, shown in Fig. 1, may conduct simultaneously. This would result in a low resistance path between VDD and ground. Therefore, a large current, known as shoot-through current, would be induced. This would cause significant energy losses degrading energy-use efficiency.

To minimize shoot-through induced losses, the overlap of PMOS and NMOS drivers on periods during the transitions should be minimized. This can be achieved by employing non-overlapping circuit configurations, which generate two non-overlapped signals to drive the power transistors [20], [21]. Also, suitably designed distinct driving circuits for PMOS and NMOS transistors may help eliminate shoot-through current [22]. Another significant challenge stems from the need to drive various loads with very different specifications. A possible solution is to use a configurable class-D power amplifier in which the active configuration can be selected through a tuning signal [23].

It is also worth considering adoption of closed loop class-D amplifiers similar in structure to class-D audio power amplifiers shown in Fig. 2 [24]. With this configuration, the amplifier performance can be improved through a feedback mechanism to mitigate imperfections and distortions. Table 1 summarizes the performance of various high-voltage and high-power Class-D power amplifiers reported in the literature. The implementations reported in Table 1 have used a wide range of technologies such as Bipolar, CMOS, and DMOS (BCD) process to satisfy the reported performances.

B. ELECTRICAL ISOLATOR

In the proposed interface, the power transistors as well as the read-back circuits have to communicate with the control unit. Due to high electrical potential differences, there are cases where the control unit cannot be connected directly to the gate drivers. Therefore, an electrical isolation between the control unit and gate drivers is needed. As shown in Fig. 3, several classes of isolation techniques can be adopted, including optocouplers, integrated transformers, and capacitive couplers. Although optocouplers can provide the required isolation, they suffer from undesirable aging effects, which cause the couplers gain to decrease over time [25]. This affects their performance and efficiency. In addition, optocouplers are fabricated with GaAs technology, and hence they cannot be integrated with the rest of the system if a SoC is targeted. CMOS isolators exploiting on-chip transformers [18] can be utilized to cope with the optocouplers limitations. Transformer based isolators can consume little power but they tend to consume large silicon area. Although, capacitve isolators are easy to be integrated with smaller area compared to inductive isolators, they tend to consume more power [19], [26].

There is room for research on new methods to implement required isolators in a more compact way, while achieving a high data communication rate and high isolation. Single transformer configuration, pulse polarities, and pulse count method are some of the previously introduced solutions for realizing digital isolators with small integration area [27]–[29]. Furthermore, a highly integrated Watt-level power transfer system implemented in a standard silicon technology has been recently introduced in [30]. It is of interest that this previously reported solution does not need post-processing steps or external components. Other promising research avenues on isolator design try exploiting 2.5-dimensional

(2.5D) and 3-dimensional (3D) implementations based on Micro Electro Mechanical Systems (MEMS) processes.

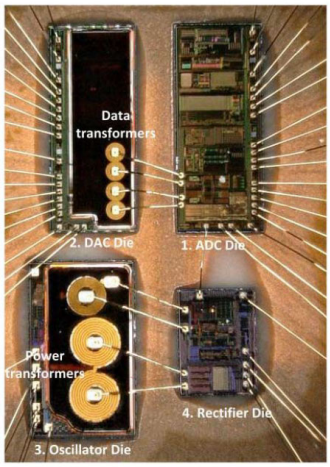


FIGURE 4. SiP of the fully isolated amplifier in [31].

C. PROGRAMMABLE GAIN AMPLIFIER

Usually, each actuator comes with its own sensor. These sensors convert the physical signals (movement, pressure, etc.) into electrical signals. In order to support a wide range of sensors specifications, programmable gain amplifiers (PGAs) are used as a first block in the read-back path [32]. The amplifier gain is programmed so that it generates an output signal that is compatible with the input dynamic range of the analog-to-digital converter (ADC). Several gain programming techniques (analog and digital) have been presented in the literature [33]. Some of these techniques that are used in open loop PGA topology include varying the transconductance by tuning a bias current, exploiting controlled current dividers, and introducing a source degeneration resistor. In contrast, in closed loop PGA configurations, the gain can be tuned by changing a feedback resistor or an input resistor.

Since the PGA is the first circuit in the feedback path, it has to tolerate all types of anomalies on its inputs. For example, in power conversion applications, like power system control and protection, several parameters have been defined by safety standards to help mitigate a wide range of fault conditions [34]. An example is the 1-minute isolation withstand voltage that shows the circuit tolerance to short duration over-voltage that may occur when switching loads or following some faults. Also, the surge withstand voltage is another parameter that represents tolerance to a particular transient profile. Thus, a very high common voltage rejection PGA design should be considered. Therefore, an electrical isolation barrier including circuits to transmit and receive the signal across this barrier has to be employed. Several approaches have been proposed to obtain this isolation. In [31], an amplifier exploiting galvanic isolation based on successive approximation register (SAR) converters has been presented. It achieves an isolation rating of 600 Vrms and 5 kVrms over 1 min duration. However, it has a high complexity, and four dies are required to construct the whole amplifier in an SiP as shown in Fig. 4. Another galvanic isolated amplifier exploiting two integrated Hall-effect sensors was reported in [35]. This approach shows continuous isolation working voltage of 550 V.

D. FILTERS

Filters are required in the projected interface to condition signals from the PGAs before applying them to the ADCs. These filters must have tunable gain and bandwidth to support a wide range of sensor specifications. In [45], a tunable biquad switched-capacitor filter was presented. It supports low-bandwidth applications. The bandwidth of that filter can be tuned by changing the frequency of the sampling clock. In [46], a variable gain filter was constructed with a combination of continuous-time and switched capacitor integrators. In this design, a variable resistor array was used to tune the DC gain of the filter in the -13.3 dB to 16.4 dB range. An ADC with an embedded anti-aliasing filter (AAF) has recently been implemented in [47]. The authors claim that merging such filter with the ADC reduces chip area and power consumption. Similar concepts can be adopted to implement the filters used in the proposed sensor interface, while utilizing inverter-based operational transconductance amplifiers to drastically reduce the power consumption [48]. It is of interest that providing reconfigurable gain and bandwidth without increasing the design complexity is a major challenge.

E. ANALOG-TO-DIGITAL CONVERTER

The analog signals amplified by the PGA are assumed to be applied to an ADC. Then, the resulting digitized signal is transferred back to a control unit. However, the proposed interface is intended to cover a wide range of sensors specifications. Some system functions need high precision tuning, while other functions do not need such high precision. This sets a need to have resolution tuning as an important feature of the ADCs. Variable resolution ADCs allow reducing the power consumption when a medium or low resolution mode is used [43], [49]–[53]. For example, the resolution-tunable ADC reported in [43] consumes 1.6 mW at 18 bit resolution, while it consumes only 0.39 mW when running at 11 bit resolution. Several approaches have been presented in the literature to control the resolution of ADCs. A pipelined ADC given in [52] allows tuning resolution from 10 to 12 bits, which does not meet some sensor interface requirements. A wider resolution tuning range (from 6 to 10 bits) is offered by the pipelined ADC in [53]. Also, a 5 to 10 bit design was presented in [49]. These ADCs, like the one reported in [52], suffer from the limited resolution tuning range.

Apart from achieving reconfigurable resolution, various high resolution ADCs have been introduced in the literature. A 22 bit 3rd order single loop incremental ADC was presented in [54] for instrumentation and measurement applications. Also, a 20 bit incremental zoom-ADC has been given in [55]. In addition to the need for high resolution, there is a

TABLE 2. Performance comparison of different incremental ADCs as well as resolution-tunable ADCs.

References	JSSC 2017 [36]	TCAS-II 2018 [37]	JSSC 2015 [38]	TCAS-II 2019 [39]	JSSC 2019 [40]	JSSC 2019 [41]	JSSC 2019 [42]	IEEE Access 2019 [43]	TCAS-I 2013 [44]
Architecture	IADC1 + Multis-lope	IADC2	IADC1 + IADC2	SAR + IADC1 + EC	IADC + SAR	I $\Delta\Sigma$	Linear-exponential IADC	IADC + SAR	Pipeline
Process (nm)	180	180	65	180	180	180	65	180	90
Supply (V)	1.5	1.2	1.2	1.8	1.8	3	1.2	1.8	1.2
Sampling freq. (Hz)	642 k	10 k	96 k	1.24 M	0.4 M	3 M	10.24 M	33.3 M	0.4 M to 44 M
BW (Hz)	1 k	100	250	2 k	2.04 k	100 k	20 k	6.3 k	0.2 M to 22 M
Resolution (bit)	16	16	16	18	16	15	12	11 to 18	10 to 12
Power consumption (μW)	34.6 μ	0.24 μ	10.7 μ	176 μ	25.4 μ	1.098 m	550 μ	0.39 m to 1.6 m	0.184 m to 22.87
Area (mm^2)	0.5	0.55	0.2	0.78	0.66	0.363	0.13	0.64	1
Max. SNR (dB)	98.4	93.4	NA	103.9	96	88.2	NA	110.4	NA
Max. SNDR (dB)	96.8	NA	90.8	101.4	95.5	86.6	100.8	107.9	65.1
DR (dB)	99.7	NA	99.8	109.1	102.2	91.5	101.8	116.1	NA

need for wide dynamic range ADCs. In [56], a wide dynamic range ADC based on the delta-sigma modulation technique was proposed for automotive sensor interfaces. Implemented with switched capacitor circuits, it offers 20 kHz signal bandwidth.

All these possible requirements combined with the need to minimize power consumption. A delta-sigma modulator exploiting a shared inverter based operational transconductance amplifier shows a good efficiency when it comes to resolution and power consumption [48]. For instance, the modulator proposed in [48] consumes 60 μW while offering a 20 kHz signal bandwidth. A key challenge regarding ADC design is to provide a variable resolution architecture offering an improved maximum resolution, while maintaining low power and area consumption.

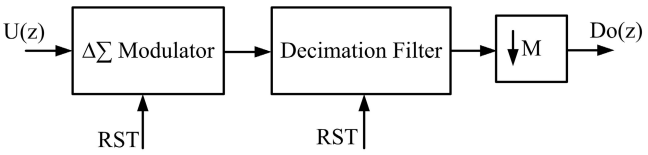


FIGURE 5. Block diagram of incremental ADC.

It is also required that ADCs be capable of sampling multiple channels to allow reading signals from numerous sensors attached to the interface. The need of a multi-channel ADC with relatively high and reconfigurable resolution suggests using incremental ADCs that offer excellent solutions for low-frequency high-accuracy sensor interfaces [36]–[44], [57]. Figure 5 shows the conceptual block diagram of an incremental ADC, where an embedded modulator is used to perform noise shaping, which helps improving accuracy. In that ADC, a reset signal (RST) is used to clear all the memory elements after each conversion cycle lasting for M clock periods. Thus, incremental ADCs operate intermittently and provide a sample-by-sample conversion, which is compatible with applications where some multiplexed low-frequency signals with high-accuracy need to be converted. Table 2 summarizes the measured performances of several significant recently reported incremental ADCs as well as resolution-tunable ADCs.

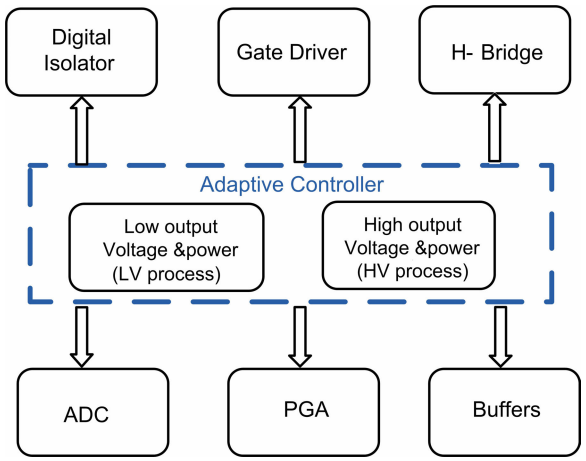


FIGURE 6. DC-to-DC converters required to supply the interface's blocks.

F. DC-TO-DC CONVERTER

In industrial environments, the DC source supply may not be stable. Nevertheless, the sensor interface requires clean and steady DC supply voltage for proper operation. Providing stable and clean power supply with a high conversion efficiency to sensitive sensor interfaces by drawing power from an unstable source is challenging. The proposed architecture tackles this challenge with DC-to-DC converters. As shown in Fig. 6, the proposed architecture uses two main converters; a high-voltage and high-power converter to feed the high voltage blocks (HVBs) and a low-voltage and low-power

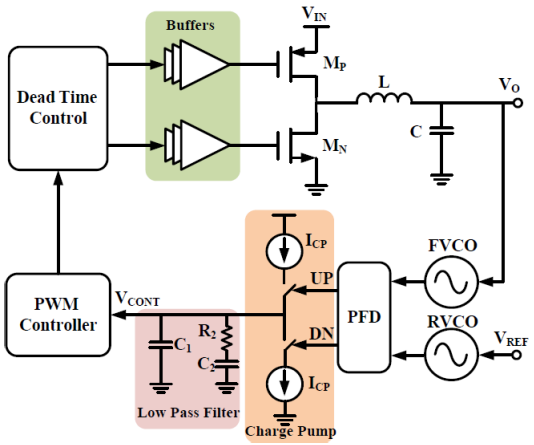
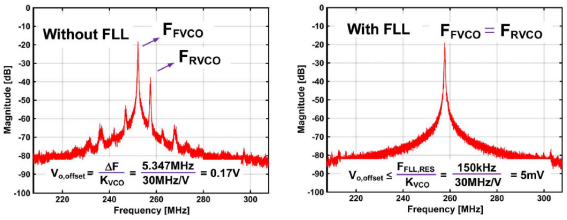


FIGURE 7. Block diagram of a proposed time-based controller for buck converter [58].



(a) (b)

FIGURE 8. Frequency spectra of the two VCOs in the time-based controller [59] (a) without FLL and (b) With FLL.

one to supply the low voltage blocks (LVBs). Switching-mode DC-to-DC converters are adopted as they provide higher efficiency compared to linear converters. Switching buck converters can be designed using either controllers with hysteresis or pulse width modulation (PWM) based controllers. Although control with hysteresis has low complexity and is simple to implement, while providing good efficiency and fast transient response, its non-linear behavior can lead to large output ripple and wide variations in switching frequency. On the other hand, PWM controllers can operate with constant switching frequency while offering excellent efficiency. However, they require large inductance and capacitance (L and C) values that are either impractical or impossible to integrate. One solution to decrease the size of the L and C is to increase the switching frequency. This, however, increases the switching losses with a corresponding degradation of the converter efficiency. Burst mode control and segmented output control can be used to further improve the efficiency [60]. In addition, increasing the switching frequency complicates the design of proportional-integral-derivative (PID) compensators and makes it very difficult to obtain wide output voltage range without compromising stability [61]. Although digital controllers can operate at high frequency, they suffer from large ripple at the output, poor transient response and high consumed power [61], [62]. Recently, a time-based controller was presented in [58], [59], [63]–[65]. In this approach, time is used as the processing variable, where voltage-mode and current-mode DC-to-DC converters are controlled by time-domain circuits, including voltage-controlled oscillators (VCOs), phase detectors, and voltage-controlled delay lines. This eliminates the need for wide bandwidth amplifiers, fast voltage comparators, and high-resolution ADCs, which results in lower power consumption, higher efficiency, and smaller silicon area.

Time-based controllers are thus preferred in the proposed SoC/SiP sensor interface. Fig. 7 shows our preliminary proposed time-based controller for the intended buck converter. One key challenge in the presented design is the use of two identical VCOs where any mismatch between them results in output voltage offset. To overcome this issue, a frequency calibration scheme is needed. In [59], a frequency locked loop (FLL) has been employed to calibrate the two VCOs, where the output spectra of the two VCOs has been measured as shown in Fig. 8. When the FLL is turned off, a 5.35 MHz offset frequency has been observed which resulted in an output offset voltage of 170 mV. On the other hand, when the FLL is included, the frequency error has been decreased to 0.15 MHz which resulted in only 5 mV output voltage offset. Another possible calibration scheme has been presented in [66], where the same control loop with an additional low-pass filter can be used to calibrate the two VCOs. Table 3 summarize the proposed interface's main blocks and their functions and projected specifications.

IV. TECHNOLOGICAL CHALLENGES

From the supply voltage point of view, two types of integrated circuits (ICs) will be implemented; high-voltage and low-voltage. As the high-voltage environment has a nominal specification of more than 20 V and target specifications set requirements such as high density and high performance, selecting the right integration technology requires careful consideration. In addition to the high voltage requirements, high-current capabilities are required in some blocks in the projected interface such as the power stage circuits. These circuits are constructed from power transistors to deliver a large amount of current to off-chip actuators. Also, power stages are involved in the high-voltage DC-DC converters to allow a stable supply voltage to the HVBs. Adopting power transistors based on silicon-on-insulator (SOI) technology can reduce the capacitance loss, and thus improve the efficiency [22]. On one-hand, several high-voltage processes (Bulk and SOI) are available to implement the HVBs. On the other hand, a standard 65 nm CMOS process offers a good option due to its availability, affordability, reliability, and high density. It is also possible that both HVBs and LVBs be implemented with a same high-voltage BCD process, like the AMS 0.35 μm HV CMOS process [68], [69]. Such a process facilitates SoC integration. However, using such a technology can become impractical or significantly increase power consumption if the LVBs are very complex. Indeed, the normal low-voltage power supply is 3.3 V, which increases power consumption over the

TABLE 3. Summary of the proposed interface main blocks with their functions and projected functional requirements.

Block	Function	Selected Architecture	Specifications/requirements
Class-D Power Amplifier	Provide proper current or voltage waveforms to excite external actuators	Closed loop class-D amplifier	High efficiency, provide a configurable waveform, high-voltage high-power design, good immunity against power supply bounce, and drive various loads with very different specifications.
Electrical Isolator	Allows isolation between the control unit and gate drivers	Pulse polarities or pulse count-based digital isolator	Fully integrated, high data communication rate, and high isolation capabilities.
Programmable Gain Amplifier (PGA)	Amplify signals received from the external sensors	Hall-effect-based PGA	Programmable gain feature, tolerate all types of anomalies on its inputs, and very high common voltage rejection.
Filters	Condition signals from the PGAs before applying them to the ADCs	A new topology that could be embedded with the ADC should be developed	Tunable gain and bandwidth (to support a wide range of sensor specifications), low power, and small area.
Analog-to-Digital Converter	Digitizes the PGA's output signals	Incremental ADC	High and tunable resolution, sampling multiple channels, low power, and small area.
DC-to-DC Converter	Provides a stable and clean power supply	Time-based DC-to-DC converter	High conversion efficiency, and minimized switching losses

TABLE 4. Various processes that can be used to integrate the high-voltage blocks.

Process	AMSP35	CMOSP8	XH035	XT018 (SOI)	BCD8sP	BCD8s (SOI)	GaN500
Foundry	AMS	Teledyne DALSA	X-FAB	X-FAB	STMicro-electronics	STMicro-electronics	NRC
Gate Length (μm)	0.35	0.8	0.35	0.18	0.16	0.16	0.5
High-Voltage (V)	20/50/120	Up to 300	45/100	10- 200	5/10/18 /27/42/60	20/40/70 /100/140/200	Up to 40
Low-voltage (V)	3.3/5	2.7/5	3.3	1.8/5	1.8/5	3.3/6	5
Metal Layers	4	3	3	6	4	4	2
Poly Layers	2	2	1	1	1	1	NA
Max. Junction Temp.	125°C	NA	175°C	175°C	175°C	175°C	350°C*

* Experimentally characterized up to 600°C [67].

commonly available 1 V of 65 nm technologies. Other valuable options are Teledyne DALSA 0.8 μm CMOS (High-Voltage) [70], [71], the 0.18 μm isolated SOI CMOS Technology, offered by X-FAB [72], and the STMicroelectronic 0.16 μm BCD [73]. Besides, non-silicon processes such as GaN 500, offered by the Canadian National Research Council (NRC) can be considered. This process has technology files that support design operating up to 350°C [74] and was shown to work reliably up to 600°C [67]. Some key features of these different high-voltage processes are summarized and compared in Table 4. Although the integration of both HVBs and LVBs with the same process (SoC) would make the design compact, using two different technologies (SiP) could reduce the power consumption or allow to support more extreme system specifications.

V. SYSTEM-IN-PACKAGE (SiP) IMPLEMENTATION

A System-in-Package (SiP) generic sensor interface implementation can be obtained by assembling high-voltage and low-voltage chips on a single substrate. In the following subsections we explore various packaging techniques that could be used for such SiP integration.

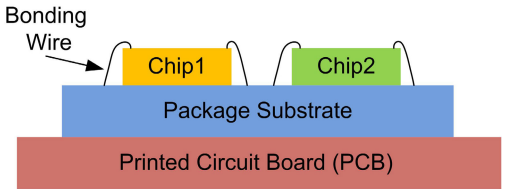


FIGURE 9. SiP integration with muliple chip modules (MCM) packaging.

A. MULTICHIP MODULE (MCM) PACKAGING

A natural solution for SiP integration is the use of multichip module (MCM) packaging, where bare chips are directly connected together on a common interconnecting substrate as shown in Fig. 9. Three main technologies exist to form the package substrate [75]. In laminated MCMs (MCM-L), copper conductors are patterned on fiberglass/resin-impregnated sheets. Under heat and pressure, these sheets are laminated

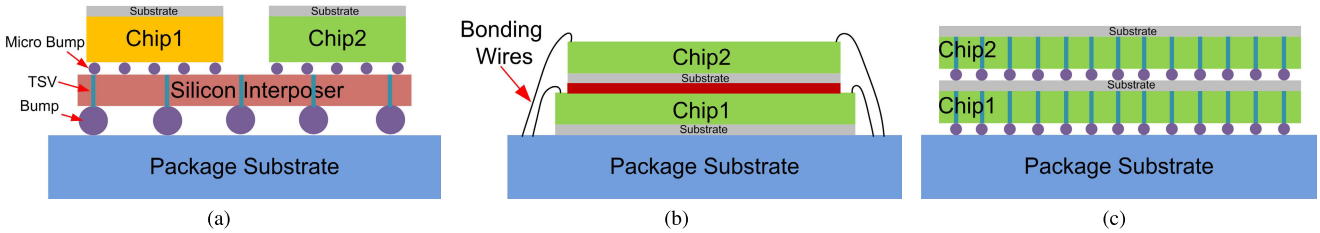


FIGURE 10. Advanced packaging techniques: (a) 2.5D packaging, (b) Traditional 3D packaging based on wire bonding, and (c) TSVs-based 3D packaging.

together, where through via holes are used to connect conductors on various sheets. On the other hand, a prefired ceramic material has also been used to form the substrate in ceramic MCMs (MCM-C). By contrast, a silicon substrate was employed in deposited MCMs (MCM-D), which results in very fine sizes and high wiring densities. In addition, capacitors, resistors, and transistors could be built as part of the substrate. In MCM, the chip to substrate connection can be implemented through wire bonding, tape automated bonding, or solder-bumps. It is of interest that flip-chip solder-bumps are suitable for high-frequency applications since this die attachment method offers lower parasitic inductance and capacitance compared to wire bounding and tape automated bounding [76].

B. 2.5D AND 3D PACKAGING

Advanced packaging technologies such as dies stacking, 2.5-dimensional (2.5D), 3-dimensional (3D), and package on package could also be considered. With these technologies, signal paths between heterogeneous chips (high-voltage and low-voltage) and passive components are shortened. This allows more compact and high-performance SiP solutions. Fig. 10(a) shows an example of 2.5D packaging, where dies are placed side by side on top of a silicon interposer. Thus, die-to-die connections are implemented through the silicon interposer. In addition, through silicon vias (TSVs) are used in the silicon interposer to provide the connections required between the chips and the package substrate.

Traditional 3D packaging is obtained by stacking dies using wire bonding as depicted in Fig. 10(b). Moreover TSVs-based 3D packaging could be considered where connections between bare dies are done using TSVs as shown in Fig. 10(c). 3D integration provides several benefits in terms of electrical performance by increasing the device density, offering design flexibility, reducing signal delay and authorizing new circuits and architectures design. However, it adds complexity and challenges on the thermal management and cooling of SiP, in addition to associated manufacturing costs and introducing various testing and reliability issues.

C. WAFER-LEVEL PACKAGING

Seeking denser SoC and SiP integration with lower cost, thinner profile and better electrical and thermal performance, the wafer-level chip scale packaging (WLCSP) solution was developed to offer better electrical performance and higher density. The proposed solution exploits redistribution layers (RDLs). These RDLs are used to re-route the contacts of the die to another desired location. In Fan-in (FI) approach, as shown in Fig. 11(a), the RDL traces are routed inside the area of the die. However, in Fan-out (FO) (Fig. 11(b)), traces could be expanded outside the die area. To perform heterogeneous integration using dissimilar chips with different functions, fan-out wafer-level packaging (FOWLP) is an attractive solution. In addition to providing greater I/O density, die size shrinking improves thermal and electrical performance. Fig. 12 shows more features of SiP systems exploiting FOWLP. When a RDL process is created before die bonding, the packaging is called chip-last (CL). By contrasts, incorporating the chips in a material structure (molding) followed by RDL fabrication, the process is then known as chip-first (CF).

An improved version of FOWLP is the embedded wafer-level BGA (eWLB) [77]. It eliminates the laminated substrate and improves the pitch. In parallel, a fully molded (FM) configuration is proposed in [78] to eliminate die edge discontinuities and to solve the issue of die shift in the FOWLP structure. Furthermore, fan-out chip-last package (FOCLP) technology was developed [79] to retain the advantages of eWLB technology while providing higher integration density and volume production capacity of the packaging technique. In addition, fan-out panel-level packaging (FOPLP), demonstrated in [80], reduces warpage by using a thicker epoxy molding compound (EMC) and with thinner dies. Fig. 13 illustrates and contrasts three FO packaging technologies: eWLB, FM and FOCLP. Note that eWLB and FM are based on chip-first packaging process, whereas FOCLP is a chip-last process.

D. COST CONSIDERATIONS

Sensor interfaces are usually connected to different loads and sensors that typically have their own current and voltage requirements. Therefore, the sensor interfaces should be adjusted for different needs. Unlike conventional interfaces, the proposed SoC/SiP-based sensor interface have improved versatility, which allows supporting a wide range of sensors/actuators requirements. This results in one SoC/SiP module that could be used for different types of sensors and actuators. Thus, the non-recurring engineering costs of

deploying and maintaining interfaces to serve diverse requirements is reduced. Using advanced packaging technologies like 2.5D, 3D, and Wafer-level packaging increase cost. But they allow a significant reduction in the overall size of the projected SiP interface. By contrast, conventional multi-chip packaging offers low-cost solution. Low-cost options are favored in our first SiP prototype.

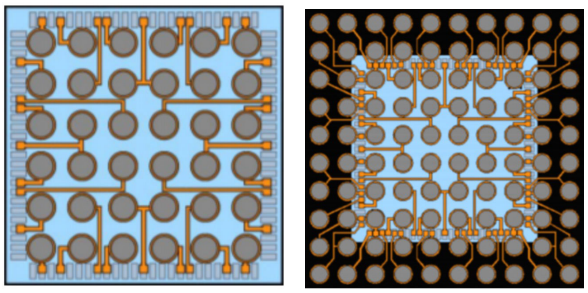


FIGURE 11. RDL configurations: (a) Fan-in: inside the die area (bottom view), and (b) Fan-out: Expanded outside the die area (bottom view).

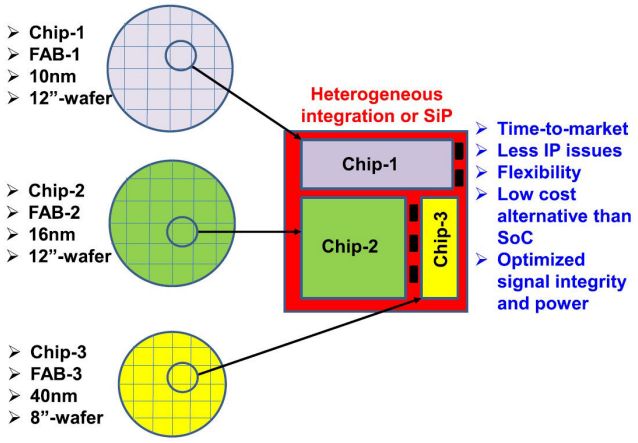


FIGURE 12. Features of an SiP based on FOWLP reported in [81].

VI. THERMAL MANAGEMENT IN SiP

Thermal management is a key issue that should be considered to obtain reliable electronic systems, especially in SoC and SiP implementations. With higher integration density, thermal coupling between adjacent chips becomes critical in addition to the self-heating effect of each chip. High temperatures result in performance degradation and reliability problems.

A. THERMAL MODELING OF SiP

To handle the thermal impact on the performance of SiP, a careful packaging design should be considered. This could be done by using thermal models to predict the thermal performance of packaged chips. Several aspects should be considered in the packaging process to mitigate the thermal

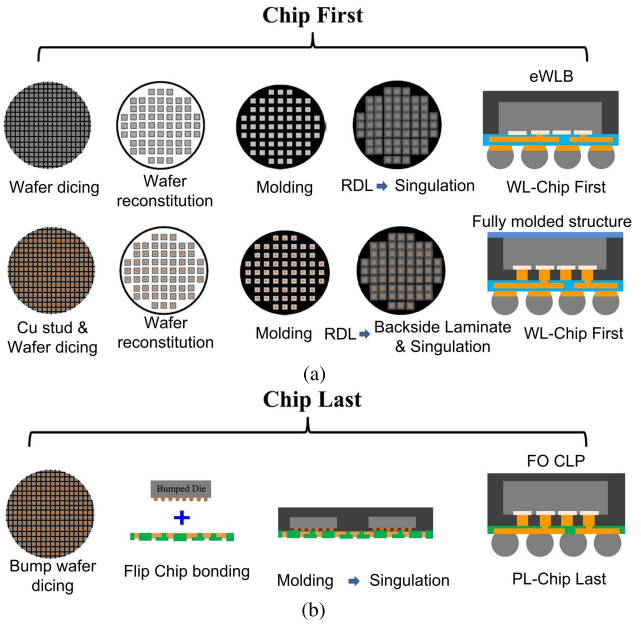


FIGURE 13. Schematic illustrations of FO packaging technology fabrication process flow for [82]: (a) chip-first and (b) chip-last structures.

impact, including the thickness of the package, the type of package and the packaging technology. In addition, the static and dynamic thermal properties of the integrated chips should be investigated during the design of the package.

1) MODELING OF MULTICHIP PACKAGING

A methodology to extract parameters of thermal compact models for multichip packaging system is proposed in [83]. It is based on finite element modeling (FEM) method and experimental temperature measurements of packaged chips. Different types and cross-section areas of packages are investigated in the time and frequency domains of temperature measurements. The extracted compact model was used to show that ultra thin chips ($<20\ \mu$m) suffer crucial increase of temperature in case of localized heat dissipation. Besides, the study showed that temperature variations become independent from the thermal boundary conditions of the chip at high heat pulsing frequencies (>10 kHz).

2) MODELING 3D PACKAGES

Critical analysis of thermal management problems should be investigated when designing very dense systems exploiting 3D interconnection. For instance, thermal characteristics of TSVs and inter-die bonding layers should be analyzed carefully. More precisely, a model for heat dissipation of 3D integrated systems should consider important factors such as density, junction-to-air thermal resistance, multiple junction temperature, and multiple heat sources in a 3D implementation. Analytical and numerical models are developed in [84] to predict the thermal feasibility of 3D SiP. Fig. 14 shows the thermal resistance network of that models, which include 3D

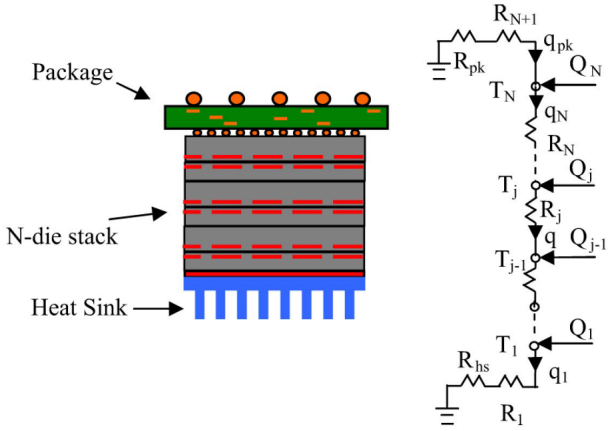


FIGURE 14. Schematic of the general N-die stack and the thermal resistance network with multiple heat generating junctions [84].

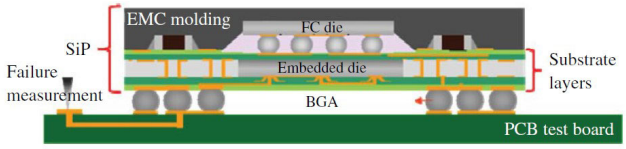


FIGURE 15. Cross sectional view of the studied 3D SiP approach in [85].

integration of N vertically stacked chips. N sources of heat are considered along with the equivalent resistance of package (R_{pk}) and heat sink (R_{hs}). R_N represents the silicon thermal resistance of die N. The dies are stacked face-to-face separated by a back-end-of-line (BEOL) metal-dielectric stack. The thermal resistance between two successive junctions, R_j, includes the thermal resistance of two BEOL layers and the micropad bonding layer between a pair of dies under consideration. At each node (j), Q_j and T_j represent respectively heat generation and temperature. The heat that transfers from one node to the following is represented by q. This network is significant as it allows to model how the temperature rises of each layer is caused not only by the heat generated locally but also by the heat generated by the other layers as well. The analytical model and corresponding equations extracted from this network could be used as a guideline to optimize the thermal design of a system exploiting 3D integration. This model considers the impact of internal thermal resistances on the maximum temperature, the best arrangement of multiple layers, the thermal physical related limits of 3D packaging and the package and heat sink thermal characteristics for 3D ICs.

FEM simulations have also been conducted in [84], showing that down scaling of die footprint in 3D integration produces an increase in the maximum temperature. In addition, the numerical modeling was used to show that the overall power dissipation induced by wiring parasitics could be reduced by 30% when converting a system from traditional 2D packaging into 3D integration technology. Furthermore,

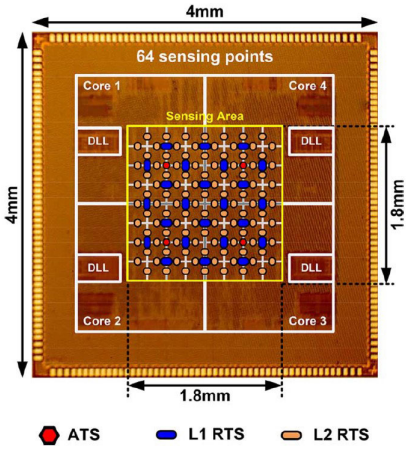


FIGURE 16. Chip photo of the hybrid temperature sensor network reported in [87].

TABLE 5. Performance comparison of some on-chip thermal sensors.

Reference	[87]	[88]	[89]	[90]
Process (CMOS)	130 nm	160 nm	22 nm	65 nm
Power supply (V)	1.2	1.5 to 2	1.5	0.6 to 1
Area per sensing point (μm^2)	2,624	80,000	6,100	115
Frequency (MHz)	400	NA	10	NA
Temperature range (°C)	28 to 33 and 43 to 45	-55 to 125	-10 to 110	0 to 100
Accuracy	NA	±0.15°C	±0.19°C	8.8 °C

a trade-off between thermal and electrical considerations was noted in the design of 3D integration [84]. For instance, stacking dies vertically offers shorter wires. However, this technique produces considerable thermal challenges due to an increase of local power density. Similarly, while it is beneficial to attach high-power dies close to the heat sink, this procedure results in more integration challenges with 3D technology due to the large number of connections required between the high-power die and the package. Consequently, more TSVs must be routed through the remaining stacked dies to connect high-power dies to the package.

Another possible configuration to perform 3D SiP is studied in [85]. The main SiP, including passive components, is packaged on the substrate with the ball grid array (BGA) approach after molding the SiP with epoxy molding compounds (EMC). In the substrate layers, embedded dies benefit from shorter interconnections and better electrical performance. Fig. 15 describes the packaging process of the studied 3D SiP, where the substrate is employed to package passive elements and flip-chip (FC) dies, and interlayers are used to embed dies. Then, the substrate is assembled on a testing printed circuit board (PCB) using BGA solder

balls. Thermal cycling (T/C) reliability tests are performed along with FEM simulations. The study found that, because of the complexity of embedded dies SiP configuration, the position of failure-prone BGA connections changed between inner and corner BGA solder ball positions. In addition, it was noted that the inner positions of the BGA are more susceptible to failure than corner ones. To perform the transient thermal analysis of large and multiscale geometries of 3D SiP structures, a discontinuous Galerkin time-domain (DGTD) algorithm is proposed in [86]. The developed DGTD method solved the issues of multiscale meshes and factorization of massive matrix equations. The robustness and accuracy of the proposed algorithm was verified numerically and analytically.

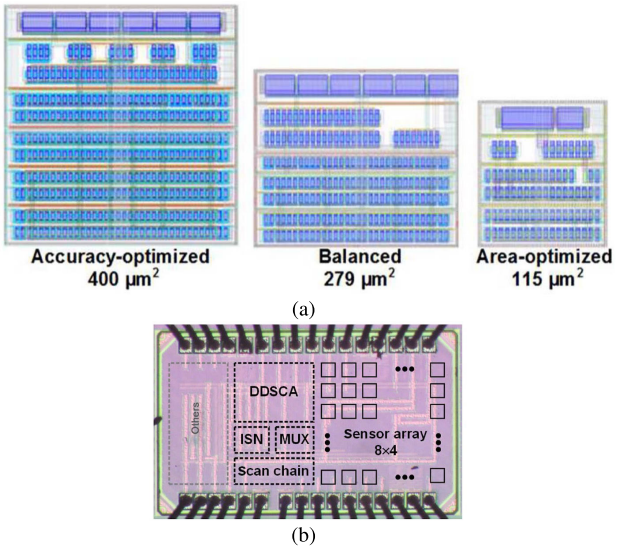


FIGURE 17. (a) Layouts of three sensor front ends, and (b) Die micrograph [90].

3) MODELING OF WAFER-LEVEL PACKAGING

To examine the thermal, mechanical and electrical response of the three Fan-out (FO) packaging technologies shown in Fig. 13, a 3D numerical model is proposed in [82]. The study confirmed that FOCLP has the highest warpage due to the CTE mismatch between the molding materials and the thin substrate. The CTE mismatch is better in FM technology, because of its backside laminate film that reduces warpage. In addition, the thermal cycling test showed that the creep strain energy density (CSED) is localized in the upper region of the outermost solder ball. The FOCLP technology has the lowest CSED value profiting from the low CTE mismatch between the package and the PCB. The heat dissipation capacity of the three packages was found to be better than that of the conventional WLCSP due to the wider package size and higher number of I/Os contacts. It is also found that by reducing the length of interconnects, FOCLP offers the lowest inductance variance and coupling. This study suggests means to optimize packaging to improve CSED in presence of thermal cycling to improve fatigue related lifetime.

A novel chip-first FOWLP is demonstrated in [81] to implement a thin heterogeneous integration (SiP) including 4 chips and 4 capacitors. The investigated FOWLP method is based on a new assembly process to implement the RDLs. Consequently, a 300 μm package thickness is reported. This reduces the amount of needed epoxy molding compound (EMC).

B. ON-CHIP THERMAL MONITORING

Dynamic thermal management (DTM) is an essential requirement in SoC and SiP approaches. Its primary role is to maximize the system performance by cooling down the hotspots by dissipating the heat out over the whole integrated system. Monitoring thermal distribution over chip area provides significant information for DTM. Such thermal map is usually provided by implementing an on-chip sensing network. To reduce overhead, the area of each embedded temperature sensor should be reduced.

A real-time thermal monitoring algorithm of industrial integrated systems was presented in [91]. This approach was validated using the MCUXpresso tool applied to a Freescale embedded sensor board to monitor and predict its temperature profile in real time by programming the embedded sensor into the FRDM-KL26Z board.

Fig. 16(a) shows the die micrograph of a hybrid thermal sensor architecture applied to a quad-core processor [87]. This solution combines a small number of precise thermal sensors along with a large number of less precise thermal sensors. A high spatial resolution thermal map is obtained by combining the collected data. The sensors are carefully positioned to facilitate modeling. An upsampling algorithm was applied to obtain a high-resolution thermal map from readouts of both accurate absolute temperature sensors (ATS) and less precise relative temperature sensors (RTS). This system has only 4 ATSs (one per core) surrounded by a network of RTSs. Thus, it is an area efficient approach.

To meet low supply voltage (VDD) and area efficiency requirements, an ultra-compact and scalable supply voltage temperature sensor was implemented in [90]. Three configurations of sensor front ends, implemented in 65 nm CMOS process, were demonstrated, as shown in Fig. 17, with respective silicon area of 115, 279 and 400 μm^2. The VDD of this sensor can be scaled down from 1 V to 0.6 V without degradation in its performance. This easily enables its integration with digital circuits without additional power regulations. Consequently, dense thermal monitoring can be integrated to digital-based SoC. When used to predict temperatures in the 0°C to 100°C range, a balanced front-end sensor was reported to have a worst case error of 7°C. The die photo of a test chip is reproduced in Fig. 17. This die includes prototypes of three types of sensor front ends organized as an 8 × 4 array along with the back-end read-out circuits. It occupies

an area of 0.9 × 0.72 mm^2. The performance of the hybrid thermal sensor reported in [87] and the one presented in [90] are compared to other sensor's solutions presented in [88], [89] (see Table 5).

VII. CONCLUSION

In this paper, we presented a high-level study of a promising solution for industrial sensor interfaces. With the proposed versatile SoC/SiP interface, cost, size, weight and power could be reduced. Also, it allows versatility, flexibility, and reconfigurability to support different loads and sensors with different specifications. At this stage, we identified numerous design considerations and key challenges associated with each building block. Also, possible solutions to all identified challenges have been discussed. In addition, we introduced the various available processes for high-voltage circuits integration. Also, various packaging technologies that could be used for the projected SiP integration have been presented. Furthermore, thermal management issues and mitigation methods in SoC and SiP implementations, including thermal modeling of SiP and on-chip thermal monitoring approaches have been reviewed.

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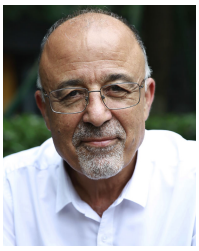

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