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Novel Variable Switching Frequency PWM Strategy for a SiC-MOSFET-Based Electric Vehicle Inverter to Increase Battery Usage Time

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ABSTRACT In this study, a novel variable switching frequency pulse width modulation (VSFPWM) strategy is proposed to achieve improved electric vehicle inverter efficiency. The silicon carbide (SiC) MOSFET inverter has excellent switching characteristics, thus enabling pulse width modulation control with a high switching frequency. The high switching frequency can reduce the voltage ripples in DC-link capacitors, which enables their use at a reduced capacitance. The switching frequency is typically set to a level that is within the limits of the voltage ripple in the maximum output region. Given that the same switching frequency is applied to the entire operating region, there is a sufficient margin with respect to the limits of the voltage ripple in the low-to-medium output range. The proposed method is designed to consider the real-time minimum switching frequency by considering the voltage ripple of the capacitor during operation under loaded conditions, thereby minimizing the switching loss. In addition, the method is suitable for high-switching frequency control because the calculation time is short. Because it does not require additional hardware, it is easy to apply to the existing inverter. The validity of the proposed method was verified based on simulations and experiments.

INDEX TERMS Electric vehicle, SiC-MOSFET, switching losses, variable switching frequency, voltage ripple.

I. INTRODUCTION

Because of the problems associated with air pollution from the emissions of internal combustion engine vehicles, electric vehicles (EVs), which are eco-friendly alternative means of transportation, have drawn attention as a solution to environmental problems [1]–[3].

The representative electric components of EVs include motors, inverters, converters, and battery systems [4]–[6]. All these EV parts must be equipped with high efficiency for improved mileage and high-power density solutions to overcome spatial constraints. To achieve improved mileage, increasing the battery capacity may be the easiest approach; however, given the increase in the volume and cost involved, it is not a practical solution. In this study, we aim to address this problem by implementing high-efficiency and high-power-density solutions for the inverter, a motor driving system in EVs.

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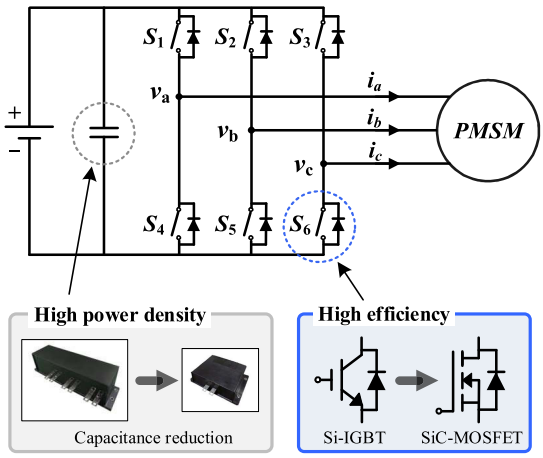

FIGURE 1. Inverter equivalent circuit for vehicles with SiC-MOSFET.

The configuration of the inverter that controls the driving motor of the vehicle is shown in Figure 1, where the power semiconductors are the key components. To date,

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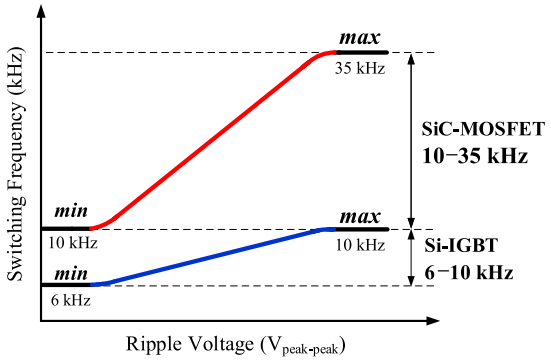

FIGURE 2. Comparison of ranges of variable switching frequency between Si-IGBT and SiC-MOSFET inverters.

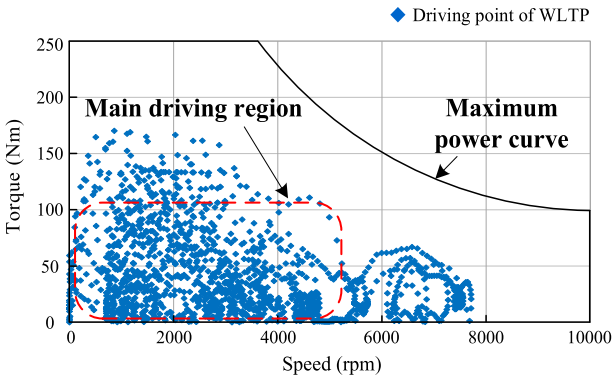

FIGURE 3. Worldwide harmonized light-vehicle test procedure (WLTP) driving cycle speed–torque curve.

research has been conducted to achieve the implementation of a high-efficiency and high-power-density inverter, primarily employing silicon (Si)-based power semiconductor devices. However, there are physical limitations to the properties of the devices to meet the recent requirements of the EVs market for an efficiency greater than 98% and power density greater than 50 kW/L [4]–[6]. Silicon carbide (SiC) MOSFETs, which are wide-band-gap devices, offer solutions with excellent electrical properties [7]–[9].

The SiC-MOSFET has excellent switching performance and low on-resistance, enabling the efficiency of inverters to be improved. In terms of the volume composition of an inverter for EVs, DC-link capacitors, power semiconductors, cooling systems, connectors, and control units account for 23%, 17%, 20%, 15%, and 25%, respectively [4]. The excellent switching performance of the SiC-MOSFET allows a reduction in the size of the cooling system as well as the size of the DC-link capacitor. Because of these advantages, a significant improvement in the inverter power density can be achieved.

The design of a DC-link capacitor should consider its lifetime and capacitance. The lifetime is determined by the root-mean-square (RMS) value of the current ripple of the capacitor, and the variation in the RMS current ripple with respect to the switching frequency is insignificant [10], [11]. This variation does not affect the lifespan of the designed capacitor, including the margin. Conversely, the capacity of the DC-link capacitor is determined by the voltage ripple. Given that the voltage ripple exhibits a large variation with respect to the switching frequency and has an inverse relationship with it, it is possible to reduce the capacitor's capacity by increasing the switching frequency. Herein, the switching frequency is selected as a value that satisfies the voltage ripple condition of the capacitor in the maximum output range of the load. Therefore, when the inverter is driven based on the constant switching frequency pulse width modulation (CSF-PWM) strategy, the voltage ripple has a sufficient margin compared with the limit value in the operating range lower than the maximum output.

In the Si-IGBT inverter, even if a separate switching frequency is selected in real-time considering the capacitor voltage ripple margin, the typical range of the variable switching frequency (VSF) is limited to the range of 6–10 kHz, as shown in Figure 2 [12]. Conversely, in the case of the SiC-MOSFET inverter operating at a high switching frequency, the VSF has a wider range (10–35 kHz) compared with the Si-IGBT inverter. Therefore, if the optimal switching frequency is selected for each operation range, a significant improvement can be achieved in terms of the switching loss. Furthermore, according to the driving cycles of the worldwide harmonized light vehicle test procedure (WLTP), EVs are mostly driven in the low- to mid-power range, as shown in Figure 3; thus, reducing the switching loss in this range will greatly improve the efficiency in terms of battery usage time and mileage.

Meanwhile, there has been recent active research on the VSF pulse width modulation (VSFPWM) strategy to improve the inverter's efficiency, based on various theoretical backgrounds. Examples of published studies include a VSF control method that ensures only minimum control precision based on the real-time rotational speed (revolutions per minute) of the motor [13], a VSF control method for reducing the phase current ripple applied to the load and minimizing the switching frequency [14]–[20], and a control method with random variation of the switching frequency to reduce the peak magnitude of the load phase current [21], [22]. The various methods employed in previously published studies have been effective at reducing switching loss and improving the total harmonic distortion (THD) of the phase current. However, given that these existing methods do not consider the effect of voltage ripples, which is a key design factor of the capacitor, some limitations remain, including reduced control stability of the inverter and the voltage utilization ratio. In addition, the problem of voltage ripples also affects the battery state of health (SOH). To address these limitations, a previous study [12] proposed a PWM technique at a varying switching frequency to the minimum value that satisfies the voltage ripple condition of DC-link capacitors. However, with this approach, a separate current sensor needs to be added

to the input side of the inverter, and the voltage ripple is observed through the integration of the sensed current. This involves an increase in the inverter cost. Additionally, it is not easy to apply this method to SiC-MOSFET-based high-switching frequency PWM inverters because of the increase in the calculation time required for analog-to-digital (AD) conversion of the sensed current and the related signal processing.

To address the limitations associated with previously published studies, a novel VSFPWM strategy to improve the efficiency of the SiC-MOSFET-based inverter for EVs is proposed in this paper. The proposed method is based on a mathematical model of voltage ripple and does not require additional hardware, such as sensors or circuits. In addition, in the offline state, the voltage ripple factor is extracted in advance and incorporated into the algorithm. In the online state, the switching frequency is determined through the minimum calculation between the pre-calculated ripple factor and the load phase current. Because the real-time calculation is thus minimized, the calculation time is short, which makes it suitable for application to the SiC-MOSFET-based PWM inverter, which operates at a high switching frequency. To examine and verify the validity of the proposed method, the performance of the proposed technique was verified through simulations and experiments.

The remainder of this paper is organized as follows: Section II describes the effects of DC-link voltage ripples on inverter control performance and the correlation between the voltage ripple and inverter switching frequency. Section III presents the theoretical background for voltage ripple estimation, which is the basis for selecting the optimal switching frequency. Section IV describes the principle of the proposed VSFPWM strategy. In Sections V and VI, the simulation and experimental results are presented, and the validity and performance of the proposed method are verified based on the simulation results and experiments. Finally, Section VII presents a summary and conclusions.

II. EFFECTS OF DC-LINK VOLTAGE RIPPLE AND RELATIONSHIP WITH SWITCHING FREQUENCY

A. EFFECT ON INVERTER

To achieve stability with respect to the inverter control and secure voltage utilization ratio, it is important to maintain the DC-link voltage stability [23].

Figure 4 shows the range of voltage vectors that can be synthesized using the space vector pulse width modulation (SVPWM) scheme. In the figure, the maximum possible range for synthesizing the voltage vectors is the inner region of the hexagon, and the region where all the phases can be synthesized with the same magnitude is the inner region of a circle inscribed in the hexagon. In the case of the SVPWM method, inverter control is performed based on the area of the inscribed circle, and the maximum magnitude of the voltage is $V_{dc}/\sqrt{3}$ (maximum phase voltage).

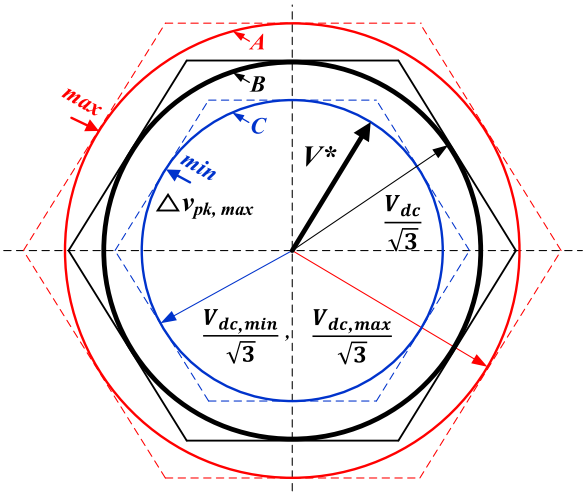

FIGURE 4. Range of output voltage by DC-link voltage ripple of the inverter with space vector pulse width modulation applied.

In Figure 4, $\Delta v_{pk,max}$ denotes the magnitude of the maximum voltage ripple of the DC-link capacitor. This causes instantaneous fluctuation in the range of the hexagon and inscribed circle regions in the figure, which causes the inverter control to be unstable. For example, if the range of the output voltage vector is reduced to the C-inscribed circle by $\Delta v_{pk,max}$, and the reference voltage vector V^* exceeds the range of the C-inscribed circle, the desired voltage magnitude cannot be generated. This causes a problem regarding control stability. To prevent this problem, the range of V^* is usually limited to the C-inscribed circle. As shown in (1), this limitation reduces the maximum value of the phase voltage that can be output from the inverter by $V_{phase,decrease}$ thereby reducing the maximum speed of the loaded motor drive.

$$V_{phase,decrease} = \frac{1}{\sqrt{3}}(V_{dc} - V_{dc,min}) \tag{1}$$

Therefore, it is important to limit the value of $\Delta v_{pk,max}$ of the DC-link capacitor to within the allowable magnitude and maintain a constant value when considering the inverter control stability and voltage utilization ratio.

B. RELATION BETWEEN VOLTAGE RIPPLE AND SWITCHING FREQUENCY

To limit the magnitude of $\Delta v_{pk,max}$ of the DC-link capacitor to within the allowable range and to maintain a stable voltage control, selecting a capacitor with an appropriate capacity is important [24]–[26]. The DC-link capacitance C can be designed based on (2), and the derivation process and details of this equation can be found in (16) in Section 3.

$$C = \frac{1}{4f_{sw}} \frac{I_o}{\Delta v_{pk,allowed}} \tag{2}$$

where f_{sw} $(=1/T_s)$ is the switching frequency, I_o is the maximum value of the output phase current, $\Delta v_{pk,allowed}$ is the allowable voltage ripple magnitude, and the constant 1/4 is

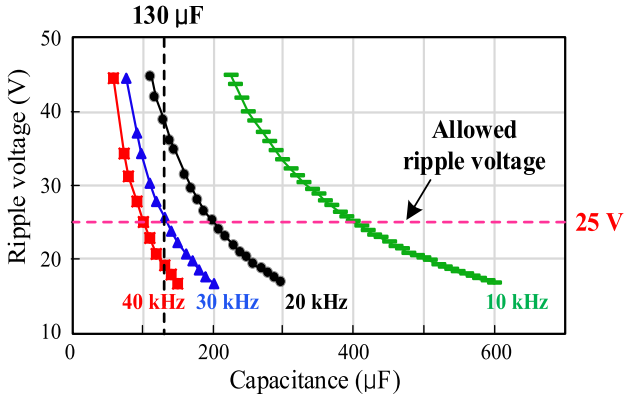

FIGURE 5. Relation between DC-link voltage ripple and switching frequency.

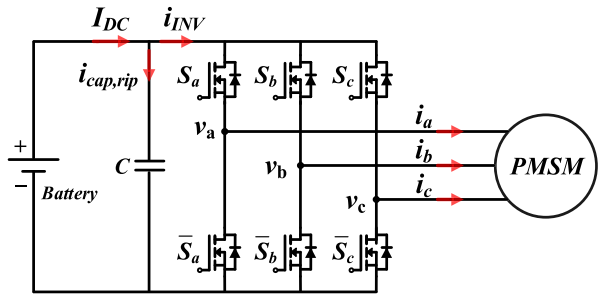

FIGURE 6. Configuration and main current of the three-phase voltage source inverter.

the voltage ripple factor $K_{v,rip}$. That is, if I_o is determined by the load condition, C can be designed considering the $\Delta v_{pk,allowed}$ and f_{sw} conditions. Therefore, if f_{sw} is increased, a capacitor with a smaller capacity can be used.

Figure 5 shows the relationship between $\Delta v_{pk,max}$, and C according to f_{sw}. For example, at a point at which C is 130 μF, when f_{sw} increases, $\Delta v_{pk,max}$ decreases, and when f_{sw} decreases, $\Delta v_{pk,max}$ increases. That is, if the magnitude of $\Delta v_{pk,max}$ and the margin compared to the allowable limit of the magnitude can be accurately known in real-time in an inverter system with a constant C, the inverter efficiency can be improved by optimizing f_{sw}.

III. ESTIMATION OF DC-LINK VOLTAGE RIPPLE

A. MAIN CURRENTS OF THREE-PHASE VOLTAGE SPOURCE INVERTER (VSI)

Figure 6 shows the basic equivalent circuit of the three-phase VSI applied to the SiC-MOSFET.

In the figure, I_{DC} denotes the output current of the battery, i_{INV} is the input current of the inverter, and $i_{cap,rip}$ is the capacitor current ripple. I_{DC} can be defined as in (3) [24], where $cos\theta$ is the power factor (pf) and m_a is the voltage modulation index, which can be expressed by (4) and (5). In (4), i_{ds}, i_{qs}, v^*_{ds}, and v^*_{qs} indicate the feedback current and reference voltage in the rotating coordinate system, respectively.

$$I_{DC} = \frac{3}{2} m_a I_o \, cos\theta \tag{3}$$

$$cos\theta = \frac{(i_{ds}v^*_{ds} + i_{qs}v^*_{qs})}{\left[\left(\sqrt{i^2_{ds} + i^2_q}\right)\left(\sqrt{v^{*2}_{ds} + i^{*2}_q}\right)\right]} \tag{4}$$

$$m_a = \frac{V^*}{\left(\frac{1}{\sqrt{3}} V_{dc}\right)} \tag{5}$$

i_{INV} can be expressed as a switching function, as shown in (6). In the equation, the switching functions of phases a, b, and c are denoted as S_a, S_b, and S_c, respectively. When the switch is on, these values are equal to one; when it is off, the values are zero. i_a, i_b, and i_c indicate the currents in each phase.

$$i_{INV} = S_a i_a + S_b i_b + S_c i_c \tag{6}$$

After applying Kirchhoff's current law to Figure 6, $i_{cap,rip}$ can be expressed as (7) by substituting (3) and (6).

$$\begin{aligned} i_{cap,rip} &= i_{INV} - I_{DC} \\ &= (S_a i_a + S_b i_b + S_c i_c) - \frac{3}{2} m_a I_o \, cos\theta \end{aligned} \tag{7}$$

In the three-phase inverter, if the output current is three-phase symmetrical, i_{INV} has a ripple component with a periodicity of every 60°. Therefore, assuming that I_{DC} is constant in (7), $i_{cap,rip}$ shows symmetry every 60°, and this pattern is repeated. In conclusion, it is possible to derive a generalized formula for $\Delta v_{pk,max}$ by analyzing only the operating characteristics of *Sector 1* (0° to 60°) in the space vector diagram (d-q axis stationary coordinate system) of Figure 7(a).

B. TIME OF VOLTAGE VECTOR APPLICATION

Figure 7 is a space vector diagram of the three-phase inverter, showing the output voltage vectors V_0–V_7 and the reference voltage vector V^*. In the space vector diagram, V^* is synthesized using the adjacent output voltage vectors. For example, to generate V^* located in *Sector 1*, as shown in Figure 7(a), the nearest active voltage vectors V_1 and V_2 and the reactive voltage vectors V_0 and V_7 are synthesized. Figure 7(b) shows the switching pattern used to minimize the current ripple when V^* is located in *Sector 1*. As shown in the figure, the reactive voltage vectors V_0 and V_7 are located at both ends of the rising and falling carrier sectors. Here, T_s represents the switching period. The active voltage vector application times T_1 and T_2, and the reactive voltage vector application time T_0 are represented in (8), (9), and (10), respectively.

$$T_1 = m_a \frac{T_s}{2} \, sin(60 - \theta) \tag{8}$$

$$T_2 = m_a \frac{T_s}{2} \, sin\theta \tag{9}$$

$$T_0 = \frac{T_s}{2} - (T_1 + T_2) = \frac{T_s}{2} \left[1 - m_a \, sin(60 - \theta)\right] \tag{10}$$

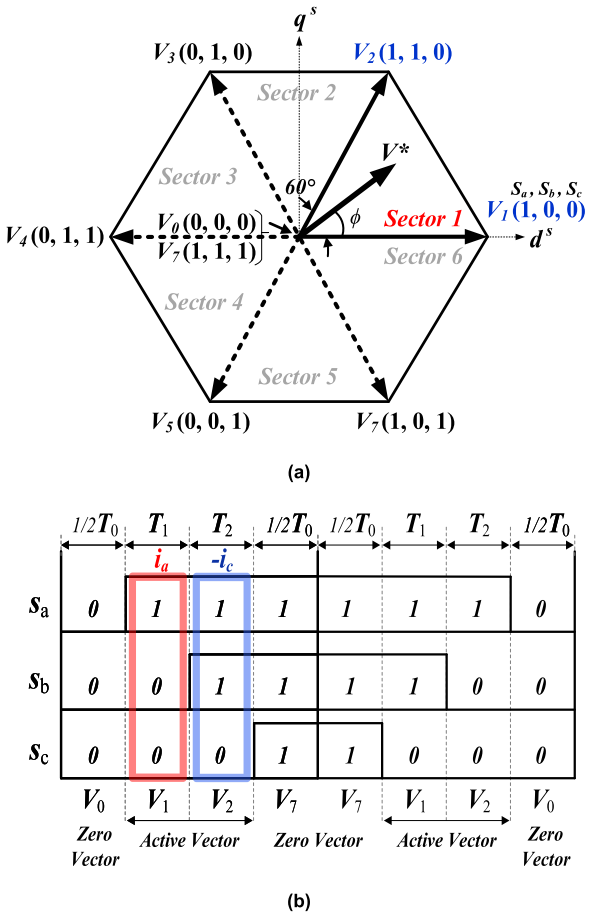

FIGURE 7. Voltage modulation in the three-phase inverter. (a) Space vector diagram and (b) switching operation to generate the reference voltage vector.

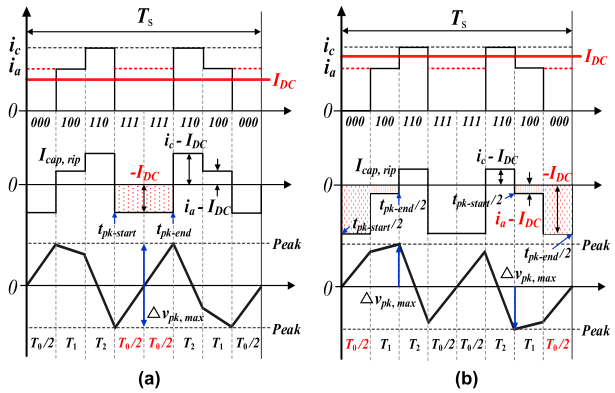

FIGURE 8. DC-Link voltage ripple analysis in T_s. (a) $i_a > I_{DC}$(b) $i_a < I_{DC}$.

C. VOLTAGE RIPPLE ESTIMATION

Figure 8 shows $i_{cap,rip}$ and the maximum voltage ripple $\Delta v_{pk,max}$ according to the conditions of i_a and I_{DC} when the switching pattern is as shown in Figure 7(b) [24]–[26]. In Figure 8(a), i_a is greater than I_{DC}($i_a > I_{DC}$), and in Figure 8(b), i_a is smaller than I_{DC} ($i_a < I_{DC}$).

In general, the voltage ripple $\Delta v_{pk,max}$ of the capacitor during the time from $t_{pk,start}$ to $t_{pk,end}$ can be expressed by (11) below.

$$\Delta v_{pk,max} = \left| \frac{1}{C} \int_{t_{pk,start}}^{t_{pk,end}} i_{cap,rip} dt \right| \tag{11}$$

In the case of Figure 8(a), the total time in the region where $\Delta v_{pk,max}$ occurs is T_0 (= $1/2T_o + 1/2T_o$), and the magnitude of $i_{cap,rip}$ is $-I_D$. Reorganizing this relationship using (11), $\Delta v_{pk,max}$ can be expressed by (12) below.

$$\Delta v_{pk,max} = \frac{1}{C} I_{DC} T_0 \tag{12}$$

Finally, if (3) and (10) are substituted into (12) and expanded, when $i_a > I_{DC}$, $\Delta v_{pk,max}$ can be expressed as (13). Here, θ indicates the phase difference between the inverter output voltage vector and the current vector.

$$\Delta v_{pk,max} = \frac{3}{4\sqrt{3}} \frac{I_o T_s}{C} m_a \cos\theta \left[1 - m_a \sin(60 + \phi)\right] \tag{13}$$

In the same manner as in Figure 8(a), the total time with the maximum magnitude $\Delta v_{pk,max}$ in Figure 8(b) is T_0 (= $1/2T_o$+$1/2T_o$)+$2T_1$ (= T_1+T_1), and the magnitude of $i_{cap,rip}$ is $-I_{DC}$ at T_0 and i_a–I_{DC} at T_1. By reorganizing using (11), $\Delta v_{pk,max}$ can be expressed as (14).

$$\Delta v_{pk,max} = \frac{2}{C} \left[I_{DC} \frac{T_0}{2} + (I_{DC} - i_a) T_1 \right] \tag{14}$$

Likewise, by substituting (3), (8), and (10), in (14), and expanding. Finally, when $i_a < I_{DC}$, $\Delta v_{pk,max}$ can be expressed according to (15).

$$\begin{aligned} &\Delta v_{pk,max} \\ &= \frac{3}{4\sqrt{3}} \frac{I_o T_s}{C} m_a \left| \cos\theta \left[1 - m_a \sin(60 + \phi)\right] \right. \\ &\quad \left. + \frac{4}{\sqrt{3}} \sin(60 - \phi) \left[\frac{3}{2\sqrt{3}} m_a \cos\theta - \cos(\phi - \theta) \right] \right| \end{aligned} \tag{15}$$

(13) and (15) can be generalized and expressed as (16). In the equation, In the equation, $K_{v,rip}$ is the voltage ripple factor and is determined by m_a, θ, and ϕ.

$$\Delta v_{pk,max} = \frac{I_o T_s}{C} K_{v,rip}(m_a, \theta, \phi) \tag{16}$$

Under conditions (13) and (15), it can be observed that $K_{v,rip}$ is expressed differently. At this time, given that $\Delta v_{pk,max}$ denotes the maximum voltage ripple, $K_{v,rip}$ in (16) is determined to be the larger value between (13) and (15). A detailed analysis indicates that $K_{v,rip}$ is 0.25 at the maximum, which corresponds to the constant 1/4 in (2) [23].

IV. PROPOSED VSFPWM STRATEGY

Figure 9 shows the maximum voltage ripple $\Delta v_{pk,max}$ in the inverter system, the allowable voltage ripple $\Delta v_{pk,allowed}$, and the ripple margin, which is the difference between the two values when the switching pattern is as shown in Figure 7(b).

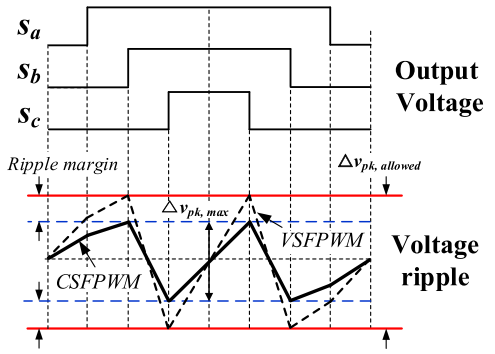

FIGURE 9. Operating principle of the proposed VSFPWM strategy.

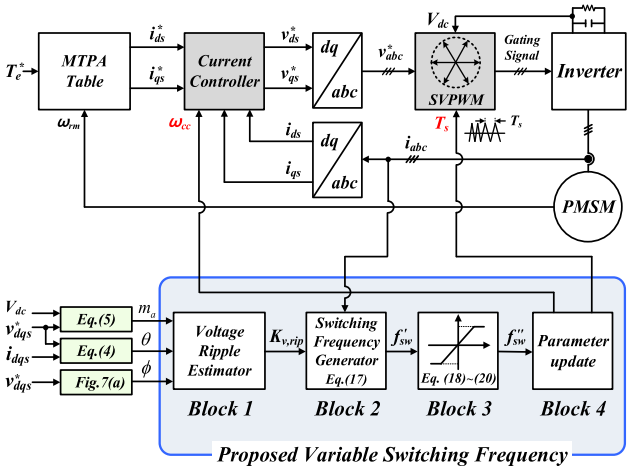

FIGURE 10. Entire control block diagram of the proposed VSFPWM strategy.

In general, when the CSFPWM is applied, C and f_{sw} are designed such that $\Delta v_{pk,max}$ is smaller than $\Delta v_{pk,allowed}$ in the maximum output region. At this time, if the output is decreased at the same f_{sw}, the ripple margin increases. Therefore, the inverter efficiency can be improved by reducing f_{sw}. In this study, we propose a VSFPWM that sets $\Delta v_{pk,allowed}$ as the target value and determines the optimal f_{sw} by real-time consideration of the ripple margin values.

Figure 10 shows the motor control algorithm that applies the proposed VSFPWM. As shown in the figure, the proposed VSFPWM is composed of four blocks.

In *Block 1*, $K_{v,rip}$ from (16) is generated based on the states of m_a and θ, as well as the voltage angle ϕ. To implement the high-switching frequency PWM control by reducing the calculation load, $K_{v,rip}$ is determined by alternately substituting the values of m_a, θ, and ϕ (the parameters of $K_{v,rip}$) in advance to generate a lookup table (LUT), and $K_{v,rip}$ is determined based on the generated LUT, instead of applying complicated real-time calculations using (13) and (15). Herein, the LUT consists of the input values of m_a, θ, and ϕ, and the output values of $K_{v,rip}$, as shown in Figure 11.

In *Block 2*, the minimum switching frequency f'_{sw} that satisfies $\Delta v_{pk,allowed}$ is calculated based on the input $K_{v,rip}$.

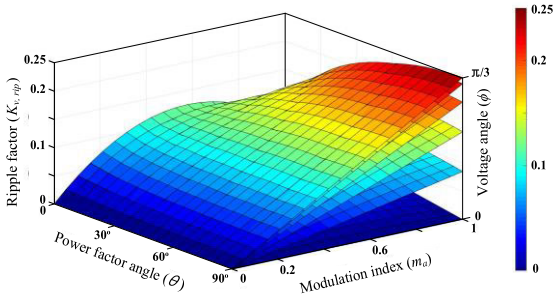

FIGURE 11. Construction of a Look-up-table of voltage ripple factors.

f'_{sw} can be calculated using (17), which can be derived through (16) for voltage ripple estimation. (17) shows that the f'_{sw} value required to meet the control target value $\Delta v_{pk,allowed}$ can be determined by considering $K_{v,rip}$, and I_o, which reflects the real-time operating status of the inverter, without having to add separate sensors or circuits and at low calculated loads.

$$f'_{sw} = K_{v,rip}(m_a, \theta, \phi)\frac{I_o}{\Delta v_{pk,allowed} C} \tag{17}$$

In *Block 3*, the optimal switching frequency f''_{sw} is determined by comparing the input f'_{sw} with the condition of the VSF limiter. In this case, the VSF limiter is determined using (18), (19), and (20). (18) serves as the minimum value limiter of the input f'_{sw}, and the limit value is $f_{sw,min}$. This value is related to the total harmonic distortion (THD) of the output current of the inverter. If it is lowered without limit, it may cause noise problems in the motor. Therefore, the $f_{sw,min}$ value should be selected in consideration of the audible noise and output current precision allowed by the system. (19) serves as the maximum value limiter of f'_{sw}, and the limit value is $f_{sw,max}$.

This value is selected based on the upper limit of the temperature of the device junction, considering the loss of the power semiconductor. (20) shows that the value of f''_{sw} does not exceed the range between $f_{sw,min}$ and $f_{sw,max}$, and the input value f'_{sw} is output without any limits.

$$if\ (f'_{sw} \le f_{sw,min}) \quad f''_{sw} = f_{sw,min} \tag{18}$$

$$if\ (f'_{sw} \ge f_{sw,max}) \quad f''_{sw} = f_{sw,max} \tag{19}$$

$$Otherwise \quad f''_{sw} = f_{sw,min} \tag{20}$$

Finally, *Block 4* is responsible for updating the related parameters and changing the switching frequency at the same time based on the selected f''_{sw}. The main parameters updated include the control and switching period T_s and the current controller bandwidth ω_{cc}. In the motor control block in Figure 10, T_e^* is the torque reference, v_{abc}^* are the phase voltage references, and i_{ds}^*, i_{qs}^* and v_{ds}^*, v_{qs}^* represent the current and voltage references, respectively, based on the rotating coordinate system. To apply the proposed VSFPWM, the transient response characteristic of the inverter switching device was determined through the gate resistance considering the case

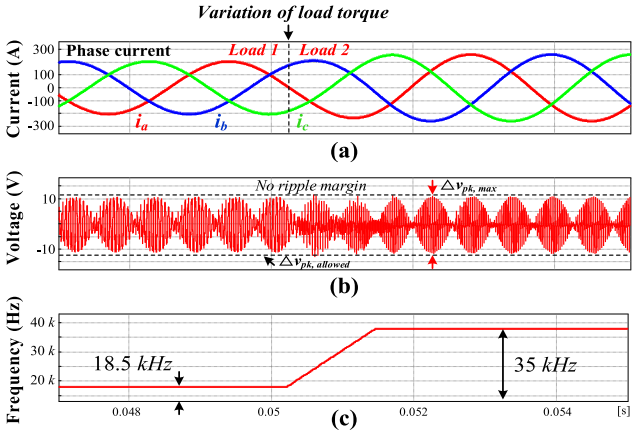

FIGURE 12. Load variation simulation results with proposed VSFPWM. (a) Phase current, (b) DC-link voltage ripple, and (c) switching frequency.

of operating at $f_{sw,max}$ under the maximum load condition. After that, the same was applied to all variable switching frequency sections.

V. SIMULATION

To validate the VSFPWM proposed in this study, a simulation was performed using PSIM (Version 11.1.5, POWERSIM). Tables 1 and 2 present the specifications of the system used for the simulation.

The purpose of the simulation was to verify that inverter control can be performed by changing the optimal switching frequency f''_{sw} in real-time by reflecting the real-time operating status of the inverter under two conditions, i.e., Load 1 and Load 2, when the proposed VSFPWM is applied. At this time, $\Delta v_{pk,max}$ should be stably controlled at values lower than the target value $\Delta v_{pk,allowed}$. The evaluation conditions were as follows: V_{DC} of 850 V, $\Delta v_{pk,allowed}$ of ±25 V, Load 1: output phase current equal to 140 A rms, and Load 2: 180 A rms. Load 2 corresponds to the maximum output region of the inverter.

Figure 12 shows the waveforms of the simulation performed to evaluate the operation of the proposed VSFPWM. Figure 12(a) shows the phase current waveform applied to the load motor. According to the waveforms, the statuses of Loads 1 and 2 can be observed. Figure 12(b) shows $\Delta v_{pk,max}$ for Loads 1 and 2. In general, when the CSFPWM is applied, f_{sw} is designed to have no ripple margin in the maximum output region. Therefore, there is no ripple margin in the case of Load 2, but the margin can be observed in the case of Load 1, which has a smaller output than is the case for Load 2. However, in the case of Load 1 in Figure 12(b) with the application of the proposed VSFPWM, because of the real-time variation of the optimal switching frequency f''_{sw}, $\Delta v_{pk,max}$ is controlled within the target value $\Delta v_{pk,allowed}$ without errors.

In the simulation, f''_{sw}, in which $\Delta v_{pk,max}$ is controlled within the target value $\Delta v_{pk,allowed}$, is calculated in real-time by reflecting the inverter operation status according to the load conditions. Thus, the inverter control with optimum variation of the switching frequency to f''_{sw} was confirmed without any problems regarding the control stability.

TABLE 1. System parameters of inverter.

Symbol	Quantity	Value	Unit
P_i	max. power	120	kW
V_{dc}	DC-Link voltage	850	V
I_o	phase current	260	A
C	capacitance	110	μF
$\Delta v_{pk,allowed}$	allowed ripple voltage	±25	V

TABLE 2. System parameters of test motor.

Symbol	Quantity	Value	Unit
P_m	max. power	100	kW
n	max. speed	8000	rpm
T	max. torque	250	Nm
-	rotor type	IPM	-
p	number of pole pairs	4	-

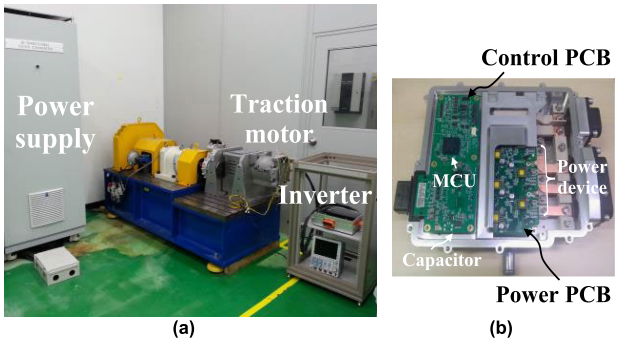

FIGURE 13. Experimental setup. (a) Dynamometer system and (b) inverter with SiC-MOSFET.

VI. EXPERIMENTAL RESULTS

The experimental validation of the effects of the proposed VSFPWM strategy was performed regarding three aspects.

First, the operating performance of the proposed VSFPWM was evaluated. Second, the effect of the inverter efficiency improvement was verified based on the use of a dynamometer system when the proposed VSFPWM method was applied to the SiC-MOSFET inverter. Finally, by applying the efficiency evaluation data to the international standard, the WLTP driving cycles, battery usage time, and mileage per charge were analyzed to confirm the improvement in terms of battery usage. The results of these experiments are presented as follows.

Figure 13 shows the experimental setup used for the performance validation of the proposed method. Figure 13(a) shows the dynamometer system used for the evaluation of the operation performance and efficiency of the inverter, and Figure 13(b) shows the inverter equipped with the SiC-MOSFET

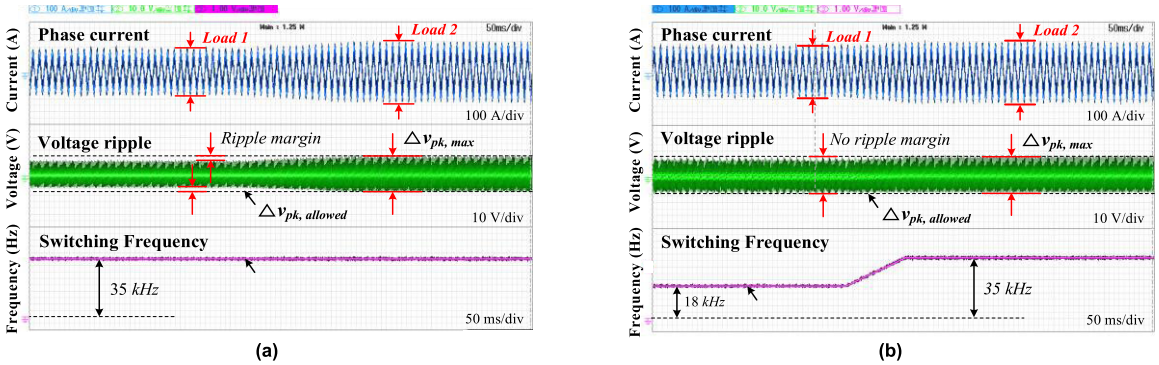

FIGURE 14. Evaluation of inverter operation under various load conditions, (a) with CSFPWM and (b) with the proposed VSFPWM.

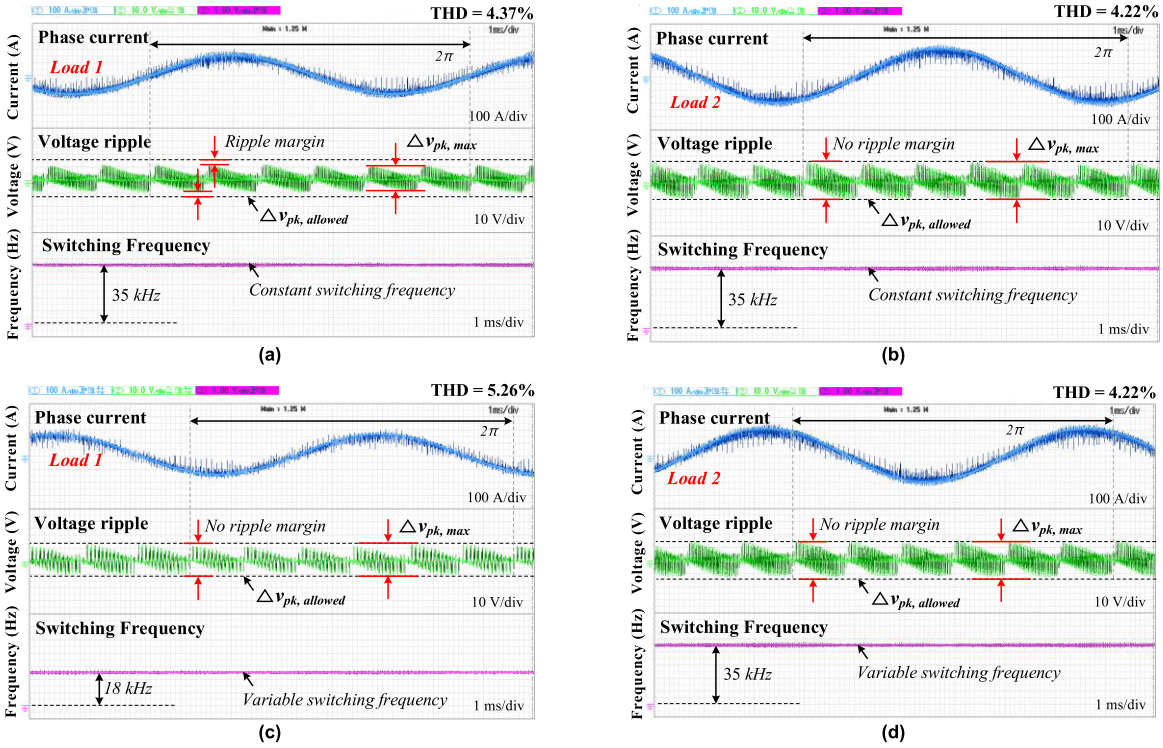

FIGURE 15. Enlarged waveforms (a) with CSFPWM under load 1, (b) with CSFPWM under Load 2, (c) with the proposed VSFPWM under Load 1, and (d) with the proposed VSFPWM under load 2.

used to drive the motor. The inverter in Figure 13(b) consists of two parts: a power unit and control unit. The power unit is designed to operate at 120 kW and consists of a SiC-MOSFET module (FS03MR12A6, Infineon) and a gate drive (ACPL-344JT, Avago). The control unit consists of a 32-bit digital signal processing module (MPC5676R, NXP), current sensors (HC5FW500, LEM), and a motor position signal processing unit. The detailed conditions of the inverter and motor system used in the experiment are listed in Tables 1 and 2, respectively.

A. OPERATING PERFORMANCE EVALUATION

Figure 14 shows the experimental results following the evaluation of the operating performance when the CSFPWM and the proposed VSFPWM were applied.

The purpose of the experiment is to verify that inverter control can be achieved by changing the optimal switching frequency f''_{sw} in real-time by reflecting the real-time operating status of the inverter under two conditions, i.e., Load 1 and Load 2, when the proposed VSFPWM is applied. At this time, $\Delta v_{pk,max}$ should be controlled within the target value $\Delta v_{pk,allowed}$ without errors. The conditions of the experiments are as follows: $\Delta v_{pk,allowed}$ of ± 25 V, Load 1 condition with an output phase current at 140 A rms, and Load 2 at 180 A rms. Load 2 corresponds to the maximum output region of the inverter.

Figure 14(a) shows the waveforms of the inverter operation when CSFPWM was applied. As described above, in the case of the CSFPWM, f_{sw} was generally designed such that $\Delta v_{pk,max}$ satisfies the target value $\Delta v_{pk,allowed}$ in the

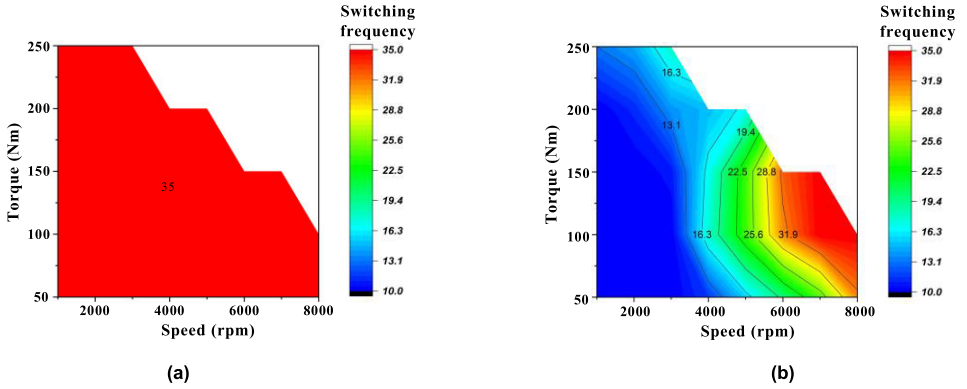

FIGURE 16. Switching frequency map. (a) CSFPWM and (b) VSFPWM.

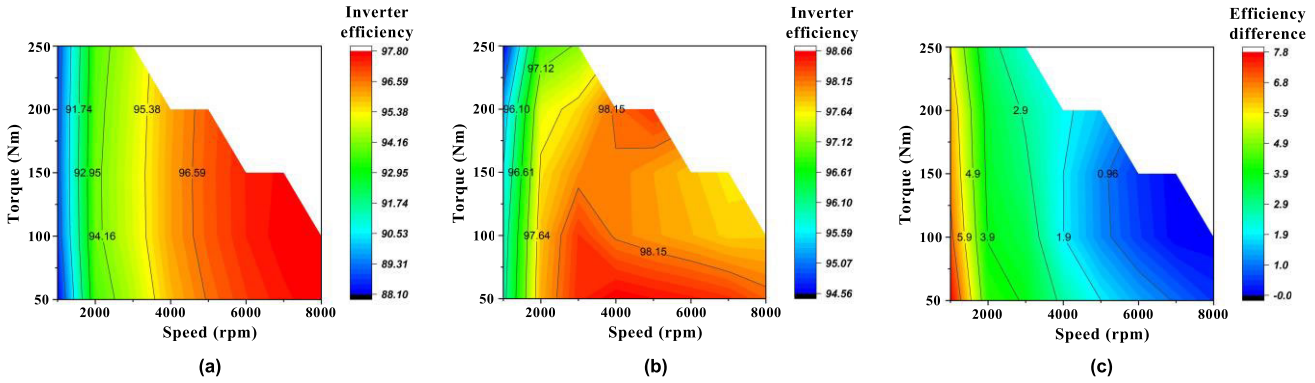

FIGURE 17. Inverter efficiency map in the speed–torque curve. (a) CSFPWM, (b) VSFPWM, and (c) efficiency difference map.

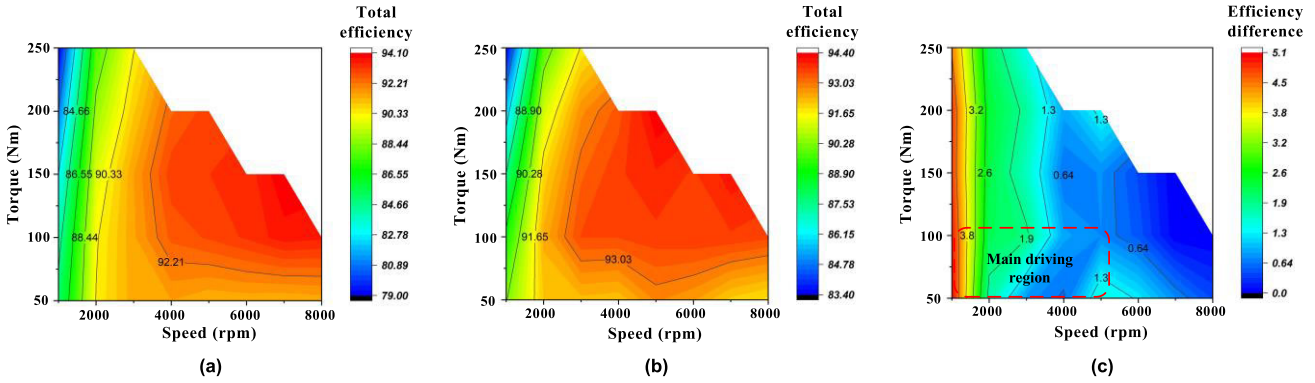

FIGURE 18. Total (motor and inverter) efficiency map in the speed-torque curve. (a) CSFPWM, (b) VSFPWM, and (c) efficiency difference map.

maximum output region. In the experiment, the inverter operated at 35 kHz, which is the f_{sw} determined in this manner. It can be observed that in the case of Load 2, the maximum output region, there was no ripple margin. However, when operated under Load 1, where the output was smaller than that of Load 2, the inverter operated at the same f_{sw} of 35 kHz, and $\Delta v_{pk,max}$ had a sufficient ripple margin of ± 7 V with respect to the value of $\Delta v_{pk,allowed}$.

Figure 14(b) shows the waveforms of the inverter operation when the proposed VSFPWM was applied. It was confirmed that in the case of Load 2, the inverter operated at 35 kHz, which is the optimum f_{sw} calculated by reflecting the real-time inverter operation status, and there was no ripple margin. In addition, when operated under Load 1 conditions, wherein the output was smaller than that of Load 2, the inverter operated at a f''_{sw} of 18 kHz, which is the optimum value calculated by reflecting the current real-time inverter operation status, and it was also confirmed that $\Delta v_{pk,max}$ was controlled within the target value $\Delta v_{pk,allowed}$ without errors.

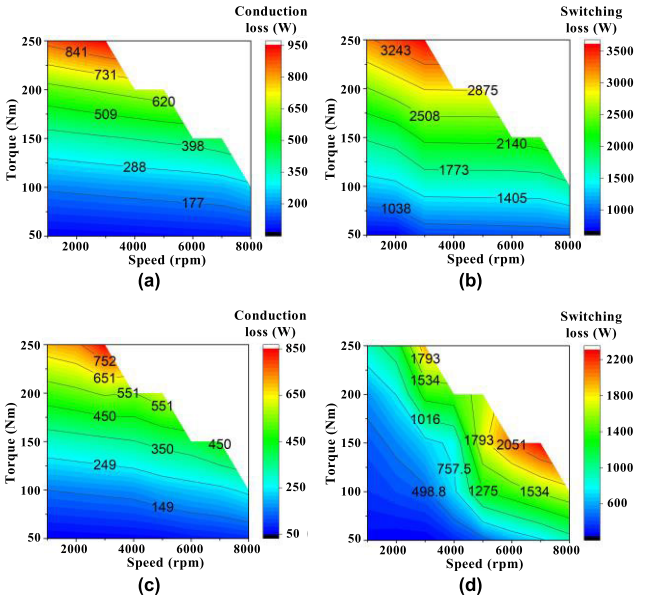

FIGURE 19. Loss map in the speed-torque curve. (a) Conduction loss with CSFPWM, (b) switching loss with CSFPWM, (c) conduction loss with VSFPWM, and (d) switching loss with VSFPWM.

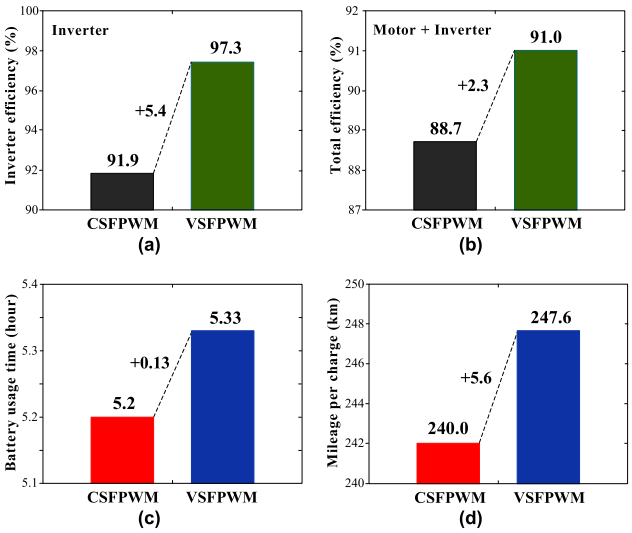

FIGURE 20. Comparative evaluation of performance based on WLTP driving cycles. (a) Inverter average efficiency, (b) total average efficiency, (c) battery usage time, and (d) mileage per charge.

Figure 15 shows the waveforms of the inverter operation with the enlargement of Loads 1 and 2 in Figure 14.

B. COMPARATIVE EVALUATION OF EFFICIENCY

To verify the effects of the application of the proposed control method to the SiC-MOSFET inverter, an efficiency evaluation was performed using the dynamometer system.

Figure 16 shows the f_{sw} of the inverter on the speed–torque curve of the motor. Figure 16(a) shows a constant f_{sw} with the application of CSFPWM, and Figure 16(b) shows f''_{sw}, which is the f_{sw} calculated by the algorithm when the proposed VSFPWM was applied.

Figure 17 shows the inverter efficiency map for each operating point in the speed–torque curve of the motor. Figure 17(a) shows the inverter efficiency with the CSFPWM, and Figure 17(b) shows the efficiency of the proposed VSFPWM.

Additionally, Figure 17(c) shows the difference in efficiency between Figure 17(a) and 17(b), and when the proposed technique was applied, the efficiency improved by 5.0% or more in the operation region where the improvement effect is significant. Figure 19 shows the results of loss analysis for inverter efficiency in the speed-torque curve of the motor. Figure 19(a) and 19(b) show the conduction loss and switching loss of the inverter when CSFPWM is applied. Figure 19(c) and 19(d) show the conduction loss and switching loss of the inverter when the proposed VSFPWM is applied. As can be seen from the analysis results, the improvement in inverter efficiency by the application of the proposed method is mostly due to the reduction of the switching loss.

Variations in the switching frequency for the purpose of improving the efficiency of the inverter may affect the efficiency of the load motor due to THD changes of the inverter output current. Therefore, both the efficiency of the inverter and the efficiency of the motor were analyzed. Figure 18 shows the total efficiency maps based on the considerations of both the inverter and motor efficiency. Figure 18(a) shows the total efficiency with CSFPWM, and Figure 18(b) shows the total efficiency with the proposed VSFPWM. Figure 18(c) shows the difference in efficiency between Figure 18(a) and 18(b). The efficiency was improved by up to 3.8% when the proposed VSFPWM was applied compared with the CSFPWM. Furthermore, as shown in Figure 2, the dotted line area in the lower left of Figure 18(c) is the region frequently used in the WLTP driving cycle, and the generated results in this region demonstrated improvements with respect to the total efficiency.

C. ANALYSIS OF EFFECTS ON BATTERY USAGE TIME AND MILEAG

To verify the effects of the algorithm in terms of the state of EVs, the efficiency evaluation results obtained from the dynamometer system experiment were applied to the vehicle driving conditions to analyze the effects in terms of the average inverter efficiency, total average efficiency, battery usage time, and mileage per charge. For the analysis, WLTP driving cycles were applied to assume the conditions of a battery capacity of 66 kWh and a total vehicular weight of 2,180 kg, considering five passengers in the vehicle

Figure 20 shows a comparison of the average performance of the CSFPWM and the proposed VSFPWM. Figure 20(a) shows the average efficiency comparison of the inverter only, and Figure 20(b) shows the comparative analysis of the average efficiency considering both the inverter and motor efficiency. As can be seen from the figure, when the proposed method was applied, the average efficiency of the inverter was

improved by 5.4%, and the total average efficiency (including the motor) was improved by 2.3%. Additionally, Figure 20(c) shows the total battery usage time after full charging, and Figure 20(d) shows the analyzed results for mileage per charge. When the proposed technique was applied, the battery usage time increased by 13 min, and the mileage per charge increased by 5.6 km.

These analyses confirm that the battery usage time and mileage per charge were improved, even when only the proposed VSFPWM was applied, without the use of additional devices.

VII. CONCLUSION

In this study, a novel VSFPWM strategy was proposed to improve the efficiency of the inverter used in EVs operated with SiC-MOSFETs and high-switching frequency PWM. The proposed method yielded the $\Delta v_{pk,max}$ of the DC-link capacitor in real-time and changed $f_{sw}^{''}$ to improve the inverter efficiency. Consequently, this led to an improvement in the battery usage time and mileage per charge in EVs. In addition, the proposed method is expected to improve the inverter's efficiency in applications such as permanent magnet synchronous generators (PMSG) using a three-phase inverter.

The main findings of this study are as follows.

1) A novel VSFPWM strategy with a shortened calculation time and simple implementation was proposed by minimizing the parts that required real-time calculations. Therefore, this method is advantageous for applications in inverters that perform SiC-MOSFET-based high-switching frequency PWM. Because the algorithm is simple, it is not difficult to apply to inverters using the conventional CSFPWM strategy.

2) Most of the existing VSFPWM methods were developed based on the Si-IGBT inverter. Although the SiC-MOSFET inverter has very good efficiency because of its excellent electrical properties, it is mostly used for high-switching frequency operation. Thus, if VSFPWM can be applied, a significant reduction in the switching loss can be expected. In this study, the effects of the proposed method were verified in terms of operating performance and efficiency improvement by applying the new VSFPWM strategy to the SiC-MOSFET inverter.

3) Battery usage time and mileage per charge have emerged as important indicators of subsidy support policies for EVs in many countries. In this study, the validity of the algorithm was confirmed by analyzing the main indicators in terms of battery usage and efficiency of the components of the inverter and motor.

In conclusion, the proposed VSFPWM strategy can be applied to an inverter without installing a separate additional device. The simple application of the algorithm led to improvements in the inverter efficiency and battery usage of EVs. The performance of the proposed method was verified through simulation and experiments.

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