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A Generalized High Gain Multilevel Inverter for Small Scale Solar Photovoltaic Applications

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ABSTRACT The contribution of renewable energy, especially small-scale solar photovoltaics (PV), is increasing exponentially in the energy sector. In general, high gain DC-DC converters are used as front-end converters to increase the low voltage of PV panels; further, the DC-AC converter (multilevel inverters) is used for standalone AC loads or grid integration. To avoid the front-end converter and achieve both objectives, this paper proposes a nine-level quadruple boost inverter topology for small-scale solar PV applications. The proposed topology operates on a switched capacitor technique to boost the voltage, and has self-voltage balancing of capacitors. This paper presents the detailed operation of the proposed nine-level inverter, voltage stress calculations, loss analysis, and designing of circuit parameters. In addition, a high-gain generalized multilevel inverter (MLI) topology is also reported. Furthermore, the proposed MLI is compared with competitive inverters available in the recent literature. The proposed MLI topology has advantages such as a minimum total standing voltage and a reduced component count; it can also produce bipolar voltage inherently. The performance of the proposed MLI topology is validated through the MATLAB-based simulations and an experimental prototype. Further, the experimental results are presented by considering load variations, modulation index variations, and output frequency variations. The experimental efficiency obtained is in the range of 96.2% to 92.8% for proposed 9-level inverter.

INDEX TERMS High-gain multilevel inverter, small-scale solar PV, switched capacitor, self-voltage balancing.

I. INTRODUCTION

The energy consumption of the world is continuously increasing day-to-day. To meet the increased load demand, large-scale renewable sources, especially solar photovoltaic, are integrated into conventional power generation. Generation of photovoltaic energy at a single location in large amounts and transmission of its power to long distances reduce the efficiency of the system. Recently, distributed generation has been introduced to overcome this problem and increase the efficiency of the system [1], and, the percentage of PV generation through solar rooftop has increased by a large quantity, approximately more than 20% of total PV generation capacity is through solar rooftop [2]. The small-scale solar PV system for rooftop applications is of 0.5kw to 2kw, and voltage ratings range are from 60 Volts to 100Volts [3].

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Generally, solar PV is preferred to operate in a grid-connected mode to avoid bulky and costly batteries. The solar rooftop is connected to a low voltage distribution network of 415V (3-Φ) and 230V (rms) for 1-Φ shown in Figure.1. To get compatibility between low DC voltage PV systems and AC grid voltage, the high gain DC-DC converters [4] are used at the front end for the DC-AC converters. For DC-AC conversion, an enormous number of MLI topologies are proposed in the literature. Among those, diode clamped [5], flying capacitor (FC), and cascaded H-bridge multilevel inverters are the popularly known topologies. Diode clamped MLI and FC MLI have the problem of unbalanced capacitor voltages, which requires an additional voltage balancing circuit [6]. Cascaded H-bridge MLI is modular in structure, requiring more isolated DC sources [7].

Recently, various reduced switch nine-level inverter topologies have been presented in [8]–[11]. These topologies use fewer switches and diodes to get the same number of

levels compared with the basic MLI topologies. In the topologies mentioned above, the gain of the topologies is limited, and they may not be suitable for applications that require boost in input voltage. In [10], [11], topologies require more isolated DC sources, and the number of sources increases with an increase in voltage levels. In [12]–[21] are some recently proposed topologies based on the switched-capacitor (SC) technique. In these topologies, each capacitor is connected alternatively in parallel and series with the DC source in each cycle of output voltage. They are charged in parallel and discharged to load in series. In [12]–[14], the topologies generate five-level output with a gain of two. In [15]–[17], topologies produce seven-level output voltage with a triple boost. In [19]–[21] topologies generate nine-level output voltage. Although these topologies generate a nine-level output voltage, they have a low voltage boosting ability (gain = 2). In [24], a generalized boost MLI is proposed based on the switched-capacitor technique; it consists of series-parallel connection of switches, diodes, capacitors for level generation, and H-bridge for polarity generation. Reference [25] Topology has a hexagonal switched cell and switches capacitor units with two isolated DC sources. The inverter in [26] has a quasi-resonant unit with switched capacitor technique for level generation. It uses one inductor in the resonance circuit, and H-bridge is used for polarity generation. In [27], a generalized step-up MLI has repeating switched capacitor units and one DC source. Each switched capacitor unit has five switches and one capacitor, and for an increase in two levels, it requires a switched capacitor unit. The inverter in [28] has two T-type modules connected both ends of repeating cross-connected SC units. Each cross-connected unit has six switches and two capacitors. The number of levels and the gain of the MLI increase with the number of SC units. In [29], a cascaded H-bridge is formed with capacitors in place of DC sources. The capacitors are charged using a switched capacitor technique with a single DC source and additional switches and diodes. Reference [30] Generalized MLI with ladder structure has a repeating unit of one isolated DC source and three switches. It has only one capacitor to get a gain of two by using the switched capacitor technique. In [31], a generalized switched capacitor MLI consists of a T-type module, a half-bridge, a repeating SC unit, and cross-connected switches. Each switched capacitor unit has one capacitor and three switches. In [32], a nine-level switched capacitor-based MLI with quadruple boost has been introduced for PV grid integration applications. It has been introduced for transformer-less grid integration. In [33], a hybrid T-type nine-level inverter with gain three is introduced for PV applications. It has four capacitors for voltage boosting, and a five-level T-type module is used at the output end. In [34], a reduced switch quadruple boost nine level inverter is introduced for electrical vehicle and industrial drive applications. In [36], a five-level switched capacitor-based inverter and is extended to generalized topology with high gain. The repeating unit consists of four switches and a capacitor. In [37], a generalized high gain inverter is formed by a repeating switched capacitor (SC) unit of two switches, one diode, a capacitor and a H-bridge is used for polarity generation. In [35], a seven-level switched capacitor topology is proposed. The gain of the topology is three and the total harmonic distortion (THD) ranges for seven-level is of 25%. In small scale PV grid integration applications, the input DC voltage is much less compared to the grid voltages. To get compatible grid voltages with the low voltage PV panels, it requires more gain and low THD limits. To meet these requirements in this paper the topology in [35] is improved to produce nine-level with gain of four and better THD which also reduces the size of filter requirement. Further, its high gain generalized structure has (2N+1) levels with a gain of N is proposed. It is based on the switched-capacitor technique, and each repeating SC unit has three switches and one capacitor. It has low voltage stress on the switches, leading to low TSV of the topology. The proposed topology has the following merits:

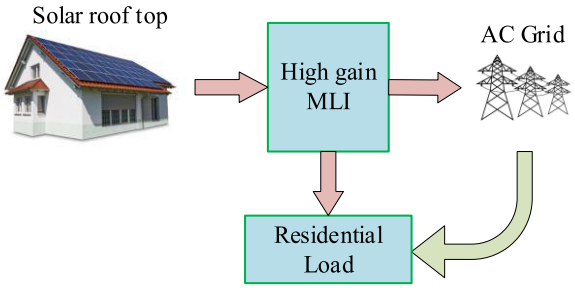

FIGURE 1. Solar rooftop PV application.

- Single DC source is used to get 9-level voltage and 2N+1 in generalized topology.
- Quadruple boost in voltage, voltage gain = 4(9 level) and for generalized gain = N(2N+1 level).
- The minimum voltage stress on switches.
- Self-voltage balancing of capacitors.
- Four out of 13 switches have only one transition in a cycle and are operated at a load frequency (50Hz).
- Inherent polarity generation without H-bridge.

The remainder of the paper is organized as follows. Section 2 explains the proposed nine-level topology, generalized topology, voltage stress on switches, self-voltage balancing of capacitors, modulation scheme, calculation of capacitance and efficiency. The comparative study is done with recently proposed nine-level and generalized topologies in Section 3. Section 4 contains a simulation results and analysis. Section 5 contains experimental analysis of the proposed topology. Finally, in Section 6, the complete work is concluded.

II. PROPOSED TOPOLOGY

The proposed quadruple boost nine-level topology shown in Figure.2. It is structured with 1 DC source, 3 capacitors (C_1, C_2 & C_3) and 13 switches in which 11 unidirectional switches (g_1-g_6& g_9-g_{13}) and 2 bidirectional switches (g_7& g_8). These switched capacitors are charged by using

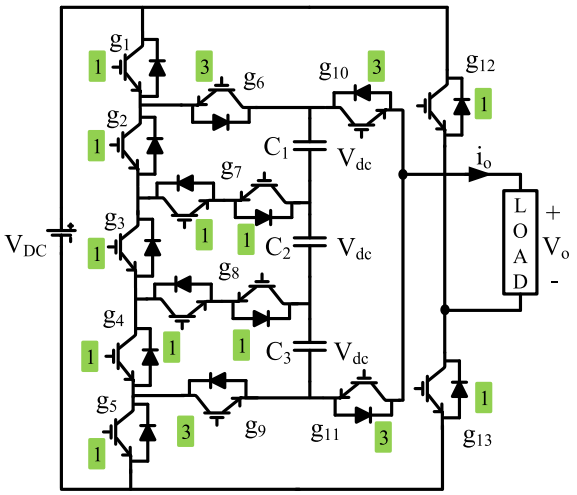

FIGURE 2. Proposed 9-level quadruple boost inverter (proposed 1).

a series-parallel technique. Each capacitor is individually charged to V_{dc} and discharged to load by connecting in series with the DC source to obtain a high voltage gain. The output voltage of nine levels has $\pm 4V_{dc}$, $\pm 3V_{dc}$, $\pm 2V_{dc}$, $\pm V_{dc}$, and zero levels. To avoid source and capacitor short circuit, switches pair (g_{12}, g_{13}) and (g_{10}, g_{11}), are operated complimentary. Switches g_{10}, g_{11}, g_{12}, and g_{13} have only transitions (on to off & off to on) for each load voltage cycle. Therefore, these switches operate at the load frequency (50Hz) and have low switching losses, which improve the overall efficiency of the topology. Switches (g_1-g_5) and (g_{12}-g_{13}) have a maximum blocking voltage (MBV) of V_{dc}, since most of the switches have low voltage stress, the total standing voltage (TSV) of the topology will be a low value. The voltage stress on each switch (g_{12}-g_{13}) are represented beside every switch in multiples of V_{dc} as shown in Figure.2. where '1' denotes V_{dc} and '3' denotes $3V_{dc}$. The proposed topology has 3 capacitors; each of them is charged to V_{dc}. The 3 capacitors are made to balance at V_{dc} by sequential charging and discharging in every cycle of load voltage. The gate signals for the switches of the proposed topology are given according to Table 1. In this table at each voltage level turn-on and turn-off states of the switches are shown as 1 & 0 respectively. The charging, discharging, and floating conditions (without charging or discharging) of the capacitors are represented as '↑', '↓' and '-' respectively.

A. OPERATING MODES OF PROPOSED TOPOLOGY

1) POSITIVE VOLTAGE LEVELS

It has two possibilities for zero voltage level; the switches g_1, g_6, g_{10}, and g_{12} are turned on to get zero voltage.

Simultaneously, C_1 is charged to V_{dc} by turn-on the switches g_3, g_4, g_5, and g_7 as shown in Figure.4(a). zero voltage level can also be obtained by turn-on the switches g_5, g_9, g_{11}, and g_{13} and simultaneously, switches g_1, g_2, g_3, and g_8 are turned on to charge C_3 to V_{dc}. In the $+V_{dc}$ state,

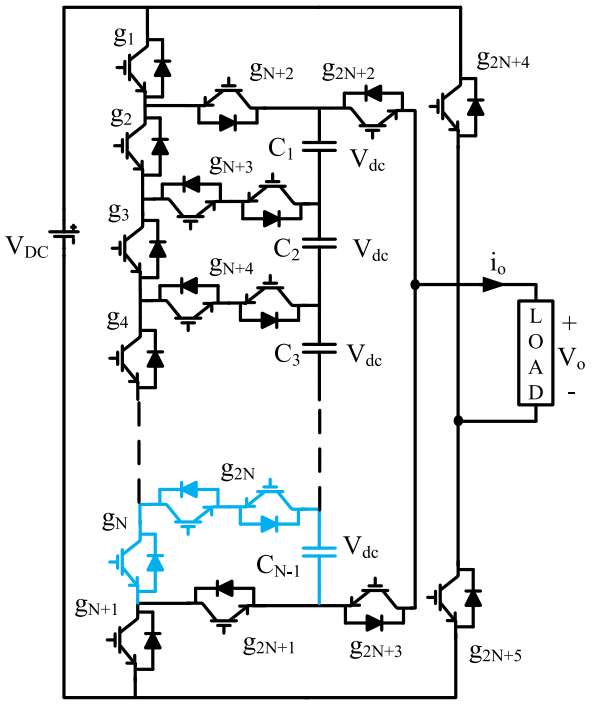

FIGURE 3. Proposed generalized MLI topology (proposed 2).

switches g_1, g_6, g_{10}, and g_{13} are turned on to obtain the $+V_{dc}$ voltage level. Simultaneously, switches g_3, g_4, g_5, and g_7 are turned on to charge C_1. During this time, C_2 and C_3 are in floating condition, as shown in Figure.4(b). In $+2V_{dc}$ state, charged C_1 is connected in series with the DC source to obtain $+2V_{dc}$ level by turning on the switches g_1, g_2, g_7, g_{10}, and g_{13}. Simultaneously, C_2 is charged by turning on the switches g_4, g_5, and g_8. During this voltage level, C_3 will be in floating condition as shown in Figure.4(c). To obtain the $+3V_{dc}$ voltage level, charged C_1 & C_2 are connected in series with the DC source by turning on the switches g_1, g_2, g_3, g_8, g_{10}, and g_{13}. Simultaneously, by turning on the switches g_5 and g_9; C_3 is charged to V_{dc} as shown in Figure.4(d). In $+4V_{dc}$ voltage level, charged C_1, C_2 and C_3 are connected in series with DC source by turn on switches g_1, g_2, g_3, g_4, g_9, g_{10}, and g_{13} as shown in Figure.4(e).

2) NEGATIVE VOLTAGE LEVELS

In $-V_{dc}$ state, the switches g_5, g_9, g_{11}, and g_{12} are turned on to get the $-V_{dc}$ level. Simultaneously, switches g_1, g_2, g_3, and g_8 are turned on to charge C_3. During this state, C_1 & C_2 are in floating condition as shown in Figure.4(f). In $-2V_{dc}$ state, the switches g_4, g_5, g_8, g_{11}, and g_{12} are turned on to connect the charged C_3 in series with the DC source. Simultaneously, switches g_1, g_2, and g_7 are turned on to charge C_2 to V_{dc}. At this level, C_1 is in floating condition as shown in Figure.4(g). In $-3V_{dc}$ state, the switches g_3, g_4, g_5, g_7, g_{11}, and g_{12} are turned on to connect charged C_2 and C_3 in series with the DC source. Simultaneously, by turning on switches g_1, g_6; C_1 is charged as shown in Figure.4(h).

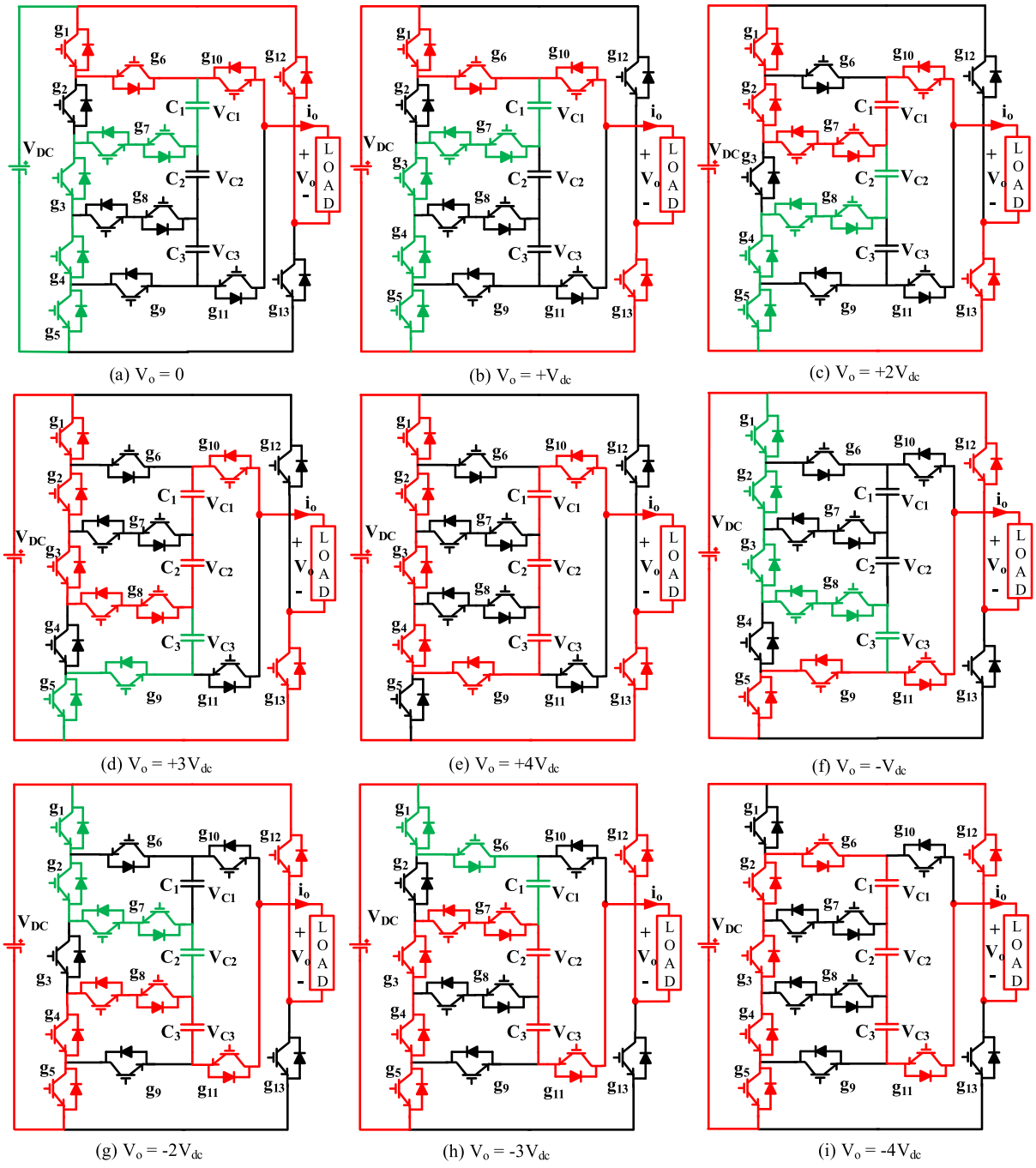

FIGURE 4. Operating modes of proposed topology (red indicates output voltage path and green indicates charging path).

In $-4V_{dc}$ state, the switches g_2, g_3, g_4, g_5, g_6, g_{11}, and g_{12} are turned on to connect C_1, C_2 and C_3 in series with the DC source as shown in Figure.4(i).

B. PROPOSED GENERALIZED 2N+1 LEVEL MLI

In grid integrated PV applications, due to the requirement of higher grid voltages, the gain of proposed quadruple boost 9-level inverter may not be compatible in some cases. To achieve high gain with better THD, a generalized topology is proposed with extension circuit consists of one unidirectional switch, one bidirectional switch, and a capacitor for PV grid integration applications. By adding 'x' extension circuits to the proposed topology, the output voltage with '2x+9' levels and 'x+4' gain can be obtained. A generalized 2N+1 level with gain = N is shown in Figure.3 by extending this repeating unit highlighted in blue. The generalized topology consists of N+7 unidirectional switches, N-2 bidirectional switches, N-1 capacitors and one DC source. The proposed

TABLE 1. Switching states and their effect in switched capacitors.

V_o	g_1	g_2	g_3	g_4	g_5	g_6	g_7	g_8	g_9	g_{10}	g_{11}	g_{12}	g_{13}	C_1	C_2	C_3
0	1	0	1	1	1	1	1	0	0	1	0	1	0	↑	-	-
V_{dc}	1	0	1	1	1	1	1	0	0	1	0	0	1	↑	-	-
$2V_{dc}$	1	1	0	1	1	0	1	1	0	1	0	0	1	↓	↑	-
$3V_{dc}$	1	1	1	0	1	0	0	1	1	1	0	0	1	↓	↓	↑
$4V_{dc}$	1	1	1	1	0	0	0	0	1	1	0	0	1	↓	↓	↓
0	1	1	1	0	1	0	0	1	1	0	1	0	1	-	-	↑
$-V_{dc}$	1	1	1	0	1	0	0	1	1	0	1	1	0	-	-	↑
$-2V_{dc}$	1	1	0	1	1	0	1	1	0	0	1	1	0	-	↑	↓
$-3V_{dc}$	1	0	1	1	1	1	1	0	0	0	1	1	0	↑	↓	↓
$-4V_{dc}$	0	1	1	1	1	1	0	0	0	0	1	1	0	↓	↓	↓

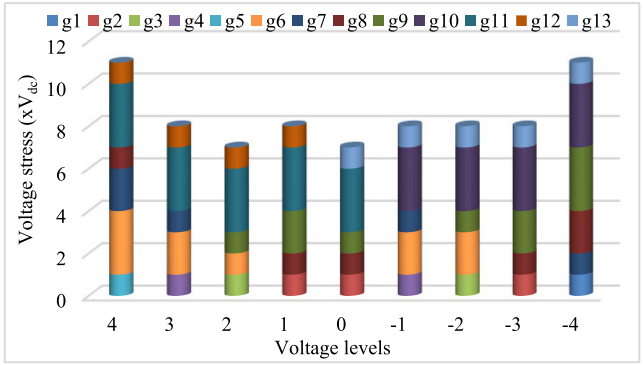

FIGURE 5. Voltage stresses on switches at different voltage levels.

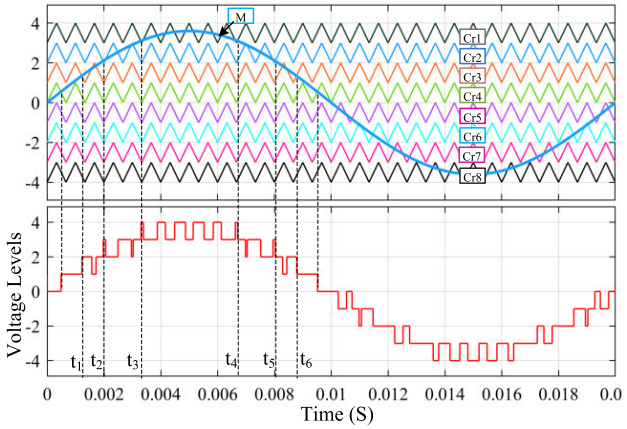

FIGURE 6. Level-shifted pulse width modulation scheme.

generalized topology has a MBV of (N-1) $*$ V_{dc} for only four switches and (N+3) switches are having a low blocking voltage of V_{dc}. This makes the TSV lower even with an increase in levels. The $TSV_{(p.u)}$ for the proposed generalized topology is (7N-5)/N.

C. VOLTAGE STRESS ON THE SWITCHES AND SELF-VOLTAGE BALANCING OF SWITCHED CAPACITORS

In the proposed topology, the maximum blocking voltage (MBV) of $3V_{dc}$ is for 4 switches (g_6, g_9, g_{10} & g_{11}). Bidirectional switches g_7 & g_8 block the voltage of is $2V_{dc}$ and 7 switches (g_1-g_5 & g_{12}-g_{13}) have low blocking voltage of V_{dc}. As the proposed topology is having low blocking voltages for more number of switches, it is having minimum total standing voltage (TSV).

The TSVp.u of the inverter is calculated using Equation (1).

$$TSV_{p.u} = \frac{\sum V_{sw\_off} + \sum V_{D\_off}}{V_{omax}} \quad (1)$$

Here, Vsw_off is the blocking voltage of each switch, VD_off is the diode reverse blocking voltage, and Vomax is the maximum output voltage.

TSVp.u. for the proposed quadruple boost nine-level inverter topology is 5.75. To represent the voltage stress on each of the switches at different voltage levels a bar chart is drawn in Figure.5. Where, the voltage stresses on switches are represented with different colours in multiples of Vdc over each level of output voltage.

Capacitors are balanced by continuously connecting in series, parallel with DC source which continuously discharge and charge respectively in each cycle of output. C_1 charges in $+V_{dc}$ and zero levels and discharges in $+4V_{dc}$, $+3V_{dc}$ and $+2V_{dc}$. C_2 charged at $+2V_{dc}$ and discharges at $+3V_{dc}$ & $+4V_{dc}$ levels. C_3 charged at $+3V_{dc}$ and discharges in $+4V_{dc}$ voltage level. Similarly, in the negative cycle by alternatively charging and discharging, the capacitor voltages are balanced.

D. MODULATION SCHEME

The level-shifted pulse width modulation (LSPWM) scheme is used to generate gate signals to the switches. To generate gate signals for a nine-level inverter LSPWM has 8 triangular carrier signals (Cr_1–Cr_8) and 1 sinusoidal modulating sinusoidal signal (M) as shown in Figure.6. By comparing this modulating signal with carrier signals, it generates 8 pluses (X_1-X_8) and these pulses are given to 13 switches through the logic gate pattern shown in Figure.7 according to Table 1. The logic pattern is obtained by adding these pulses. Here, X_1 represents comparison of (M, C_{r1}), X_2 represents (M, C_{r2}), and so on. Similarly for negative cycles X_8 represents comparison of (M, C_{r8}), X_7 represents comparison of (M, C_{r7}),

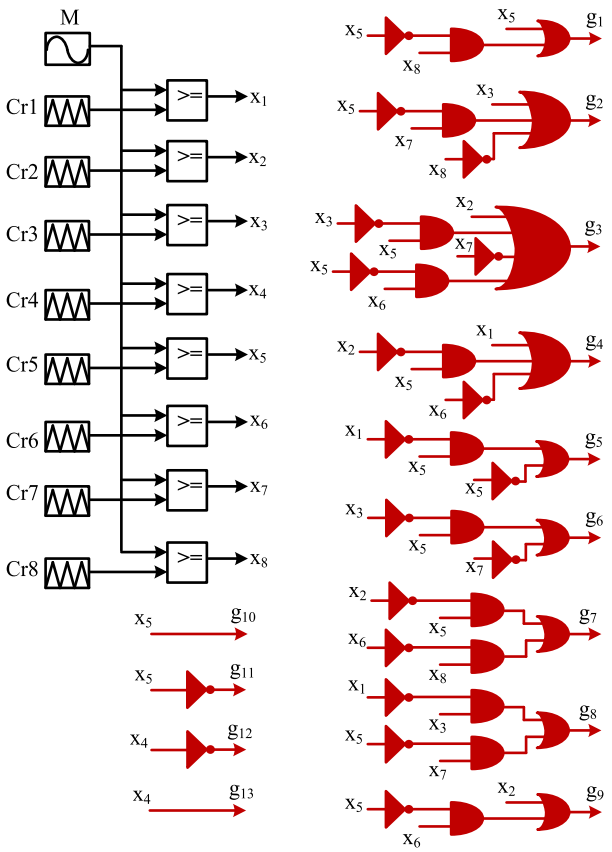

FIGURE 7. Logic pattern for gate signals.

and so on. The amplitude modulation index (Ma) is changed from 0 to 1 by varying the magnitude of the sinusoidal signal from 0 to 4 and the carrier amplitude is kept constant as 1. Frequency modulation is varied by changing the carrier signal frequency, and modulating signal frequency is kept constant at load frequency (50Hz). With the increase in carrier frequency the harmonics are shifted to higher order but with the increase in carrier frequency to large value the switching losses increases, as number of turn-on and turn-off transitions increases per cycle of output. Therefore, the carrier frequency here is limited to 5 kHz.

E. CALCULATION OF CAPACITANCE

The value of capacitors used in any circuit is defined by considering the longest discharge time of the capacitors. In the proposed nine-level topology the capacitor C_1 will discharge during $2V_{dc}$, $3V_{dc}$ and $4V_{dc}$ voltage levels. C_2 discharges during $3V_{dc}$ & $4V_{dc}$ voltage levels of $3V_{dc}$ and the C_3 discharges at $4V_{dc}$ voltage level. In Figure.6 the times of transitions of each voltage level are shown as $t_1, t_2, t_3 \ldots t_6$. These values are calculated as shown in equations (2)-(7):

$$t_1 = \frac{sin^{-1}\left(\frac{1}{4}\right)}{2\pi f_m} \tag{2}$$

$$t_2 = \frac{sin^{-1}\left(\frac{2}{4}\right)}{2\pi f_m} \tag{3}$$

$$t_3 = \frac{sin^{-1}\left(\frac{3}{4}\right)}{2\pi f_m} \tag{4}$$

$$t_4 = \frac{\pi - sin^{-1}\left(\frac{3}{4}\right)}{2\pi f_m} \tag{5}$$

$$t_5 = \frac{\pi - sin^{-1}\left(\frac{2}{4}\right)}{2\pi f_m} \tag{6}$$

$$t_6 = \frac{\pi - sin^{-1}\left(\frac{1}{4}\right)}{2\pi f_m} \tag{7}$$

The maximum amount of discharge in each cycle is obtained by integrating the current through the capacitors during the longest discharge time at maximum loading conditions (Equation (8)).

$$Q_{Ci} = \int_{t_a}^{t_b} I_{load} sin\,(2\pi f_m t)\,dt \tag{8}$$

where, Q_{Ci} is the maximum amount of discharge in i_{th} capacitor. t_a, t_b are start and end times of discharge period.

To design a capacitor with k (p.u) ripple, the amount of charge that a capacitor can store should be greater than Q/k.

The value of i_{th} capacitor is

$$C_i > \frac{Q_{Ci}}{k.V_{dc}} \tag{9}$$

Similarly, the values of capacitors C_1, C_2, and C_3 are calculated from equation (9) [22].

F. LOSS AND EFFICIENCY CALCULATIONS

There are two types of losses in semiconductor devices: switching losses and conduction losses. Switching losses occurred due to delay in turn-on and turn-off process. Conduction losses are due to on-state resistance of the semiconductors [23].

1) SWITCHING LOSSES

Switching losses occur due to non-instantaneous turn-on and turn-off processes. When the switch is turned on, the collector current (I_C) starts rising after the gate-emitter voltage (V_{GE}) becomes higher than threshold voltage (V_T). After the V_{GE} becomes greater than the V_T, the collector-emitter voltage (V_{CE}) starts to decrease. It takes a t_{on} of time for V_{CE} to reach V_{sw_on} and I_C to reach I_{sw_on}. During this t_{on}, both V_{CE} and I_C have finite nonzero values which lead to on-time switching losses, as shown in Equation (10). Similarly, during the turn-off process, both I_C and V_{CE} are finite values for t_{off} time as shown in Figure.8, which leads to the turn-off switching losses as shown in Equation (11). where $P_{SL,i(ON)}$ is the turn-on switching loss of the i_{th} switch, and $P_{SL,i(OFF)}$

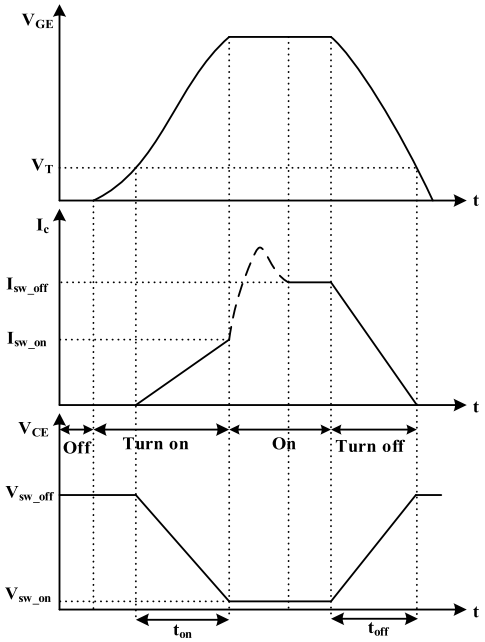

FIGURE 8. Turn-on and turn-off characteristics of the semiconductor switches.

is the turn-off switching loss of the i_{th} switch.

$$P_{SL,i(ON)} = f_{cr}\int_0^{t_{on}} V_{sw\_off,i}(t) * i(t)\,dt$$
$$= f_{cr}\int_0^{t_{on}} \left(-\frac{V_{sw\_off,i}}{t_{on}}(t - t_{on})\right)\left(\frac{I_{sw\_on1,i}}{t_{on}}t\right)dt$$
$$= \frac{1}{6}f_{cr} * V_{sw\_off,i} * I_{sw\_on,i} * t_{on} \quad (10)$$

$$P_{SL,i(OFF)} = f_{cr}\int_0^{t_{off}} V_{sw\_off,i}(t) * i(t)\,dt$$
$$= f_{cr}\int_0^{t_{off}} \left(\frac{V_{sw\_off,i}}{t_{off}}t\right)\left(-\frac{I_{sw\_off2,i}}{t_{off}}(t - t_{off})\right)dt$$
$$= \frac{1}{6}f_{cr} * V_{sw\_off,i} * I_{sw\_on2,i} * t_{off} \quad (11)$$

The number of turn-on and turn-off of each switch and diode are calculated from the equation (12). Where, N_{s_on} & N_{s_off} are the number of turn-on and turn-off in one cycle respectively. f_m is modulating frequency and f_{cr} is carrier frequency.

$$N_{S\_on} = N_{S\_off} = \frac{f_{cr}}{f_m} \quad (12)$$

The total switching losses of all switches are calculated by adding the total turn-on and turn-off losses of all switches from Equation (13).

$$P_{SL(Total)} = \sum_{i=1}^{N_{sw}}\left(\sum_{j=1}^{N_{on(i)}} P_{SL\_on(ij)} + \sum_{j=1}^{N_{off(i)}} P_{SL\_off(ij)}\right) \quad (13)$$

where $P_{SL(Total)}$ is the total switching losses and N_{sw} is the total number of switches in the MLI topology.

2) CONDUCTION LOSSES

Conduction losses in the semiconductor switches occur during the on-state of the switches. During the on-state, losses occur due to on-state resistance of the switch and voltage drop across the switch. The conduction losses of the switches and diodes can be calculated by Equation (14) and Equation (15), respectively:

$$P_{con\_sw} = V_{sw\_on} * i_{sw\_avg} + R_{sw\_on} * i^2_{sw\_rms} \quad (14)$$
$$P_{con\_D} = V_{D\_on} * i_{D\_avg} + R_{D\_on} * i^2_{D\_rms} \quad (15)$$

where, P_{con_sw} is conduction loss of semiconductor switch, P_{con_D} is conduction loss of diode, V_{sw_on} is on-state voltage across switch (V_{DS}), V_{D_on} is on-state voltage across diode, R_{sw_on} and R_{D_on} are on state resistance of switch and diode respectively. i_{sw_avg}, i_{sw_rms}, I_{D_avg}, i_{D_rms} are average & RMS currents of switch and diode respectively.

$$P_{con(V_o=+1V_{dc})} = 7\left(V_{sw\_on} * i_{sw\_avg} + R_{sw\_on} * i^2_{sw\_rms}\right) + 2\left(V_{D\_on} * i_{D\_avg} + R_{D\_on} * i^2_{D\_rms}\right)$$
$$P_{con(V_o=+2V_{dc})} = 8\left(V_{sw\_on} * i_{sw\_avg} + R_{sw\_on} * i^2_{sw\_rms}\right) + 2\left(V_{D\_on} * i_{D\_avg} + R_{D\_on} * i^2_{D\_rms}\right)$$
$$P_{con(V_o=+3V_{dc})} = 7\left(V_{sw\_on} * i_{sw\_avg} + R_{sw\_on} * i^2_{sw\_rms}\right) + 2\left(V_{D\_on} * i_{D\_avg} + R_{D\_on} * i^2_{D\_rms}\right)$$
$$P_{con(V_o=+4V_{dc})} = 7\left(V_{sw\_on} * i_{sw\_avg} + R_{sw\_on} * i^2_{sw\_rms}\right)$$
$$P_{con(V_o=-1V_{dc})} = 7\left(V_{sw\_on} * i_{sw\_avg} + R_{sw\_on} * i^2_{sw\_rms}\right) + 2\left(V_{D\_on} * i_{D\_avg} + R_{D\_on} * i^2_{D\_rms}\right)$$
$$P_{con(V_o=-2V_{dc})} = 8\left(V_{sw\_on} * i_{sw\_avg} + R_{sw\_on} * i^2_{sw\_rms}\right) + 2\left(V_{D\_on} * i_{D\_avg} + R_{D\_on} * i^2_{D\_rms}\right)$$
$$P_{con(V_o=-3V_{dc})} = 7\left(V_{sw\_on} * i_{sw\_avg} + R_{sw\_on} * i^2_{sw\_rms}\right) + 2\left(V_{D\_on} * i_{D\_avg} + R_{D\_on} * i^2_{D\_rms}\right)$$
$$P_{con(V_o=-4V_{dc})} = 7\left(V_{sw\_on} * i_{sw\_avg} + R_{sw\_on} * i^2_{sw\_rms}\right) \quad (16)$$

In each level of output voltage, the number of switches and diodes are in conduction changes, therefore the conduction losses are separately calculated in each voltage level. In $+V_{dc}$, $+3V_{dc}$ levels seven switches and two diodes are in conduction. During the $+2V_{dc}$ level eight switches and two diodes are in the conduction, and in $+4V_{dc}$ voltage level

TABLE 2. Comparison of the proposed topology with other 9-level topologies.

Topology	N_{sw}	N_d	N_c		N_s	$N_{Drivers}$	Gain	$TSV_{(p.u)}$	MBV ($*V_{dc}$)	H-bridge	N_{Total}
			V_{dc}	$2V_{dc}$							
2014[24]	8	6	3	0	1	8	4	8	4	Yes	17
2017[26]	10	4	4	0	1	10	4	8.5	4	Yes	18
2018[27]	19	0	3	0	1	19	4	4.75	1	No	22
2018[28]	17	0	4	0	1	13	4	6.5	4	No	21
2019[29]	18	5	4	0	1	18	4	7	4	Yes	27
2020[36]	16	0	3	0	1	16	4	7	4	No	19
2021[34]	10	1	1	1	1	10	4	5.75	4	No	13
2021[37]	10	3	3	0	1	10	4	6	4	Yes	16
2021[32]	14	0	4	0	1	14	4	6	4	No	18
2021[33]	12	2	4	0	1	11	3	7.5	3	Yes	18
Proposed 1	15	0	3	0	1	13	4	5.75	3	No	18

TABLE 3. Comparison of proposed generalized MLI topologies with other 2N+1 level topologies.

Topology	N_{sw}	N_d	N_c	N_s	$N_{Drivers}$	Gain	$TSV_{(p.u)}$	MBV ($*V_{dc}$)	H-bridge	N_{Total}
2017[25]	4N+6	2N	2N	2	4N+6	N/2	(6N+8)/(N+2)	N	Yes	8N+6
2017[26]	2N+2	N	N	1	2N+2	N	$(N^2+9N+16)/(2N)$	N	Yes	4N+2
2018[27]	5N-1	0	N-1	1	5N-1	N	(5N-1)/N	1	No	6N-2
2018[28]	3N+5	0	N	1	2.5N+4	N	(7N-2)/N	4	No	4N+5
2019[29]	4N+2	N+1	N	1	4N+2	N	7N/N	N/2	Yes	6N+3
2019[30]	N+8	0	1	N/2	N+6	2	$(24N-8)/N^2$	1	No	N+9
2020[31]	3N+9	(N-6)/2	(N+2)/2	1	3N+8	N/2	(6N-5)/N	2	No	4N+7
2020[36]	4N	0	N-1	1	4N	N	$(N^2+3N)/N$	N	No	5N-1
2021[37]	2N+2	N-1	N-1	1	2N+2	N	(7N-4)/N	N	Yes	4N
Proposed2	3N+3	0	N-1	1	2N+5	N	(7N-5)/N	N-1	No	4N+2

N_{sw}= number of switches, N_d = number of series diodes, N_c = number of capacitors, N_s = number of sources, $TSV_{(p.u)}$ = total standing voltage (per unit), MBV = maximum blocking voltage, $N_{Drivers}$ = number of gate driver circuits, $N_{Total} = N_{sw} + N_d + N_c$.

only seven switches are in conduction. The same repeats for the negative cycle of the output voltage as shown in Equation (16).

The total conduction losses are obtained by adding the conduction losses at each level as shown in Equation (17).

$$\begin{aligned} P_{con(Total)} = {} & P_{con(V_o=+1V_{dc})} + P_{con(V_o=+2V_{dc})} \\ & + P_{con(V_o=+3V_{dc})} + P_{con(V_o=+4V_{dc})} \\ & + P_{con(V_o=-1V_{dc})} + P_{con(V_o=-2V_{dc})} \\ & + P_{con(V_o=-3V_{dc})} + P_{con(V_o=-4V_{dc})} \end{aligned} \quad (17)$$

The overall efficiency of the multilevel inverter is given from Equations (18) and (19):

$$\text{Efficiency } \eta = \left(\frac{P_{input} - P_{losses}}{P_{input}}\right) * 100 \quad (18)$$

$$\eta = \left(\frac{V_{dc} * I_{dc} - P_{con(Total)} - P_{SL(Total)}}{V_{dc} * I_{dc}}\right) * 100 \quad (19)$$

where, η is MLI efficiency, V_{dc}& I_{dc} are input DC voltage and current respectively, $P_{con(total)}$ and $P_{SL(total)}$ are total conduction and switching losses respectively of all switches.

III. COMPARISON WITH OTHER RECENTLY PROPOSED TOPOLOGIES

The proposed 9-level quadruple boost inverter topology is compared with some of the recently proposed topologies shown in Table 2. The comparison is done based on the number of switches, number of series diodes, number of capacitors, number of DC sources, number of gate drivers, gain of the topology, TSV (p.u) of the topology, MBV (in multiples of Vdc) of the topology and whether polarity is generated inherently or not.

In topology [24] having eight switches and six diodes. Even though it is having less number of switches the TSV of the topology is very high which increases the rating of the switches. It also uses H-bridge for polarity generation. In [26], the quasi-resonant structure for boost in voltage and having high TSV. It has an extra inductor in the resonance circuit, and uses an H-bridge for polarity generation. The topology [27] has a large number of switches and driver circuits that decrease the efficiency of the inverter. In [28], have more switches compared to the proposed topology, it also has an additional capacitor, and the TSV is higher compared to the proposed topology. In [29], topology has more number of switches, five additional diodes, and one additional capacitor compared to proposed topology. In [32], topology has one switch less than proposed topology but it is using an extra capacitor and more gate drivers than proposed topology. The TSV and MBV are higher than the proposed topology. In [33], topology has an equal number of total components but it has high TSV and it has low voltage gain of three. In [36], topology uses a greater number of switches and having high value of TSV compared to the proposed topology. In [34],

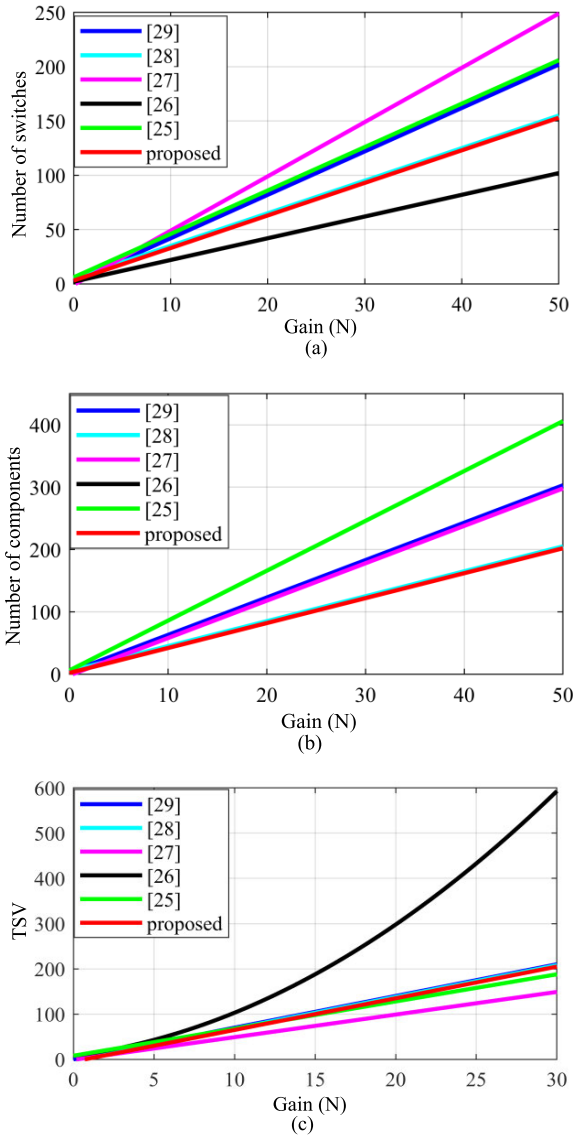

FIGURE 9. Comparison plots with recently proposed generalized topologies for (a) the number of switches, (b) the total number of components, and (c) the total standing voltage (TSV).

topology is having is having large MBV and more voltage rating capacitor than proposed topology. Reference [37] uses H-bridge for polarity generation which leads to a high value of TSV and MBV. The proposed topology is having less TSV and MBV then compared to other topologies in Table 2, which shows it is having low voltage stresses on the switches. It has an equal or less total number of components while compared with others in Table 2.

The comparison for proposed generalized topology and recently proposed other competitive generalized topologies is shown in Table 3. In [25], the topology consists of N+3 more switches compared to the proposed topology and uses the H-bridge for polarity generation. [26] uses fewer switches compared to the proposed topology, but the total number of

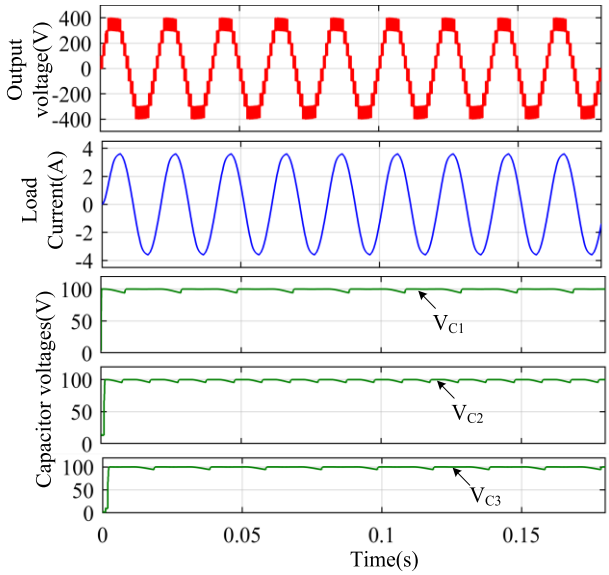

FIGURE 10. Output voltage, current, and capacitor voltages at 100Ω+120mH.

components are equal and TSV and MBV are high compared to the proposed topology. It also uses H-bridge for polarity generation. In [27], topology is having 2N-4 more switches compared to the proposed topology. In [28], the topology has two additional switches & one additional capacitor than the proposed topology. Topology in [29] is having a greater number of switches, diodes and capacitors compared to proposed topology. In [30], topology has fewer switches compared to the proposed topology, but it has a gain of only 2. In [31], topology has five switches more than proposed topology and has low voltage gain of N/2. In [36], topology has a greater number of switches compared to proposed topology and TSV is increasing largely with increase in levels. The TSV of [37] is more compared to the proposed topology and it uses additional H-bridge for polarity generation which increases the MBV. In Figure.9 (a) a comparison is made for the number of semiconductor switches (N_{sw}) with respect to gain (N) of generalized 2N+1 level inverters. In Figure.9 (b) total number of components (N_{Total}) sum of switches, diodes and capacitors is plotted with respect to gain (N). In Figure.9 (c) the total standing voltage (TSV) is plotted with respect to gain (N) for the topologies listed in the Table 3.

IV. SIMULATION RESULTS AND ANALYSIS

The performance of the proposed topology is analyzed under different conditions in MATLAB/Simulink. The ratings of the components used in the simulation are $V_{dc} = 100V$ and $C_1 = C_2 = C_3 = 2200\mu F$. In Figure.10, the load voltage, current, and balanced capacitor voltages of the proposed topology under RL load of 100Ω+120mH are shown for the DC source voltage of 100V and the amplitude modulation index ($M_a = 1$). The output voltage is nine levels with 400V peak amplitude, and three capacitor voltages are balanced at 100V. The voltage THD during this case is 16.49% and fundamental component magnitude of 389.9V shown in Figure.11.

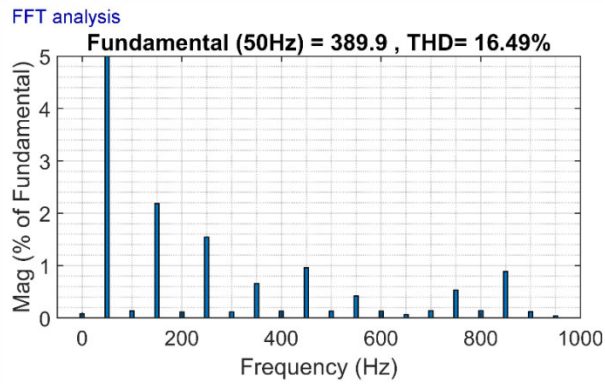

FIGURE 11. THD of the load voltage at 100Ω+120mH.

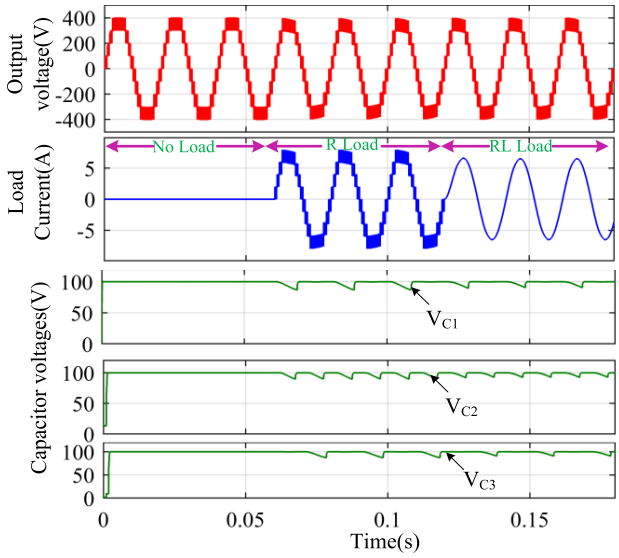

FIGURE 12. Output voltage, current and capacitor voltages for no load, 50Ω and 50Ω+100mH.

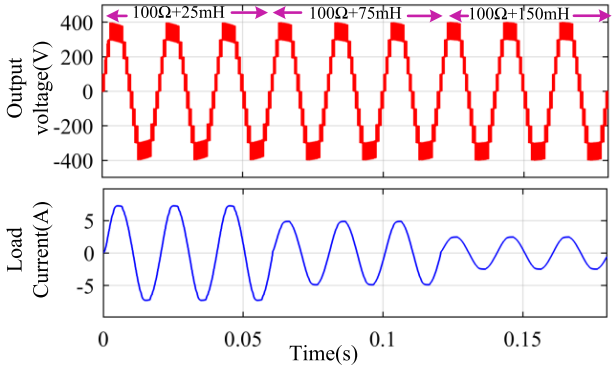

FIGURE 13. Output voltage and current for RL = 100Ω+25mH, 100Ω+75mH, 100Ω+150mH.

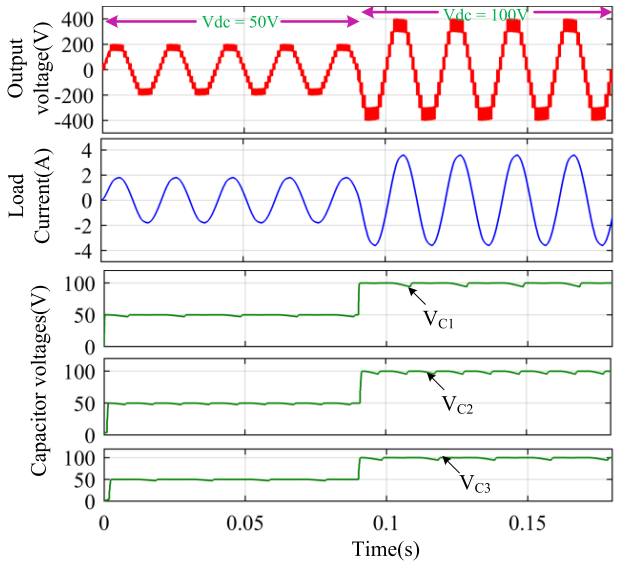

FIGURE 14. The output voltage, load current, and capacitor voltages for the DC supply change from 50 V to 100 V.

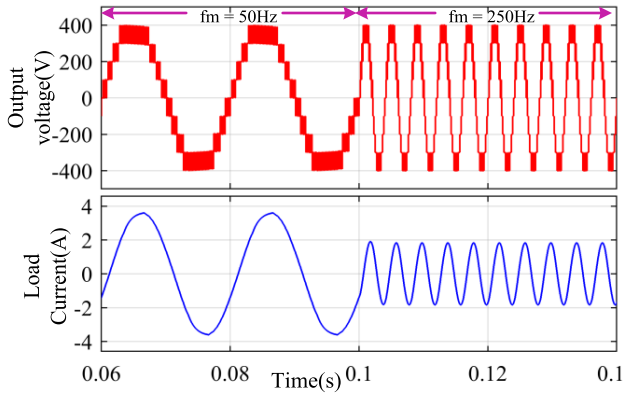

FIGURE 15. Output voltage and current for load frequency change of 50 Hz to 250 Hz.

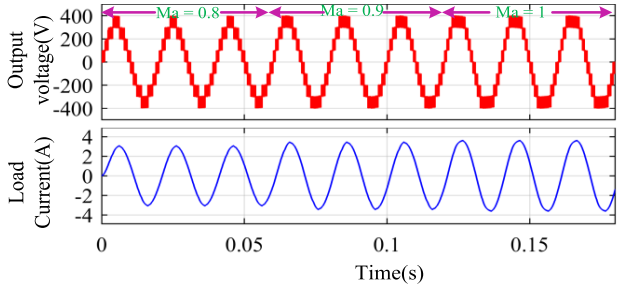

FIGURE 16. Output voltage and current for M_a = 0.8, 0.9 and 1 at 100Ω+120mH.

In Figure.12 the load variations are made for no-load, 50Ω and 50Ω+100mH and their respective load voltage, current and capacitors voltages are analyzed. During these load changes, the load voltage is maintained constant and the load current is varied as zero current, phase current, and lagging current. And capacitors voltage ripple is in permissible limits of below 10% during these load changes. In Figure.13 the load variations are done from 100Ω+25mH to 100Ω+75mH

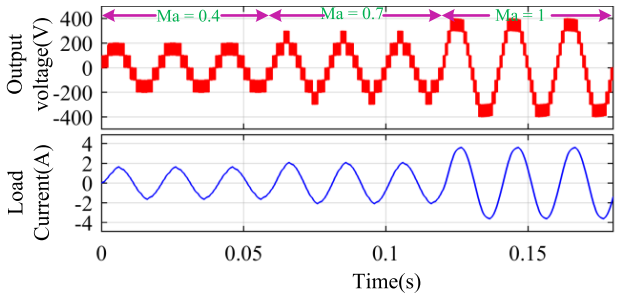

FIGURE 17. Output voltage and current for $M_a = 0.4, .7$ and 1 at 100Ω+120mH.

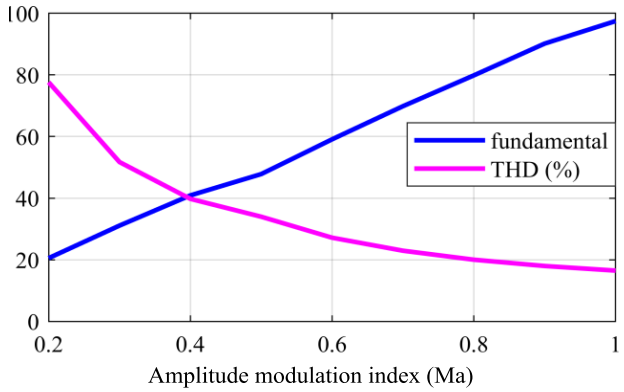

FIGURE 18. THD and fundamental component for Ma = 0.2 to 1.

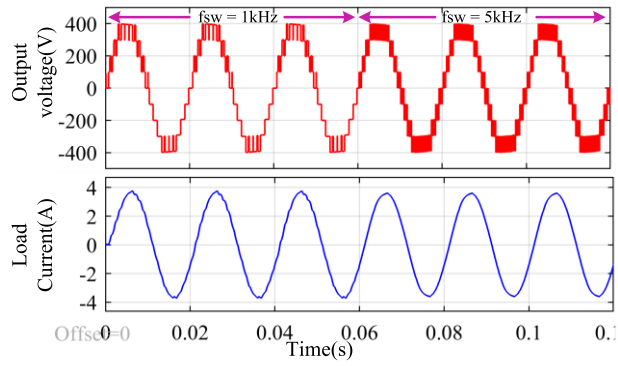

FIGURE 19. Output voltage and current for $f_{sw} = 1$ kHz and 5 kHz 100Ω+120mH.

to 100Ω+150mH and their load voltage and current are shown. The load current decreases in magnitude and becomes more lagging as inductive load increases.

In Figure.14 the input DC voltage is varied from 50V to 100V and the corresponding load voltage, current, and capacitors voltages are displayed. In both the cases the load voltage is having nine levels but the magnitude of peak has been doubled. The capacitor's voltages are balanced from 50V to 100V. In Figure.15 modulating signal frequency has changed from 50Hz to 250Hz and the corresponding load voltage and current are displayed. By increasing the supply frequency, the

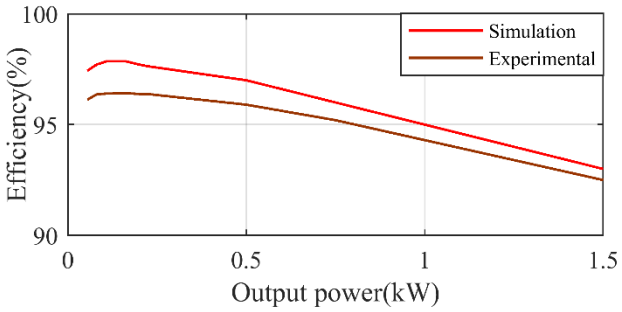

FIGURE 20. Efficiency for load changes from 0 to 1.5 kw.

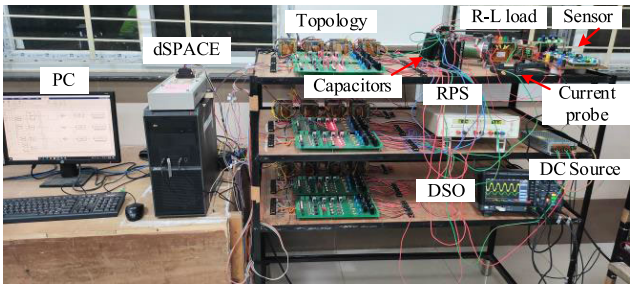

FIGURE 21. Experimental prototype.

TABLE 4. Components used in the experimental prototype.

Components	Ratings / Values
DC Voltage Sources	20 Volts
Switches (15)	IRFP460
Power diodes (15)	MUR860
Capacitors (3)	2200μF,450V
Resistive loads	100Ω
Inductive loads	300mH, 150mH.
Switching frequency	5kHz, 2.5kHz, 1kHz
Load frequency	50Hz

load current magnitude has decreased due to the increasing load impedance. The load frequency has been changed from 50Hz to 250Hz, which resembles that the proposed topology is suitable for high-frequency applications.

In Figure.16 load voltage and current are analysed for amplitude modulation index changes for $M_a = 0.8$, $M_a = 0.9$ and $M_a = 1$. For these M_a variations, the voltage levels are retained, but the width of the $+4V_{dc}$ and $-4V_{dc}$ levels is changed, which resembles the fundamental component variations as 319.4V, 360.7V, 389.9V for $M_a = 0.8, 0.9, 1$ respectively, and their corresponding voltage THD are 20.02%, 17.85%, and 16.49%. In Figure.17 load voltage and current are shown for the modulation index variations for $M_a = 0.4$, $M_a = 0.7$, and $M_a = 1$. With these M_a variations, the output voltage levels are changed to five, seven, and nine for $M_a = 0.4, 0.7, 1$ respectively, and the corresponding load current magnitude is changed. This happens because in LSPWM when $M_a = 0.4$ the modulating signal is compared with only four carriers (C_{r3}–C_{r6}). During $M_a = 0.7$ it was compared with only six carrier signals (C_{r2}–C_{r7}) and for $M_a = 1$ it was

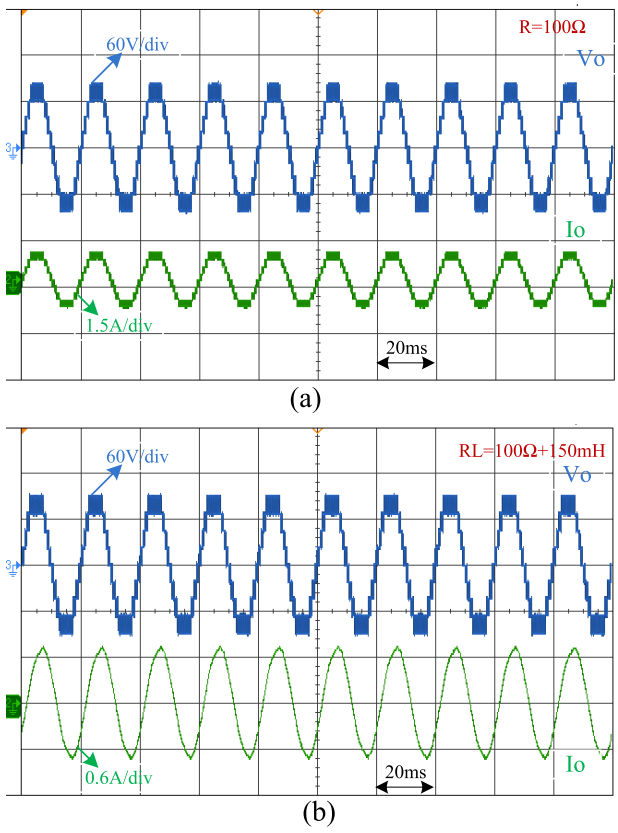

FIGURE 22. Output voltage and current (a) for the R = 100Ω load and (b) for the RL = 100Ω+150mH load.

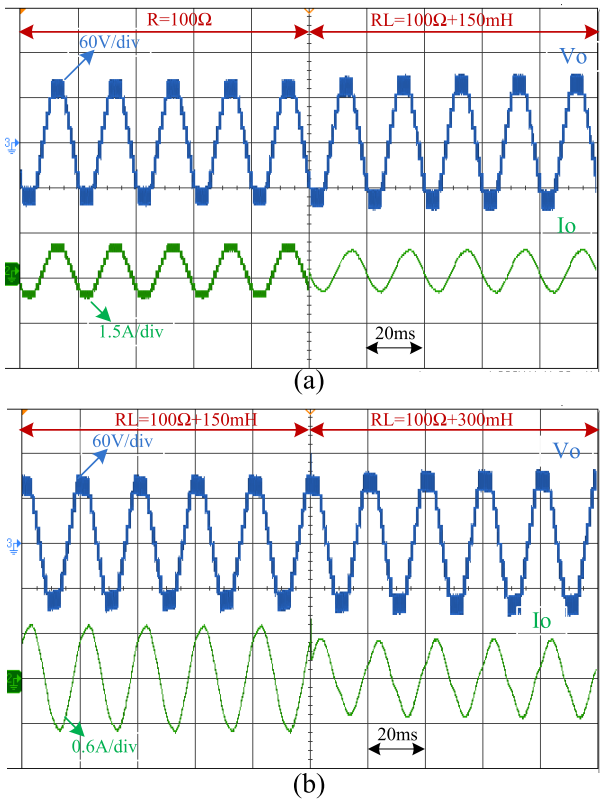

FIGURE 23. Output voltage and current (a) for the R = 100Ω to RL = 100Ω+150mH load changes and (b) for RL = 100Ω+150mH -to-RL = 100Ω+300mH load changes.

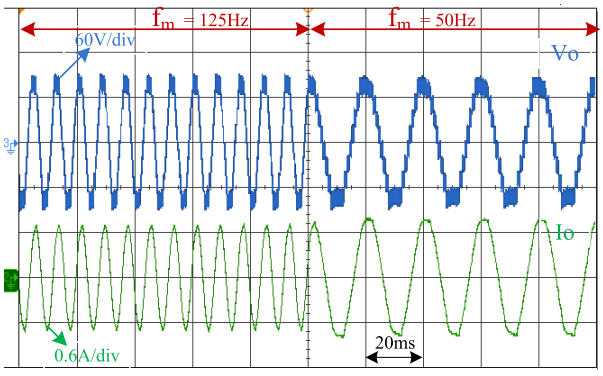

FIGURE 24. Output voltage and current for modulating frequency changes for modulating frequency changes of f_m = 125 Hz to f_m = 50 Hz.

compared with the eight carriers (C_{r1}–C_{r8}). In Figure.18 the voltage THD and fundamental component of the proposed topology is calculated for various modulation index values from M_a = 0.2 to 1 and a graph is plotted for THD (%), fundamental component in percentage of output peak voltage with respect to amplitude modulation index (M_a). Figure.18 shows that with increasing M_a, the fundamental component increases and the corresponding THD (%) decreases.

In Figure.19 the load voltage and current are observed for the changes in the switching frequency (carrier frequency) of f_{sw} = 1 kHz and f_{sw} = 5 kHz. With the increase in carrier frequency, the number of switching in each voltage level increases; which leads to increase in switching losses. But by increasing the carrier frequency the harmonics are shifted to higher order which reduces the size of the filter in grid connecting applications. In Figure.20 efficiency of the proposed topology is plotted for load variations of 0 to 1.5 kW. For the efficiency calculations switching losses and conduction losses of MOSFET and its antiparallel diode are considered.

V. EXPERIMENTAL RESULTS

Experimental studies are done on the prototype shown in Figure.21. The components and ratings used in the experimental setup are listed in Table 4. The control scheme for PWM signals shown in Figure.7 is designed in the Dspace1104 controller.

In Figure.22 (a) load voltage and current of the proposed 9-level topology are shown for R = 100Ω load and for RL = 100Ω + 150mH is shown in Figure.22 (b). In Figure.23 (a), the load change has been made from R load to RL load, and the transition is observed. The current is changed from in-phase to lagging. In Figure.23 (b) the load has been changed from RL = 100Ω+150mH to RL = 100Ω+300mH, with the increase in inductive load value the

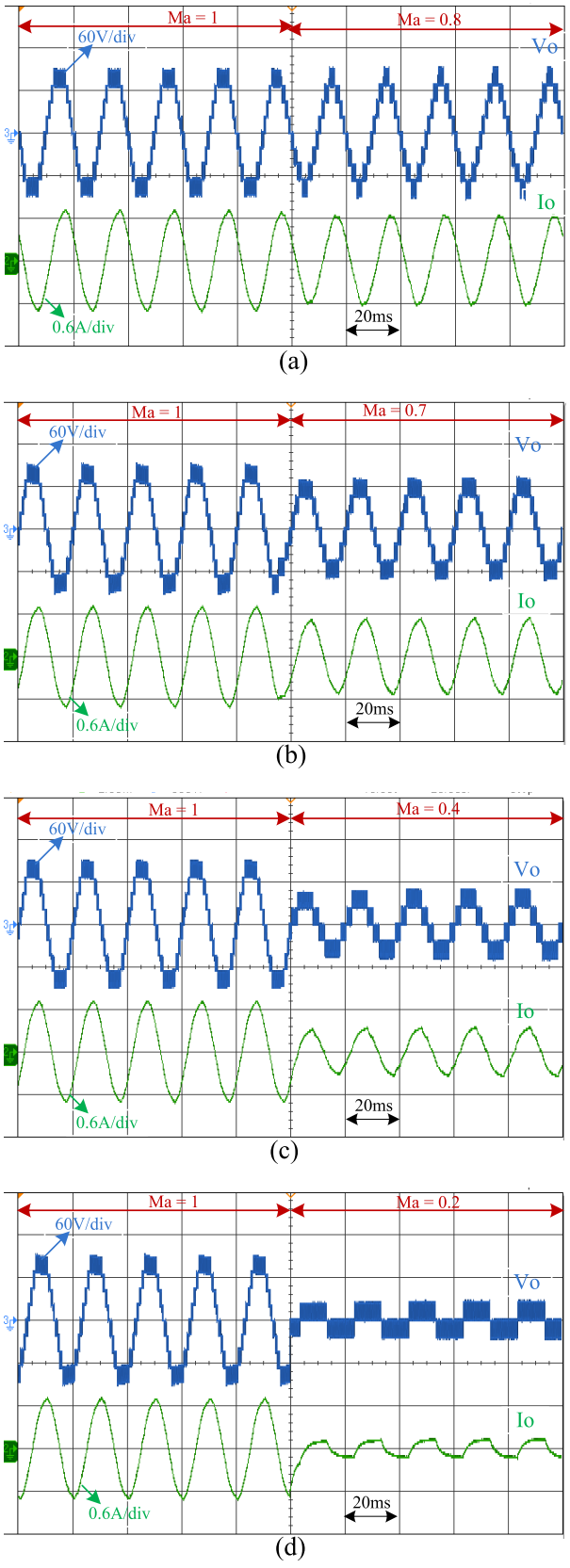

FIGURE 25. Output voltage and current for amplitude modulation (Ma) changes (a) Ma = 1–0.8, (b) Ma = 1–0.7, (c) Ma = 1–0.4, and (d) Ma = 1–0.2.

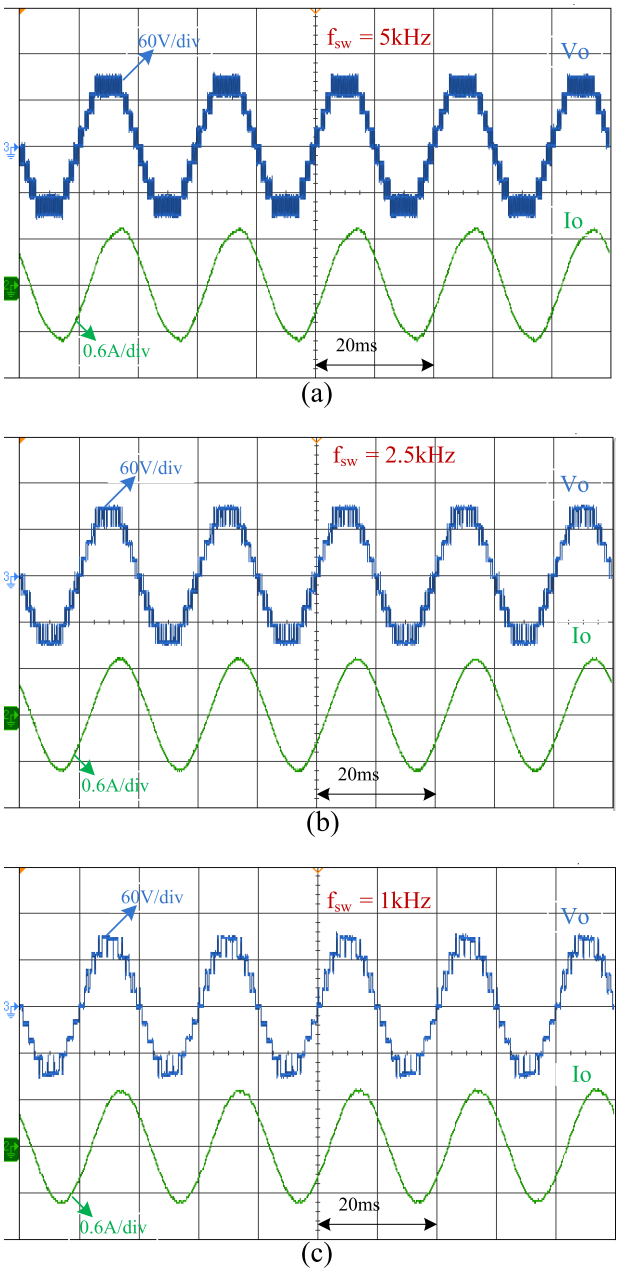

FIGURE 26. Output voltage and current for different switching frequencies (f_{SW}) (a) f_{SW} = 5 kHz (b) f_{SW} = 2.5 kHz (c) f_{SW} = 1 kHz.

current has decreased and became more lagging. In Figure.24 the modulating frequency is changed from 125Hz to 50Hz and the change in output frequency is observed and it is noted that proposed topology is suitable for high frequency applications. In Figure.25 (a) the amplitude modulation index is changed from Ma = 1 to 0.8 the voltage levels are retained but the width of the $+4V_{dc}$ & $-4V_{dc}$ level has been reduced as the number of comparisons between M and C_{r1} has reduced.

In Figure.25 (b) the modulation index is changed from 1 to 0.7 the output voltage levels are reduced from nine to

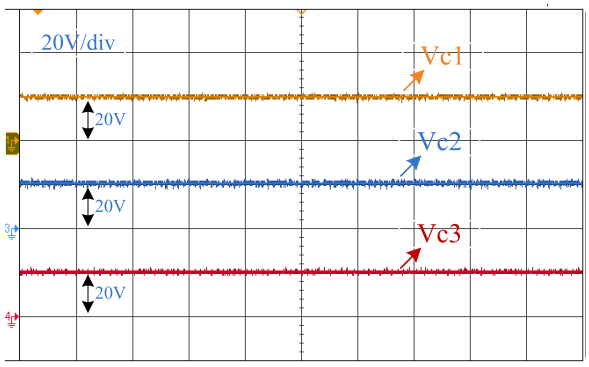

FIGURE 27. Balanced capacitor voltages of c_1, c_2 and c_3 for $V_{dc} = 20$ V.

seven as the modulating signal is not got in comparison with C_{r1} & C_{r8}. In Figure.25 (c) the modulation index is changed from 1 to 0.4 as a result, the voltage levels change from nine to five. In this case the modulating signal has been compared with C_{r3}, C_{r4}, C_{r5} and C_{r6}. In Figure.25 (d) the modulating index is changed from 1 to 0.2 then the voltage levels are reduced from nine to three, as in this case the modulating signal is compared with only two carriers C_{r4}& C_{r5}. In Figure.26 (a) load voltage and current are shown for RL load at a switching frequency (carrier frequency) of 5 kHz, in Figure.26 (b) for a switching frequency of 2.5 kHz and in Figure.26 (c) for a switching frequency of 1 kHz. With reduced switching frequency, the number of transitions in each voltage level has been reduced. In Figure.27 the voltage of the capacitors C_1, C_2 and C_3 are shown and it shows that the three capacitor voltages are balanced to V_{dc}. In Figure 20 the efficiency of 9-level prototype is calculated for load variations and compared with simulation efficiency. The prototype has maximum efficiency of 96.2%. Overall, with the results and analysis shown above, the properties mentioned of the proposed topology are validated.

VI. CONCLUSION

This paper proposes a high gain generalized MLI and quadruple boost nine-level inverter for small scale solar PV applications. It has the advantages of low switch stress and self-voltage balancing of capacitors. A comparative study is conducted with recent literature. The proposed topology is tested for different load variations, supply voltage variations and load frequency variations and it is suitable for all type of loads. And with different load variations, the voltage ripples of the capacitor are within the allowable limits. The topology is analyzed with LSPWM technique for changes in amplitude modulation, frequency modulation, and corresponding THD and fundamental component variations are observed. The efficiency is analyzed for the variations in load. The effectiveness of the proposed topology is verified by various simulation and experimental results.

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