IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received February 1, 2022, accepted February 14, 2022, date of publication February 17, 2022, date of current version March 3, 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3152536

Comparative Assessment of Multi-Port MMCs for High-Power Applications

YUAN LI, (Student Member, IEEE), AND GREGORY J. KISH, (Senior Member, IEEE)
Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 1H9, Canada

Corresponding author: Yuan Li (yl8@ualberta.ca)

This research was undertaken thanks in part to funding from the Canada First Research Excellence Fund.

ABSTRACT Multi-port converters can interconnect different dc and ac systems while reducing semiconductor requirements and losses by eliminating redundant power conversion stages. Modular multilevel converter (MMC)-based multiport systems are well suited for application in mixed ac-dc grids containing high-voltage dc (HVDC) and medium-voltage dc (MVDC) systems. This paper conducts a detailed comparative assessment of multi-port dc-dc-ac MMCs for high power applications. Four representative topologies are chosen for study due to their contrasting internal power processing characteristics. Three different network scenarios are investigated that include HVDC and MVDC applications, covering several different power flow cases. The multi-port MMCs are compared in terms of losses, semiconductor effort, internal energy storage and magnetics requirements. The results are extensively discussed and general conclusions are summarized.

INDEX TERMS Ac and dc grids, dc-dc modular multilevel converter, multi-port converter.

NOMENCLATURE

p, s, g	Primary, secondary and ac grid.
u, l	Upper and lower arm.
$P_{dc,p}$, $P_{dc,s}$	Primary and secondary dc port power injection.
P_{ac}	Ac port power injection.
P_{conv}	Converter rated power.
P^{ac}_{arm}, P^{dc}_{arm}	Average ac and dc power absorbed by $arm \in \{p, s\}$.
$V_{dc,p}$, $V_{dc,s}$	Primary and secondary dc port voltage.
G_v	Converter dc step ratio.
$V_{ac,LL(rms)}$	Grid line-to-line RMS voltage.
$i_{g,i}$	Grid current in phase i $\in \{a, b, c\}$.
i_Δ	Abstract current for frequency decoupling.
S_w	Total MVA rating of transformer windings.
$S_{w,j,i}$	MVA rating of transformer winding on side $j \in \{p, s, g\}$ for phase i $\in \{a, b, c\}$.
$V_{w,j}$	Transformer inter-winding dc voltage stress on side $j \in \{p, s, g\}$.
$i_{w,j,i}$	Transformer winding current on side $j \in \{p, s, g\}$ for phase $i \in \{a, b, c\}$.
α, β	Per-unitized power tapped from ac port and from primary dc port.
N	Number of submodules.
N_{HB}, N_{FB}	Number of half-bridge and full-bridge submodules.
k_s	Safety factor for capacitor voltage balancing.
C_{arm}	Individual submodule capacitance in $arm \in \{p, s\}$.
V_c	Submodule capacitor nominal voltage.
v_c, Δv_c	Submodule capacitor voltage, capacitor peak-to-peak voltage ripple.
E_{cap}	Total capacitive stored energy.
ΔE_{cap}	Capacitive energy peak-to-peak variation over one fundamental cycle.
λ	Semiconductor effort.
$P_{tr,loss}$	Transformer losses.
$P_{cond,loss}$	Converter conduction losses.
$P_{sw,loss}$	Converter switching losses.
T	Fundamental frequency period.
θ_v, θ_i	Phase angles of voltage and current.
$\hat{V}$, $\hat{I}$	Peak fundamental frequency ac component of voltage and current.
x_{arm}	Quantity $x \in \{P, v, i, N, N_{HB}, N_{FB}, V_c, \hat{V}, \hat{I}, C, E_{cap}, \Delta E_{cap}\}$ in $arm \in \{p, s\}$.
$x_{arm,i}$	Quantity $x \in \{v, i, V_c\}$ in phase $i \in \{a, b, c\}$ of $arm \in \{p, s\}$.
$x_{arm,u/l,i}$	Upper/lower arm quantity $x \in \{v, i, V_c\}$ in phase $i \in \{a, b, c\}$ of $arm \in \{p, s\}$.

The associate editor coordinating the review of this manuscript and approving it for publication was Elisabetta Tedeschi.

x^{dc}, x^{ac} Dc and ac components of $x \in \{P, v, i\}$.
$\hat{V}^{y}$ Peak fundamental frequency ac component of arm voltage for $y \in$ {MP-F2F, MP-AT, MP-MMC, MP-CT}

I. INTRODUCTION

The growing global trend of integrating renewable energy resources such as wind turbines and photovoltaics into the legacy ac grid is giving rise to mixed ac/dc power systems. High-voltage dc (HVDC) is now widely used for transmission systems [1] while medium-voltage dc (MVDC) is emerging as a key part of future distribution systems [2], [3]. Innovative concepts such as ac overlaid meshed dc systems, often referred to as supergrids, allow higher utilization of existing ac infrastructure while improving reliability and flexibility [4]. These supergrids are likely to evolve over time from the interconnection of many smaller independent systems. During this development process, existing high-voltage ac (HVAC) grids will be upgraded or integrated to the HVDC grids to enhance their power transfer capability and system stability.

Mixed ac-dc power systems can utilize multi-port converters to control power flows between the different dc and ac grids, e.g., to inject power extracted from offshore wind turbines to the onshore ac load centres [5]. Moreover, multi-port converters can enable power exchange between existing interconnected networks via HVDC or MVDC links. The term *multi-port* denotes a converter system with multiple dc and/or ac voltage ports; in this work, multi-port dc-dc-ac converters are specifically studied. Power electronic dc-dc and dc-ac converter stages will thus be the key building blocks of multi-port dc-dc-ac converters. The dc-dc converters can be galvanic isolated or non-isolated [6], and voltage-sourced converter or line-commutated converter technologies can be used for dc-ac conversion [7]. The simplest way to form a multi-port converter is to combine separate dc-dc and dc-ac converters, but this imposes multi-stage power conversion that can lead to lower efficiency and higher cost [8]. Alternatively, multi-port converter structures can be realized that avoid unnecessary conversion stages by merging dc-dc and dc-ac stages into a single converter arrangement. This can increase system efficiency and provide a more compact footprint. Such multi-port converters are increasingly being studied for various applications, e.g. [9]–[11], however, limited work has been carried out on high-voltage and high-power multi-port topologies due to the increased structural and control complexity relative to their lower voltage and power counterparts.

Dc-dc converter topologies that exploit established modular multilevel converter (MMC) technology to accommodate high voltage and power applications have emerged in recent years [6], [12], [13]. Multi-port dc-dc-ac MMCs can be created by augmenting dc-dc MMCs with a dc-ac stage. Based on this premise, a two-stage multi-port dc-dc-ac MMC is realized in [14] and [15] by using a three-winding transformer in the front-to-front (F2F) configured dc-dc MMC. However, although providing galvanic separation, the full power processing by the internal transformer and the two stage dc-ac/ac-dc process contributes to higher losses. To reduce power losses and semiconductor devices, several multi-port converters have been proposed that exploit partial power processing. In [16]–[19], the HVDC autotransformer (HVDC-AT) originally proposed in [14] is adapted into a multi-port structure, where a number of controllable dc and ac outputs are provided from series-stacked MMCs. This multi-port autotransformer only processes partial power and thus an improvement in conversion efficiency is obtained. In [13], [20], and [21], MMC-based dc-dc converters have been adapted for ac grid connectivity by multitasking the transformers to carry both dc and ac currents. Some multi-port MMCs are examined and compared in [5], but the comparison is limited to a couple of basic design scenarios and so few general conclusions are drawn. The main focus of [5] is on converter modeling and control. In [22], the lower arms of the conventional dc-ac MMC are shared the upper arms are isolated to achieve direct multiple dc port connection. However, these publications provide limited insight into the actual design, viability, and overall performance of multi-port MMCs for a wide range of different application scenarios.

This paper performs a detailed comparative assessment of multi-port dc-dc-ac MMCs for high power applications, where two different dc systems are interconnected with an external ac grid. Such systems can be adopted for large-scale integration of renewable power generations into HVDC transmission or local ac/dc distribution systems with different dc and ac voltage levels. The main contributions of this work are: 1) Classifying and assessing the emerging multi-port dc-dc-ac MMCs based on their internal power transfer mechanisms, organized into two categories (i) multi-port MMCs that use conventional transformers, and (ii) multi-port MMCs that multitask transformers to realize additional power transfer mechanisms. 2) Carrying out a detailed comparative study between four representative multi-port MMCs in terms of losses, semiconductor effort, energy storage and magnetics. A total of nine power flow cases are considered for three different design scenarios, including both HVDC and MVDC. Key outcomes of the analysis are summarized.

II. MULTIPORT MMCs UNDER STUDY

Figs. 1(a)-(d) show the four different multi-port MMCs selected for study: the MP-F2F, MP-CT, MP-AT and MP-MMC. These exemplar topologies are chosen as they represent different classes of multi-port MMCs with contrasting internal power processing characteristics. Multi-port MMC topologies, e.g. [17], [21]–[23] are not compared here as they share strong structural similarly to the four representative topologies. Each multi-port MMC interfaces two dc systems, $V_{dc,p}$ and $V_{dc,s}$, with an ac system. Subscripts p and s denote primary and secondary sides, respectively. $P_{dc,p}$, $P_{dc,s}$ and

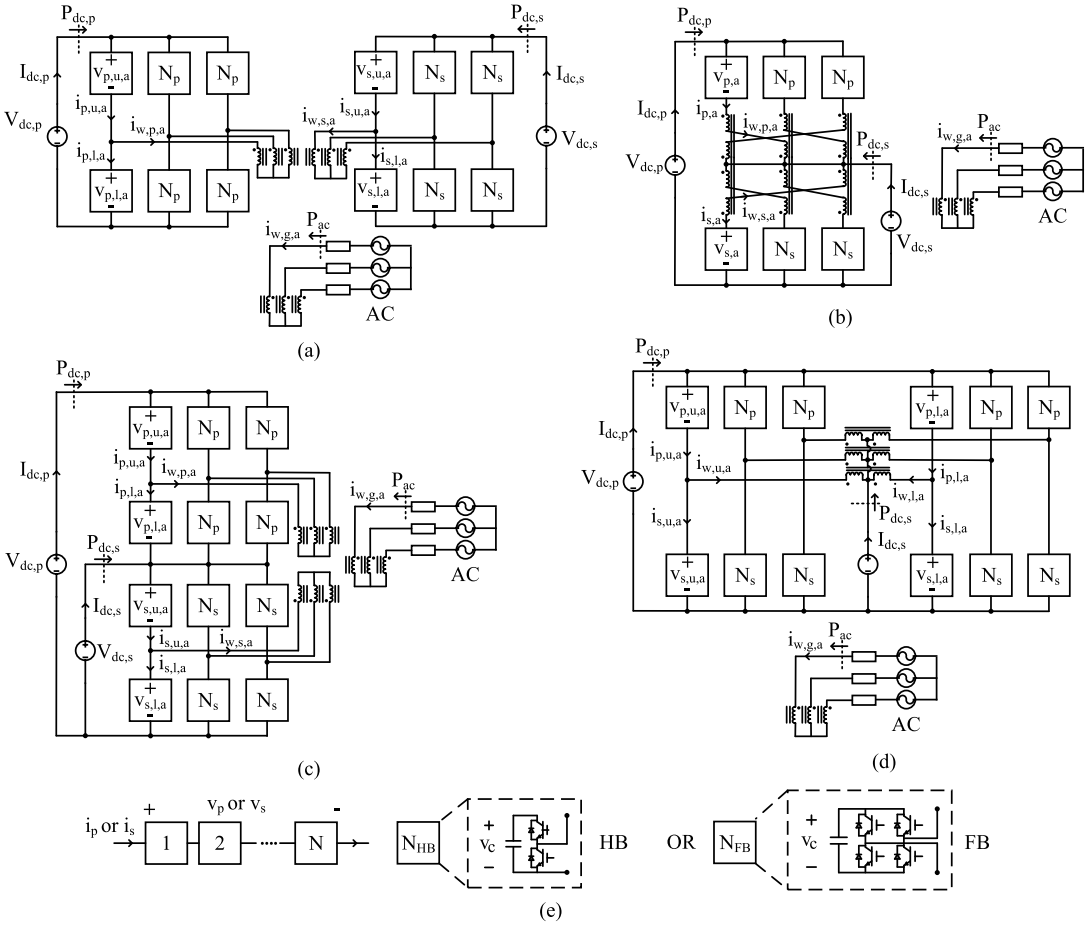

FIGURE 1. Multi-port MMCs under study: (a) MP-F2F [14], [15], (b) MP-CT, (c) MP-AT [16]–[19], (d) MP-MMC [20], (e) composition of individual phase arms.

P_{ac} denote average power injections at the dc and ac ports. The p and s phase arms comprise N_p and N_s series cascaded submodules (SMs), which can be half-bridge (HB) or full-bridge (FB) type, as shown in Fig. 1(e). An overview of the internal power processing characteristics of the four topologies is provided in sections II-A and II-B, where the converters are categorized based on their contrasting characteristics.

Assuming lossless energy conversion, the steady-state average power absorbed by each arm in Figs. 1(a)-(d) must be equal to zero as the SMs contain only capacitive energy storage, e.g., $P_p = \frac{1}{T}\int_0^T v_p i_p dt = 0$ in Fig. 1(b). The arm currents and voltages comprise dc and fundamental frequency ac components. Harmonic power balance [24], [25] necessitates the dc power absorbed by an arm, P^{dc}_{arm}, must be balanced by average power absorption at fundamental frequency, P^{ac}_{arm},

$$P^{ac}_{arm} = P^{dc}_{arm}, \tag{1}$$

where

$$P^{ac}_{arm} = \frac{1}{2}\hat{V}_{arm}\hat{I}_{arm}cos(\theta_{v_{arm}} - \theta_{i_{arm}}) \tag{2}$$

$$P^{dc}_{arm} = V_{arm}I_{arm}, \tag{3}$$

and placeholder subscript $arm \in p, s$. Variables $\hat{V}_{arm}$, $\hat{I}_{arm}$ and V_{arm}, I_{arm} are the (peak) fundamental frequency ac and dc components of the arm voltages and currents in Fig.1(e). In the subsequent sections, equation (3) is used to explore the average power processing characteristics of the phase arms within the different multi-port topologies. The power handling requirements of the different transformer windings will also be examined, as influenced by port power flow demands.

For all multi-port topologies, dc step ratio G_v is defined as

$$G_v = \frac{V_{dc,s}}{V_{dc,p}}. \tag{4}$$

A. POWER PROCESSING CHARACTERISTICS OF TOPOLOGIES WITH CONVENTIONAL AC TRANSFORMER: MP-F2F AND MP-AT

The MP-F2F and MP-AT in Figs. 1(a) and 1(c) are similar with respect to utilizing a conventional ac transformer between MMCs. The MP-F2F is realized by adding a third winding (for ac grid interface) to the well known front-to-front dc-dc MMC [15], [16]. Alternatively, the two MMCs can be series stacked on their dc sides which leads to the non-isolated MP-AT topology Fig. 1(c) [16]–[19]. The MP-F2F

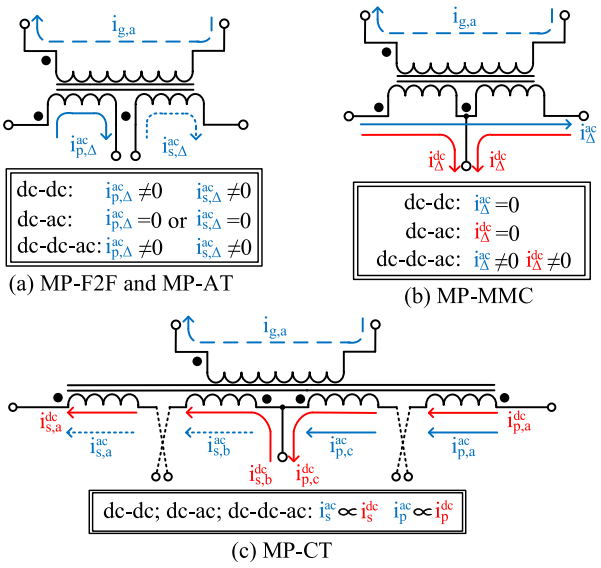

FIGURE 2. Frequency components of transformer winding currents for (a) MP-F2F and MP-AT; (b) MP-MMC; (c) MP-CT.

and MP-AT both use transformer action to transfer ac power between the MMCs and grid. However, their internal converter power processing characteristics are different due to the different ways in which the MMCs are interconnected.

For the MP-F2F, the average power processed by the semiconductor switches in the p and s arms depends on port power flow conditions

$$P_p^{dc} = \frac{1}{6}P_{dc,p}, \quad P_s^{dc} = \frac{1}{6}P_{dc,s}. \tag{5}$$

The six p (and s) arms must collectively process the full dc power transfer associated with $V_{dc,p}$ (and $V_{dc,s}$). This is due to use of separate dc/ac MMC stages.

Based on (1) and assuming for ease of analysis that reactive power transfer is negligible, the power processed by the p side winding $S_{w,p,a}$, s side winding $S_{w,s,a}$, and grid side winding $S_{w,g,a}$ for phase a of the MP-F2F transformer is

$$S_{w,p,a} = \left|\frac{P_{dc,p}}{3}\right|, \quad S_{w,s,a} = \left|\frac{P_{dc,s}}{3}\right|, \quad S_{w,g,a} = \left|\frac{P_{ac}}{3}\right|. \tag{6}$$

The results of (6) indicate the transformer must be rated to handle the full rated power transfer between ports. This outcome for the MP-F2F is a consequence of the two-stage dc-ac/ac-dc conversion process.

In contrast to the MP-F2F, the MP-AT can realize reduced semiconductor and magnetics power processing requirements. This is because the two MMCs are now series-stacked on their dc sides, i.e. $V_{dc,p}$ is formed in part by $V_{dc,s}$, and hence fewer total semiconductors are needed to support the same dc port voltages. Also, the dc ports are no longer decoupled through an ac link and consequently the transformer can realize partial power processing. The average power processed by the p and s arms in the MP-AT is

$$P_p^{dc} = \frac{1}{6}(1 - G_v)P_{dc,p}, \quad P_s^{dc} = \frac{1}{6}(G_v P_{dc,p} + P_{dc,s}), \tag{7}$$

The results of (7) depend on dc step ratio G_v defined in (4). This is an outcome of the partial power processing property of the MP-AT. Contrasting (7) with (5) reveals the dc powers processed by the arms in the MP-AT can be reduced relative to the MP-F2F, depending on G_v and the port power flows.

The amount of power transferred by the p, s and grid side windings for phase a of the MP-AT transformer is

$$S_{w,p,a} = \left|\frac{(1 - G_v)P_{dc,p}}{3}\right|, \quad S_{w,s,a} = \left|\frac{G_v P_{dc,p} + P_{dc,s}}{3}\right|$$
$$S_{w,g,a} = \left|\frac{P_{ac}}{3}\right|. \tag{8}$$

Converter-side windings ratings $S_{w,p,a}$ and $S_{w,s,a}$ in the MP-AT both depend on the dc step ratio, however, $S_{w,g,a}$ indicates the grid-side winding must always process the rated ac port power similar to the MP-F2F case. Comparing (8) with (6) confirms the power processed by the MP-AT transformer converter-side windings can be reduced relative to the MP-F2F, depending on G_v and the port power flows.

The frequency components for phase a winding currents of the MP-F2F and MP-AT transformers are illustrated in Fig. 2(a), including the impact of port conversion modes (i.e. whether dc-dc, dc-ac and dc-dc-ac conversions are taking place). Abstract currents $i^{ac}_{p,\Delta} \triangleq i^{ac}_{p,u,a} - i^{ac}_{p,l,a}$ and $i^{ac}_{s,\Delta} \triangleq i^{ac}_{s,u,a} - i^{ac}_{s,l,a}$ are defined here to highlight the ac current paths in the transformer. As expected, only fundamental frequency ac current exists as both converters use classical transformer action to shuttle power between the MMCs and grid. However, the MP-F2F and MP-AT have different internal power processing characteristics as shown by (5),(6) and (7),(8). This is because the MP-AT employs single-stage dc-dc conversion due to its partial power processing structure.

B. POWER PROCESSING CHARACTERISTICS OF TOPOLOGIES WITH MULTITASKING TRANSFORMERS: MP-CT AND MP-MMC

The MP-CT and MP-MMC in Figs. 1(b) and 1(d) also realize partial power processing for dc-dc conversion, similar to the MP-AT. However, whereas the MP-AT (and F2F-MMC) use the ac transformer solely to transfer average ac power between p and s MMCs, the MP-CT and MP-MMC multitask their transformers to enable additional internal power transfer mechanisms beyond classical transformer action. This *multitasking* requires the transformer winding currents to have multiple frequency components. In the MP-CT and MP-MMC, the converter-side windings carry both dc and ac currents. However, due to the windings orientations, dc flux cancellation is imposed in the transformer cores [20], [26].

The MP-CT in Fig. 1(b) is a new topology proposed here by adding a grid interfacing winding to the dc-dc MMC proposed in [26], and uses a zig-zag arrangement for the converter-side windings to realize core dc flux cancellation. Alternatively, the MP-MMC in Fig. 1(d) uses center-tapped windings on the converter-side to realize dc flux cancellation [20]. The MP-MMC requires dual MMCs in a differential configuration;

a single-ended configuration could be realized with more complicated converter-side windings arrangement, such as in [21] and [5]. However, the internal power processing characteristics would remain identical, and thus the MP-MMC in Fig. 1(d) is selected for analysis.

Figs. 2(b) and 2(c) illustrate the frequency components for phase a transformer winding currents of the MP-MMC and MP-CT, respectively, including the impact of power conversion modes. In Fig. 2(b), the frequencies of the center-tapped winding currents depend on the power conversion mode. Only dc (or fundamental frequency ac) components exist in the converter-side windings for pure dc-dc (and pure dc-ac) conversion, while both frequency components are present for multi-port dc-dc-ac conversion. This is elucidated by defining abstract currents $i_{\Delta}^{dc} \triangleq i_p^{dc} - i_s^{dc}$ and $i_{\Delta}^{ac} \triangleq i_p^{ac} - i_s^{ac}$ to decouple frequency components. In contrast, the MP-CT zig-zag windings in Fig. 2(c) must always carry both dc and fundamental frequency ac currents, regardless of the power conversion mode. This is because the converter-side windings in Fig. 1(b) are placed in series with the phase arms.

Due to the commonality of partial power processing, the average powers processed by the p and s arms in the MP-CT and MP-MMC are the same as for the MP-AT, see (7).[1] The power processed by the grid side transformer winding in the MP-CT and MP-MMC, $S_{w,g,a}$, is also the same as for the MP-AT (and also the F2F-MMC), see (8). However, because the converter-side transformer windings in the MP-CT and MP-MMC multitask by carrying multiple frequency components as discussed above, the power processing of these windings are different from the MP-AT and the F2F-MMC.

The amount of power transferred by the p and s converter-side windings for phase a of the MP-CT transformer is

$$S_{w,p,a} = \sqrt{\frac{3}{2}} \cdot \frac{(1 - G_v)P_{dc,p}}{3}, \qquad S_{w,s,a} = \sqrt{\frac{3}{2}} \cdot \frac{G_v P_{dc,p} + P_{dc.s}}{3} \tag{9}$$

These values are higher than the MP-AT results of (8) by a factor of $\sqrt{3/2}$. This leads to a commensurately higher core power rating, and is due to higher rms currents in the MP-CT converter-side transformer windings. But this comes with the benefit of eliminating inter-winding dc voltage stresses that plague the MP-AT, leading to overall reduced core area-product (and associated losses) for the MP-CT magnetics. Further details on this trade-off can be found in [26].

In the MP-MMC, the center-tapped winding in each phase is shared between p and s arms. To maintain notational consistency with other topologies, the power rating of the winding on the upper and lower side is represented as $S_{w,p,a}$ and $S_{w,s,a}$, respectively. The power handling requirements of the center-tapped winding for phase a is

$$S_{w,p/s,a} = \frac{1}{2} \frac{\sqrt{(P_{dc,p} + P_{dc,s})^2 + kP_{dc,s}^2}}{3},$$

[1]For MP-CT, denominator of (7) should be 3 as it has $3p$ (and $3s$) arms.

where

$$k = \frac{1}{2} \frac{\left(\frac{\hat{V}_{arm}}{V_{dc,p}}\right)^2}{G_v^2}. \tag{10}$$

The MP-MMC is the only multi-port topology in Fig. 1 where the magnetics do not provide voltage matching between phase arms, i.e. a turns ratio does not link p and s phase arms. Consequently, the power rating of the converter-side center-tapped winding depends on the choice of modulated ac arm voltage, $\hat{V}_{arm}$, for a given G_v, as represented by k in (10). More discussions on this design consideration will be included as part of the comparative analysis in the subsequent sections.

III. CASE STUDY MULTIPORT SCENARIOS AND ASSESSMENT CRITERIA

This section carries out a comparative analysis of the four multi-port converter topologies in Fig. 1. Three different multi-port scenarios (A, B and C) are considered as shown in Fig. 3, where each scenario is further broken down into three sub cases based on different port power flow demands. These scenarios consider both HVDC and MVDC applications. The following parameters are fixed in all scenarios: $V_{dc,p} = 400$ kV, $V_{ac,LL(rms)} = 220$ kV. The following comparison assumes that: 1) reactive power transfer to the grid is negligible; and 2) the three-phase ac grid is balanced positive sequence.

Scenario A considers the interconnection of two HVDC grids with different nominal voltages and one HVAC grid. $V_{dc,s}$ is set to 200 kV, which corresponds to dc step ratio $G_v = 0.5$. All ports are rated for $P_{conv} = 400$ MW.

Scenario B is a variation of Scenario A where $V_{dc,s} = 320$ kV, yielding a dc step ratio $G_v = 0.8$ and reflecting two HVDC grids with more similar nominal voltage levels. All ports are rated for $P_{conv} = 400$ MW.

Scenarios A and B consider exclusively HVDC voltage levels for the dc systems. In contrast, Scenario C investigates interfacing a 40 kV MVDC system with the 400 kV HVDC system. This will explore implications of a relatively low dc step ratio $G_v = 0.1$. All ports are rated for $P_{conv} = 300$ MW.

In Fig. 3, Scenarios A, B and C are further divided into three sub cases based on different power flows between the three ports. Specifically,

1) Cases $A1$, $B1$, $C1$: $P_{dc,p}$ as ± 1 pu, and α (or per-unitized P_{ac}) is varied between 0 and 1, red lines;
2) Cases $A2$, $B2$, $C2$: $P_{dc,s}$ as ± 1 pu, and α (or per-unitized P_{ac}) is varied between 0 and 1, green lines;
3) Cases $A3$, $B3$, $C3$: P_{ac} as ± 1 pu, and β (or per-unitized $P_{dc,p}$) is varied between 0 and 1, blue lines.

Cases $A1, B1, C1$ and $A2, B2, C2$ reflect the ac system tapping power from dc ports. Cases $A3$, $B3$, $C3$ can be viewed as an external dc system ($V_{dc,p}$) tapping power from the other ports. Notation $\pm$ denotes positive/negative power flows.

Based on the scenarios in Fig. 3, four multi-port converters in Fig. 1 are compared in terms of semiconductor efforts,

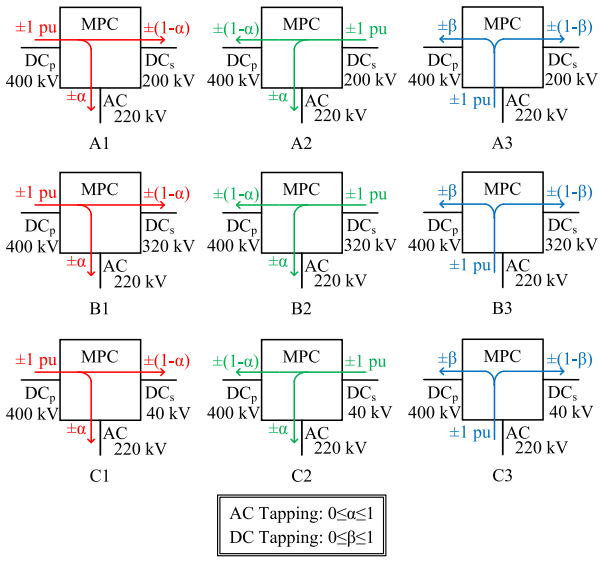

FIGURE 3. Multiport converter (MPC) scenarios under study, where $V_{dc,p}$ = 400 kV and $V_{ac,LL(rms)}$ = 220 kV are held constant, and (i) Scenarios $A1, A2, A3$ have $G_v = 0.5$, $P_{conv} = 400$ MW, (ii) Scenarios $B1, B2, B3$ have $G_v = 0.8$, $P_{conv} = 400$ MW, (iii) Scenarios $C1, C2, C3$ have $G_v = 0.1$, $P_{conv} = 300$ MW.

efficiency, internal stored energy and magnetic requirements. To provide a fair comparison, all multi-port converters are designed to provide fault blocking capability at the dc and ac ports by using the necessary number of FBSMs in the arms.

A. CURRENT STRESSES AND SEMICONDUCTOR EFFORT

A sufficiently high number of SMs are needed in each converter arm, N_{arm}, to generate the required arm voltage v_{arm}, where subscript $arm \in p, s$. The fundamental frequency component of the arm voltage, $\hat{V}_{arm}$, dictates the fundamental frequency ac currents flowing within the converter. Based on (1)-(2), and assuming peak ac arm voltages $\hat{V}_p$ and $\hat{V}_s$ are generated at p and s arms, respectively, the peak ac current seen by p and s arms in all multi-port topologies are

$$\hat{I}_p = 2\frac{P_{p,dc}}{\hat{V}_p cos(\theta_{v_p} - \theta_{i_p})}, \quad \hat{I}_s = 2\frac{P_{s,dc}}{\hat{V}_s cos(\theta_{v_s} - \theta_{i_s})} \tag{11}$$

$\hat{I}_p$ and $\hat{I}_s$ can be minimized by maximizing ac arm voltages $\hat{V}_p$ and $\hat{V}_s$ [26], [27]. Note that if the generated arm ac voltage is greater than arm dc voltage, solely FBSMs are employed in that arm to ensure SM capacitor balance can be satisfied [28]. In this work, the maximal value of $\hat{V}_p$ and $\hat{V}_s$ of each converter are limited to

$$\hat{V}_p^{MP-F2F} = \frac{1}{2}V_{dc,p}, \quad \hat{V}_s^{MP-F2F} = \frac{1}{2}V_{dc,s} \tag{12}$$

$$\hat{V}_p^{MP-AT} = \frac{1}{2}(1 - G_v)V_{dc,p}, \quad \hat{V}_s^{MP-AT} = \frac{1}{2}V_{dc,s} \tag{13}$$

$$\hat{V}_p^{MP-MMC} = \frac{1}{2}V_{dc,p}, \quad \hat{V}_s^{MP-MMC} = \frac{1}{2}V_{dc,p} \tag{14}$$

$$\hat{V}_p^{MP-CT} = (1 - G_v)V_{dc,p}, \quad \hat{V}_s^{MP-CT} = V_{dc,s} \tag{15}$$

In HVDC applications, fault blocking is usually an important requirement to maintain high transmission security and reliability [29]. In a meshed system, it is also important to disconnect the correct (i.e. faulted) line but keep the remaining system operational. The F2F dc-dc MMC inherently offers bidirectional fault blocking due to the galvanic separation property of the intermediate ac transformer. However, with the addition of the grid-side winding in Fig. 1(a), the MP-F2F loses dc fault blocking capability as the external ac grid can now source fault current. Consequently, a sufficient number of FBSMs have to be installed in the arms to enable the MP-F2F to provide bidirectional dc fault blocking. In all topologies, each converter arm requires sufficient blocking capability in both forward and reverse directions to block dc faults in both the primary and secondary dc sides [29]. In addition to the dc fault interrupting capability, utilizing FBSMs provides freedom to control the maximum arm ac voltage regardless of the available dc voltage. This is commonly done in dc-dc MMC topologies, e.g. [1], [30], [31], which can enable the reduction of arm ac current. FBMSs are thus chosen here to conduct a fair comparison of the four topologies. It is worth noting that other submodule configurations, such as those studied in [32], can be utilized to potentially further reduce converter losses while maintaining fault interrupting capability. Table 1 summarizes the arm voltage requirements of the multi-port MMCs in Fig. 1 to achieve fault blocking on all ports. The red text indicates FBSMs are necessary for the required arm voltage generation.

TABLE 1. v_{arm} generation requirements for multi-port MMCs of Fig. 1 to ensure fault blocking on all ports (red text denotes FBSMs).

	[min, max] voltage injection required
v_{arm}	MP-F2F
v_p	$[-\hat{V}_p, \frac{1}{2}V_{dc,p} + \hat{V}_p]$
v_s	$[-\hat{V}_s, \frac{1}{2}V_{dc,s} + \hat{V}_s]$
v_{arm}	MP-AT
v_p	$[-\frac{1}{2}V_{dc,s} - \hat{V}_p, \frac{1}{2}V_{dc,p} + \hat{V}_p]$
v_s	$[-\hat{V}_s, \frac{1}{2}V_{dc,s} + \hat{V}_s]$
v_{arm}	MP-MMC and MP-CT
v_p	$[-V_{dc,s} - \hat{V}_p, V_{dc,p} + \hat{V}_p]$
v_s	$[-\hat{V}_s, \frac{1}{2}V_{dc,s} + \hat{V}_s]$

The number of SMs required in a converter arm N_{arm} can be estimated by the nominal voltage V_c of the SM capacitors and the maximum (peak) value of arm voltage v_{arm} that has to be generated as per Table 1

$$N_{arm} = k_s \frac{max(v_{arm})}{V_c}, \tag{16}$$

where k_s is an additional safety factor that is set to 120% in this study. FBSMs are needed only if a negative arm voltage is required (as indicated by red text in Table 1). The number of FBSMs required is

$$N_{FB,arm} = k_s \frac{|min(v_{arm})|}{V_c} \tag{17}$$

Therefore, the number of HBSMs is

$$N_{HB,arm} = N_{arm} - N_{FB,arm} \tag{18}$$

The semiconductor effort λ is often used as a measure of the power rating of switches that has to be installed per Watt of P_{conv} [26], [29], [33]. The switch rating of FBSMs will be two times of HBSMs due to the fact that FBSM consists of 4 semiconductors.

B. SUBMODULE CAPACITIVE STORED ENERGY

The total capacitive stored energy E_{cap} is the energy per megawatt (MW) stored in the MMC converter [34]. In this work, the SM capacitance can be different between p and s arms. This is because the power processed by the arms in a multi-port converter can be different. The capacitive stored energy E_{cap} in $arm \in \{p, s\}$ is

$$E_{cap,arm} = \frac{\frac{1}{2} \cdot N_{arm} C_{arm} V_c^2}{P_{conv}} \tag{19}$$

where N_{arm}, C_{arm} and V_c are total number of SMs, individual SM capacitance in $arm \in \{p, s\}$ and nominal SM capacitor voltage, respectively.

The submodule capacitance required to achieve a certain capacitor peak-to-peak voltage ripple Δv_c may be predicted by considering the total energy stored in each arm. It is related to the capacitive energy peak-to-peak variation over one fundamental cycle ΔE_{cap} [30]:

$$C_{arm} = \frac{\Delta E_{cap,arm}}{N_{arm} V_c^2 \cdot \Delta v_c} \tag{20}$$

For fixed values of $\Delta E_{cap,arm}$, N_{arm} and V_c, lower values of submodule capacitance reduces the converter cost but results in higher voltage ripples. In this study, C_p and C_s values are picked to yield peak-to-peak capacitor voltage ripples Δv_c of around 16% at rated power transfer. Thus, the total energy stored in the converter can be calculated from the total capacitor energies in each arm as

$$E_{cap} = q(E_{cap,p} + E_{cap,s}) \tag{21}$$

Where $q = 6$ for the MP-F2F, MP-AT and MP-MMC; and $q = 3$ for the MP-CT. In the conventional dc-ac MMC, a total capacitive stored energy of 30-40 kJ/MW yields a submodule peak-to-peak capacitor voltage ripple in the range of 20% [35], [36].

C. POWER LOSSES

This section calculates the power losses of the four multi-port converter systems in Fig. 1. It is assumed that conduction and switching losses are the primary sources of losses in each converter. An average losses calculation method is chosen. A detailed breakdown of calculations involved for conduction and switching losses used in this work can be found in [30] and [31]. Due to the symmetry of the converters, conduction and switching losses are estimated separately for each arm by considering the voltages and currents of one submodule and then summed up the losses to determine the total losses of the converter.

Since the semiconductor losses calculation is dependent on technology, the Mitsubishi CM1200HC-90R HVIGBT with a rating of 4500 V and 1200 A is used for all topologies (datasheet parameters available in [37]). As the current carried by the semiconductors substantially increases for lower conversion ratios, IGBTs are paralleled as needed to accommodate arm currents that exceed switch ratings [30]. The converters operate at f = 50 Hz due to ac grid connection.

In addition to converter switching and conduction losses, this paper use a method similar to [26], [31] to approximate the magnetics losses. This method approximates losses as 0.5% of the transformer MVA rating.

IV. STUDY RESULTS AND DISCUSSION

Fig. 4(a) shows the converter losses, semiconductor efforts, required apparent power ratings of magnetics and the total capacitive stored energies for the MP-F2F, MP-AT, MP-MMC and MP-CT considering the nine different power flow cases in Fig. 3. The bar graphs are organized into three rows to separate scenarios A, B, C, and are further apportioned into columns to separate sub cases 1,2,3, e.g., the first column comprises cases $A1, B1, C1$. The first two columns correspond to tapping 400α MW ac power (cases $A1, A2, B1, B2$) and 300α MW ac power (cases $C1, C2$) from the dc ports, where $\alpha \in [0, 1]$. The third column corresponds to tapping 400β MW dc power (cases $A3, B3$) and 300β MW dc power (case $C3$) from the other ports, where $\beta \in [0, 1]$. The bar graphs summarize results for some key values of α and β, due to space limitations. For ease of comparison, the bar graph results are normalized as follows: λ by P_{conv}, S_w by $2P_{conv}$, and losses by P_{conv}.

Figs. 4(b),(c),(d) show the multi-port converter topology with the lowest overall losses for every operating point in Scenarios A, B, C, respectively, for all possible values of α and β. Results are plotted $P_{dc,s}$ versus P_{ac} where $P_{dc,p} = -(P_{dc,s} + P_{ac})$. In each plot, the operating areas are divided into 6 segments (by the dotted lines) corresponding to the different power flow sub cases, where red, blue, green and black represents the MP-F2F, MP-AT, MP-MMC and MP-CT, respectively.

The discussion of comparison results is organized into four subsections as follows:

- Contrasting key comparison results for the four converters
- Discussing implications of the magnetics being used
- Contrasting multi-port (dc-dc-ac) and two-port (dc-dc and dc-ac) conversion processes
- Presenting exemplar simulation results

A. COMPARISON OF FOUR MULTI-PORT CONVERTER TOPOLOGIES

The four multi-port topologies are divided into two categories as discussed in section II. The MP-F2F and MP-AT are grouped together based on their use of classical transformer action for inter-arm power transfers. The MP-CT and MP-MMC are grouped together because they both multi-task their transformers to achieve additional power transfer mechanisms. However, the MP-AT, MP-CT and MP-MMC

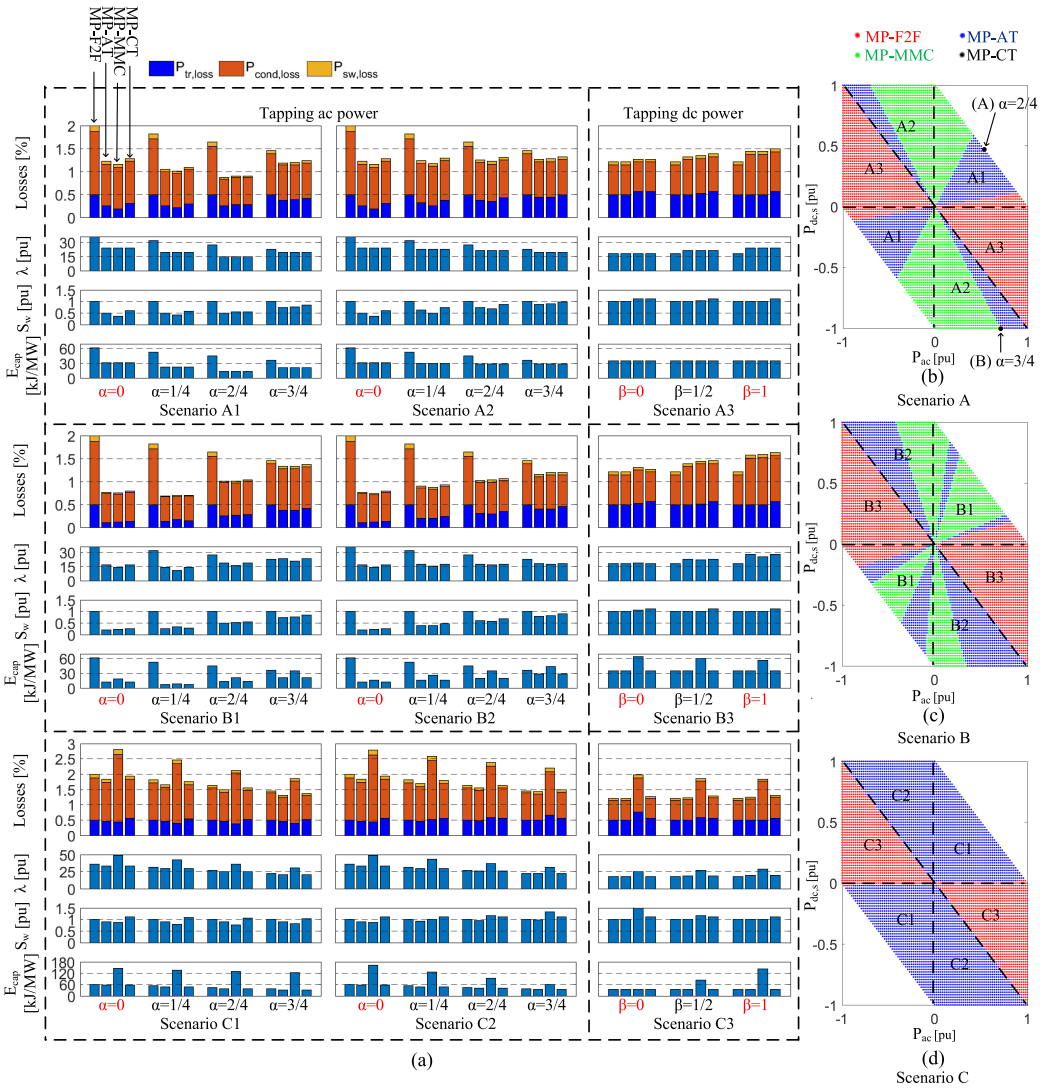

FIGURE 4. Results of comparative analysis for power flow cases in Fig. 3. (a) Bar graphs showing results for key values of α and β: semiconductor effort λ (normalized to P_{conv}), magnetics total MVA rating S_W (normalized to $2P_{conv}$), capacitive stored energy E_{cap} and losses (normalized to P_{conv}). (b)(c)(d) topologies with lowest overall losses for all possible power flows in scenarios *A*, *B*, and *C*, respectively.

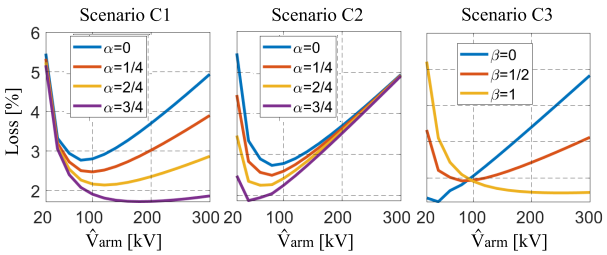

FIGURE 5. Losses of the MP-MMC of Scenario *C* for different arm ac voltages.

all practice partial power processing. Therefore, the MP-AT shares some performance similarities with the MP-CT and MP-MMC even though they are not categorized together. The reason is that the MP-AT, MP-MMC and MP-CT all have the same amount of power being processed by the semiconductor switches in the p and s arms (see (7)). However, their transformers still process different amounts of power, ultimately resulting in different performance outcomes between them.

1) AC POWER TAPPING

The first two columns in Fig. 4(a) compare the four different multi-port MMCs for tapping different amounts of ac power from the dc ports, considering different dc step ratios $G_v = \{0.5, 0.8, 0.1\}$. There is a significant reduction in overall losses for the MP-AT, MP-MMC and MP-CT relative to the MP-F2F for $G_v = 400/200 = 0.5$ (cases $A1, A2$) and $G_v = 400/320 = 0.8$ (cases $B1, B2$). The MP-F2F also experiences higher semiconductor efforts, magnetic requirements and capacitive energy storage requirements. This outcome is due to the higher average power processed by the magnetics as well as the semiconductor switches for the MP-F2F, see (5)-(7), due to the lack of partial power

processing. The multi-port topology with the lowest overall losses for every operating point in Scenarios A and B is shown in Figs. 4(b)[2] and 4(c). respectively. Fig. 4(b) shows that in regions $A1$ and $A2$ (and $B1$ and $B2$) the MP-MMC and MP-AT have the highest efficiencies, barring a small set of power flow conditions adjacent to region $A3$ (and $B3$) where the MP-F2F has lower losses. Although the MP-CT does not appear in Figs. 4(b) and 4(c), it's important to highlight its performance is nearly identical to the MP-AT, regardless of dc step ratio, as quantified by the results in Fig. 4(a). The MP-CT suffers from a slightly lower efficiency due to its slightly higher magnetics requirements, as the MP-CT transformer always handles both dc and ac currents while the MP-AT transformer handles only ac currents, see Figs. 2(a) and 2(c). Figs. 4(b) and 4(c) show the benefits of the MP-MMC are most pronounced at $G_v = 0.5$ (cases $A1, A2$). The MP-AT exhibits increasingly higher efficiency as the dc step ratio increases from $G_v = 0.5$ (cases $A1, A2$) to $G_v = 0.8$ (cases $B1, B2$). This is seen by the reduction in green area (and corresponding increase in blue area) when contrasting Figs. 4(b) and 4(c). In scenario B, the relative higher capacitive stored energy of the MP-MMC also makes it less attractive compared with the MP-AT.

The significant reduction in losses for the MP-AT, MP-MMC and MP-CT relative to the MP-F2F starts to diminish as the dc step ratio becomes smaller, seen in Fig. 4(a) for cases $C1, C2$ where $G_v = 400/40 = 0.1$. The power processed by the p and s arms for the MP-AT, MP-MMC and MP-CT are nearly the same as the MP-F2F as G_v approaches zero, see (5) and (7). Specifically, the extremely high current stresses in the MP-MMC at very low G_v makes its losses and capacitive stored energy even higher than the MP-F2F. The total stored energy for the MP-MMC in scenario C is over 140 kJ/MW. This is because the MP-MMC lacks a transformer for inter-arm ac voltage maximization that hinders low G_v application; the relationship between the arms ac current and voltage is given by (11). Fig. 5 shows the impact of arm ac voltage variations on the overall losses of the MP-MMC in Scenario C. The losses can be reduced by adjustment of $\hat{V}_{arm}$ based on power flow cases. For example, 200 kV can be considered as the optimal arm ac voltage for $\alpha = 3/4$ in case $C1$. In scenario C, $\hat{V}_{arm}$ is set to 100 kV for achieving relatively low losses in all cases. Among the four multiport topologies, the MP-AT has the lowest overall losses in cases $C1$ and $C2$, see Fig. 4(d).

In summary, for power flow cases $A1, A2, B1, B2, C1, C2$ corresponding to ac power tapping, the MP-MMC has advantages over the MP-AT around $G_v = 0.5$. However, the MP-AT becomes increasingly more attractive over the MP-MMC as the dc step ratio deviates from $G_v = 0.5$. This is reflected by the change in dominance from green to blue in Figs. 4(b) through to 4(d).

[2]To elucidate the connection with Fig. 3, two exemplar operating points in Fig. 4(b) are marked as point A ($\alpha = 2/4$ in region $A1$) and B ($\alpha = 3/4$ in region $A2$).

TABLE 2. Magnetics inter-winding dc voltage stress relative to grid-side winding.

	$V_{w,p}$	$V_{w,s}$	$V_{w,g}$
MP-F2F	$1/2\ V_{dc,p}$	$1/2\ V_{dc,s}$	0
MP-AT	$1/2\ (V_{dc,p} + V_{dc,s})$	$1/2\ V_{dc,s}$	0
MP-MMC	$V_{dc,s}$	N/A	0
MP-CT	$V_{dc,s}$	$V_{dc,s}$	0

2) DC POWER TAPPING

The third column in Fig. 4(a) investigates the performance of the four topologies for tapping dc power from the other ports (cases $A3, B3, C3$). Interestingly, the MP-F2F has the superior performance across all dc step ratios for these cases (red dominates in regions $A3, B3, C3$ in Figs. 4(b),(c),(d)). The MP-AT, MP-MMC and MP-CT also have good performance, except for the MP-MMC in case C3. The MP-F2F has especially good efficiency when power is transferring between $V_{dc,p}$ and the AC port, as indicated by red text $\beta = 1$ in Fig. 4(a). The results indicate the two-stage MMC structure of Fig. 1(a) is likely the preferred multi-port topology for dc power tapping when interfacing HVDC and MVDC systems with a local ac grid.

B. IMPLICATIONS OF MAGNETICS SOLUTIONS

The multi-port MMCs in Fig. 1 utilize different magnetics solutions. The MP-F2F and MP-AT can use conventional three-phase three-winding ac transformers, which can be designed similar to conventional grid interfacing transformer. The transformer in the MP-MMC is a three-phase two-winding transformer, however, it has an open ended winding with a center tap on the converter side. The MP-CT utilizes transformer with dual zig-zag windings and an extra winding to create an ac grid interface. The MP-MMC has arguably the lowest complexity design while the MP-CT design is likely the most complex.

It is important to highlight the MP-F2F and MP-AT transformers must support dc voltage stresses between the two converter-side windings, while the MP-MMC and MP-CT do not have this issue. The transformer windings dc voltage stresses (relative to the grid side winding, $V_{w,g}$) for the four topologies are summarized in Table 2. The MP-F2F has a dc voltage bias of $1/2(V_{dc,p} - V_{dc,s})$ between primary and secondary windings, while the MP-AT has a constant value of $1/2V_{dc,p}$. This is a notable drawback of the MP-AT as the converter-side windings must be insulated to tolerate 50% of the highest dc port voltage between them, regardless of the dc step ratio. The MP-MMC and MP-CT do not have any dc voltage stresses between primary and secondary windings. The additional dc voltage stresses between windings for the MP-F2F and MP-AT lead to increased magnetics size, weight and core design complexity.

The comparison in section IV-A approximated the magnetics losses as 0.5% of the transformer total MVA rating [31]. The inter-winding dc voltage stresses were not considered, similar to other comparative works [16], [30], [31]. That is, it did not account for an increase in the magnetic losses

TABLE 3. Comparison of converter arrangements in Fig. 6.

	λ [pu]	S_w [pu]	E_{cap} [kJ/MW]
Two-port solution Fig. 6(a)	21	0.75	33
Multi-port solution Fig. 6(b)	15	0.5	14

that results from increased size of the magnetics core, due to extra insulation requirements needed to accommodated inter-winding dc voltage stresses. Reference [26] recently proposed a method to approximate the relative change in core area product between different transformers in two-port dc-dc converters, to quantify the impact on converter efficiency. The work in [26] shows that such dc stresses lead to significant increases in core area product and ultimately increased magnetics losses. Therefore, although analytically outside the scope of this paper, the insight from [26] suggests that accounting for inter-winding dc voltage stresses would likely result in

- The MP-MMC becoming more attractive when tapping ac power (cases $A1$, $A2$, $B1$, $B2$) due to reduced magnetics size and associated losses;
- The MP-AT transformer having higher losses across all dc step ratios, potentially shifting preference to the MP-CT for certain power flow cases $A1$, $A2$, $B1$, $B2$, $C1$, $C2$.

C. CONTRASTING TWO-PORT AND MULTI-PORT POWER CONVERSION

This section compares the losses and cost of realizing a dc-dc-ac system using two options: (a) separate two-port dc-dc and dc-ac MMCs, and (b) one multi-port dc-dc-ac MMC. The two-port dc-dc HVDC-AT [16] and the MP-AT in Fig. 1(c) are assumed in this case study comparison, along with the conventional two-port dc-ac MMC.

Fig. 6 illustrates an example scenario where DC_s (200 kV) and AC (220 kV) systems send an equal amount of power (200 MW) to DC_p (400 kV). Fig. 6(b) corresponds to the MP-AT in scenario $A1$ of Fig. 4(a) with $\alpha = 2/4$ (i.e. 50% of the power sourced from the ac port). In contrast, Fig. 6(a) uses the HVDC-AT and conventional dc-ac MMC. Note in Fig. 6(a) that operation of the HVDC-AT and MMC are respectively equivalent to power flow case $A2$ with $\alpha = 0$ (MP-AT operating solely as dc-dc converter) and power flow case $A3$ with $\beta = 1$ (MP-F2F operating solely as dc-ac converter). The HVDC-AT is designed with sufficient number and type of submodules to provide black start capability similar to the MP-AT in Fig. 6(b).

Fig. 6 shows that for identical port power flows the MP-AT option has approximately 29% lower losses than the two-port solution that requires multiple converters. Table 3 summarizes other key metrics for Fig. 6, showing significant reductions in semiconductor effort, magnetics MVA rating and capacitive energy storage can also be realized with the MP-AT option. This points to a lower overall converter station footprint for the MP-AT.

The comparison in Fig. 6 is carried out to emphasize the potential benefits of using multi-port dc-dc-ac converters in comparison to deploying separate dc-dc and dc-ac converters. Depending on the application and port power flow demands, multi-port converters can be attractive from the perspective of reducing overall system losses and investment cost.

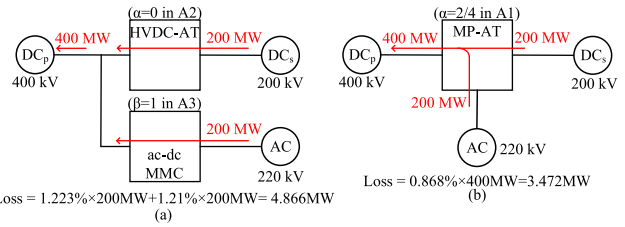

FIGURE 6. Configuration and losses for dc-dc-ac systems using (a) separate two-port MMCs; (b) multi-port MMC.

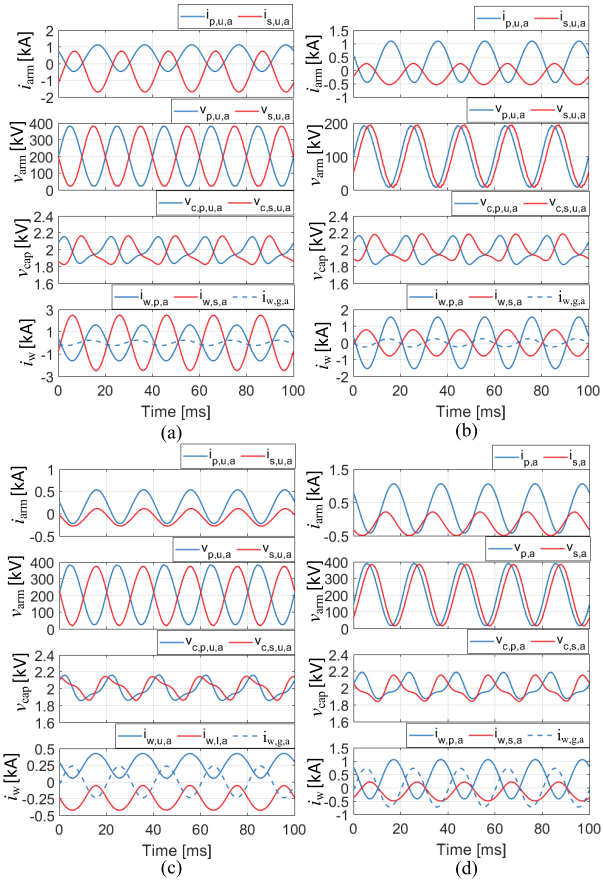

FIGURE 7. Voltage and current waveforms corresponding to Scenario $A1$ with $P_{ac} = 1/4$ pu (a) MP-F2F; (b) MP-AT; (c) MP-MMC; (d) MP-CT.

D. EXEMPLAR SIMULATION RESULTS

This section provides exemplary simulation results using PSCAD/EMTDC to verify the comparative analysis.

Fig. 7 shows simulation results for the four multi-port topologies in scenario $A1$ with $\alpha = 1/4$. With $V_{dc,p} = 400$ kV and $V_{dc,s} = 200$ kV, the upper and lower arms in the primary side of MP-F2F must support 200 kV_{dc} while upper and lower arms in the secondary side must support 100 kV_{dc}. The generated ac arm voltage are 180 kV_{ac} and 90 kV_{ac}. This is confirmed by Fig. 7(a), where the resulting arm currents

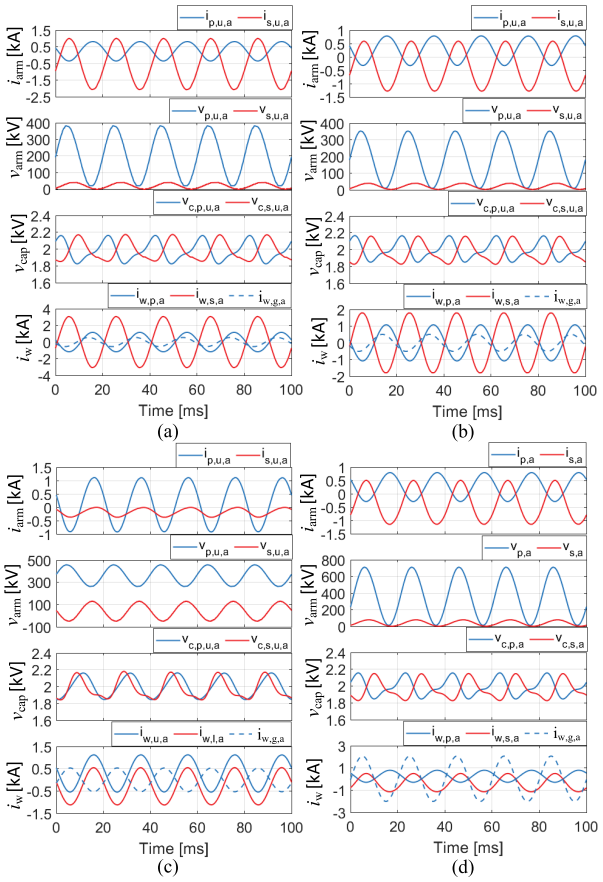

FIGURE 8. Voltage and current waveforms corresponding to Scenario $C1$ with $P_{ac} = 3/4$ pu (a) MP-F2F; (b) MP-AT; (c) MP-MMC; (d) MP-CT.

are also presented. The MP-MMC in Fig. 7(c) and MP-CT Fig. 7(d) have identical generated arm dc and ac voltages as the MP-F2F. The primary and secondary arms in the MP-AT only need to support 100 kV_{dc} as shown in Fig. 7(b), with 90 kV_{ac} generated arm ac voltages. The SM capacitor voltages of all toplogies are successfully regulated to 2 kV. The transformer windings in the MP-F2F and MP-AT for primary, secondary and ac grid side carry only ac currents. However, as expected, the transformer windings of the MP-MMC and MP-CT will carry both ac and dc currents. This is consistent with the analysis in Fig. 2.

Fig. 8 shows simulation results for the four multi-port topologies in scenario $C1$ with $\alpha = 3/4$. With $V_{dc,p} = 400$ kV and $V_{dc,s} = 200$ kV, the arm voltages in the primary and secondary side of four topologies are notably different. The MP-F2F arms supports 200 kV_{dc} and 20 kV_{dc} in the primary and secondary arms respectively, while the MP-AT supports 180 kV_{dc} and 20 kV_{dc} respectively. 360 kV_{dc} and 40 kV_{dc} are generated in primary and secondary arms in the MP-CT to achieve primary dc voltage $V_{dc,p} = 400$ kV. The MP-MMC arms supports 360 kV_{dc} and 40 kV_{dc} in the primary and secondary side, respectively. With $\hat{V}_{arm} = 90$ kV, the MP-MMC have to generate negative arm voltages in the secondary side as shown in Fig. 8(c).

V. CONCLUSION

This work carries out a detailed assessment and comparison of four multi-port dc-dc-ac MMC-based converters for high power applications. The topologies under study were chosen as they represent multi-port converters with contrasting internal power processing characteristics. These characteristics include two-stage conversion, partial power processing, and the multi-tasking of magnetics by allowing multiple frequency components in the winding currents. The semiconductor effort, losses, magnetics ratings and internal stored energy of the multi-port MMCs are compared, considering a total of nine different power flow cases from three core application scenarios. The converters are designed to have fault blocking capability on all ports. The key findings are:

- The MP-MMC and MP-AT offer the best performance for ac tapping in dc-dc-ac systems with moderate dc step ratios, e.g., 400/200 kV and 400/320 kV, where substantial savings in losses, semiconductors, capacitive energy storage and magnetics can be achieved relative to the MP-F2F. The MP-CT has a similar performance except for a slightly lower efficiency due to higher magnetics losses. The MP-MMC, MP-AT and MP-CT realize these benefits courtesy of partial power processing for the dc-dc stage, although the MP-F2F retains galvanic separation property. The benefits of the MP-MMC are most pronounced at $G_v = 0.5$, while the MP-AT performance becomes better as the dc step ratio deviates from $G_v = 0.5$. The MP-AT becomes the superior choice for ac tapping with low dc system step ratios, e.g., 400/40 kV, where the MP-MMC has prohibitively high current stresses.
- The MP-F2F has the best performance for dc tapping in dc-dc-ac systems, with moderate reductions in losses, semiconductors, capacitive energy storage and magnetics relative to the other topologies depending on the power flows. Its internal transformer makes the MP-F2F well suited for interfacing HVDC and MVDC systems. The MP-F2F is the only multi-port topology with galvanic separation between dc ports.
- The MP-CT and MP-MMC are the only multi-port topologies without dc voltage stresses between converter-side transformer windings. This can simplify core design and reduce the magnetics size and losses. Accordingly, taking this into account, the MP-CT may become preferable over the MP-AT for ac tapping in dc-dc-ac systems for certain power flow demands.
- A comparison between two-port and multi-port converter systems for dc-dc-ac applications shows the latter can achieve significant reductions in losses, semiconductor effort, capacitive stored energy and magnetics rating. Thus, multi-port converters can be attractive alternatives to deploying separate two-port converters, helping to reduce converter station footprint and investment cost.

REFERENCES

[1] M. Barnes, D. Van Hertem, S. P. Teeuwsen, and M. Callavik, "HVDC systems in smart grids," *Proc. IEEE*, vol. 105, no. 11, pp. 2082–2098, Nov. 2017.
[2] J. Yu, A. Moon, K. Smith, and N. Macleod, "Developments in the angle-DC project; Conversion of a medium voltage AC cable and overhead line circuit to DC," in *Proc. CIGRE Paris Session*, 2018, pp. 1–10.
[3] Working Group C6.31, "Medium voltage direct current (MVDC) grid feasibility study," CIGRE, Paris, France, WG C6.31, Tech. Rep., 793, 2020.
[4] D. Van Hertem and M. Ghandhari, "Multi-terminal VSC HVDC for the European supergrid: Obstacles," *Renew. Sustain. Energy Rev.*, vol. 14, no. 9, pp. 3156–3163, Dec. 2010.
[5] M. Rouhani and G. J. Kish, "Multiport DC–DC–AC modular multilevel converters for hybrid AC/DC power systems," *IEEE Trans. Power Del.*, vol. 35, no. 1, pp. 408–419, Feb. 2020.
[6] G. P. Adam, I. A. Gowaid, S. J. Finney, D. Holliday, and B. W. Williams, "Review of DC–DC converters for multi-terminal HVDC transmission networks," *IET Power Electron.*, vol. 9, no. 2, pp. 281–296, 2016.
[7] C. Li, P. Zhan, J. Wen, M. Yao, N. Li, and W.-J. Lee, "Offshore wind farm integration and frequency support control utilizing hybrid multiterminal HVDC transmission," *IEEE Trans. Ind. Appl.*, vol. 50, no. 4, pp. 2788–2797, Jul. 2014.
[8] F. Nejabatkhah and Y. W. Li, "Overview of power management strategies of hybrid AC/DC microgrid," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7072–7089, Dec. 2015.
[9] C. Perera, J. Salmon, and G. J. Kish, "DC/AC voltage sourced converter with auxiliary DC port for renewable energy applications," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2020, pp. 1842–1849.
[10] Z. Tang, Y. Yang, and F. Blaabjerg, "An interlinking converter for renewable energy integration into hybrid grids," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2499–2504, Mar. 2021.
[11] C. Perera, J. Salmon, and G. J. Kish, "Multiport converter with independent control of AC and DC power flows for bipolar DC distribution," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 3473–3485, Mar. 2021.
[12] J. D. Paez, D. Frey, J. Maneiro, S. Bacha, and P. Dworakowski, "Overview of DC–DC converters dedicated to HVdc grids," *IEEE Trans. Power Del.*, vol. 34, no. 1, pp. 119–128, Feb. 2019.
[13] G. J. Kish, "On the emerging class of non-isolated modular multilevel DC–DC converters for DC and hybrid AC–DC systems," *IEEE Trans. Smart Grid*, vol. 10, no. 2, pp. 1762–1771, Mar. 2019.
[14] A. Schon and M.-M. Bakran, "A new HVDC-DC converter for the efficient connection of HVDC networks," in *Proc. PCIM Eur. Conf.*, 2013, pp. 525–532.
[15] E. Kontos, H. Papadakis, M. Poikilidis, and P. Bauer, "MMC-based multiport DC hub for multiterminal HVDC grids," in *Proc. PCIM Eur. Conf.*, 2017, pp. 1–8.
[16] A. Schon and M.-M. Bakran, "High power HVDC-DC converters for the interconnection of HVDC lines with different line topologies," in *Proc. Int. Power Electron. Conf.*, May 2014, pp. 3255–3262.
[17] W. Lin, J. Wen, and S. Cheng, "Multiport DC–DC autotransformer for interconnecting multiple high-voltage DC systems at low cost," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6648–6660, Dec. 2015.
[18] F. Alsokhiry and G. P. Adam, "Multi-port DC-DC and DC-AC converters for large-scale integration of renewable power generation," *Sustainability*, vol. 12, no. 20, p. 8440, Oct. 2020.
[19] G. P. Adam, I. Abdelsalam, L. Xu, J. Fletcher, G. Burt, and B. Williams, "Multi-tasking DC–DC and DC–AC converters for DC voltage tapping and power control in highly meshed multi-terminal HVDC networks," *IET Power Electron.*, vol. 10, no. 15, pp. 2217–2228, Dec. 2017.
[20] Y. Li, D. Liu, and G. J. Kish, "Generalized DC-DC-AC MMC structure for MVDC and HVDC applications," in *Proc. 20th Workshop Control Modeling Power Electron. (COMPEL)*, Jun. 2019, pp. 1–8.
[21] S. Cui, J.-H. Lee, J. Hu, R. W. De Doncker, and S.-K. Sul, "A modular multilevel converter with a zigzag transformer for bipolar MVDC distribution systems," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1038–1043, Feb. 2019.
[22] D. Ma, W. Chen, L. Shu, X. Qu, and C. Hu, "A MMC-based multiport AC–N–DC converter for hybrid AC/DC systems," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 12, pp. 3567–3571, Dec. 2021.
[23] S. Wenig, M. Goertz, C. Hirsching, M. Suriyah, and T. Leibfried, "On full-bridge bipolar MMC-HVDC control and protection for transient fault and interaction studies," *IEEE Trans. Power Del.*, vol. 33, no. 6, pp. 2864–2873, Dec. 2018.
[24] S. H. Kung and G. J. Kish, "A modular multilevel HVDC buck–boost converter derived from its switched-mode counterpart," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 82–92, Feb. 2018.
[25] J. A. Ferreira, "The multilevel modular DC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4460–4465, Oct. 2013.
[26] Y. Li and G. J. Kish, "The modular multilevel DC converter with inherent minimization of arm current stresses," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12787–12800, Dec. 2020.
[27] R. Razani and Y. A.-R.-I. Mohamed, "Operation limits of the hybrid DC/DC modular multilevel converter for HVdc grids connections," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4459–4469, Aug. 2021.
[28] W. Lin, D. Jovcic, S. Nguefeu, and H. Saad, "Full-bridge MMC converter optimal design to HVDC operational requirements," *IEEE Trans. Power Del.*, vol. 31, no. 3, pp. 1342–1350, Jun. 2016.
[29] A. Schon and M.-M. Bakran, "A new HVDC-DC converter with inherent fault clearing capability," in *Proc. 15th Eur. Conf. Power Electron. Appl. (EPE)*, Sep. 2013, pp. 1–10.
[30] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge, and R. W. De Doncker, "Comparison of the modular multilevel DC converter and the dual-active bridge converter for power conversion in HVDC and MVDC grids," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 124–137, Jan. 2015.
[31] A. Schon and M.-M. Bakran, "Comparison of modular multilevel converter based HV DC-DC-converters," in *Proc. 18th Eur. Conf. Power Electron. Appl. (EPE ECCE Europe)*, Sep. 2016, pp. 1–10.
[32] Y. Tian, H. R. Wickramasinghe, P. Sun, Z. Li, J. Pou, and G. Konstantinou, "Assessment of low-loss configurations for efficiency improvement in hybrid modular multilevel converters," *IEEE Access*, vol. 9, pp. 158155–158166, 2021.
[33] F. Zhang, W. Li, and G. Joos, "A transformerless hybrid modular multilevel DC–DC converter with DC fault ride-through capability," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2217–2226, Mar. 2019.
[34] J. Peralta, H. Saad, S. Dennetiere, J. Mahseredjian, and S. Nguefeu, "Detailed and averaged models for a 401-level MMC–HVDC system," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1501–1508, Jul. 2012.
[35] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, and T. U. Jonsson, "VSC-HVDC transmission with cascaded two-level converters," in *Proc. CIGRE Paris Session*, 2010, pp. B4–B110.
[36] M. Zygmanowski, B. Grzesik, and R. Nalepa, "Capacitance and inductance selection of the modular multilevel converter," in *Proc. 15th Eur. Conf. Power Electron. Appl. (EPE)*, Sep. 2013, pp. 1–10.
[37] Mitsubishi. *HVIGBT Modules CM1200HC-90R*. Accessed: Aug. 27, 2020. [Online]. Available: http://www.mitsubishielectric.com/semiconductors/

YUAN LI (Student Member, IEEE) received the B.Eng. degree in electrical engineering from the University of Liverpool, Liverpool, U.K., in 2016, and the M.Sc. degree in future power networks from the Imperial College London, London, U.K., in 2017. He is currently pursuing the Ph.D. degree in electrical engineering with the University of Alberta, Edmonton, AB, Canada. His research interests include modular multilevel converter topologies for hybrid ac/dc grids and sustainable energy systems.

GREGORY J. KISH (Senior Member, IEEE) received the B.E.Sc. degree in electrical engineering from the University of Western Ontario, London, ON, Canada, in 2009, and the M.A.Sc. and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, ON, in 2011 and 2016, respectively. He is currently an Associate Professor with the University of Alberta, Edmonton, AB, Canada. His research interest includes the development and application of converter systems in electric grids. He was a recipient of the First Place Prize Paper Award for 2016 by IEEE TRANSACTIONS ON POWER ELECTRONICS.