A 5–11 GHz 8-bit Precision Passive True-Time Delay in 65-nm CMOS Technology

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ABSTRACT In this paper, we present an 8-bit precision passive true-time delay (TTD) operating at 5–11 GHz in 65-nm CMOS technology. To achieve a precision time delay control, the 8-bit TTD employs a 4-bit time delay circuitry that utilizes two LC delay networks in parallel to reduce the effects of the nonideal lumped components and layout imbalance of a conventional TTD. To design an 8-bit TTD, a 4-bit TTD with conventional LC networks was also used for the 5th bit to the 8th bit (MSB) time-delay for coarse delay control. The implemented 8-bit TTD circuit achieved a minimum delay of 1.56 ps and a maximum delay of 400 ps, demonstrating the smallest loss per delay among the recently reported state-of-the-art silicon-based TTDs without dissipating any DC power and with a chip area of 2.76×1.01 mm^2.

INDEX TERMS CMOS, phased arrays, phase shifters, true-time delay.

I. INTRODUCTION

Recently, phased array antenna systems have been widely applied in modern radar and wireless communication systems owing to the development of cost-effective electrically controllable beam-steering devices with the advancement of semiconductor technology. The widely utilized beam-steering devices for analog and hybrid phased array systems are the phase shifter and true-time delay (TTD) [1]–[7].

A phase shifter is a device that generates a desired phase change at the operating frequency. Phase shifters are mainly categorized into quadrature phase shifters [8], [9], vector phase shifters [10], [11], and high/low-pass filter (HPF/LPF) phase shifters [12]–[15]. As illustrated in Fig. 1(a) and (b), the beam steering of a phased array antenna with a phase shifter or TTD is achieved by shifting the phase of the signal of each antenna element consecutively so that the synthesized phase front can be formed in the designated direction. The disadvantage of using a phase shifter is the beam squint phenomenon for a wideband signal [15]. A beam squint is caused by the mismatch between the expected phase from the required delay time (τ) and the assigned phase from the phase shifter at the working frequency because the equivalent phase for a given τ is a direct function of the working frequency.

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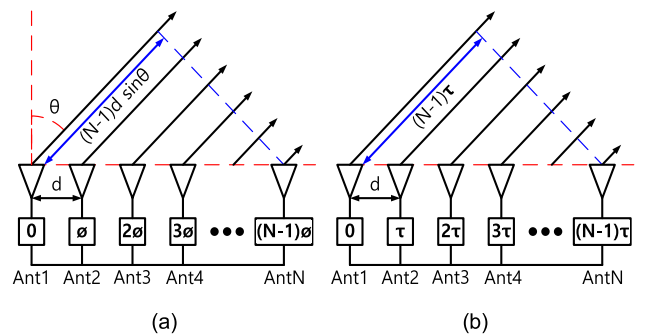

FIGURE 1. Basic concept of phased array system (a) with a phase shifter (b) with a time-delay.

The required delay time ($\Delta\tau$) and the corresponding phase step ($\Delta\phi$) for each unit antenna is given by

$$\Delta\tau = \frac{d}{c}\sin(\theta),$$
$$\Delta\phi = \omega\Delta\tau = 2\pi f \cdot \frac{d\sin(\theta)}{c} = kd\sin(\theta), \quad (1)$$

where c is the speed of light, d is the distance between each antenna unit, θ is the scanning angle of the main beam, and $k = \omega/c$ is the wavenumber.

From (1), the effective delay time varies with the operating frequency for a phase shifter with a fixed phase step using

a conventional phase shifter and, thus, results in the beam squint phenomenon for a wideband signal [15]. Therefore, it is essential to develop a precision TTD for broadband phased array antenna systems for use in advanced radar systems and next-generation ultrafast wireless communication systems.

In a TTD, a delay is determined by the physical length of a transmission line (T-line) divided by the phase velocity of the delivered signal. Considering the unacceptable length of a real T-line in achieving the required delay time, an artificial T-line is employed by constructing a cascaded *LC* network of lumped inductors and capacitors [1], [6], [7]. However, due to the self-resonance frequency (SRF) of the capacitors and inductors used in an artificial T-line, the effective value of the passive components can significantly change when the working frequency is close to the self-resonance frequency (SRF). As a result, a serious error occurs in the time delay around the SRF. To mitigate this issue, a trombone structure or changeable g_m structure has been introduced, but it consumes DC power [2], [4], [5]. Moreover, it is quite difficult to achieve a precision TTD with a minimum delay time of less than 2 psec without using a varactor because the parasitics in the conventional *LC* delay cell may limit the controllable delay time [16].

To address this problem, we introduce a precision time delay cell with less variation in the delay time and insertion loss over a wide bandwidth by controlling the group delay of the artificial T-lines for both the delay and reference path to achieve fine control of the delay time. We design an 8-bit precision TTD by utilizing the proposed delay cell as a fine control together with the conventional one which is composed of the cascaded *LC* networks for a coarse control. The implemented whole 8-bit TTD achieves a maximum delay of 400 ps and an LSB of 1.56 ps with an 8-bit control, which is equivalent to a phase shift of 1440° in steps of 5.625° at 10 GHz.

This paper is organized as follows. We present a new precision time delay structure in Section II. Section III describes the detailed designs of the core blocks that include the precise delay cells for the fine control of the delay time, SPDT and DPDT switches, and conventional delay cells for coarse delay control. The measurements of the implemented chip are presented in Section IV followed by the conclusion in Section V.

II. PROPOSED ARCHITECTURE

When a delay is implemented through an actual T-line, a large area is required for the expected delay time control configuration. In this paper, instead, a π-type *LC* network is constructed with a series *L* and two shunt *C*/2 at each side of the *L*. Each π-type *LC* network provides a delay time $t_D = 1/\sqrt{LC}$ with the pole frequency at $f_C = 1/\pi\sqrt{LC}$. The value of the inductor and capacitors of this structure is
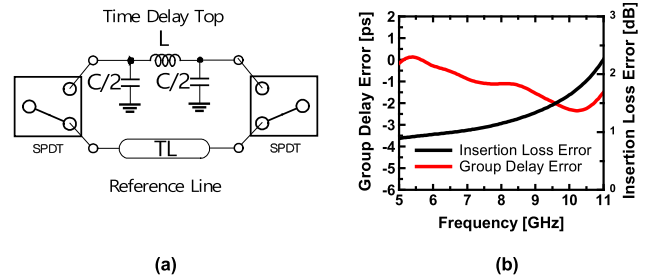

FIGURE 2. (a) Schematic diagram of the conventional delay element with a single π-section. (b) Group delay error and insertion loss error over frequency.
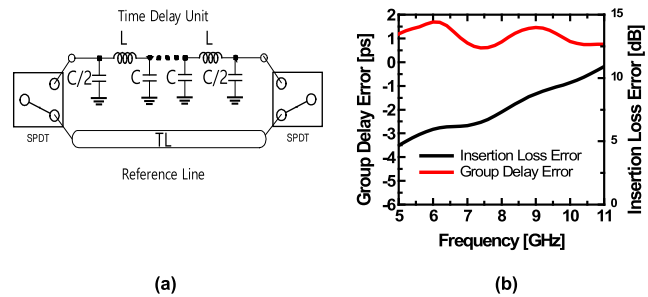

FIGURE 3. (a) Schematic diagram of the conventional delay element with cascaded multiple π-sections. (b) Group delay error and insertion loss error over frequency.
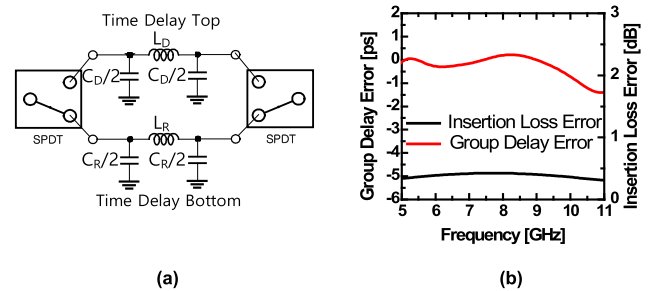

FIGURE 4. (a) Schematic diagram of the proposed delay element with the π-sections both at the delay and reference path. (b) Group delay error and insertion loss error over frequency.

calculated by [15]

$$L = -\frac{Z_0 \sin(\Delta\varphi/2)}{\omega}, \qquad (2)$$

$$C = -\frac{\tan(\Delta\varphi/4)}{\omega Z_0}, \qquad (3)$$

where $\Delta\varphi = \omega_0 t_D$ is the phase shift from the desired delay time T_D at the center frequency ($\omega_0/2\pi$). The characteristic impedance of the artificial T-line is given by $Z_0 = \sqrt{L/C}$.

To achieve a longer delay time T_D, the artificial T-line can be extended by cascading n number of π-type *LC* networks.

Then, the expected T_D is given by

$$T_D = n\sqrt{LC}. \qquad (4)$$

It should be noted that the maximum operating frequency must be below the pole frequency (f_c) of the unit delay

section. To increase the working frequency, the number of the π-section should be increased by n after scaling down each L and C by $1/n$ for the same delay time t_D. In this case, the expected time delay of the n-cascaded LC network is expressed as

$$f_c = \frac{1}{\pi\sqrt{\frac{L}{n}\cdot\frac{C}{n}}} = \frac{n}{\pi\sqrt{LC}}. \tag{5}$$

Hence, the size limitation of L and C necessitates a large number of cascaded π-sections to achieve the desired delay time T_D. When a single π-section is used for a relatively large T_D, the SRF of the inductor can be very close to the operating frequency, resulting in a drastic change in the reactance value. Moreover, the transfer function characteristic of the second-order Butterworth filter is quite different from that of the real T-line of the group delay because it changes over the frequency. Therefore, the conventional delay element presented in Fig. 2(a) suffers from the group delay error as well as the insertion loss variation over the frequency as presented in Fig. 2(b). The delay time difference in the conventional delay element with a single π-section is expressed as

$$\Delta T_D = \Delta\tau_\pi - \tau_{TL}, \tag{6}$$

where $\Delta\tau_\pi$ is the time delay of the single π-section and τ_{TL} is the delay time from the real T-line used in the conventional delay element.

To avoid the adverse effect of using a relatively large L and C in a single π-section design, n-cascaded π-sections can be used as shown in Fig. 3(a). From Fig. 3(b), we can observe that the group delay error is noticeably reduced while the insertion-loss variation and its absolute loss difference between the delay and reference path are remarkably increased. To minimize the group delay and insertion loss errors in the conventional delay elements, a new delay element is proposed that consists of two π-sections for both the delay ($\Delta\tau_{\pi D}$) and reference path ($\Delta\tau_{\pi R}$), as illustrated in Fig. 4(a). Then, the delay time difference between the two delay elements using the single π-section is given by

$$\Delta T_D = \Delta\tau_{\pi D} - \Delta\tau_{\pi R}. \tag{7}$$

Because both the delay and reference path utilize the π-section, the variation in the group delay and insertion loss can be significantly reduced over the frequency for a given ΔT_D as presented in Fig. 4(b). In addition, the impedance difference can be carefully adjusted to minimize the insertion loss of the delay and reference artificial T-lines.

The transfer function of the single π-type CLC network (in the red rectangle) in Fig. 5 is given by

$$H(s) = \frac{R}{s^3LC^2R + s^2LC + 2sRC + 1}. \tag{8}$$

The phase of the π-type network is expressed as

$$\angle H = \tan^{-1}\left(\frac{2\omega R(C_1) - \omega^3 LC_1^2 R}{1 - \omega^2 LC_1}\right). \tag{9}$$
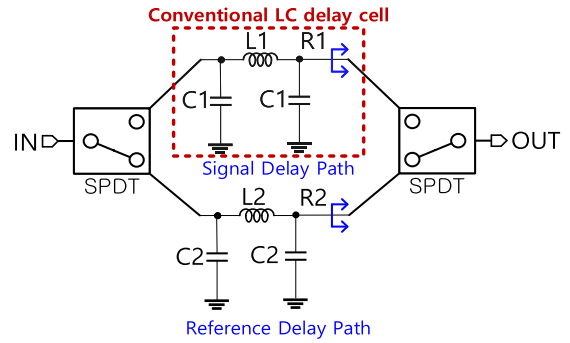

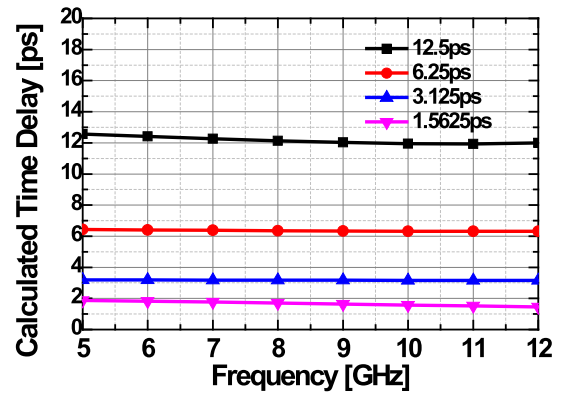**FIGURE 5. Schematic of the proposed precision time delay.**

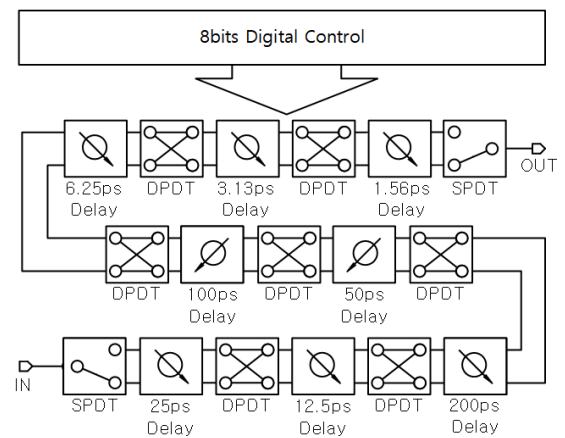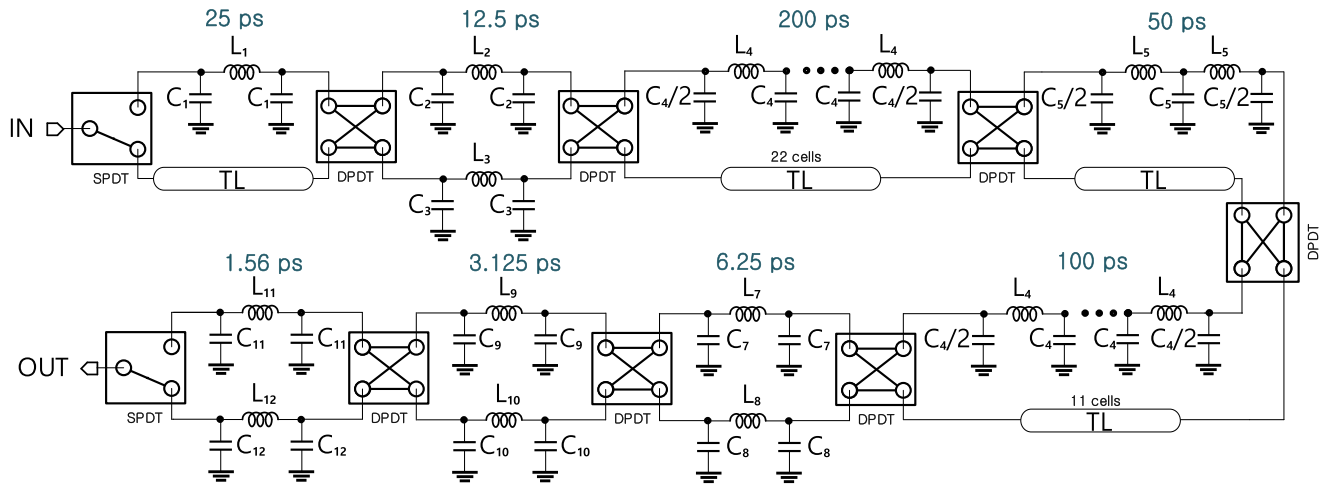**FIGURE 6. Calculated time delay over the operating frequency.**

FIGURE 7. Block diagram of the proposed 8-bit precision true-time delay (TTD).

Hence, the phase difference between the leading and lagging delay line in Fig. 5 is expressed as

$$\Delta\phi = \angle H_{leading} - \angle H_{lagging}$$
$$= \tan^{-1}\left(\frac{2\omega R_1(C_1) - \omega^3 L_1 C_1^2 R_1}{1 - \omega^2 L_1 C_1}\right)$$
$$- \tan^{-1}\left(\frac{2\omega R_2(C_2) - \omega^3 L_2 C_2^2 R_2}{1 - \omega^2 L_2 C_2}\right) \tag{10}$$

FIGURE 8. Schematic of the proposed 8-bit true time delay (TTD) circuit.

By using equation (10), we can derive the precise time delay of the single π-section ($\Delta\tau_\pi$) as

$$\Delta\tau = \frac{\Delta\phi}{\omega}$$

$$= \frac{\left[\tan^{-1}\left(\dfrac{2\omega R_1(C_1) - \omega^3 L_1 C_1^2 R_1}{1 - \omega^2 L_1 C_1}\right) - \tan^{-1}\left(\dfrac{2\omega R_2(C_2) - \omega^3 L_2 C_2^2 R_2}{1 - \omega^2 L_2 C_2}\right) \right]}{\omega} \quad (11)$$

The calculated time delay of each element using the proposed architecture is presented in Fig. 6. By controlling the L and C values in the delay and reference path, the delay variation can be significantly reduced.

III. WIDEBAND 8-BIT TRUE-TIME DELAY DESIGN

Fig. 7 presents a block diagram of the proposed 8-bit TTD. The delay cells from 1.56 ps to 12.5 ps of delay time utilize artificial T-lines at both sides of the delay and reference paths, and for the delay cells from 50 ps to 200 ps, a typical true-time delay with an artificial T-line structure with *LC* networks is adopted. The schematic diagram of the designed 8-bit TTD is presented in Fig. 8. The proposed TTD architecture was used for the delay elements up to the 12.5 ps delay cell. A conventional π-type delay cell for the delay path combined with
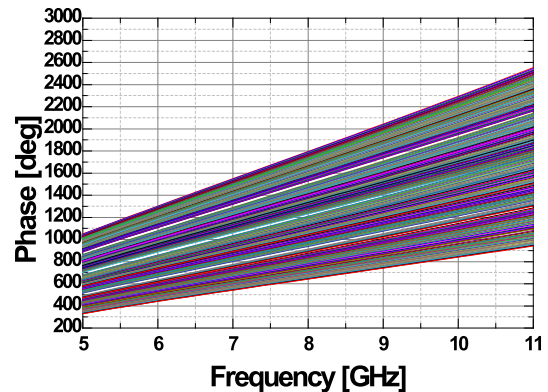

FIGURE 9. Simulated phase shift levels in all phase states.

a short T-line for the reference path was used for the 25 ps delay cell. Two 25 ps delay cells were cascaded to achieve the 50 ps delay cell. For the 100 ps and 200 ps delay cells, multiple π-type *LC* networks were cascaded so that the SRF of the required inductors is much higher than the working frequency. Additionally, the characteristic impedance of 75 Ω was used for the reduced insertion loss. To minimize insertion loss variation and group delay error, a 50-75-50 Ω matching network was applied to the reference line.

Fig. 9 shows the results of a phase simulation that increases linearly with the frequency of the time delay circuit, and the
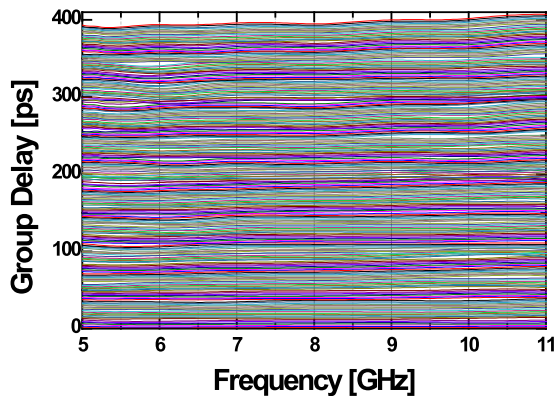
Device parameters

L_1	L_2	L_3	L_4	L_5	L_6	L_7	L_8	L_9	L_{10}	L_{11}	L_{12}
900pH	600pH	130pH	200pH	900pH	200pH	510pH	250pH	300pH	110pH	300pH	300pH
C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}
296fF	263fF	100fF	296fF	400fF	400fF	111fF	42fF	51fF	25fF	136fF	102fF

FIGURE 10. Simulated relative delay results in all time delay states.

FIGURE 12. Chip-photograph of the fabricated 5-11 GHz 8-bit true-time delay (TTD) in 65-nm CMOS technology.

results of all relative delay states are presented in Fig. 10. A low-loss switching mechanism is required to perform the time-delay-shifting function with a coverage of 400 ps in steps of 1.41 ps. The SPDT and DPDT switches configure the path through the time delay elements to produce the desired time delay. The true-time delay employs two SPDT (single pole double throw) switches and seven DPDT (double pole double throw) switches to control corresponding delay cells as shown in Fig. 11 [14]. For the SPDT switch, the series transistor (M_1) performs the primary switching function, and shunt transistors (M_2) are added to improve the isolation between the different paths. When designing the SPDT and DPDT switches, the gate terminals are biased through a large resistor R_G to reduce the fluctuations in V_{GS} and V_{GD} due to voltage swings at the drain and source. This R_G maintains the on-resistance of the transistors unchanged and avoids excessive voltage across the gate dielectric that causes breakdown.

< True Time Delay Measurement >

FIGURE 13. The measurement setup for the S-parameters, phase shift, and time delay over the frequency.

FIGURE 11. Schematic and all device parameters of the SPDT (left) and DPDT (right) switches [14].
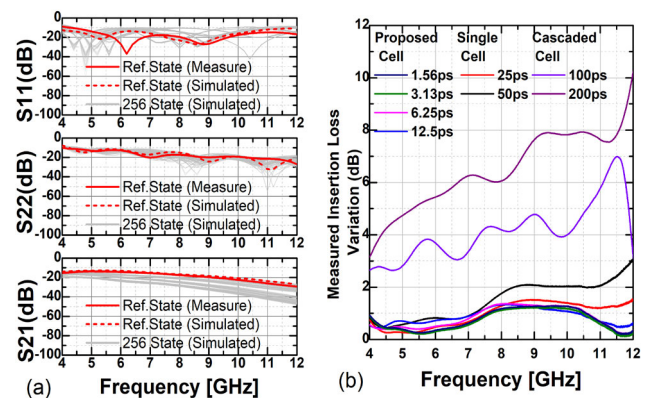

FIGURE 14. Simulated and measured results for the (a) S_{11}, S_{22}, and $S21$ and (b) the insertion loss variation of the true-time delay circuit based on 256 different group-delay states.

IV. MEASUREMENT RESULTS

The designed 8-bit precision true-time delay (TTD) was fabricated in 65-nm CMOS technology. A chip photograph is presented in Fig. 12. The chip size of the fabricated 8-bit

TTD is 2.76×1.01 mm^2 including the RF and DC pads. The implemented 8-bit TTD chip was characterized using on-chip probing with a Keysight N5224A network analyzer as illustrated in Fig. 13. A 64-bit serial peripheral interface (SPI) scan chain was integrated for the digital control of each delay unit.

The measured S11, S22, S21, and insertion loss variation in all the delay states are presented in Fig. 14. The input and output return loss from 5 GHz to 11 GHz was better than 10 dB. Comparing the insertion loss variation of the delay cell with the conventional one in Fig. 3(a) with that of the proposed structure in Fig. 4(a), the relative variation is reduced from 8 dB to 1 dB over the operating band. Specifically, the reduction in variation of the proposed TTD is more distinctive

TABLE 1. Comparison with previously reported True-Time Delay circuits.

| Ref.	This work	[1]	[2]	[3]	[4]	[5]	[6]	[7]
Tech	65nm CMOS	65nm CMOS	130nm CMOS	250nm SiGe	130nm CMOS	250nm SiGe	180nm CMOS	28nm CMOS
Structure	TTD (Low Pass LC in parallel)	TTD (LC+T-line)	TTD (trombone)	TTD (LC w/ varactor)	TTD (trombone)	TTD (LC w/ varactor+ Gm-RC)	TTD (Low Pass LC)	TTD (All Pass LC)
f_{RF} [GHz]	5-11	20-30	1-20	10-50	15-40	20-40	5-20	3-30
Maximum Delay[ps]	400	35.2	400	32.8	42	12.5	106	68.5
Resolution	1.54ps	0.56ps	5ps	cont	5.2ps	cont	3.3ps	4.9ps
Maximum Loss[dB]	41	12.3	45	25	14	-	38	13.5
Loss/Delay [dB/ps]	0.103	0.35	0.113	0.76	0.33	-	0.36	0.2
Delay/size [ps/ mm²]	137 163(Core)	196(Core)	100	149(Core)	42	125(Core)	120	201(Core)
IP1dB (dBm)	11.2	6.5	2.5	15.5	8-10	18/13	-	6.2
DC power [mW]	passive	passive	2.6-6	passive	8.6-24.6	33	passive	passive
Chip area [mm²]	2.91 / 2.46(core)	0.18(core)	4	0.22(core)	0.99	0.1(core)	0.88	0.34(core)
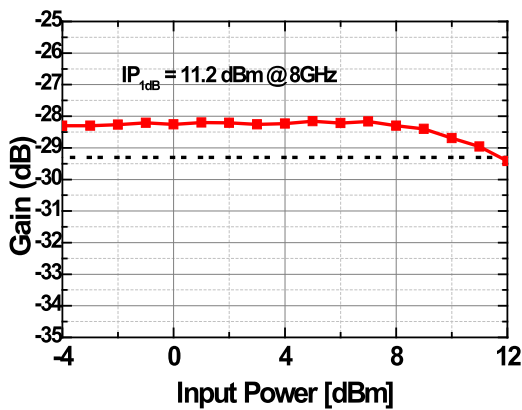
FIGURE 15. Measurement gain compression curve with the largest delay state at 8 GHz.

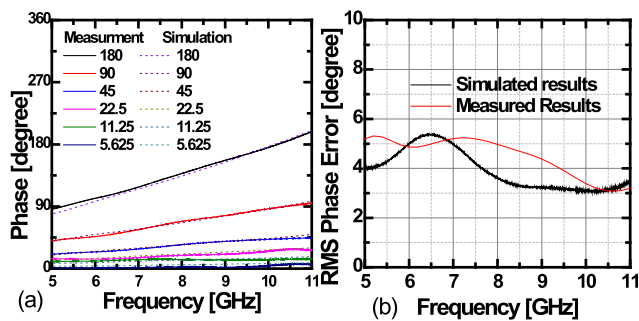**FIGURE 16.** Simulated and measured results of the (a) phase for the main phase states and (b) the RMS phase error over the frequency.

FIGURE 17. (a) Measured group delay of the main delay states, and (b) Simulated and measured results of the RMS group delay error over frequency.

as the operating frequency increases. Fig. 15 presents the gain compression of the implemented 8-bit TTD with the largest delay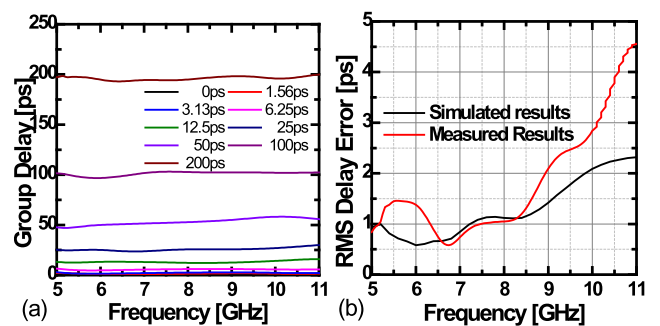 state at 8GHz. The measured input 1-dB compression point (IP1dB) was 11.2 dBm. Fig. 16 shows the simulated and measured results for the phase and RMS phase errors within a phase-shifting range of 360° with only the first 6-bit controls. The measured phase values corresponded well with the simulation over the working band. The RMS phase error was less than 5.2° within the working band.

Fig. 17 shows the measured group delay concerning the reference state and the simulated and measured results of the RMS group delay error over the operating frequency. Operating as the time delay block, the phase of each state increases linearly with frequency. The RMS delay error was less than 4.5 ps within the working band. The delay range was up to 400 ps, and the difference from the simulation result was approximately 2%.

Table 1 compares the implemented true-time delay with those of recently published CMOS and SiGe-based active as well as passive TTD chips. By reducing insertion loss and delay variation with the proposed architecture, the

implemented 8-bit passive TTD achieved the smallest loss per delay with a comparable overall performance among the recently reported silicon-based TTD chips without any DC power dissipations.

V. CONCLUSION

In this paper, we introduce a precision 8-bit true-time delay (TDD) for a wideband phased array antenna system in 65-nm CMOS technology. The presented 8-bit TTD utilizes two *LC* delay networks in parallel to achieve precision time control that can efficiently reduce the variations in the insertion loss and time delay. The implemented 5–11 GHz passive 8-bit TTD demonstrates an outstanding overall performance with the smallest loss per delay compared with recently reported state-of-the-art TTDs without any DC power dissipation.

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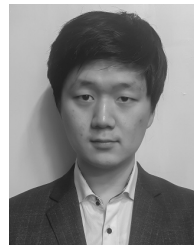
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JUNG-DONG PARK (Senior Member, IEEE) received the B.S. degree from Dongguk University, Seoul, South Korea, in 1998, the M.S. degree from the Gwangju Institute of Science and Technology (GIST), Gwangju, South Korea, in 2000, and the Ph.D. degree in EECS from the University of California at Berkeley, Berkeley, in 2012. From 2000 to 2002, he worked with the Institute for Advanced Engineering (IAE), Yongin, South Korea, where he was involved with the design of 35-GHz radar/radiometer transceivers. From 2002 to 2007, he was a Senior Researcher with the Agency for Defense Development (ADD), Daejeon, South Korea, where he was responsible for the development of millimeter-wave (mmW) passive/active sensors and related mmW modules. From 2007 to 2012, he was with the Berkeley Wireless Research Center (BWRC), where he worked on silicon-based RF/millimeter-wave/terahertz circuits and systems. From 2012 to 2015, he worked at Qualcomm Inc., San Jose, CA, USA, where he designed various RF/analog integrated circuits. He is currently an Associate Professor with the Division of Electronics and Electrical Engineering, Dongguk University. His research interests include wireless communications, remote sensors, microwave electronics, analog, RF, mixed-signal, and millimeter-wave circuits. He was a recipient of the 2017 Most Frequently Cited Papers Award as a Lead Author at the 2017 IEEE Symposium on VLSI Circuits, in Kyoto, from 2010 to 2016.

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