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Assessing the Figures of Merit of Graphene-Based Radio Frequency Electronics: A Review of GFET in RF Technology

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ABSTRACT Graphene has been extensively investigated in the context of electronic components due to its attractive properties, such as high carrier mobility and saturation velocity. In the past decade, the graphene field-effect transistor (GFET) has been considered one of the potential devices to be used in future radio frequency (RF) applications and can help usher in the Internet of Things and the 5G communication network. This review presents recent developments of GFETs in RF applications with a focus on components such as amplifiers, frequency multipliers, phase shifters, mixers, and oscillators. Initially, the figures of merit (FoMs) for the GFET are briefly described to understand how they affect these RF components. Subsequently, the FoMs of GFET-based RF components are compared with other non-GFET-based RF components. It is found that, due to its zero-band gap and ambipolar characteristics, GFETs are more suitable for use in frequency multiplier and phase shifter applications, outperforming non-GFET-based RF components. Finally, future research on GFETs themselves as well as GFET-based RF components is recommended. This review provides valuable insights into such components that could give rise to innovative applications in industry.

INDEX TERMS Field-effect transistors, figure of merit, GFET, radio frequency.

I. INTRODUCTION

Radio frequency (RF) applications typically require electronic devices to operate in the electromagnetic spectrum, with frequencies varying from 3 kHz to 300 GHz. There is a myriad of emerging RF applications thanks to the recent drive in the communications industry to usher in the Internet of Things and to transit from 4G to 5G telecommunication standards set by the International Communication Union. Although the RF spectrum covers a wide frequency range, the usable spectrum is typically limited, mainly due to technology constraints as well as federal regulations. For example, 5G communication networks typically require operational frequencies of 700 MHz, 3.50 GHz, and 28.00 GHz. Therefore, innovation in miniaturized electronic devices operating at such frequencies is necessary. Starting with the introduction of the GaAs metal-semiconductor field-effect transistor (MESFET) in the 1970s, the RF transistor modernized with the evolution of the III-V high electron mobility transistor (HEMT) in the 1980s, followed by Si bipolar and SiGe bipolar complementary metal-oxide-semiconductors (BiCMOSs) in the 1990s, planar CMOS and GaN HEMTs in the 2000s, and the non-planar metal-oxide-semiconductor field-effect transistor (MOSFET) in 2011 [1], [2]. The keys to the successful evolution of RF transistors are the choice of semiconductor materials and the miniaturization of such devices [2], [3].

For high frequency RF applications, semiconductor materials with high carrier mobility are preferred [1]. So far, III-V-based and Si-based bulk materials have dominated the field. GaAs, InP, and GaN, for example, have electron mobilities of 8500, 4600, and 2000 cm^2/Vs, respectively. Si and SiGe, on the other hand, have electron mobilities between 1450 and 3900 cm^2/Vs. These carrier mobilities as well

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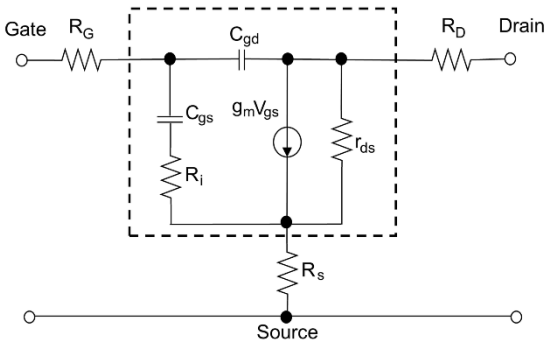

FIGURE 1. Schematic illustration of the small-signal equivalent circuit of a FET [3].

as other parameters such as carrier drift velocity, thermal resistance, and energy band gap determine the intrinsic characteristics of the RF components, i.e., speed, operating voltage, and power handling capability [4]. The dominance of such materials was challenged in 2004 with the discovery of graphene. Graphene is essentially a single layer of carbon atoms and exhibits an ultrahigh carrier mobility above 15,000 cm^2/Vs [3]. The outstanding carrier mobility together with its other unique properties make graphene an excellent material for transistors. Many excellent reviews have summarized the progress of graphene field-effect transistors (GFETs), including material synthesis, material characterization, device fabrication, and characterization, as well as various GFET-based applications [5]–[9]. One of the best properties of a GFET is its ambipolar characteristics, and it is best used in RF components [10]–[13]. To date, several GFET-based RF components have been demonstrated, such as oscillators [14]–[20], phase shifters [21], [22], amplifiers [23]–[26], mixers [27]–[31], and frequency multipliers [32], [33]. A GFET in RF was first demonstrated in 2008 [34], and since then, its performance has gradually improved. However, performance is limited by issues such as low surface quality of graphene [35], insufficient drain current saturation, and low cutoff frequency (f_T) [36]. Hence, for GFETs to gain acceptance in RF design communities, these issues need to be addressed.

This review aims to provide an overview of the current state of GFET-based RF components. The first part of this review focuses on RF performance of GFETs, and its FoMs are discussed. The second part highlights the performance of GFET-based RF components. Herein, its FoMs are systematically defined, evaluated, and assessed. Then, the FoMs are compared with other available non-GFET-based RF components. Furthermore, the limitations of GFET-based RF components and solutions to improve them are discussed. Finally, the paper concludes with an outlook on the future enhancement that can be done to best utilize the GFET in RF components.

II. FIGURES OF MERIT FOR GFET

Figures of merit (FoMs) are commonly used to evaluate the performance of transistors in RF components. They help in estimating the limits of performance of transistors, which is essential in selecting the RF band of operation [21]. For GFETs in RF components, the two most widely used FoMs are the cutoff frequency, f_T, and the maximum oscillation frequency, f_{max}. The f_T is defined as the frequency at which the magnitude of the current gain becomes unity (0 dB), while f_{max} is defined as the frequency at which unilateral power gain becomes unity (0 dB) [3]. The expressions can be extracted from the hybrid-π model that make use of a small-signal equivalent circuit as shown in Figure 1 [3] and are given as follows in Equations (1) and (2) [37], [38]:

$$f_T = \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)\left(1+R_c g_{ds}+\frac{C_{gd}g_m R_c}{C_{gd}+C_{gs}}+\frac{C_{pg}}{C_{gd}+C_{gs}}\right)} \tag{1}$$

$$f_{max} = \frac{g_m}{4\pi C_{gs}\sqrt{g_{ds}\left(R_i+R_s+R_G\right)+g_m R_G\frac{C_{gd}}{C_{gs}}}} \tag{2}$$

where $g_{ds} = 1/r_{ds}$ is the intrinsic differential-drain conductance, g_m represents the intrinsic transconductance, r_{ds} is the differential drain resistance, C_{gs} is the gate-source capacitance, C_{gd} is the gate-drain capacitance, and C_{pg} is the external parasitic capacitance. Next, R_G, R_s, R_D, and R_i are the gate resistance, source series resistance, drain series resistance, and charging resistance of the gate-source capacitance, respectively.

For transistors to be useful in RF components, high f_T and f_{max} are needed [3], [36]. To make this possible, g_m should be high in value, while the other elements of the equivalent circuit should have small values. The f_T and f_{max} of GFETs have been investigated and compared with other transistors such as InP HEMT, GaAs metamorphic high electron mobility transistor (mHEMT), GaAs pseudomorphic high electron mobility transistor (pHEMT), Si MOSFET, and carbon nanotube field-effect transistor (CNTFET). The comparisons were published previously by Schwierz [3] and are shown with permission in Figure 2. As can be seen from the figure, GFETs show a remarkable f_T, with the highest reported to be 427 GHz, which fares extremely well with InP HEMTs and GaAs mHEMTs. However, compared to the other competing transistors, GFETs behave poorly in terms of f_{max}, where the highest f_{max} reported is in the range of 30.00–45.00 GHz only. The substantially lower f_{max} is reportedly due to the large g_{ds} that is caused by the combination of low saturation current and high source-drain series resistance of GFETs. These issues arise because graphene has zero bandgap characteristics [3]. Nevertheless, even with much lower f_{max}, by taking advantage of the graphene's ambipolar conduction, frequency multipliers and oscillators have been successfully demonstrated, proving that GFETs are also suitable for use as the transistor in RF components [18], [32], [33].

III. GFET-BASED RF COMPONENTS

The GFET was first introduced as an RF transistor in 2008 by Metric and his group [39]. They demonstrated a top-gated GFET with an f_T over 14.70 GHz. Over the years, the

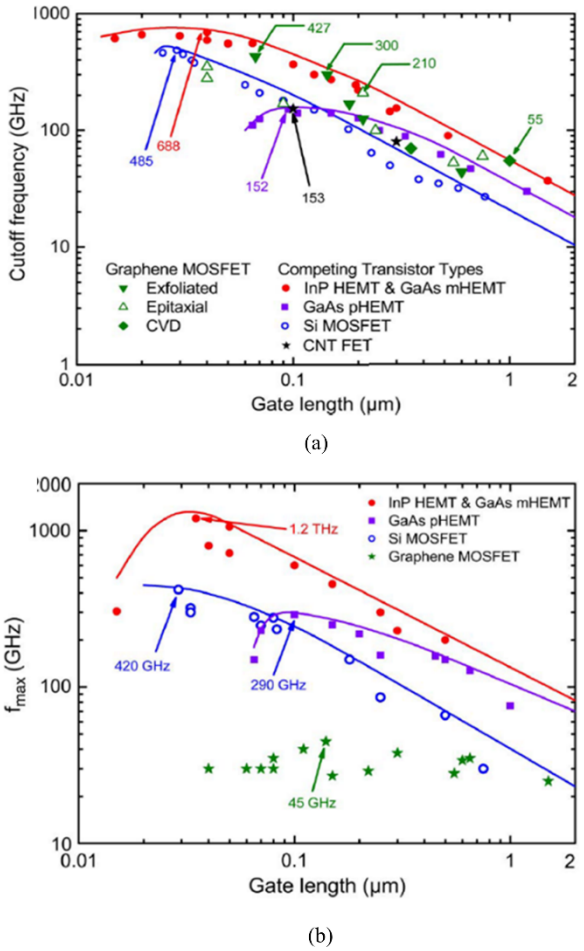

FIGURE 2. (a) Cutoff frequency, f_t and (b) maximum oscillation frequency, f_{max}, versus gate length performance of RF transistors [3].

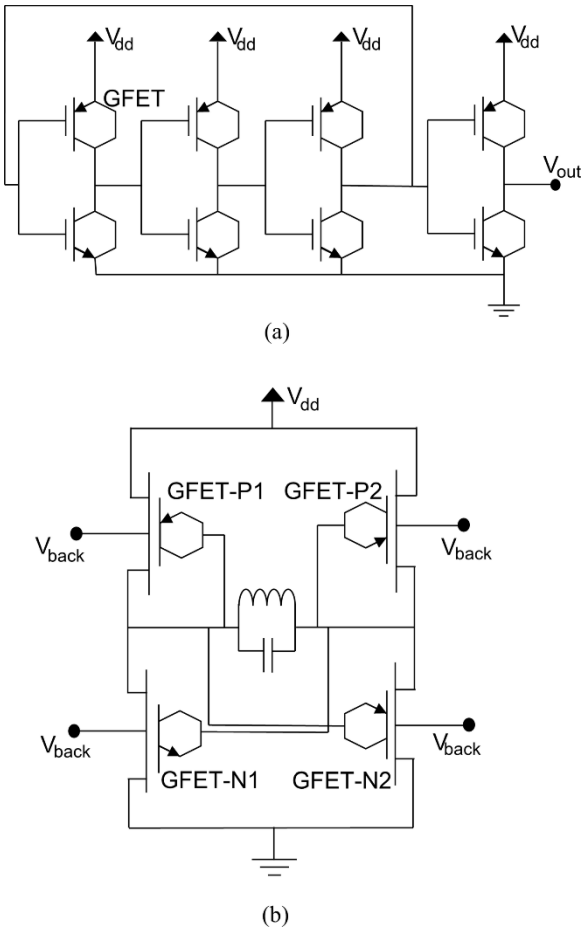

FIGURE 3. Schematic of GFET-based oscillators: (a) LC oscillator; (b) RO oscillator [14], [19].

evolution of GFETs for RF transistors has continued, with researchers striving for improvement in f_T. Remarkably, in 2012, Chuan and his group successfully demonstrated a GFET with an f_T as high as 427.00 GHz, which was achieved by fabricating a GFET with transferred gate stacks [40]. This achievement makes the GFET a promising RF transistor for further development of RF components. In the following few sections, the recent developments of various GFET-based RF components are presented. In order to comprehensively assess their performance, the performance metrics of GFET-based RF components are considered and then compared with the earlier published RF components.

A. OSCILLATORS

Oscillators are used in electronic devices to produce a periodic oscillating signal. Recently, a GFET-based oscillator was developed in 2019 by Gilardi and his research group [18]. The oscillator is realized by integrating a top-gated GFET with an Si CMOS D latch and timing RC circuit. It has an oscillation frequency, f_o, in the range of 4.00 kHz to 4.00 MHz. To the best of our knowledge, it is the first oscillator that can be operated as a voltage-controlled oscillator (VCO) as well as a pulse-width modulator (PWM). Moreover, other types of oscillators based on GFET have also been introduced, namely ring oscillators [14]–[17], and LC oscillators [19], [20].

The ring oscillator was first introduced in 2013 using a top-gated GFET structure [15], and within the same year, the second one was developed using a back-gated structure [16]. The latest ring oscillator based on GFETs was presented in 2020 by Safari and Dousti [14]. Their study simulated a ring oscillator based on a monolayer GFET to study the effect of channel length, L_{ch}, variations on the performance of the oscillator. The ring oscillator is designed by cascading an odd number of GFET inverters, as shown in Figure 3a. The design satisfied the Barkhausen's criterion, which is the criteria needed in designing an oscillator. For evaluating the performance of the recently developed oscillator, a common FoM as in Equation (3) was used [41].

$$FoM = L_N.\Delta f - 20log\frac{f_O}{\Delta f} + 10log\frac{P_{diss}}{1mW} \quad (3)$$

where $L_N \cdot \Delta f$ is the phase noise at the frequency offset, P_{diss} is the power dissipation, and L_N is the phase noise. The performance of the GFET-based oscillators is tabulated in Table 1. As a reference, performances of other available ring oscillators are also included.

TABLE 1. Performance comparison of the ring oscillators.

Techno -logy	L_{ch} (μm)	f_0 (GHz)	P_{diss} (mW)	$L_N.\Delta f$ (dBc/Hz)	FoM (dBc/Hz)	Ref.
GFET	0.18	24.12	9.98	-104.10 @ 0.1 MHz	-201.80	[14]
GFET	2.00	2.25	1.90	-121.40 @ 1 MHz	-185.60	[14]
GaAs FET/ BJT	-	1.46	5.30	-146.00 @ 0.1 MHz	-212.00	[41]
180-nm CMOS	-	2.40	1.09	-141.00 @ 1 MHz	-208.20	[42]
180-nm CMOS	-	1.60	7.30	-99.00 @ 1 MHz	-154.40	[43]
SiGe HBT	-	2.50	3.30	-80.00 @ 1 MHz	-142.80	[44]

The GFET-based ring oscillator with $L_{ch} = 0.18\ \mu$m has more power dissipation but higher oscillation frequency compared to CMOS, SiGe heterojunction bipolar transistor (HBT), and GaAs FET/BJT. As the L_{ch} increases to 2.00 μm, the oscillation frequency drops from 24.12 GHz to 2.25 GHz, and the power dissipation is reduced from 9.98 mW to 1.90 mW. The results show that the L_{ch} greatly impacts the power dissipation and f_o of a GFET. At the frequency offset of 0.10 MHz, the FoM for the GFET ring oscillator shows a comparable value with the GaAs FET/BJT. However, at a 1.00 MHz offset, the CMOS ring oscillator performs better with a FoM of –208.20 dBc/Hz. Even so, the GFET ring oscillator still outperforms the SiGe HBT with a difference of 42.86 dBc/Hz.

As for the LC oscillator, the component was demonstrated with GFET in 2015 [20]. The proposed GFET-based LC oscillator is designed and simulated using the multi-swarm optimization (MSO) technique. With the MSO, the LC oscillator oscillates at 2.58 GHz. In the following year, another GFET-based LC oscillator was introduced [19]. The LC oscillator was designed with four GFETs, and its structure is shown in Figure 3 (b). It can be operated at 1.8 GHz frequency, with a voltage swing of 1.29 peak-to-peak voltage, $V_{(p-p)}$. The performance summary and comparison of various types of LC oscillators are shown in Table 2. At a 1 MHz offset, the GFET-based LC oscillator has the lowest FoM, while CMOS performs the best. According to [45], the significantly lower FoM is due to the higher power consumption. Hence, it is understandable that the GFET LC oscillator has the lowest FoM as it cannot be turned off due to the graphene characteristic, which has zero bandgap, leading to high power consumption. Despite that, the GFET LC oscillator has a low phase noise level, better than the CMOS, BiCMOS, and GaN HEMT LC oscillators.

B. PHASE SHIFTERS

A phase shifter is used to adjust the transmission phase in RF applications while constantly maintaining its amplitude.

TABLE 2. Performance comparison of the LC oscillators.

Technology	f_0 (GHz)	P_{diss} (mW)	$L_N.\Delta f$ @ 1 MHz (dBc/Hz)	FoM (dBc/Hz)	Ref.
GFET	2.58	11.74	-92.92	-150.40	[20]
180-nm CMOS	2.40	2.86	-124.00	-187.30	[45]
65-nm CMOS	11.58	6.00	-112.62	-198.60	[46]
130-nm CMOS	8.00	6.60	-134.30	-204.00	[47]
130-nm BiCMOS	12.67	17.70	-120.60	-190.00	[48]
500-nm CMOS	1.94	20.00	-153.00	-205.70	[49]
GaN-on- SiC HEMT	7.90	-	-135.00	-213.00	[50]

Conventional phase shifter structures are limited to varactors [51] or transistor-based architectures [52]. These structures were adapted to reduce the complexity of the circuit and achieve an output with high precision. As an alternative, GFET-based phase shifters with the schematic shown in Figure 4 have been demonstrated [21], [22]. For both phase shifters, a pair of bias tees are used to combine the signals and the DC biases. Each bias tee consists of an ideal capacitor, C and an inductor, L to block the DC or AC signal, respectively. The GFET-based phase shifter presented in [21] has also included the input matching networks (IMN) and output matching networks (OMN) in their design. IMN and OMN allow the phase shifter to maximize the power transfer and minimize the signal reflected from the load. The phase shift measurement for the reported GFET-based phase shifters is done by independently tuning the supplied V_{gs} to the GFET. The V_{gs} altered the carrier concentration in the GFET channel causes changes to the quantum capacitance and channel resistance. Consequently, the change affected the phase of the output signal. A phase shifter needs to achieve a large-phase control range with small phase-shift step size, low insertion loss, low power consumption, miniaturized structure, and easier to be controlled [53]. To compare the performance of the phase shifters, FoM as defined in (4) is used [54], [55]. The FoM is defined as a ratio of the maximum relative phase shift, $\Delta\varphi$ over the maximum insertion loss (IL). Several published works on various types of phase shifters design were reviewed and their FoMs are calculated and presented in Table 3.

$$FoM = \frac{\Delta\varphi}{IL} \tag{4}$$

The calculated FoMs have shown that the GFET-based phase shifter has the highest FoM as compared to SiGe HBT, CMOS, and BiCMOS phase shifters. The lower FoM is owing to the low IL value, which is favorable for a high-performance phase shifter [53]. As seen in Table 3, the IL for the GFET-based phase shifter is the lowest compared to other

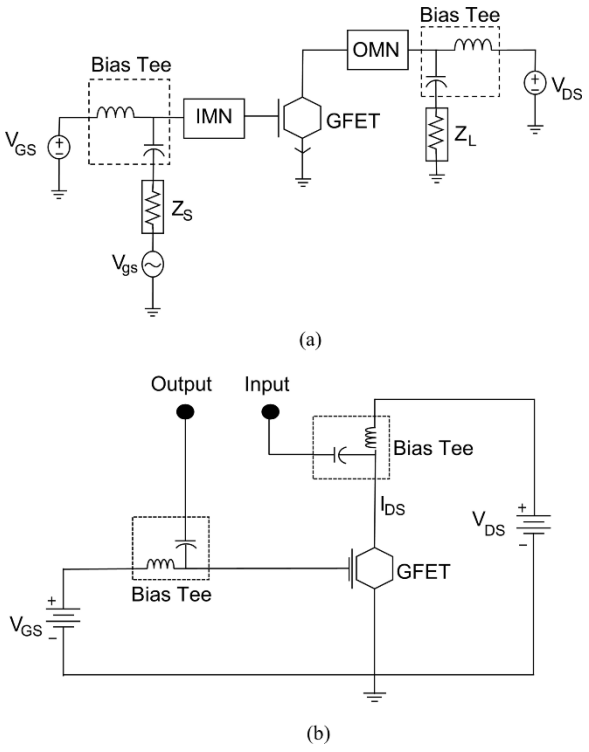

FIGURE 4. Schematic of the GFET-based phase shifters: (a) phase shifter with a GFET having a channel length and width of 1 μm; (b) phase shifter with a GFET having a channel length of 2 μm and width of 50 μm [21], [22].

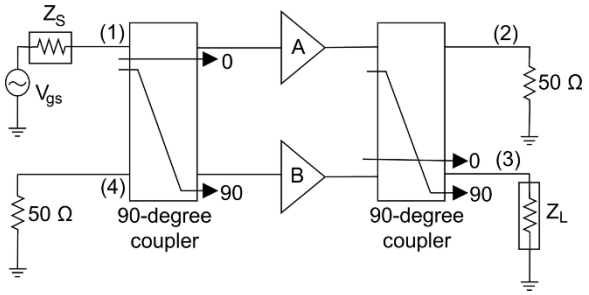

FIGURE 5. Schematic of the balanced amplifier configuration. A and B amplifiers with the schematic shown in Figure 4a along with 90° hybrid couples are employed [21].

phase shifters. However, when focusing on the phase shift range, the GFET-based phase shifter only yields a range that is half of the other available phase shifters. Nevertheless, 80° shift is enough for a good performance phase shifter as many antenna arrays only require no more than a 10° shift in their pointing [21]. The performance of the GFET-based phase shifter with frequency variations have been investigated by Li and his group [22]. Here, the phase shifter recorded a 40° shift at 8 GHz, while a 75° shift was observed at 30 GHz. They claimed that the phase modulation is enhanced at a higher frequency due to the high f_T of the GFET. Hence, if the GFET-phase shifter in [21] is observed at a higher frequency, a broader phase shift range can possibly be achieved, making the GFET a competitive transistor in phase shifter components.

TABLE 3. Performance comparison of the phase shifters.

Technology	Frequency (GHz)	Phase shift (°)	*IL* (dB)	FoM (°/dB)	Ref.
GFET	3.00	85.00	0 - 1.30	65.40	[21]
GFET	8.00	40.00	-	-	[22]
GFET	30.00	75.00	-	-	[22]
GaN HEMT	8.00 – 16.00	22.50	< 2.00	11.30	[51]
SiGe HBT	5.00	170.00	-	-	[52]
32-nm CMOS	60.00	175.00	3.50 - 7.10	24.70	[56]
65-nm CMOS	60.00	180.00	5.00 - 8.30	21.70	[57]
130-nm SiGe BiCMOS	60.00	156.00	4.00 - 6.20	25.20	[58]

Further enhancement on the architecture of the GFET-based phase shifter can help in improving the phase shift range. Medina-Rull and his group [21] suggested a multi-stage phase shifter configuration to compensate for the lower value phase shift. The configuration involves an additional balanced amplifier, as shown in Figure 5. With this method, an increase in the phase shift can be seen. For example, by cascading four balanced amplifiers, a phase shift range of 360° could be easily obtained for a phase shifter with an 80° shift. This finding shows that by enhancing the device architecture, a higher value of phase shift can be achieved, making the performance of the GFET-based phase shifters better than the other available ones.

C. POWER AMPLIFIERS

A power amplifier (PA) is used to increase the power of the input signal to a usable value that can drive the output devices. Its performance metrics include output power, P_{out}, gain, G, power added efficiency (PAE), carrier frequency, f, and linearity. When a PA is designed, it should be designed for these parameters to be high but to consume very minimal power [59], [60]. PA can be sorted into a linear PA or switching-mode PA (SMPA) based on the biases that are applied to the RF transistors. It can be further classified into linear class-A, -B, -AB, and -C; and SMPA class-D, -E, and -F [59], [60]. Apart from the classes of PAs, its architecture is another important factor that needs to be considered when designing an application-specific PA. A myriad of architectures, such as envelope elimination and restoration (EER), envelope tracking (ET), Doherty (DPA), linear amplification using nonlinear components (LINC), distributed PA [59], [61], differential cascade, and power combining [60], have been developed. These PA architectures can increase the PAE without losing linearity or in certain cases with an improved linearity [61].

The architecture development was driven by the proliferation of a variety of RF transistors using materials such as

GaN, GaAs, and AlGaAs-InGaAs and involving alternative structures such as HEMT, pHEMT, and HFET. Excitingly, with the recent discovery of two-dimensional material such as graphene, its use in PA has also shown promising results. In 2017, Hanna *et al.* demonstrated a GFET-based PA using an epitaxial-grown graphene layer [24]. Additionally, in 2019, Peng and his group demonstrated another GFET-based PA using chemical vapor deposition (CVD) monolayer graphene [23]. Both GFET-based PAs were demonstrated, and their large signal amplifying characteristics were evaluated. In this review, the performance of PAs that were developed based on various types of transistors and architectures was evaluated. The evaluation was conducted using the FoM that considers the performance metrics of the PAs. It was introduced by the International Technology Roadmap for Semiconductors (ITRS) and is defined as in (5) [59]. The FoM values are calculated and tabulated as in Table 4.

$$FoM = P_{out}.G.PAE.f^2 \tag{5}$$

From Table 4, the FoM calculated for GFET-based PA is 2.6×10^2, whereas the best calculated FoM for non-GFET-based PA is 2.3×10^5, using GaN HEMT. These three orders of magnitude differences are mainly influenced by the order differences of the performance metrics for the PAs. With a comparable $f \sim 2.00$ GHz, the GFET-based PAs only show a single order of magnitude for all the performance metrics, lower than the non-GFET-based PAs. Focusing on the G, a comparable G can be observed for the GFET-, AlGaAs-InGaAs-, GaN HFET MMIC-, and GaAs FET-based PAs. However, a significant difference is observed when the GFET-based PA is compared to GaN HEMT-, Si CMOS-, and GaAs pHEMT MMIC-based PAs. GFET has a large variation of drain current that leads to a large variation of transconductance. These variations caused the gain to reach its saturation value and justify the reason behind the low gain obtained by the GFET-based PA [24].

Next, for the PAE, the GFET-based PA has shown a considerable difference compared to the other non-GFET-based PAs. PAE is defined as the ratio of effective P_{out} to the DC input power, P_{dc}. The P_{dc} causes heat dissipation in the transistor. As the GFET cannot be effectively turned off, it will have greater heat dissipation than the other RF transistors [70], [71]. With this large value of P_{dc}, together with low P_{out}, it is understandable that the PAE for the GFET-based PA has the lowest value. Furthermore, as is summarized in Table 4, the GFET-based PA is developed only with a conventional common source architecture. In contrast, all the non-GFET-based PAs are developed with advanced PA architectures.

With such advanced architectures, high PAE and P_{out} of the non-GFET-based PAs are expected. It is believed that by introducing advanced architecture to the GFET-based PAs, its FoM could be improved as well. Hence, from the comparison of the FoMs, we can conclude that GFETs together with conventional common source architecture are not suitable to be used for PA, while GaN HEMT with one of the advanced PA architectures is the best choice, followed by GaAs pHEMT, GaN FET, Si CMOS, and GaAs FET.

D. LOW-NOISE AMPLIFIER

A low-noise amplifier (LNA) is another core component in RF applications. It amplifies the amplitude of the weak signal at its input to a more reasonable output signal with minimum self-generated additional noise. The performance metrics of the LNA are its gain, G, noise figure, NF, and power consumption, P [72], [73]. Generally, the LNAs should have higher G and lower NF [2], [25]. G is defined as the power ratio dissipated in the load to the power delivered to the transistor input and NF is defined as the amount of noise generated by the RF transistors. Their performances are related to the matching conditions of the transistors. The maximum G and a minimum NF cannot be obtained simultaneously, as the matching conditions differ for each situation. For a transistor with a minimum NF, the G obtained is usually lower than the maximum G [1]. In general, NF is affected by the g_m, f_T, and f_{max}. Their values depend upon the gate and drain bias voltage. Hence, it is crucial to determine the best bias point to obtain the minimum NF for LNA [26].

Various LNAs have been developed using conventional silicon and III-V materials, such as LNAs based on GaAs FET, Si CMOS, and GaN/Si HEMT. To date, due to the active development of flexible integrated circuits for wireless communications, GFET has been explored for the implementation of flexible LNA. It was first demonstrated in 2014 by Yeh and his group, when they fabricated a GFET-based LNA using CVD graphene [26]. The gate of the GFET was designed with a T-shaped structure to reduce charge trapping and the parasitic resistance at the gate/channel interface and source/drain contacts, respectively. Recently, in 2021, Yu *et al.* reported another GFET-based LNA [25]. In their study, the LNA Monolithic Microwave Integrated Circuit (MMIC) was fabricated with a monolayer GFET, and it was the first LNA MMICs demonstrated that incorporate both noise and small-signal models.

To assess the suitability of the GFET as a transistor in LNA, the performance of GFET-based LNA is compared with other available non-GFET-based LNAs. Table 5 summarizes their performance comparisons. Focusing on the NF, the measured NFs for the LNAs are below 5 dB, which is a good value for the transistor to avoid any additional noise errors at the other stage of the receiver [74]. The lowest measured NF is 1.34 dB. It is obtained by the GFET-based LNA in [26], and interestingly it outperforms the NF measurement for LNA based on GaAs FET, CMOS, and GaN/Si HEMT.

The low NF is obtained when the GFET is biased at $V_{DS} = 0.60$ V and $V_G = 0.05$ V at a frequency of 5.50 GHz. As mentioned previously, high G cannot be concurrently obtained with low NF. For this reason, a GFET-based LNA shows a low G, ranging from 8.34 to 11.95 dB, while GaAs FET and AlGaN/GaN HEMT show a far more superior G than other FETs. Although GFET-based LNA has shown the

TABLE 4. Performance comparison of the power amplifiers.

Technology	PA architecture	Application	f (GHz)	G (dB)	PAE (%)	P_{out} (dBm)	FoM	Ref.
GFET	Conventional common source	-	2.50	8.20	1.40	5.10	2.6×10^2	[24]
GaN HEMT	Coupled resonators	Dual-band 802.11ax	2.40 – 6.00	30.20 - 34.70	38.00 – 53.00	35.20 - 36.30	2.3×10^5	[62]
GaN HEMT	Transmission Line (TLIN) output matching class E	Wideband Code Division Multiple Access (WCDMA)	1.90	10.20	57.00	37.00	7.8×10^4	[63]
GaN FET	Power combining class AB	S-band	2.00	18.00	49.00	36.90	1.3×10^5	[64]
AlGaAs–InGaAs pHEMT	Distributed class J	Broadband	2.00	10.00	~43.00	~29.70	5.1×10^4	[65]
GaAs pHEMT MMIC	Combiner class AB	Multi-standard system	2.00 - 6.50	24.00 – 27.00	31.40 - 51.50	31.00	1.9×10^5	[66]
GaAs FET	Real Frequency Technique (RFT)	L- and S- band	2.00	14.89	20.00	17.00	2.0×10^4	[67]
GaN HFET MMIC	Distributed class AB	Multiband	2.00	~12.00	30.00	30.00	4.3×10^4	[68]
65-nm CMOS	Power combining	WLAN	2.40	26.50	40.30	26.90	1.7×10^5	[69]

TABLE 5. Performance comparison of the low-noise amplifiers.

Technology	f (GHz)	Noise Figures (dB)	G (dB)	Ref.
GFET MMIC	5.50 - 5.80	4.96	8.34	[25]
GFET	5.50	1.34	11.95	[26]
AlGaN/GaN HEMT MMIC	3.00	1.60	> 25.00	[75]
GaAs FET MMIC	20.00 – 40.00	3.00	20.00	[76]
GaAs FET MMIC	7.00 – 14.00	2.00	30.00	[77]
130 nm CMOS	8.00 – 12.00	1.50 - 13.60	17.60	[78]
65 nm CMOS	150.00	4.70 - 6.20	17.90	[79]
GaN/Si HEMT MMIC	18.00 – 56.00	2.20 - 4.40	16.00 - 21.50	[80]
InAlGaN/GaN HEMT	33.00 – 41.00	3.00	15.00	[81]

lowest G, it is still relevant for use in high-performance RF front-end circuits in the gigahertz range [26].

E. MIXER

An ideal mixer translates the incoming signals from one frequency to another by modulating or demodulating them. It mixes two signals at two different frequencies, namely the RF and LO input signals, to produce an intermediate frequency (IF) output signal [82]. Since the GFET was first introduced as an RF transistor, its use in frequency mixers has gradually increased. The first novel GFET-based mixer was introduced in 2012 by Habibpour and colleagues [29]. Their study demonstrated a subharmonic resistive GFET-based mixer, and its circuit structure is shown in Figure 6. As opposed to the conventional subharmonic mixers, the design of their mixer realized a more compact structure as it is implemented using only one transistor. Thus, with this success, more GFET-based mixers have been investigated by fabricating the mixers with GFETs using monolayer [27]–[29] or bilayer graphene [30], [31].

One important performance metric of a mixer is the conversion loss (CL), and a high-performance mixer should have a low CL [30]. CL is defined as the difference between the signal's power at the RF port and the power exiting the IF port [83]. In this review, the CL performances of the GFET- based mixers are compared with the non-GFET-based mixers fabricated using Si CMOS, SiGe BiCMOS, GaAs mHEMT, and GaAs pHEMT. The performance comparisons are summarized in Table 6. Among the mixers that have been reviewed, the mixer based on the SiGe BiCMOS technology has the best CL, which is 8.50 dB. For monolayer GFET-based mixers, a high CL, ranging from 24 dB to 45 dB, was obtained. In contrast, bilayer GFET-based mixers obtained a better CL in the range of 12.70 to 18 dB. The CLs for these bilayer GFET-based mixers were seen to be comparable with the other non-GFET-based mixers.

In order to optimize the CL, different ways to enhance it have been discussed in several published articles. For example, a study done in [30] stated that a low CL can be achieved by reducing the on-state channel resistance, and a study done in [31] suggested increasing the off-state resistance. Both can be achieved by using graphene with high mobility or high charge density, obtained, for example, in a pure bilayer graphene. In addition, the authors in [27] demonstrated that CL could be enhanced by reducing the LO power.

TABLE 6. Performance comparison of the RF mixers.

Technology	Scheme	L_{ch} (nm)	f (GHz)	LO Power (dBm)	CL (dB)	Ref.
GFET	Monolayer graphene	500.00	185.00 – 210.00	11.50 - 12.50	28.00 – 31.00	[27]
GFET	Monolayer graphene	100.00 600.00	4.00 4.00	15.00	31.00 45.00	[28]
GFET	Monolayer graphene	1000.00	2.00	15.00	24.00	[29]
GFET	Bilayer graphene	160.00 70.00	2.20 2.20	15.00	12.70 ~15.00	[30]
GFET	Bilayer graphene	100.00	88.00 – 100.00	-	18.00	[31]
65-nm CMOS	-	-	230.00	5.00	18.50	[84]
180-nm CMOS	-	-	15.00 – 50.00	10.00	13.00 – 17.00	[85]
130-nm SiGe BiCMOS	-	-	450.00 – 500.00	-1.00	8.50	[86]
GaAs mHEMT	-	130	29.50	2.00	11.00	[87]
GaAs pHEMT	-		37.00 – 85.00	10.00	9.00 – 14.00	[88]

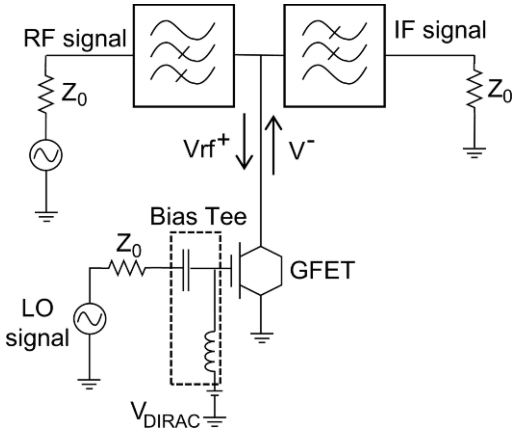

FIGURE 6. Schematic of the GFET-based mixer [29].

TABLE 7. Performance comparison of the frequency multipliers.

Technology	Output frequency (GHz)	Multiplier order	Efficiency (%)	Ref.
GFET	3.90	Tripler	80.00	[32]
GaAs pHEMT	37.64	Tripler	11.00	[83]
GFET	5.20	Quadrupler	97.00	[32]
GFET	0.01	Quadrupler	50.00	[33]
InP DHBT	120.00	Quadrupler	10.00	[90]
90-nm CMOS	62.00 – 70.00	Quadrupler	3.66	[91]
GaAs HBT-HEMT	23.20 - 29.60	Quadrupler	8.00	[92]

The reduction of the LO power can be achieved by reducing the gate dielectric thickness or selecting materials with high carrier mobility [29]. Furthermore, an increase in CL was observed at a shorter L_{ch} in a study reported by Tian and his group [30], who fabricated bilayer GFET-based mixers with different L_{ch} of 160 nm and 70 nm. At 2.20 GHz, a CL of 12.70 dB and 15 dB was achieved at the respective thicknesses. Therefore, it is essential to determine an optimized L_{ch} for a better-performing mixer. By improving the GFET fabrication process, the CL for the GFET-based mixers could be reduced, making it a promising transistor for RF mixers in the future.

F. FREQUENCY MULTIPLIERS

A frequency multiplier is a device that generates an output signal resulting from the harmonic product of the input frequency. The conventional frequency multipliers usually produce output powers of high-order harmonics much lower than the low-order harmonics [89]–[92]. To overcome this issue, the conventional frequency multipliers are designed with complicated device structures, where additional filter circuits or multistage doublers are required. As an alternative for the complex structure, GFET is explored as a transistor for the frequency multiplier. By taking advantage of the GFET ambipolar transfer characteristics, a much simpler configuration of the GFET-based frequency multipliers and remarkable improvement in the output spectral purity is demonstrated. The schematics for the back-gated and dual-gated GFET-based frequency multipliers discussed in this review are illustrated in Figure 7a and Figure 7b, respectively.

Their performances are compared with non-GFET-based frequency multipliers, such as those using GaAs pHEMT, InP DHBT, GaAs HBT-HEMT, BiCMOS, and CMOS technology. The multipliers are evaluated by observing their performance efficiencies, which are summarized in Table 7. As can be seen, the non-GFET-based frequency multipliers only obtained a very low efficiency ranging from 3.66% to 11%. With GFET-based frequency multipliers, efficiencies above 50% can be obtained for frequency triplers and quadruplers. These outstanding performances indicate that GFET has proved to be a better transistor choice in developing frequency multipliers.

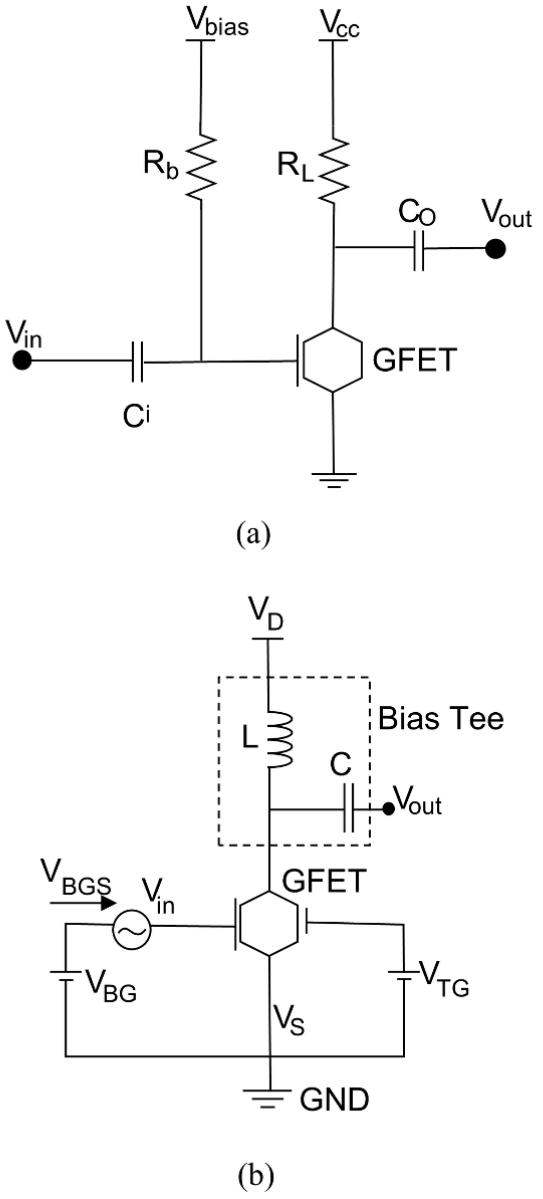

FIGURE 7. (a) A back-gated GFET-based frequency multiplier. The C_i and C_o are the DC block capacitors, R_b is the resistor for gate bias, and R_L is the load resistor. (b) A dual-gated GFET-based frequency quadrupler [32], [33].

The efficiency of the GFET-based frequency multiplier is highly dependent on the symmetry of the GFET transfer curve. GFET has an ambipolar characteristic and typically produces a V-shaped transfer curve. However, to produce a high efficiency GFET-based frequency multiplier, a W-shaped transfer curve (I_D–V_G) or an M-shaped resistance–gate voltage ($R - V_G$) curve is required. Although these curves are uncommon for GFET, some methods have been discussed to reliably obtain them. In [32], Peng *et al.* demonstrated that the M-shaped $R-V_G$ curve can be obtained by reducing the L_{ch} of the GFET, which will also reduce the GFET size. They suggested that the L_{ch} should be below 1.60 μm. In [33], Cheng *et al.* demonstrated that the shapes can be obtained by controlling the doping concentration. In their study, a W-shaped I_D–V_G curve was obtained when the CVD-grown graphene layer was doped with two different concentrations on different parts of the surface of the graphene. These methods need to be optimized to ensure the reproducibility of the W-shaped I_D–V_G curve or M-shaped $R - V_G$ curve. For a frequency tripler, the curve's symmetry does not impact the output waveform. The existence of the two resistance peaks is adequate for the GFET to function as a frequency tripler and achieve high efficiency. As reported in [32], 80% of efficiency is demonstrated for the tripler without considering its curve symmetry. However, the symmetry of the curve is essential when operating a frequency quadrupler. If a curve with symmetrical peaks is applied, the efficiency can reach up to 97%. Similarly, for the quadrupler demonstrated in [33], the output signal could provide nearly 100% efficiency if a curve with symmetrical peaks is used. In contrast, if the asymmetrical curve is applied, the efficiency decreases to 50%. As the GFET-based frequency multipliers perform better than the conventional frequency multipliers, the increase in its use is predicted in future RF applications.

IV. ISSUES OF GFET-BASED RF COMPONENTS

GFETs perform well as phase shifters, frequency multipliers, and oscillators. Nevertheless, there are issues that need to be ironed out if GFETs are to be used for other RF components.

A GFET-based PA for example, shows low PAE. The low PAE is due to the high-power consumption in the circuit caused by large contact resistance, R_c, and low saturation current, $I_{ds,sat}$ of the GFET [23], [24]. For R_c, there are several ways to reduce it. First, a suitable type of metal must be chosen for use as the electrode contact. The contacts made of pure gold, Au, provide a low R_c compared to contacts with a combination of metal and additional adhesion layers, such as Ti/Au, Ni/Au, and Pd/Au [15], [36]. The second method is by using a contact patterning process, as demonstrated by Smith and colleagues in [93]. The patterning process is done by introducing parallel cuts on graphene in the contact regions. This method maximizes the length of graphene edges bonded with metal, thus reducing the average R_c by 32%. Moreover, R_c can be reduced by etching holes in the contact area of graphene before metal deposition [94]. The holes are created using e-beam lithography followed by reactive ion etching in oxygen plasma. With this method, $R_c = 23\ \Omega\mu$m can be obtained for pure Au contacts compared to $R_c = 200\ \Omega\mu$m for graphene with no holes. The final method is by using ultraviolet-ozone (UVO) treatment. This method requires the graphene to be exposed under UVO before the metallization process. It was proven in [95]–[97] that values of R_c less than 200 $\Omega\mu$m can be achieved.

Next, as for the low $I_{ds,sat}$, it is essentially caused by the carrier mobility degradation in the graphene layer. The mobility is degraded due to the contaminated surface and defects introduced during the GFET fabrication process [98]. Therefore, an effort was made by Deokar *et al.* to address this

issue [99]. In their study, by optimizing the pre-annealing, gas flow, and wet transfer processes, high quality and hence high carrier mobility graphene can be produced. Another option to increase the $I_{ds,sat}$ is by increasing C_{ox}, the gate oxide capacitance. Higher C_{ox} can be achieved by reducing the oxide thickness or increasing the dielectric constant [10]. The former is not favorable, as excessive oxide thickness reduction could lead to a large leakage current. Hence, high dielectric constant materials such as hafnium oxide (HfO_2), aluminum oxide (Al_2O_3), and yttrium oxide (Y_2O_3) are strongly suggested to be used as dielectrics in GFETs.

Another main issue is the low cutoff frequency, f_T, of the GFET. As mentioned earlier, the f_T must be high. For example, a higher f_T has demonstrated a GFET-based phase shifter with better performance. Hence, some methods for enhancing the f_T value were suggested in this review. Based on the study in [26], f_T is inversely proportional to L_g. Therefore, the L_g of the GFET must be minimized in order to achieve a higher f_T. In addition, high f_T can be achieved by reducing the g_m value and a high-quality graphene layer to fabricate the GFET [10], [37]. Methods for obtaining high-quality graphene have been previously discussed. Additionally, the f_T can be improved by controlling the RC time constant. The RC time constant is defined as the time required to charge or discharge the capacitor through the resistor. In RF components such as the frequency multiplier, the RC time constant should be small in value as it is correlated with the f_T of the GFET. To enhance the RC time constant, both parasitic capacitance and output resistance need to be reduced. The parasitic capacitance can be lowered by improving the GFET material and structure. As suggested in [13] and [33], a highly resistive substrate such as quartz and a back-gate configuration are much preferred for this effort. For the output resistance, the reduction of the L_g to a nanoscale length is recommended.

V. CONCLUSION

A series of FoM assessments for GFET-based and various non-GFET-based RF components were carried out in this review. It was found that the GFET helps to improve the FoM of frequency multipliers, phase shifters, and mixers. GFET stands out the most as a frequency multiplier. As an example, in one of the frequency-multiplier applications, i.e., a quadrupler, nearly 100% efficiency was demonstrated. More interestingly, taking advantage of the ambipolar characteristics of the GFETs, a novel oscillator that can act as both a PWM and VCO was demonstrated as well. Despite the exemplary performance of GFETs in these three RF components, there is still much to be done for the GFET to gain acceptance in RF design communities. As a PA, for example, the FoM for a GFET-based PA is low, typically two to three orders of magnitude lower than the non-GFET based PA. As a mixer, its CL is almost double the CL of a non-GFET-based mixer. These examples show just how potentially good GFET could be but at the same time illustrate issues that need to be addressed.

Several ideas have been put forward to minimize or even remove the issues faced by GFETs. For instance, use of appropriate metal contact and contact patterning processes such as parallel cuts on graphene as well as pre-deposition hole-etching of graphene may reduce the contact resistance. Additionally, use of high mobility carriers via optimized GFET processes and high dielectric constant materials may improve the $I_{ds,sat}$. Use of appropriate structural design may also reduce parasitic capacitances. Such ideas could give rise to more innovative applications with potential uses not only in RF but also in other fields of interest.

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