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A New Hybrid Cascaded Switched-Capacitor Reduced Switch Multilevel Inverter for Renewable Sources and Domestic Loads

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ABSTRACT This multilevel inverter type summarizes an output voltage of medium voltage based on a series connection of power cells employing standard configurations of low-voltage components. The main problems of cascaded switched-capacitor multilevel inverters (CSCMLIs) are the harmful reverse flowing current of inductive loads, the large number of switches, and the surge current of the capacitors. As the number of switches increases, the reliability of the inverter decreases. To address these issues, a new CSCMLI is proposed using two modules containing asymmetric DC sources to generate 13 levels. The main novelty of the proposed configuration is the reduction of the number of switches while increasing the maximum output voltage. Despite the many similarities, the presented topology differs from similar topologies. Compared to similar structures, the direction of some switches is reversed, leading to a change in the direction of current flow. By incorporating the lowest number of semiconductors, it was demonstrated that the proposed inverter has the lowest cost function among similar inverters. The role of switched-capacitor inrush current in the selection of switch, diode, and DC source for inverter operation in medium and high voltage applications is presented. The inverter performance to supply the inductive loads is clarified. Comparison of the simulation and experimental results validates the effectiveness of the proposed inverter topology, showing promising potentials in photovoltaic, buildings, and domestic applications. A video demonstrating the experimental test, and all manufacturing data are attached.

INDEX TERMS Cascaded, multi-level inverter, self-charging, switched-capacitor, total standing voltage.

NOMENCLATURE

t_0-t_{13}	Time for each pulse of the steps (s).
S11, S12, S23	Identification for modules switches, Snm is switch of number *n* from module *m*, *n* = Switch number, *m* = module number.
T1, T2, T3, T4	Identification for inverter H-bridge switches, H-bridge switch number of n.
C11, C21	Switched capacitor identification, Cnm is switched-capacitor of number n from module m, n = Switched-capacitor number, m = module number.
N_{level}	Level numbers of the inverters.
E_{SC}	Amount of the switched-capacitor energy (J).
V_L	Load inductor voltage (V).
V_{RL}	Load resistor voltage (V).
V_{FD}	Forward voltage of the freewheeling diode (V).

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P_L	Loss power (W).
$P_{\text{MOSFET, loss}}$	Loss power of MOSFET (W).
$P_{\text{diode, loss}}$	Loss power of diode (W).
V_O	Output voltage (V).
$Q_{\text{C(N)1}}$	Magnitude of capacitor C_{N1} discharge (C).
f_0	Base Frequency (Hz).
k	Voltage ripple factor.
I_{out}	Output current (A).
ESR	Equivalent Series Resistance (Ω).
V_{dc}	DC source voltage (V).
TSV	Total Standing Voltage (V).
TBV	Total Blocking Voltage (V).
n_{level}	Level numbers of the inverters.
CF	Cost Factor.
α	1) Coefficient that measures the weighting of the TSV, and 2) The pulse angle.
N_{switch}	Number of switches.
N_{dr}	Number of drives.
N_{diode}	Number of diodes.
N_{cap}	Number of switched-capacitors.
N_{source}	Number of DC Sources.
$P_{\text{C, loss}}$	Loss power of the capacitor (W).
$P_{\text{C, leakage}}$	Leakage loss power (W).
P_{ESR}	ESR resistance (Ω).
I_{leakage}	Leakage current of a capacitor (A).
R_{ESR}	ESR resistance (Ω).
$P_{\text{L, Vout=0}}$	Loss power when the output voltage is equal to zero (W).
$P_{\text{L, Vout}\neq 0}$	Conduction loss power of non-zero voltage (W).
R_{ON}	Forward resistance of a diode (Ω).
N_M	Number of modules.
$N_{\text{switch,H}}$	Number of switches including H-bridge switches.
V_{RT}	Voltage across the switch T in ON situation (V).
τ	Constant time (s).
i	Diode Current (A).
I_s	Saturation current of the diode (A).
V_T	Thermal voltage (V).
P_{av}	Average output power (W).
T	Period (s)
P_{rated}	Rated power of the power supply (W).
P_{npk}	Power extracted from the DC source before the output voltage becomes zero (W).
P_{pk}	Peak output power (W).
Z_{eq}	Equivalent impedance (Ω).
X_L	Inductive reactance (H).
R_L	Ohmic impedance (Ω).
I_{npk}	Current extracted from the DC source before the output voltage becomes zero (A).
I_{pk}	Peak output current (A).
$P_{\text{loss,full}-\text{cycle}}$	Total loss of a full cycle application (W).
$P_{\text{loss, H}-\text{bridge}}$	Loss power of the H-bridge switches(W).
$I_{\text{Vout=0}}$	Current when the output voltage is zero (A).
I_C	Current through the capacitor (A).
E_{OFF}	Required energy to turn off the MOSFET (J).
E_{ON}	Required energy to turn ON the MOSFET (J).
V_F	Diode forward voltage drop (V).
i_F	Diode forward current (A).
V_{pk}	Peak voltage (V).
$N_{\text{switch,NH}}$	Number of switches without H-bridge switches.

I. INTRODUCTION

A. MOTIVATION AND INCITEMENT

Nowadays, multi-level inverters (MLI) play a leading role in various industries. The application of multi-level inverters has increased, especially in the grid connection of renewable energy systems. One of the problems in using voltage step-up converters is the utilization of transformers, which MLIs have already solved this problem [1].

Based on the output waveform, inverters can be classified as follows: two-level or square wave inverters, quasi-square wave inverters, two-level PWM inverters, and multi-level inverters (MLIs) [1]. The main problem with two-level square-wave and PWM inverters is their employment in high and medium power systems. The devices required for switching at the appropriate voltage and frequency are either rare or expensive. Besides, the quality of the voltage output is low and requires large filters across the load. A reasonable alternative to these types of converters (in this power range) can be MLIs. Neutral point diode clamped (NPDC), flying capacitors (FC), and cascades H-bridge (CHB) are the main types of multi-level inverters [1]. Voltage source inverters are widely used in electric motor drives and high-power quality applications. One problem with switched capacitors in multi-level inverters is the inherent unbalance of the capacitor voltage [2]. Consequently, when a higher number of voltage levels across the load results, this problem becomes more complicated. A practical solution to mitigate this problem can be the use of hybrid-source switched capacitor structures. At higher voltage levels, the number of switches is reduced by using this type of inverter [3]. Some types of inverters have numerous semiconductor switches, with the possibility of a fault in each one. Therefore, the larger the number of switches, the lower the reliability of the inverter [1]. The proposed MLI has the privilege of using fewer semiconductors and capacitors with lower voltage ratings for the step-up multi-level AC output.

B. MLIS INVOLVING TWO OR MORE DC SOURCES-LITERATURE REVIEW

The output power of some new renewable power systems, such as photovoltaics and fuel cells, is DC. Microgrids equipped with this type of power generator have a variety

of DC sources. An increase in the number of DC power generators means an increase in the number of DC sources. Single-input, multi-output transformers are also used in some applications. Each output of the transformer can be considered as an isolated DC source. Therefore, different studies have proposed various solutions for the employment of these sources. The authors of [1] introduced different topologies that use two or more DC sources. The proposed scheme also goes in the same direction. Each module requires a DC source and if the modules are connected in cascade, both the output voltage and the number of voltage levels will increase.

Since the invention of semiconductor switches, many efforts have been made to construct DC-AC inverters. In [4] multilevel converters are comprehensively discussed and the classification of them is presented. Comparisons are made between three cascaded multilevel topologies. How multilevel modules can be connected to PV systems is examined, and details from relevant research are provided. The comparison of semiconductors and the presentation of the static characteristics of new power switches used in inverters are the advantages of [4]. Over time, more powerful controllable switches have been invented. This also improved the quality of the inverter output voltage [5]. The main impetus for multi-level inverters was the reduction of semiconductor switches, dc voltage sources, and total standing voltage (TSV). Based on these constraints, various articles have presented different topologies with the concept of the reduced number of switches. In [6], a comprehensive review of MLI topologies with the reduced number of switches has been presented. In [7], an overview of some new topologies of multi-level inverters with device reduction was provided. Some challenges may arise in device reduction, which is the main point of this literature. Recent works on multilevel inverters (MLI) and their applications were discussed in [8], where different inverter configurations were divided into symmetrical, asymmetrical, and modified topologies. A single-phase reduced-switch multi-level inverter (RSMLI) was also experimentally analyzed by considering different voltage levels generated at different switching frequencies. In [9], two new topologies are proposed to reduce the number of switches. The first topology requires three DC power supplies and ten switches to achieve a voltage of 15 levels above the load. With the further development of this topology, which employed four DC power supplies and twelve switches, a voltage of 15 levels across the load was achieved. Based on the basic concept of switched-capacitor inverters, a multi-level boost converter topology is proposed in [10]. The proposed topology includes eleven unidirectional switches with a single switched capacitor unit generating a 9-level voltage across the load. In addition to voltage doubling, self-voltage balancing of the capacitor voltage was performed by reducing the voltage load, regardless of the auxiliary method. Reference [11] has presented a new inverter topology that contains two switched capacitors and nine switches. Its output voltage is 9-level and its peak voltage is about twice the input voltage. Compared with similar inverters, reduction in the number of switches and cost are some of the advantages of this inverter. Reference [12] presents a step-up reduced switch multi-level inverter that uses switched capacitors. The work [12] uses 10 switches, 2 capacitors, 2 DC sources, and 2 diodes to generate a 17-level waveform. Capacitors are inherently balanced and compared to similar inverters, the number of switches is reduced. Even though they are very similar, the topology of [12] is totally different from our topology presented. Reference [13] represented a multi-level DC-Link Inverter. This inverter consists of 14 switches, 8 clamping diodes, and 5 capacitors and generates an 11-level waveform. At first glance, [13] and the presenting topology are similar, but they are also totally different. This inverter uses 6 DC sources and the DC sources are provided by the output of 3 transformers. The transformers are single input, double output.

C. KEY CONCERNS, CONTRIBUTION, AND ARTICLE ORGANIZATION

RSMLIs are also commonly used in domestic solar PV applications. A suitable configuration of PV cells can serve as an isolated DC source in an RSMLI design capable of meeting the required power demand [14], [15]. The proposed application targets low-inductance, high-resistance domestic loads. The best usage of the presented multi-level inverter is for domestic and building applications. Some household appliances use resistive loads more than inductive loads. Lights, iron, TV, and resistive heaters are some types of resistive loads that compared to inductive loads such as refrigerators, consume more power [16]; therefore, in some houses, resistive loads can outweigh inductive loads [17]. Especially in cold regions, resistive heaters consume much more power than inductive loads. The proposed MLI is able to supply the demanded power of combined resistive-inductive loads within the allowable power range. The ability of the proposed inverter to supply the required power of inductive loads is envisioned.

Harmful reverse flowing currents of inductive loads is one of the obstacles that prevent further reduction in the number of switches. In addition to investigating the performance of inverters under resistive loads, [2]–[4], [10]–[14] have investigated the effects of inductive loads to address the current reverse flow problem.

One problem with switched capacitor MLIs is the surge current of the capacitors. This can be harmful to the switches and the capacitor. Reference [18] solved this problem by a simple auxiliary circuit that eliminates the mentioned current surges and uses zero current switching conditions for the charging switch. Reference [19] designed a multi-level inverter based on flying capacitors and using PWM switching algorithm reduced the surge current. The proposed research provided the required current by using capacitors at the output of DC sources. DC sources charge their output capacitor, and this capacitor prepares the surge current of switched capacitors. MOSFETs and IGBTs are usually capable of withstanding the surge currents that are several times higher

than the rated DC currents [20]. The datasheet of MOSFETs contains data of the most permissible current and the selection of switches was based on this factor and the safe operating area (SOA). Also, using 2 DC sources helps to reduce the effect of surge currents by distributing them between the two sources. In our work, a thorough study of output power, number of isolated power supplies, number of passive components, highest switch voltage rating, total standing voltage, and number of switches has been carried out.

The development motivations behind the new CSCMLI inverter can be summarized as follows. Based on MILHDBK-217 [21] and MIL-HDBK-338B [22] standards, under the same conditions for similar systems, the fewer electronic components of an electronic system, the better the reliability. Using fewer components reduces manufacturing costs. The smaller the number of components, the lower the losses. The output voltage of renewable energy sources such as photovoltaics and fuel cells are DC and may be used as isolated DC voltage sources in cascaded multilevel inverters. The combination of cascaded and switched capacitor multilevel inverter covers each other's weaknesses. Domestic loads are a combination of ohmic and inductive loads. The power of some low-inductance domestic loads may be supplied using the proposed CSCMLI.

The gaps of the literature are: lack of practical information on the analysis of the surge current in the ability of the DC source and the tolerance of the diodes and MOSFETs that are used in MLIs, ability to reduce the number of components while increasing the maximum output voltage, and lack of information on how to calculate the TSV of the switches that are used in MLI.

The main contributions of the paper include: reducing the number of switches and reducing the number of switched capacitors while increasing the peak output voltage of the MLI structure compared to similar inverters, extracting the formula of calculating the number of switches, the number of switched capacitors, the number of DC sources and the number of semiconductors in terms of N-level for ten similar articles to be compared with the proposed structure, and practical surge current analysis of the proposed CSCMLI for medium and high-power applications, including the current tolerance of diodes and MOSFETs, and the ability of the DC power source to supply the current.

The rest of the paper is organized as follows. Section II describes the material and methods of proposed inverter including switching pattern, capacitance and TSV calculation, circuit analysis, surge current analysis, and efficiency analysis. Section III presents comparison. Section IV and V contain simulation and experimental results. Section VI includes limitations of the study. Section VII presents open questions. Finally, section VIII describes our conclusions.

II. MATERIAL AND METHODS OF PROPOSED INVERTER

A. SWITCHING PATTERN

Using the Cascaded Switched-Capacitor multi-level inverters (CSCMLI) topology, a 17-level inverter consisting of

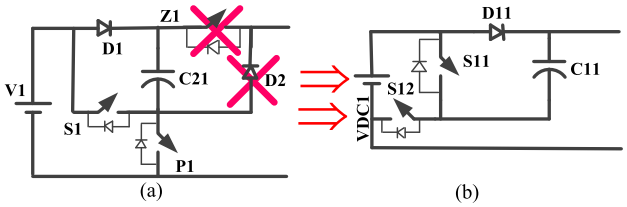

FIGURE 1. Voltage-Double was obtained by removing Z1 and B1. This Figure shows the differences between similar circuit designs and the proposed module 1 design. (a) Doubler voltage module which is presented by [1] and (b) the doubler voltage module of the proposed CSCMLI.

4 modules in a cascade arrangement was proposed in [1], pp. 7, Fig. 4]-[2] (Section C). The newly proposed topology is the result of the improvement of the existing topologies. For better understanding, modifications are presented in comparison to [1].

Fig. 1 shows one of the modules of this inverter. The first section of the inverter is obtained by eliminating Z1 and D2. This module can generate a maximum of $2V$dc. Both configurations shown in Figure 1 are voltage doubles. Z1 and D2 are designed to protect the system from backward flowing currents, which is a task of the H-bridge in the proposed topology. The second modification is a change in direction in P1, which raises the output voltage of the module from $2V$dc to $4V$dc. Figure 2 shows this change in the direction of the switch.

Reference [1] has presented an inverter which is similar to our proposed CSCMLI multilevel inverter. Both circuits in Figure 1 are voltage doublers. In the module presented in [1, Fig. 4], switch Z1 and diode D2 are placed in the inverter to close the loop of the reverse current of the inductive load, but in the proposed CSCMLI inverter, Z1 and D2 are removed. Removing these two switches serves two purposes: 1) As shown in Figure 2, the direction of switch P1 is reversed, and by modifying the switching algorithm, the loop for flowing the current required to charge capacitor C21 is closed. 2) When the voltage is zero at load, 3 of the 4 H-bridge switches are closed simultaneously. This both establishes the charging current of capacitor C21 and closes the H-bridge loop to discharge the stored energy of the inductive load.

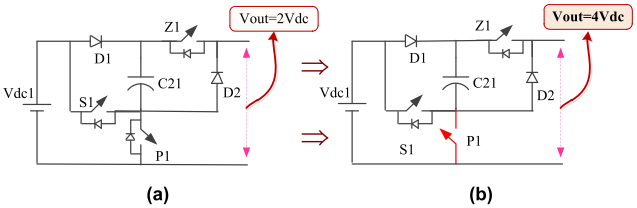

FIGURE 2. Direction changes in P1 and the resulting voltage increase from $2V$dc to $4V$dc in the proposed topology. The direction of the switch P1 is reversed. This Figure also shows the differences between similar circuit designs and the proposed module 2 design. (a) Voltage doubler proposed in [1], (b) Quadruple the voltage by modifying the structure of the [1] voltage doubler module, P1 is reversed in module 2 of the presented CSCMLI inverter.

Thus, the reverse current of the inductive load flows through the H-bridge closed-loop switches. (There is a limitation in discharging the stored energy of the inductive load, which is explained in detail in Circuit Analysis sections).

One way to achieve the output voltage of 13 levels is the cascade of module 1 in series, but there are several problems: 1) to discharge the inductor energy it is not possible to remove the components Z1 and D2, and one of the novelties of our presented article is the removal of these components to minimize the number of inverter switches, thus, the presence of module 2 allows the removal of Z1 and D2. Figure 4 of article [1] applied the module of Figure 1(a) of our presented article. Connecting three modules in series results in 13 levels and requires 13 switches, 6 diodes, and three capacitors. Compared to [1], the CSCMLI presented in our article has 9 switches, 3 diodes, and 2 capacitors.

In similar inverters, at zero time, neither h-bridge switch is closed, and if two h-bridge switches are closed, either a short circuit occurs in the circuit or a load is placed in the circuit and the load voltage will not be zero, but in our presented article When the output voltage is zero, 3 h-bridges are closed. The current flowing through the H-bridge is used to charge capacitor C21.

In general, the presence of module 2 has several advantages: 1) The CSCMLI inverter can be designed and manufactured with fewer switches compared to similar inverters, 2) Module 2 is capable of generating 9 voltage levels (of course, with the assistance of module 1) and using an appropriate switching algorithm, it can generate more cascaded voltage levels at the output, as compared to cascade module 1.

The proposed 13-level Switched-Capacitor Unit (SCU) inverter is shown in Figure 3. This topology uses H-bridge switches to prevent the inductive load current from flowing backward. The maximum voltages that can be obtained from modules 1 and 2 are $2V$dc and $4V$dc, respectively. The inverter can be expanded by using module 1 in a cascade configuration to achieve higher output voltage levels. This configuration produces six positive levels, six negative levels, and one zero level (13 levels total). Figure 4 shows how the inverter is expanded to form a cascade arrangement. Under the isolated condition, each of the modules from 2 to $N + 1$ can generate a maximum of $4V$dc. This, along with proper switching, can generate a desirable waveform at the output. The objective is to eliminate S13 and D12 to change the direction of S22 and use the H-bridge to ultimately provide protection against reverse current flow. The stored energy of the inductor is discharged in the H-bridge switches. The effect of a current flowing in reverse is shown in Figure 5. When the H-bridge switches perform their normal task of reversing the polarity, the output waveform across the load is as shown in Figure 6. In this case, not only is the behavior of the switching output undesirable, but voltage spikes can damage the semiconductors or cause them to fail. Such a negative effect occurs when the H-bridge switches' while performing their normal task, attempt to set the output voltage across the load equal

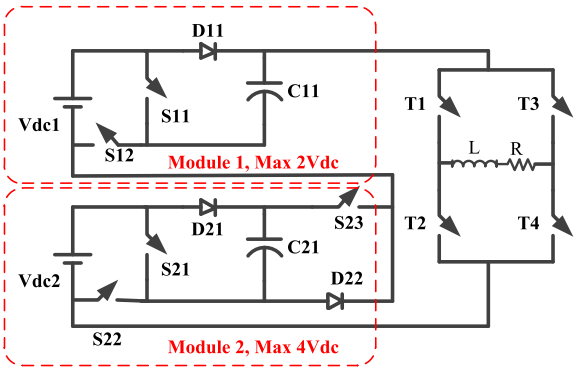

FIGURE 3. 13-level SCU inverter, aiming to eliminate S13 and D12 to change the direction of S22, and use the H-bridge to ultimately provide protection against the backward-flowing current.

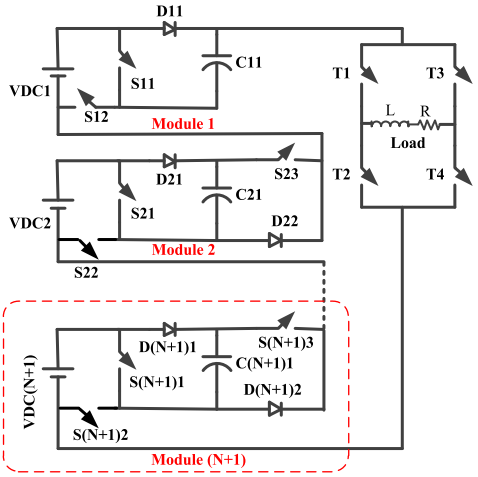

FIGURE 4. Extended cascade topology of the proposed inverter.

to zero. As long as the load type is resistive, the circuit in Figure 3 will operate with no problems. However, with an inductive load, a considerable amount of energy is discharged when the H-bridge switches are turned on, resulting in a large voltage reversal. Under such circumstances, the inverter is more likely to fail, and the total blocking voltage of the system increases. The proposed MLI can handle the inductor load, but there are limitations, which will be discussed in the following sections.

Figure 5(a) and Figure 5(b) show how an inductive load is discharged at zero voltage in conventional multi-level inverters. All four switches T1 to T4 are on (off) and the inductor is discharged by freewheeling diodes of H-bridge switches. As shown in these figures, the reverse current returns to the main circuit of the MLI, in fact, the inductive discharge loop is closed using the main circuit of the MLI and thus this energy is discharged. But in the CSCMLI inverter, the discharge of the inductive load energy is performed according to Figure 5(c) and Figure 5(d). When the output voltage of the load is zero, two switches on one of the H-bridge legs must be closed (on). Closing these switches causes capacitor

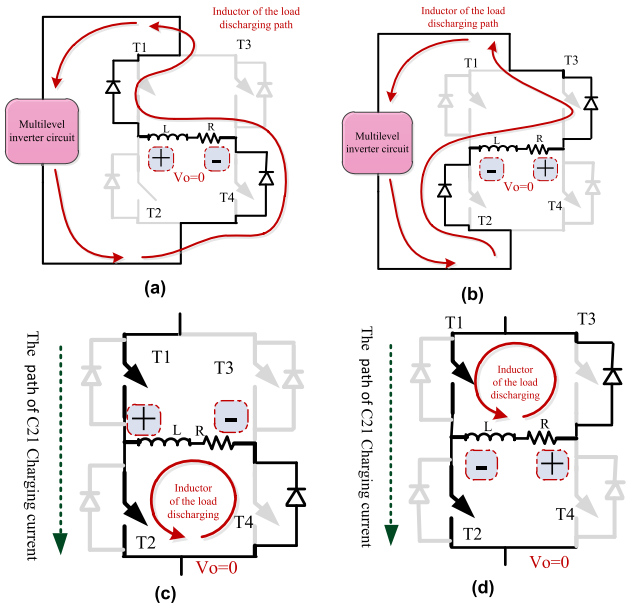

FIGURE 5. Discharging the inductive load energy and charging all the capacitors.

C21 to be charged. Figure 2 (b) shows capacitor C21 whose voltage is $3V$dc and shows the output voltage of the module is $4V$dc. Charging this capacitor and increasing the voltage of this capacitor by closing two H-Bridge switches.

Figure 5(c) and Figure 5(d) show the operation of the H-bridge switches of the proposed CSCMLI at V out $= 0$. Three switches are turned on at the moment when the voltage is zero, which serves several purposes: 1) discharging the energy of the inductive load, 2) Close the current path to charge all capacitors, 3) distributing the capacitor charging current to all H-bridge switches, and 4) distributing heat due to the discharge of the inductive load energy to all H-bridge switches. This virtually obviates the necessity of an additional switch or diode in Module 1 to prevent the undesirable effects of an inductive load. When three switches are on, two current loops are formed and the energy from the inductive load is discharged in all four switches. In the closed loops, these two loops are formed by two switches and two freewheeling diodes. With the direction of current flow to both switches, the capacitor charging current is allowed to pass. The line for reactive power path in modes of operation are shown in Figure 5(c) and Figure 5(d).

Table 1 shows the switching pattern of the proposed topology based on a sinusoidal waveform and the assumption of Vdc1$=$ Vdc2$=$ Vdc. The switches that should be turned on are indicated at the end of each column. In column A, where no voltage is applied, S11 from the module section and three switches from the H-bridge section are turned on. The same switches from the same sections are turned on in column M, where the voltage is zero again.

This eliminates the adverse effects of the inductive load and charges all the capacitors. It also distributes the heat losses among the switches, which in turn improves the reliability of the system. It is worth noting that all capacitors are charged up to $3V$dc. Table 2 shows the valid switching states for the presented topology. The highlighting indicates the sections dedicated to charging all capacitors and discharging the inductive load energy at the zero voltage of the output. Tables 1 and 2 serve as basic patterns for switching in the presented inverter. Figure 7 illustrates the switching operation of the topology. The increase of the output voltage from $1V$dc to $6V$dc is shown from left to right. The last items show how capacitor C21 is charged and the energy of the inductive load is discharged. The bold black lines show the paths through which the current flows to produce the voltage across the load, and the blue lines show the paths for charging the capacitor and discharging the inductive load. C21 is charged when there is no voltage across the load. In positive and negative half-cycles, this voltage also increases from $1V$dc to $6V$dc and the polarity is changed by the H-bridge switches. C11 is charged 4 times during a half cycle. In fact, C11 and C21

TABLE 1. Switching pattern of proposed topology based on sinus waveform.

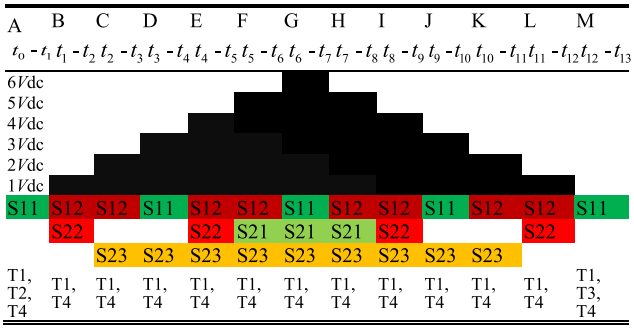

TABLE 2. Valid switching states for presented topology.

S11	S12	S21	S22	S23	T1	T2	T3	T4	Vo
1	0	0	0	0	**1**	**1**	**0**	**1**	0
0	1	0	1	0	1	0	0	1	Vdc
0	1	0	0	1	1	0	0	1	$2V$dc
1	0	0	0	1	1	0	0	1	$3V$dc
0	1	0	1	1	1	0	0	1	$4V$dc
0	1	1	0	1	1	0	0	1	$5V$dc
1	0	1	0	1	1	0	0	1	$6V$dc
0	1	1	0	1	1	0	0	1	$5V$dc
0	1	0	1	1	1	0	0	1	$4V$dc
1	0	0	0	1	1	0	0	1	$3V$dc
0	1	0	0	1	1	0	0	1	$2V$dc
0	1	0	1	0	1	0	0	1	Vdc
1	0	0	0	0	**1**	**0**	**1**	**1**	0
0	1	0	1	0	0	1	1	0	$-1V$dc
0	1	0	0	1	0	1	1	0	$-2V$dc
1	0	0	0	1	0	1	1	0	$-3V$dc
0	1	0	1	1	0	1	1	0	$-4V$dc
0	1	1	0	1	0	1	1	0	$-5V$dc
1	0	1	0	1	0	1	1	0	$-6V$dc
0	1	1	0	1	0	1	1	0	$-5V$dc
0	1	0	1	1	0	1	1	0	$-4V$dc
1	0	0	0	1	0	1	1	0	$-3V$dc
0	1	0	0	1	0	1	1	0	$-2V$dc
0	1	0	1	0	0	1	1	0	$-1V$dc

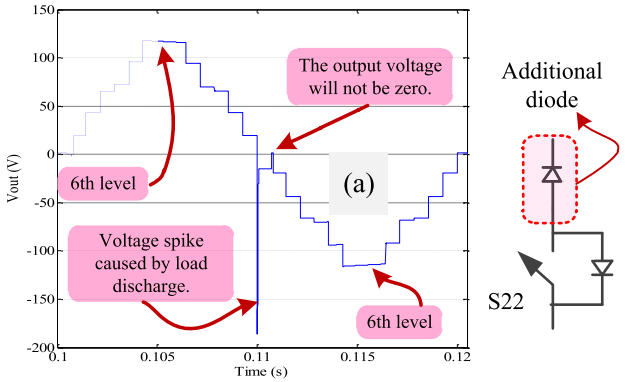

FIGURE 6. (a) Effect of a backward-flowing current on the output voltage waveform due to an inductive load, (b) The alternative circuit we used in this article instead of the body diode-free switch.

can be charged 8 and 2 times respectively in a full cycle of one period. This is a suitable charge time for both capacitors, balance their voltage, and provided the capacitance values are properly selected to avoid excessive voltage drop. Also, switch S22 should not have a freewheeling diode, and other diodes in the circuit will not allow the reverse current to pass, so this diode is not needed. Also in Figure 6, due to the charging of the switched capacitors during the operation of the inverter, the voltage drops through the path diodes and the surge current of the switched capacitors, the step voltages are not equal.

Switches that do not have a body diode may be used as S22 switches. However, if a MOSFET is used in the circuit, an additional diode should be added in series with the MOSFET to prevent current flow when the switch is OFF, as shown in Figure 6 (b).

The two power sources in such an inverter design should be able to provide the instantaneous current required to charge the capacitors. Since the total energy required to charge C11 and C21 is relatively low, the system has no difficulty providing this surge current. In other topologies, simultaneous switching of the H-bridge arms causes problems, but the proposed topology uses this simultaneity for charging switched capacitors.

B. THEORY/CALCULATION, CAPACITANCE CALCULATION

In SCMLIs, the capacitance of the capacitors plays a major role in balancing their voltage ripple. The capacitor voltage should not drop below a certain threshold when discharging. A lower voltage ripple leads to a reduction in losses and improves the efficiency of the converter [23]. The capacitance is mainly determined by the amplitude of the output current and the discharge time of the capacitor in the worst state. The maximum discharge of each capacitor is given by

$$Q_{\mathrm{C(N)1}} = \int_{t_{i+N}}^{t_{j+N}} I_{\mathrm{out}} \sin(2\pi f_0 t)dt, \tag{1}$$

where f_0 is the base frequency, k denotes the voltage ripple factor and I_{out} denotes the output current in the maximum discharge time for each capacitor [23].

$$C_{\mathrm{N1}} \geq \frac{Q_{\mathrm{C_{N1}}}}{k \times \mathrm{Vdc}}. \tag{2}$$

The resulting value is the ideal capacitance. Capacitors and inductors used in practical electrical circuits are non-ideal components. Thus, any capacitor or inductor can be considered to be connected in series with an associated resistor, which is called the equivalent series resistance (ESR).

In designing for practical applications, the selection of capacitance values is done by considering the ESR [24]. As a result, the minimum capacitance for the presented circuit was calculated. In the case of an inverter designed for practical applications, the final capacitance values can be determined from the datasheets of the capacitors, taking into account the operating frequency and ESR. Also, the calculation of the gain voltage in terms of input voltage is accomplished by the following equation:

$$G_v = 0.6062 \ln(N_{\mathrm{dc}}) + 2.62, \tag{3}$$

where N_{dc} is the input DC source and G_{v} is the voltage gain of the CSCMLI.

C. TSV CALCULATION

The cost and realization of a multi-level converter are significantly influenced by the current and voltage values of its switches [25]. The magnitude of the reverse voltage across the switches is considered a major determinant when comparing different multi-level converter structures in terms of the overall cost and operating range of the switches. A smaller magnitude of reverse (or withstand) voltage across the switches has the advantage of a smaller voltage across the switch terminals [26]. The cost requirements of a semiconductor are dictated by the total standing voltage (TSV), which is sometimes referred to also as total blocked voltage (TBV) [27]. In the proposed 13-level inverter, each of the H-bridge switches has a TSV of $6V$dc. The number n_{level} of levels in the proposed inverter is determined by

$$n_{\mathrm{level}} = [4 \times (2N + 1)] + 1, \tag{4}$$

where N is the number of modules added to the circuit in a cascade arrangement. For $N = 0$, there is only one module with a maximum voltage of $2V$dc, and the inverter has 5 levels. For $N = 1$, module 2 is added to the circuit, which can provide $4V$dc at the output, and a 13-level inverter is obtained. In the 5-level inverter, there are a total of 6 switches: T1 to T4 located in the H-bridge and S11 and S12 located in the voltage doubler part of the circuit. The calculation of the TSV of the individual switches and their summation $\mathrm{TSV_{total}}$ is performed as follows:

$$\left.\begin{array}{l}\mathrm{TSV_{S11,S12}} = 1V\mathrm{dc} \\ \mathrm{TSV}_{T1-T4} = 2V\mathrm{dc}\end{array}\right\} \Rightarrow \mathrm{TSV_{total}} = (2 \times 1) + (4 \times 2) = 10V\mathrm{dc}. \tag{5}$$

Charging C21 *and discharging inductance load after positive sequence*

Charging *C21* and discharging inductance load after negative sequence

FIGURE 7. The function of the presented inverter topology.

In the 13-level inverter, T4 is in the H-bridge, S11 and S12 are in the voltage doubler section, and S21, S22, and S23 are in the first module to provide the 4 multiplier levels. The $\mathrm{TSV}_{\mathrm{total}}$ for the 13-level inverter is calculated similarly to that for the 5-level inverter as:

$$\left.\begin{aligned}&\mathrm{TSV}_{S11,S12} = 1V\mathrm{dc}\\&\mathrm{TSV}_{S22} = 2V\mathrm{dc}\\&\mathrm{TSV}_{S21,S23} = 3V\mathrm{dc}\\&\mathrm{TSV}_{\mathrm{T1\text{-}T4}} = 6V\mathrm{dc}\end{aligned}\right\} \Rightarrow \mathrm{TSV}_{\mathrm{total}}$$

$$\begin{aligned}&= (2\times 1) + 2 + (2\times 3) + (4\times 6)\\&= 34V\mathrm{dc}. \qquad (6)\end{aligned}$$

For the 21-level inverter, $\mathrm{TSV}_{\mathrm{total}}$ is calculated as follows:

$$\left.\begin{aligned}&\mathrm{TSV}_{\mathrm{S11,S12}} = 1V\mathrm{dc}\\&\mathrm{TSV}_{\mathrm{S22,S32}} = 2V\mathrm{dc}\\&\mathrm{TSV}_{\mathrm{S21,S23,S31,S33}} = 3V\mathrm{dc}\\&\mathrm{TSV}_{\mathrm{T1\text{-}T4}} = 10V\mathrm{dc}\end{aligned}\right\} \Rightarrow \mathrm{TSV}_{\mathrm{total}}$$

$$\begin{aligned}&= (2\times 1) + (2\times 2)\\&\quad +(4\times 3) + (4\times 10)\\&= 58V\mathrm{dc}. \qquad (7)\end{aligned}$$

Therefore, the TSV of the H-bridge switches and the overall TSV for N modules are given by:

$$\mathrm{TSV}_{\mathrm{T1-T4}} = (2N+1)\times 2V\mathrm{dc} \qquad (8)$$

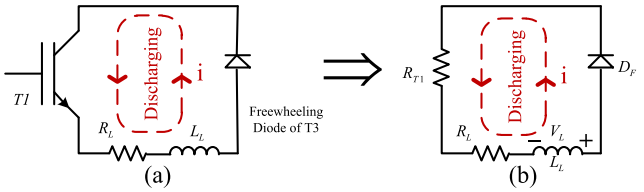

FIGURE 8. (a) The discharge circuit of the H-bridge, (b) the equivalent circuit of the discharge load.

$$\mathrm{TSV_{total}} = (24N + 10) \times V\mathrm{dc} \tag{9}$$

Of all the inverter switches, only the four H-bridge switches must withstand high voltages. The remaining switches have lower TSV and experience lower voltages. The TSV values for the switches in the inverter presented are listed in Table 3. The TSVs for the switches S11 and S12, $S_{(N+1)2}$, $S_{(N+1)1}$, $S_{(N+1)3}$ are constant and equal to 1, 2, and 3, respectively. However, the TSV of the H-bridge switches, T1 to T4, increases according to $(2N + 1) \times 2V\mathrm{dc}$ as the voltage increases. This causes the overall TSV to rise, according to $(24N + 10)V\mathrm{dc}$. The cost function, CF, is given in (10), as shown at the bottom of the next page, by [25], where alpha α is a coefficient that measures the weighting of the TSV and is set equal to 0.5 and 1.5 in two different cases.

TABLE 3. TSV of each of the switches in the presented topology.

N	N_{level}	S11, S12	$S_{(N+1)2}$	$S_{(N+1)1}$, $S_{(N+1)3}$	T1-T4	TSV_{total}
N=0	5	1	-	-	2	10
N=1	13	1	2	3	6	34
N=2	21	1	2	3	10	58
N=N	[4(2N+1)]+1	1	2	3	(2N+1) ×2Vdc	(24N+10) Vdc

D. CIRCUIT ANALYSIS

In the last step of each half cycle of the output waveform, the magnitude of $1V\mathrm{dc}$ becomes zero. Therefore, the circuit will be as a closed RL circuit, in which the inductor energy must be discharged by the circuit resistors. Due to the $1V\mathrm{dc}$ change in voltage, the change in current is high, of course, compared to the PWM switching algorithm. Thus, an RL first-order circuit needs to be solved.

Figure 8 displays the discharge energy of the inductor load. Figure 8(a) shows the discharge circuit of the H-bridge and (b) shows the equivalent current circuit of the discharge. The analysis of the circuit is as follows:

$$V_L + V_{\mathrm{RL}} + V_{\mathrm{FD}} + V_{\mathrm{R_T}} = 0. \tag{11}$$

Which V_L is the load inductor voltage, V_{RL} is the load resistor voltage, V_{FD} is the forward voltage of freewheeling diode of T3, and V_{RT1} is the voltage across the T1 in the "On" situation.

$$L\frac{\mathrm{di}}{\mathrm{dt}} + iR_L + V_{\mathrm{FD}} + iR_T = 0. \tag{12}$$

By ignoring the voltage $V_{\mathrm{FD}} = 0.7\mathrm{V}$, the equation becomes simpler and:

$$\frac{\mathrm{di}}{\mathrm{dt}} = \frac{-(R_L + R_T)i}{L}. \tag{13}$$

According to Table 1, the output voltage across the load is zero in times the t_0-t_1 and the t_{12}-t_{13}. These zero voltages repeat twice in a period of the waveform. The more time of zero voltage, the more time of discharge of the inductive load. By increasing the zero-voltage time, the proposed MLI can operate successfully at higher inductive loads. However, it should be taken into account that extending the zero voltage-time results in an increase in THD. By proceeding to solve (13),

$$\int_0^{i(t)} \frac{\mathrm{di}}{i} = -\int_{t_0}^{t_1} \frac{(R_L + R_T)}{L}\mathrm{dt}. \tag{14}$$

Thus, the current flowing through the circuit becomes:

$$i(t) = I_0 e^{-\frac{(R_L+R_T)}{L}t}, \tag{15}$$

which I_0 is the steady-state current. The steady-state time is about 5τ, which τ is the constant time of the circuit, and is equal to:

$$\tau = \frac{L}{(R_L + R_T)}. \tag{16}$$

The minimum time for discharging the load's inductor is about 5τ. The main problem of reverse current arises at zero voltage and by the time the polarity of the load voltage is changed. It must be taken into account that at the time of zero voltage, the energy of the inductor must be discharged. Therefore:

$$t_0 - t_1 > 5\tau. \tag{17}$$

THD should be taken into account here. Increasing the t_0-t_1 time results in increasing the THD; therefore, a balance between them should be performed. The main reason that the proposed inverter is appropriate for domestic load is that more loads are not inductive. Loads such as lighting, heating, iron, TV, etc., are resistive loads, and sometimes inductive loads such as a refrigerator require less power than other overall resistive loads. Of course, some homes use more inductive loads, but that is not the point here. The combination of all loads is equivalent to a resistive-inductive load, and the proposed MLI is capable of producing a sinusoidal waveform under the constraint the t_0-$t_1 > 5\tau$. This paper focuses on the topology of the multi-level inverter, and the presented switching algorithm only aims to illustrate how this inverter works. In the presented topology, it is assumed that:

$$\Delta t_{t_0-t_1} = \frac{1}{12} \times 10\,\mathrm{ms}{=}0.84\,\mathrm{ms}. \tag{18}$$

Therefore $5\tau < 0.84 \times 10^{-3}$, so:

$$\frac{5L}{R} < 0.84\,\mathrm{ms} \Rightarrow \frac{L}{R} < 0.17 \times 10^{-3}. \tag{19}$$

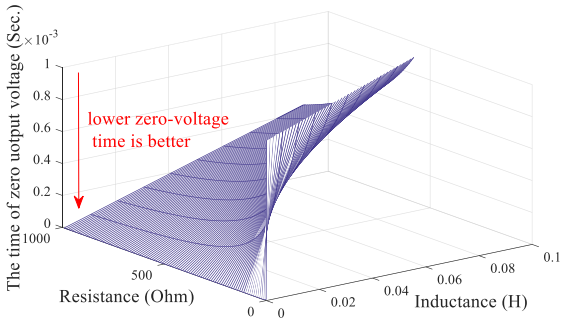

FIGURE 9. The time of output zero voltage range versus resistance, and inductance lower than 100 mH.

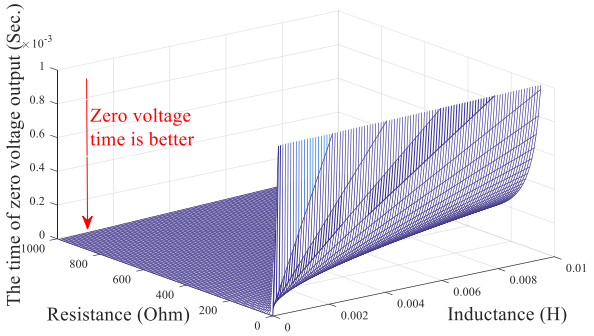

FIGURE 10. The time of output zero voltage range versus resistance, and inductance lower than 10 mH.

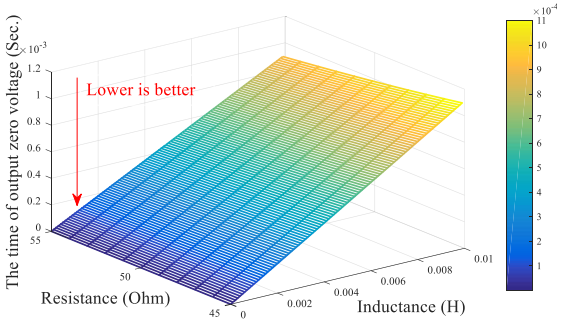

FIGURE 11. Authorized inductance range for 50-ohm resistance.

If the zero-voltage time of a half-cycle is 0.84 ms, the constraint $(L/R) < 0.17 \times 10^{-3}$ should be observed. The zero-voltage time can be changed due to the switching algorithm of MLI. The resistance of the load is 50 Ω, thus, assumed that the switch resistance is 0.3 Ω, the inductive load should not exceed 8.55 mH.

Figure 9, Figure 10 and, Figure 11 show the time of the zero-voltage range of the output voltage versus the resistance and inductance. Based on (16) and (17), these Figures are produced. These curves show that for being in authorized t_0-$t_1 > 5\tau$ time, how much resistance and inductance has to be. There must be a balance between R and L for the proper operation of the presented CSCMLI. In Figure 9 it is shown that there is a possibility to use 100 mH inductance in series RL load, but the resistance should be about 1000 Ω. It is shown that this MLI is suitable for series RL loads with low inductance.

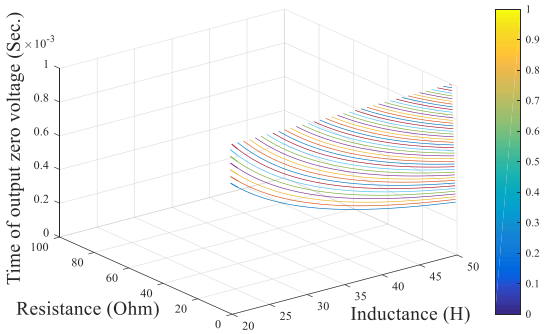

FIGURE 12. The curve of 5τ (maximum zero-voltage time of the load) for parallel RL load.

Figure 10 demonstrates the time of the zero-voltage range of the output versus the resistor, and the inductance smaller than 10 mH when viewed closer. The resistance of the simulation and the experimental test is 50 Ω. Figure 11 shows the curve of zero voltage-time of output voltage for series RL load, whose resistance is 50 Ω. As shown in this figure, the inductance of the load should be lower than about 9 mH.

The limitations in inductance for series RL loads were discussed in this chapter. There are constraints in using this MLI in series RL loads. To obtain the best performance, these Figures' data and comparisons should be considered.

E. ROLE OF FREQUENCY ON INDUCTIVE LOAD INSTANT TIME

So far, an RL load has been discussed in the series. The discussion was about the discharge time of an inductor based on instant time. Now let's discuss parallel RL loads. Figure 13 shows a parallel resistive inductive (RL) load. The equivalent impedance of the parallel RL circuit calculates as follows:

$$Z_{\text{eq}} = R||\text{X}_L = \frac{R \times \text{X}_L}{R + \text{X}_L} = \frac{Rj\omega L}{R + j\omega L} = \frac{jR^2\omega L + R\omega^2 L^2}{R^2 + \omega^2 L^2}. \tag{20}$$

Therefore, the equivalent circuit becomes like Figure 14. Again, the discharging circuit will be like Figure 8. Thus, the

$$\text{CF} = \frac{(N_{\text{switch}} + N_{\text{dr}} + N_{\text{diode}} + N_{\text{cap}} + \alpha\text{TSV}) \times N_{\text{source}}}{\frac{V_{o,\max}}{\sum_{i=1}^{N_{\text{source}}} v\text{dc}_i} N_{\text{level}}}. \tag{10}$$

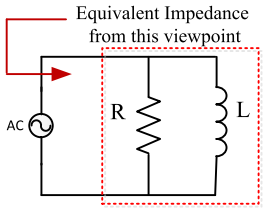

FIGURE 13. Parallel resistive inductive (RL) loads.

total resistance would be:

$$R_{\text{Total}} = R_{\text{Transistor}} + R_{\text{eq}}. \tag{21}$$

Now the instant time τ for inductor discharging will be:

$$\tau = \frac{L_{\text{eq}}}{R_{\text{Transistor}} + R_{\text{eq}}} = \frac{\frac{R^2\omega L}{R^2+\omega^2L^2}}{R_T + \frac{R\omega^2L^2}{R^2+\omega^2L^2}} = \frac{\frac{R^2\omega L}{R^2+\omega^2L^2}}{\frac{R_T(R^2+\omega^2L^2)+R\omega^2L^2}{R^2+\omega^2L^2}} = \frac{R^2\omega L}{R_T(R^2+\omega^2L^2)+R\omega^2L^2}. \tag{22}$$

In a series RL circuit, the resistance of the h-Bridge switch has not much influence on the computation of the instant time and may be ignored, but in a parallel RL circuit, this resistance cannot be neglected.

F. OPERATION OF MLI UNDER THE HIGH INDUCTIVE LOADS

It is discussed that for the best performance of the proposed MLI, the condition t_0-$t_1 > 5\tau$ should be observed. t_0-t_1 is the zero-voltage time of the output voltage across the load. The operating conditions of the series and parallel RL loads are totally different. The proposed MLI is capable of providing the power of parallel RL loads, whose inductance is very high. Figure 12 shows the curve 5τ based on (22), which means that the proposed MLI can handle the inductances between 20-H and 30-H. As shown, if the resistance of the RL load is between 1 Ω – 40 Ω, the MLI can operate correctly within the high inductance loads.

G. CALCULATION OF THE ANGLE AND PULSE TIME OF SWITCHES

The output voltage is the summation of the voltages of the switched capacitors and the DC voltage sources of the cascaded modules. One way to estimate the switching angles is to use the Fourier series [28].

$$f(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(n\omega t) + b_n \sin(n\omega t), \tag{23}$$

$$a_0 = \frac{1}{T}\int_0^T f(t)dt, \tag{24}$$

$$a_n = \frac{2}{T}\int_0^T f(t)\sin(n\omega t)dt, \tag{25}$$

$$b_n = \frac{2}{T}\int_0^T f(t)\cos(n\omega t)dt, \tag{26}$$

Owing to AC and sinus, the coefficients a_n and a_0 are zero.Also, the coefficients b_n for even n are equal to zero, thus:

$$b_n = \frac{4E}{n\pi}\sum_{k=1}^{D}\cos(n\alpha_k) \quad \text{n is odd} \tag{27}$$

$$b_n = 0 \quad \text{for even n.} \tag{28}$$

where α represents the switching angle, b_n describes the amplitude of the nth harmonics, and D is the number of individual DC sources or the maximum achievable level of the output waveform. Some articles use θ instead of α. Therefore, the output voltage can be expressed as:

$$V_{out} = \sum_{n=1}^{\infty}\left[\frac{4E}{n\pi}\sum_{k=1}^{D}\cos(n\alpha_k)\right]\sin(n\omega t). \tag{29}$$

Simplified, the relationship would look like the following:

$$V_{out} = \frac{4E}{n\pi}\sum_{n=1}^{\infty}[\cos(n\alpha_1) + \cos(n\alpha_2) + \ldots + \cos(n\alpha_N)]\sin(n\omega t) \tag{30}$$

Which $0 < \alpha_1 < \alpha_2 < \alpha_3 < \ldots < \alpha_N < \pi/2$ and likewise, the peak value of the nth harmonic is calculated as follows:

$$V_n = \frac{4V_{\text{dc}}}{n\pi}\sum_{n=1}^{\infty}\cos(n\alpha_k). \tag{31}$$

The first harmonic is a useful and ideal harmonic. To achieve a pure sine wave voltage, except for the first harmonic, the magnitude of the other harmonics must be zero. According to (31) the magnitude of the first harmonic is calculated as follows:

$$V_1 = \frac{4V_{\text{dc}}}{\pi}[\cos(\alpha_1) + \cos(\alpha_2) + \ldots + \cos(\alpha_N)] \tag{32}$$

A key factor for acceptable sinusoidal voltage is the low THD of the voltage waveform across the load, which is computed as follows:

$$\text{THD} = \frac{\left(\sum_{n=2}^{\infty} V_n^2\right)^{0.5}}{V_1}, \tag{33}$$

$$V_1 = \frac{4V_{\text{dc}}}{\pi}. \tag{34}$$

Allowing for the $0 < \alpha_1 < \alpha_2 < \alpha_3 < \ldots < \alpha_N < \pi/2$ constraint, setting the individual harmonics except the first harmonic to zero, and considering the optimal THD, the angles of each pulse may be calculated. In this paper, $\alpha_n = t_n$ is shown in Table 1.

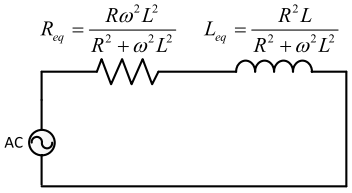

FIGURE 14. The equivalent circuit of parallel RL load.

H. THE SURGE CURRENT ANALYSIS OF THE PROPOSED CSCMLI FOR MEDIUM-POWER AND HIGH-POWER APPLICATIONS

The first issue to be noted is that there is a surge current in all topologies involving switched capacitors, and one of the disadvantages of this type of MLI is the high surge current of the capacitor charge. But in the case of the surge current of the proposed CSCMLI, two main concerns need to be considered: a) the current tolerance by diodes and MOSFETs, b) the ability of the power supply (or DC source) to provide current.

1) THE CURRENT TOLERANCE BY DIODES AND MOSFETs

The influence of the inrush current upon the diodes and semiconductor switches is different, thus they are discussed in two distinct sections as follows.

a: SEMICONDUCTOR SWITCH SELECTION CONSIDERING THE CAPACITORS SURGE CURRENT

As shown in Figure 7, when $V = 0$, the surge current of capacitor C21 flows through H-Bridge switches, S11 switches, and diodes D21 and D22. Therefore, to justify the possibility of using inverters at medium and high power, the design and manufacture of inverters should rely on the use of common components on the market. GTO and thyristor may be used in an H-bridge network. Figure 15 shows that these components can easily be selected with high voltage and current. Semiconductor switches provide in their datasheet a Safe Operation Area (SOA) that can be used to select the correct switch based on the current transit time. In the provided CSCMLI inverter, the MOSFET IRFP450 is used as the switch.

b: DIODE SELECTION CONSIDERING THE CAPACITORS SURGE CURRENT

The terms for diodes are slightly different and more difficult. One limitation of the inrush current intolerance found in semiconductors is the junction temperature. The higher the junction temperature current, the higher the probability of the component failing. Here, assuming the performance of the component at room temperature and that the semiconductor placed in the circuit can withstand that temperature, further analysis is performed. The diode employed in this circuit is SFAF1606G. The maximum average forward Rectifier current of this diode is 16 A and the peak forward peak current in 8.3 ms is 200 A. Since the transient of this current is less

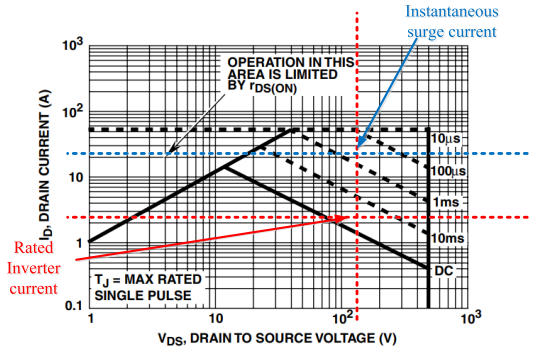

FIGURE 15. The SOA of IRFP450 MOSFET is used to select the correct switch based on the current transit time.

than 1 ms, there will be no problem in the circuit [29]. The relationship of the current flowing through the diode in the forward-bias region is as follows [30]:

$$i = I_S(e^{v/V_T} - 1), \tag{35}$$

which i is the diode current, I_S the saturation current, v is the diode forward bias voltage and the thermal voltage V_T at room temperature is:

$$V_T = \frac{kT}{q} = 25.8 \quad \text{mV}. \tag{36}$$

In (36), $k = 8.6 \times 10^{-5}$ $\left(\text{eV}/\text{K}\right)$ is the Boltzmann's constant and $q = 1.6 \times 10^{-19}$ C is the magnitude of electron charge. The following formula is obtained by simplification:

$$i = I_S e^{v/V_T} \Rightarrow v = V_T \ln\left(\frac{i}{I_S}\right). \tag{37}$$

The objective is to determine that the maximum current can be a multiple of the diode's rated current. Therefore, the proportion of the two currents is considered to determine how much the current of a diode can be in exchange for the forward voltage of the diode.

$$i_1 = I_S e^{V_1/V_T}, i_2 = I_S e^{V_2/V_T} \Rightarrow \frac{i_2}{i_1} = e^{(V_2 - V_1)/V_T}, \tag{38}$$

$$V_2 - V_1 = V_T \ln\left(\frac{I_2}{I_1}\right) \Rightarrow V_2 - V_1 = 2.3V_T \log\left(\frac{I_2}{I_1}\right). \tag{39}$$

Equation (39) shows that for 10 times the current, the forward bias voltage increases by 60 mV. The instantaneous current in Figure 21 is approximately 25 times the maximum output current. If $(I_2/I_1) = 25$ is assumed, then $V_2 - V_1 \gg 83$ mV is obtained. This voltage change is within the acceptable range of most diodes on the market. For example, in the diode, SFAF1606G used in the inverter, $\Delta V_{\max} \approx 850$ mV, which is more than ten times $V_2 - V_1 \approx 83$mV was calculated for 25-times the instantaneous current and can easily pass current in an estimated time of 700 μs [29].

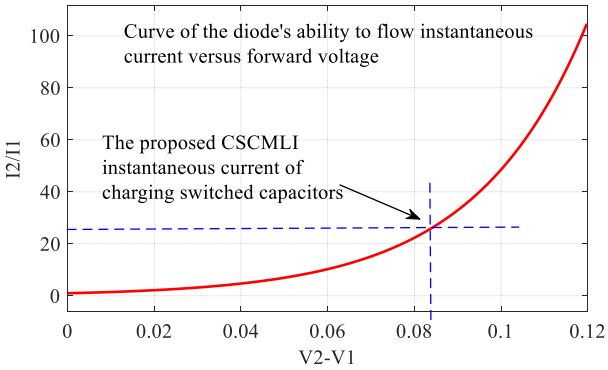

FIGURE 16. The increase in the current ratio I_2/I_1 versus the increase in the V_2 -V_1 forward voltage of the diode.

In Figure 16 the curve shows the increase in the current ratio I_2/I_1 versus the increase in the $V_2 - V_1$ forward voltage of the diode. The junction point shows the instantaneous current passing through the diode when capacitor C21 is loaded. As shown in the figure, the proposed CSCMLI inverter is easily able to charge the switched capacitor through conventional diodes. Each diode can increase the minimum voltage $\Delta V_{\max} = 0.1\,V$ and tolerate it, which corresponds to an instantaneous current of about 50-times the nominal current.

2) THE CAPABILITY OF THE POWER SUPPLY TO PROVIDE SURGE CURRENT

The two power supplies Vdc1 and Vdc2 must also be capable of providing instantaneous current. The tested inverter uses HRP-150N-24 power supplies. This power supply is 150 watts and is easily capable of supplying the required current of 1000 μF capacitors. According to MIL-HDBK-11991, the selected power supply must be capable of delivering twice the demanded load power [31]. Since the approximate total power of the inverter is 180 W, two power supplies of 150 W were used (Adding up the two power supplies is 300 W). Even if a capacitor of 1000 μs is not in the output of this power supply these DC sources are capable of easily supplying the current of 20 A instantaneously in about 700-μs [32].

The relationship between the maximum pulsed power of switching power supplies is as follows [32]:

$$P_{\text{av}} = \frac{(P_{\text{pk}} \times t) + (P_{\text{npk}} \times (T - t)}{T} < P_{\text{rated}}. \quad (40)$$

Which P_{av} is the average output power (W), t is the pulse width of the peak power (s), P_{pk} is the peak output power W, P_{npk} is the non-peak output power (W), T is the period (s), and P_{rated} is the rated power of the power supply (W). Two power supplies Vdc1 and Vdc2 are used in the provided inverter. The surge current is drawn when the output voltage is zero. Concerning (40), the power P_{npk} is the power extracted from the DC source before the output voltage becomes zero, i.e., level one step before zero. At this time, the power supply Vdc2 does not supply any power and $P_{\text{npk},V\text{dc2}=0}$, but the power

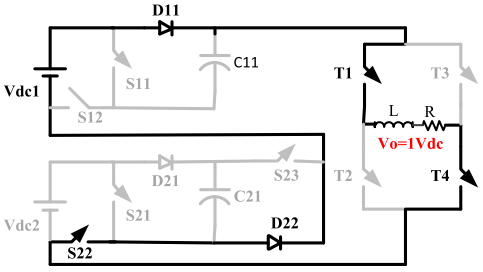

FIGURE 17. The current path when the output voltage is one level of voltage.

supply Vdc1 is responsible for supplying the power of the first step of the output voltage waveform. Figure 17 shows the connection of power supply Vdc1 in the first level of output voltage and the corresponding current. The current flowing in the bold black path results in generating one voltage level (24 V) across the load.

By simplifying (40), the relationship for calculating the maximum pulsed power is obtained as follows:

$$P_{\text{pk}} = \frac{1}{t}\left(T \times P_{\text{av}} - P_{\text{npk}}\,(T - t)\right), \quad (41)$$

$$P = VI, \quad (42)$$

If in (41), $T = 0.02$ s, $t = 700\ \mu$s, and $P_{\text{npk}} = 0$ owing to the zero level of the output voltage, the result is $P_{\text{pk}} = 4700$ W. If this power is divided by 24 V, a current of 371 A is obtained. This means that this 150 W power supply easily is capable of delivering 371 A in 700 μs at 50 Hz frequency. Therefore, this power supply and similar power supplies are easily capable of delivering this instantaneous surge current. If the Kirchhoff (42) is put in (41), the current equation is obtained as follows:

$$I_{\text{pk}} = \frac{1}{t}\left(T \times I_{\text{av}} - I_{\text{npk}}\,(T - t)\right). \quad (43)$$

In Vdc2, the current $I_{\text{npk}} = 0$, so the maximum pulsed current supplied by the power supply, for the period variations (frequency) of the output voltage, and the duration of the surge current is shown in Figure 18.

In contrast to Vdc2, I_{npk} takes a value in the supply Vdc1. The equivalent impedance of the load is equal to

$$Z_{\text{eq}} = R_L + jX_L. \quad (44)$$

And the magnitude of the impedance will be equal to:

$$|Z_{\text{eq}}| = \sqrt{R_L^2 + X_L^2}. \quad (45)$$

Thus, due to the stepped voltage level, which is DC in the corresponding time interval, and $R_L \gg X_L$, the inductance may be neglected. As a result, the current of one-step voltage will be approximately equal to:

$$I_{\text{npk}} = \frac{V}{Z_{\text{eq}}} = \frac{V}{\sqrt{R_L^2 + X_L^2}} \approx 0.5. \quad (46)$$

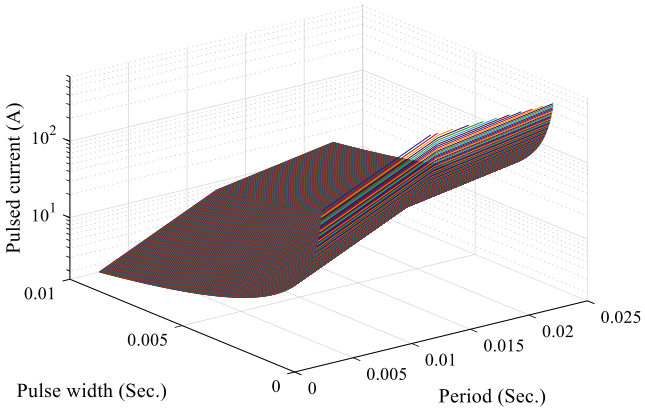

FIGURE 18. The maximum pulse current supplied by the power supply, for the period variations of the output voltage, and the duration of the surge current.

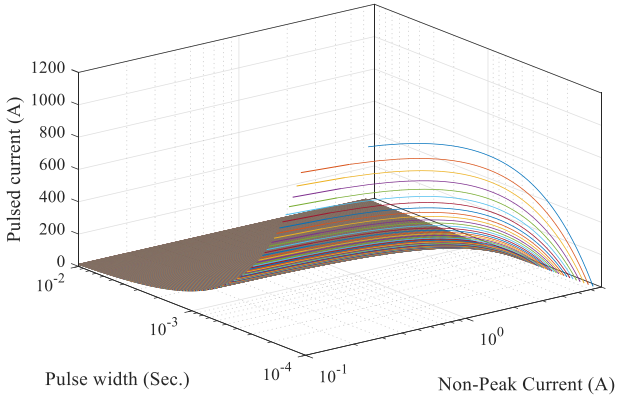

FIGURE 19. The peak pulsed output current of the power supply curve, with variables, non-peak current, and pulse width.

I_{npk}, obtained from (46), is the current one-level output voltage of the power supply for the load of 5 Ω. As the load changes, the magnitude of the current also changes. Figure 19 shows the peak output current of the power supply curve, with variables I_{npk} and pulse width. From Figure 19, it is clear that the higher the pulse width and the non-peak current, the lower the ability to provide pulse current, but the proposed inverter has the ability to operate in medium and high-power applications.

I. LOSS CALCULATION AND EFFICIENCY ANALYSIS

The loss power of each capacitor bank includes both losses due to ESR and capacitor leakage losses. The relationships for calculating capacitor losses are as follows [33]:

$$P_{\mathrm{C,loss}} = P_{\mathrm{C,lealage}} + P_{\mathrm{ESR}}, \tag{47}$$

$$P_{\mathrm{C,lealage}} = V_C \times I_{\mathrm{leakage}}, \tag{48}$$

$$P_{\mathrm{ESR}} = R_{\mathrm{ESR}} I_o^2. \tag{49}$$

where $P_{\mathrm{C,\,loss}}$ is the loss power of the capacitor, $P_{\mathrm{C,\,leakage}}$ is the leakage loss power, P_{ESR} is the ESR loss power, V_C is the capacitor voltage, I_{leakage} is the leakage current, R_{ESR} is the ESR resistance, and I_{o} is the current of the capacitor.

The proposed CSCMLI inverter loss power should be calculated using the following formula:

$$P_{\mathrm{loss}} = P_{(\mathrm{L,V_{out}=0})} + P_{(\mathrm{L,V_{out}\neq 0})}, \tag{50}$$

where $P_{\mathrm{L,\,Vout=0}}$ is the loss power when the output voltage is equal to zero, and $P_{\mathrm{L,\,Vout\neq 0}}$ is the conduction loss power of non-zero voltage. Since these losses repeat twice in each cycle, the power for each half cycle is calculated and finally multiplied by two, thus calculating the power losses of a full cycle, so we may state:

$$P_{\mathrm{loss,full\text{-}cycle}} = 2\left(P_{(\mathrm{L,V_{out}=0})} + P_{(\mathrm{L,V_{out}\neq 0})}\right)_{\mathrm{half\text{-}cycle}}, \tag{51}$$

where $P_{\mathrm{loss,\,full-cycle}}$ is the full cycle losses of the inverter. First, situation $P_{\mathrm{L,\,Vout=0}}$ is analyzed. When the output voltage is zero, the energy of the coil is discharged into the circuit loop formed as shown in Figure 8. Kirchhoff's law of power calculation is:

$$P = v(t)i(t). \tag{52}$$

At zero voltage, as shown in Figure 7 and Tables 1 and 2, at $V_{\mathrm{out}} = 0$, a current path is established to charge capacitor *C21*, so the losses consist of discharge of inductor energy at the H-bridge and losses of the current path. In the formed voltage loop, the power loss can be expressed by the following relationship:

$$P_{(\mathrm{L,V_{out}=0})} = \left(\begin{array}{l} P_{\mathrm{C21,loss}} + P_{\mathrm{C11,loss}} + \left(P_{\mathrm{loss,H\text{-}bridge}}\right) \\ + \left[I^2_{(\mathrm{V_{out}=0})} \times \left(R_{T1} + R_{T2} + R_{\mathrm{S11}}\right) \right] \\ + I_{(\mathrm{V_{out}=0})} \times \left(V_{\mathrm{D21}} + V_{\mathrm{D22}}\right) \end{array} \right)_{t_0}^{t_1}. \tag{53}$$

where $P_{\mathrm{loss,H-bridge}}$ is the H-bridge switches loss, $P_{\mathrm{C21,loss}}$ is the C21 capacitor loss, $P_{\mathrm{C11,loss}}$ is the C11 capacitor loss, $\mathrm{R_{T1}}$, R_{T2}, and R_{S11} are the resistance of T1, T2, and S11 switches, respectively. V_{D21} and V_{D22} are the forward voltages of D21 and D22 diodes. The power loss due to the energy discharge of the inductor is equal to $P_{\mathrm{loss,\,H-bridge}}$, thus according to (14), the current of the energy discharge of the coil is equal to:

$$i_{(L,V_{\mathrm{out}}=0)}(t) = \frac{V_{\mathrm{dc}}}{(R_T + R_L)} \times e^{-\left(\frac{R_T+R_L}{L}\right)t}, \tag{54}$$

$$V_L(t) = L\frac{\mathrm{di_L t}}{\mathrm{dt}}, \tag{55}$$

$$t_{\max} = 5\tau = 5 \times \frac{L}{R_T + R_L}, \tag{56}$$

$$V_L(t) = L\frac{\mathrm{di_L t}}{\mathrm{dt}} = L \times \frac{\mathrm{d}}{\mathrm{dt}}\left(\frac{V_{\mathrm{dc}}}{(R_T + R_L)} \times e^{-\left(\frac{R_T+R_L}{L}\right)t}\right), \tag{57}$$

$$V_L(t) = -V_{\mathrm{dc}} \times e^{-\left(\frac{R_T+R_L}{L}\right)t}, \tag{58}$$

$$P_{\mathrm{Loss,H\text{-}bridge}} = \frac{1}{5\tau}\int_{0=t_0}^{5\tau=t_1}\left(\frac{-V_{\mathrm{dc}}^2}{(R_T+R_L)}\right)\times e^{-2\left(\frac{R_T+R_L}{L}\right)t}\mathrm{dt}, \tag{59}$$

$$P_{\mathrm{Loss,H\text{-}bridge}} \approx \frac{-V_{\mathrm{dc}}^2}{5L}\int_{0=t_0}^{5\tau=t_1} e^{-2\left(\frac{R_T+R_L}{L}\right)t}\mathrm{dt}. \tag{60}$$

To calculate the losses along the rest of the voltage path, it is also necessary to calculate the $I_{\mathrm{Vout=0}}$ current. $I_{\mathrm{Vout=0}}$ current is equal to the charging current of capacitor *C21*. The charging current of capacitor C21 is equal to:

$$I_{(\mathrm{V_{out}=0})} = I_{\mathrm{C21}} = C_{21}\frac{\mathrm{dV_{21}}}{\mathrm{dt}}. \tag{61}$$

I_{C21} is the current of capacitor C21, which is located three times in the path of the formation of the charge loop to generate the voltage levels of 4-6, that is shown in Figure 7. Hence, again, according to the (61), the capacitor voltage droop may be calculated as follows:

$$dV_{21} = \frac{1}{C_{21}}I_{C21} \Rightarrow \int dV_{21} = \frac{1}{C_{21}}\int I_{C21}. \tag{62}$$

According to Table 1, C21 is in the load path from time *t4-t9*, and the current flowing through it is equal to the load current. Therefore, (62) will be equal to (63), as shown at the bottom of the next page, where Z_L is the load impedance, d V_{21} droop, or capacitor voltage drop C21 when $V_{\mathrm{out}\neq 0}$. When there is voltage across the load, capacitor C21 is discharged, and this discharge of the capacitor causes a voltage droop. In the above relationship, the voltage droop of capacitor C11 is ignored because it is continuously charged.

At the time $V_{\mathrm{out=0}}$, capacitor C11 is discharged and C21 is charged, so the losses of both capacitors must be included in the calculation of losses. Thus, in half a cycle:

$$P_{\mathrm{C,loss}} = P_{\mathrm{C,lealage}} + P_{\mathrm{ESR}}, \tag{64}$$

$$P_{\mathrm{C,loss,total}} = P_{\mathrm{loss,C11}} + P_{\mathrm{loss,C21}}, \tag{65}$$

$$P_{\mathrm{C21,lealage}} = V_{\mathrm{C21}} \times I_{\mathrm{leakage,C21}}\Big|_{t_0}^{t_1}, \tag{66}$$

$$P_{\mathrm{C11,lealage}} = V_{\mathrm{C11}} \times I_{\mathrm{leakage,C11}}\Big|_{t_0}^{t_1}, \tag{67}$$

$$P_{\mathrm{ESR}} = R_{\mathrm{ESR}}I^2 \Rightarrow \begin{cases} P_{\mathrm{ESR,C21}} = \dfrac{1}{(t_1-t_0)}\displaystyle\int_{t_0}^{t_1} R_{\mathrm{ESR,C21}} \times I_o^2\mathrm{dt} \\ P_{\mathrm{ESR,C11}} = \dfrac{1}{(t_1-t_0)}\displaystyle\int_{t_0}^{t_1} R_{\mathrm{ESR,C11}} \times I_o^2\mathrm{dt}. \end{cases} \tag{68}$$

TABLE 4. Components that cause losses in each level voltage loop.

Time	Output voltage level	Components
t_1-t_2, t_{11}-t_{12}	$1V\mathrm{dc}$	S12, S22, T1, T4, D11, C11
t_2-t_3, t_{10}-t_{11}	$2V\mathrm{dc}$	S12, S23, T1, T4, D11, D21, C11
t_3-t_4, t_9-t_{10}	$3V\mathrm{dc}$	S11, S23, T1, T4, C11, D21
t_4-t_5, t_8-t_9	$4V\mathrm{dc}$	S12, S22, S23, T1, T4, D11, C11, C21
t_5-t_6, t_7-t_8	$5V\mathrm{dc}$	S12, S21, S23, T1, T4, D11, C11, C21
t_6-t_7	$6V\mathrm{dc}$	S11, S21, S23, T1, T4, C11, C21

where $P_{\mathrm{C,loss}}$ is the loss of the capacitor C, $P_{\mathrm{C,leakage}}$ is the leakage loss, and P_{ESR} is the ESR loss of the capacitor C. $P_{\mathrm{C,loss,total}}$ is the total loss of the capacitors *C11* and *C21*.

Through (53)-(68), the CSCMLI loss power at time zero is obtained. The loss power $P_{\mathrm{L,\ Vout\neq 0}}$ is equal to the total loss power of the loops of each voltage level in Figure 7. Using Table 1 and Figure 7, by forming voltage loops in each path, the power loss at each voltage level can be calculated according to the following equation:

$$P_{(\mathrm{L,V_{out}\neq 0})} = \frac{1}{(t_{12}-t_1)}\int_{t_1}^{t_{12}} P_L\mathrm{dt}. \tag{69}$$

where, P_L is the loss power of the inverter. Table 4 lists the electronic components that have losses at any given time. Between each time point, the losses of the components are calculated separately, and ultimately the summation of these losses is the power loss when the voltage across the load is not zero.

The drain-source resistance of each MOSFET is listed in its datasheet, therefore, the MOSFET loss power is calculated using (73). The diode losses are calculated using (74)). The forward voltage curve of each diode depends on the current. By extracting the voltage-current fitness curve of each diode, the loss power of each diode can also be calculated [34], [35]. Another point is to consider the losses of capacitor banks C11 and C21. The current through each capacitor is known, so by extracting the ESR of each capacitor of the capacitor bank, and calculating the impedance equivalent to the ESR, these losses should also be calculated. The diode, MOSFET, and capacitor losses are thus:

$$P = RI^2, \tag{70}$$

$$P = VI, \tag{71}$$

$$P_{\mathrm{ESR}} = R_{\mathrm{ESR}} \times I^2 \Rightarrow P_{\mathrm{ESR,C21}} = \frac{1}{(t_9-t_4)}\int_{t_4}^{t_9} R_{\mathrm{ESR,C21}} \times I_o^2\mathrm{dt}, \tag{72}$$

$$P_{\mathrm{MOSFET,loss}} = \frac{1}{T}\sum_{i=1}^{n}\left(E_{\mathrm{On(i)}} + E_{\mathrm{Off(i)}} + E_{\mathrm{rr(i)}}\right). \tag{73}$$

where E_{OFF} and E_{ON} are the energy needed to turn OFF and ON the MOSFET, respectively, E_{rr} is the diode recovery loss,

TABLE 5. The efficiency of the CSCMLI inverter at three different loads.

Load	Loss (W)	Load (W)	Input (W)	Efficiency (%)
25 Ω + 10 mH	45	255	300	85
50 Ω + 10 mH	21	142	163	87
100 Ω + 10 mH	11	50	61	82

and n is the number of steps in a fundamental period of T.

$$P_{\text{diode,loss}} = \frac{1}{T}\int_0^T \left(V_F + R_{\text{ON}} i_F\right) i_F \,\text{dt}. \tag{74}$$

In which T is the fundamental frequency period, V_F represents the forward voltage drop, R_{ON} represents the forward resistance, and i_F represents the forward current through the device.

The efficiency of the inverter varies depending on the type and magnitude of the load. Table 5 shows the efficiency of the CSCMLI inverter at three different loads. The indicated efficiency is based on the datasheet of the components used in the proposed CSCMLI inverter. If the optimal components are used, the efficiency is increased, for example, if the MOSFET is used with a lower drain-source resistance, or if the capacitor is used with a lower ESR, the efficiency is improved. The proposed inverter was only a prototype to evaluate the inverter performance and was not an optimized efficiency target.

III. COMPARISON

A. COMPARISON WITH OTHER 13-LEVEL INVERTERS

Table 7 shows the results of a comparison between the proposed inverter and various 13-level inverters from recent publications. The primary objective was to reduce the number of switches. It is observed that the topology reported in [36] is the only configuration with fewer switches than the inverter proposed in this study. This is due to the one additional DC source used in the inverter presented in [36]. Despite the inclusion of an H-bridge, the present 13-level topology used a total of nine switches and only two DC sources. In contrast, the topology presented in [36], which is not a switched capacitor inverter, used eight switches but three DC sources. The additional DC source compensated for the one less switch. As a result, the proposed inverter uses the least number of switches compared to other similar inverters with the same conditions. The total number of semiconductors used in the present topology was eleven, which is a relatively small number compared to similar topologies. The inverter reported in [36] used eight semiconductors, but three DC sources, as mentioned earlier. Reference [37] used twelve semiconductors but fourteen switches for a similar inverter.

Reference [45] is one of the major investigations of 13-level MLI which used ten switches, one dc source, four diodes, and four capacitors. For the devices using one dc source, this article used a minimum of switches, compared to other similar MLIs. The application of this MLI is different from the proposed MLI. Our proposed MLI uses nine switches, but [45] used ten switches. It cannot be claimed that our proposed MLI is better than [45], but for two DC source applications, the proposed MLI has the minimal use of switches, diodes, and capacitors. The advantages of the proposed MLI over [45] are as follows: a) Our proposed MLI uses two DC sources, so the power demand of the load is distributed among them. The proposed MLI needs two low-power DC sources, but [45] needs one higher-power DC source, which would have to provide the total power by itself. b) Reference [45] uses four capacitors, so the peak currents are larger than in the proposed MLI. c) In [45], one DC source

$$\begin{aligned}
\text{dV}_{21} &= \frac{1}{C_{21}}\int_{t_4}^{t_9} I_o \text{dt} \\
&= \frac{1}{C_{21}} \times \left[\begin{array}{l}
\left(\int_{t_4}^{t_5} \frac{4V_{\text{dc}}}{Z_L}\text{dt}\right) + \left(\frac{\int_{t_5}^{t_6} 5V_{\text{dc}} - \left(1/C_{21}\right)\left(\int_{t_4}^{t_5} \frac{4V_{\text{dc}}}{Z_L}\text{dt}\right)}{Z_L}\right) \\
+ \left(\frac{\int_{t_6}^{t_7} 6V_{\text{dc}} - \left(1/C_{21}\right)\left(\int_{t_4}^{t_5} \frac{4V_{\text{dc}}}{Z_L} dt + \int_{t_5}^{t_6} \frac{5V_{\text{dc}}}{Z_L}\text{dt}\right)}{Z_L}\right) \\
+ \left(\frac{\int_{t_7}^{t_8} 5V_{\text{dc}} - \left(1/C_{21}\right)\left(\int_{t_4}^{t_5} \frac{4V_{\text{dc}}}{Z_L}\text{dt} + \int_{t_5}^{t_6} \frac{5V_{\text{dc}}}{Z_L}\text{dt} + \int_{t_6}^{t_7} \frac{6V_{\text{dc}}}{Z_L}\text{dt}\right)}{Z_L}\right) \\
+ \left(\frac{\int_{t_8}^{t_9} 4V_{\text{dc}} - \left(1/C_{21}\right)\left(\int_{t_4}^{t_5} \frac{4V_{\text{dc}}}{Z_L}\text{dt} + \int_{t_5}^{t_6} \frac{5V_{\text{dc}}}{Z_L}\text{dt} + \int_{t_6}^{t_7} \frac{6V_{\text{dc}}}{Z_L}\text{dt} + \int_{t_7}^{t_8} \frac{5V_{\text{dc}}}{Z_L}\text{dt}\right)}{Z_L}\right)
\end{array}\right]
\end{aligned} \tag{63}$$

TABLE 6. Comparison of our proposed inverter with [2] and [49] based on DC sources and modules.

	Pro. CSCMLI	[49, Sec. 4.2]	[49, Sec. 4.3]	[2]-1	[2]-2
N_M	k	k	k	k	k
N_{level}	$8k$-3	$4k$+1	$4k$+1	5^k	$\left(2\times3^k\right)-1$
$N_{\text{switch,NH}}$	$3k$-1	$4k$	$3k$+2	$6k$-4	$3k$
$N_{\text{switch,H}}$	$3k$+3	$4k$+4	$3k$+6	$6k$	$3k$+4
N_{cap}	k	$2(k$-1)	$2(k$-1)	k	k
N_{dr}	$2k$-1	$2(k$-1)	$2(k$-1)	k	$2k$
V_{pk}	$2V_1+4\sum_{j=2}^{k}V_j$	kV_{in}	kV_{in}	$2\sum_{j=1}^{k}V_j$	$2\sum_{j=1}^{k}V_j$
N_{source}	k	1	1	k	k

must supply the peak currents, but in the proposed MLI they are distributed among two DC sources.

In the inverter reported in [38], eleven switches were also used. Using fewer diodes is a favorable design choice while increasing the number of switches reduces system reliability [39]. The presented design used two capacitors and had a TSV of 5.6. It used two DC sources, which was less compared to the number of DC sources in the other similar topologies. As the number of modules increased, only the TSV of the four H-bridge switches above the load was increased, while the TSV of the other switches remained the same. The TSV per unit is obtained by:

$$\text{TSV}_{\text{Pu}} = \text{TSV} \Big/ V_{\text{out,Peak}} \tag{75}$$

The comparison of the equations of our proposed CSCMLI, [2] and [49] as a function of the number of modules k is shown in Table 6.

A comparison of all the different 13-level inverters from recent publications, as shown in Table 7, indicates a balance in the proposed configuration. Semiconductors are more likely to fail compared to passive components, such as capacitors. In other words, with fewer semiconductors (relative to the number of passive components), the probability of system failure is significantly reduced. Simply put, system reliability is improved. One advantage of the proposed inverter topology is the higher reliability achieved by reducing the number of switches.

B. COMPARISON WITH SWITCHED-CAPACITOR TOPOLOGIES HAVING 2 DC SOURCES

To validate the proposed topology in terms of cost and number of components used, it is more appropriate to compare this inverter with similar inverters employing two power supplies. Calculating CF using (10) reveals that can significantly increase the cost function and a reduction in output power leads to lower costs, which could not be taken into account in the CF ratio. One of the disadvantages of this formula is that the cost factor cannot be calculated precisely and accurately, and an increase in the number of input power supplies does not necessarily mean a cost increase of the amount envisioned. Hence, the research publications on 13-level inverters with two DC sources have been compiled

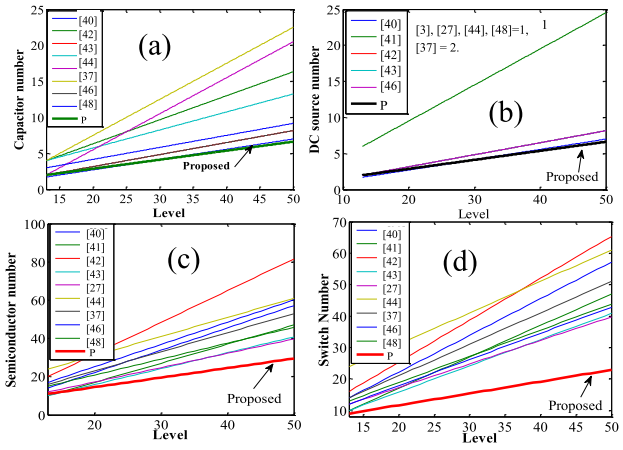

FIGURE 20. The comparison results. (a) Capacitor number vs Level, (b) DC source number vs Level, (c) Semiconductor number vs Level, (d) Switch number vs Level.

in a separate table for comparison. Table 8 shows the results of the comparison of switched-capacitor inverters with two sources. It can be observed that the CF and other parameters of the proposed configuration were lower compared to other similar configurations. The comparison indicates that the number of parameters for the proposed inverter is the lowest compared to similar inverters. Based on data collected from several publications on the subject, equations for the number of switches, diodes, dc sources, and capacitors as a function were derived and are given in Table 9. It should be noted that in some studies the method of cascade modulus expansion was not specified. Therefore, according to the information in the articles, the author has derived new formulas to extend the inverter cascading. To clarify and better understand the cascade expansion of the modules, the proposed configuration was compared with the other inverter topologies. The number of modules was increased for the configurations reported in the latest publications that allowed such an increase (and explained how it could be done). The number of modules was increased for the configurations reported in the most recent publications that allowed such an increase (and explained how it could be done).

Figure 20 shows the curves of the number of capacitors, the total number of semiconductors, the number of switches, and the number of DC sources, all as a function of the number of levels. The curves show that as the number of modules and levels increases, the proposed SCMLI topology requires the fewest power switching devices, the fewest total number of semiconductors, and the fewest capacitors compared to the other topologies. The main advantage of the proposed configuration over the other MLIs with the same number of levels is the smaller number of components and switches.

C. SUMMARY OF THE COMPARISON

Table 7 gives the comparison of the presented Cascaded Switched-Capacitor multi-level inverter with different

TABLE 7. Comparison of some new 13-level investigated multi-level inverter.

Ref. Year	n_{level}	N_{SW}	N_{dr}	PVS	N_{sem}	N_d	N_{dc}	N_C	TSV-Pu	Gain	CF, $\alpha=0.5$	CF, $\alpha=1.5$	Voltage Boosting
[3]-2020	13	12	12	0.67	16	4	1	4	4.33	6	0.438	0.494	Yes
[27]-2020	13	12	12	2	12	0	1	4	6	6	0.397	0.474	Yes
[36]-2019	13	8	8	5	8	0	3	0	4	1	4.154	5.077	No
[37]-2021	13	14	14	6	16	2	2	4	6	3	1.897	2.205	Yes
[38]-2020	13	11	10	6	12	1	2	1	6.33	3	1.342	1.666	Yes
[40]-2019	13	14	9	6	14	0	2	2	10.66	3	1.555	2.102	Yes
[41]-2018	13	16	15	6	16	0	6	0	No data	1	--	---	No
[42]-2019	13	16	16	6	20	4	2	4	5.33	3	2.188	2.461	Yes
[43]-2019	13	15	15	3	15	0	3	3	4	2	4.038	4.500	Yes
[44]-2020	13	24	24	1	24	0	1	13	4	13	0.373	0.396	Yes
[45]-2020	13	10	5	6	14	4	1	4	5.5	6	0.330	0.401	Yes
[46]-2020	13	12	12	6	14	2	2	2	6.33	3	1.598	1.923	Yes
[47]-2021	13	14	14	3	15	1	1	3	5.5	6	0.446	0.516	Yes
[48]-2020	13	13	9	3	15	2	1	3	5.33	6	0.551	0.962	Yes
[49, Sec. 4.2]-2020	13	16	16	3	20	4	1	4	4.88	3	1.29	2.53	Yes
[49, Sec. 4.3]-2020	13	15	15	3	19	4	1	4	5.27	3	1.13	2.22	Yes
Pro.	**13**	**9**	**7**	**6**	**12**	**3**	**2**	**2**	**5.6**	**3**	**1.323**	**1.610**	**Yes**

n_{level}: number of levels, N_{SW}: number of switches, N_{dr}: Number of drivers, PVS: Peak voltage stress, N_{sem}: total number of semiconductors, N_d: number of diodes (including antiparallel and series connected to a MOSFET), N_{dc}=number of dc, voltage sources, N_C= Number of capacitors, TSV_{Pu}= Total standing voltage (in per unit).

TABLE 8. Comparison of similar 13-level switched-capacitor inverters including two DC sources.

Ref.	N-level	N_{SW}	N_{dr}	PVS	N_{sem}	N_d	N_{dc}	N_C	TSV-Pu	CF, $\alpha=$ 0.5	CF, $\alpha=$ 1.5
[37]-2021	13	14	14	6	16	2	2	4	6	1.89	2.20
[38]-2020	13	11	10	6	12	1	2	1	6.33	1.34	1.67
[40]-2019	13	14	9	6	14	0	2	2	10.66	1.55	2.10
[42]-2019	13	16	16	6	20	4	2	4	5.33	2.19	2.46
[46]-2019	13	12	12	6	14	2	2	2	6.33	1.6	1.92
Proposed	**13**	**9**	**9**	**6**	**12**	**3**	**2**	**2**	**5.67**	**1.32**	**1.61**

topologies of 13-level inverters including various types of topologies, and Table 8 gives the comparison of the presented inverter with 13-level inverters using cascaded switched capacitor topology. The last row of each table indicates the characteristics of the presented inverter, which is relatively better than other inverters. An attempt has been made to review and compare all relevant new articles. Compared articles are organized in a better rank than older articles. For all articles, the year of publication of the article has also been given. The formula for increasing the number of switches, semiconductors, DC source, and switching capacitor was extracted from the data of each reference (there were no formulas in the articles) and is shown in Table 9. The curves of Figure 20 compared the increasing voltage levels versus increasing switch, semiconductor, DC source, and switching capacitor of the presented CSCMLI with other inverters. The superior state of the presented CSCMLI compared to other inverters is indicated by an arrow in the figures.

IV. SIMULATION

The proposed topology was simulated in MATLAB /Simulink. The simulation parameters are given in Table 10.

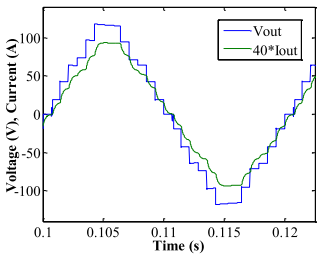

FIGURE 21. Output (current) and (voltage) across the load.

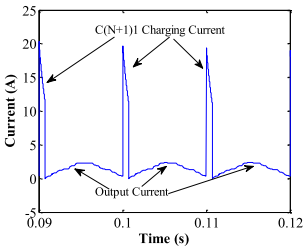

FIGURE 22. Current flowing through the H-bridge switches.

The frequency of the output voltage was 50 Hz and a resistive-inductive load was considered. At 0.1 s, the load was changed from 50 Ω+10 mH to 25 Ω+10 mH. Figure 21 shows the voltage and current waveforms across the load. The current has been multiplied by a factor of 40 so that the two waveforms can be compared. Since this is a resistive-inductive load, the current lags slightly behind the voltage. Figure 22 shows the current flowing through the H-bridge switches. The value of this surge current is always positive, even when the polarity of the voltage across the load is reversed by the H-bridge. It can be observed that the surge

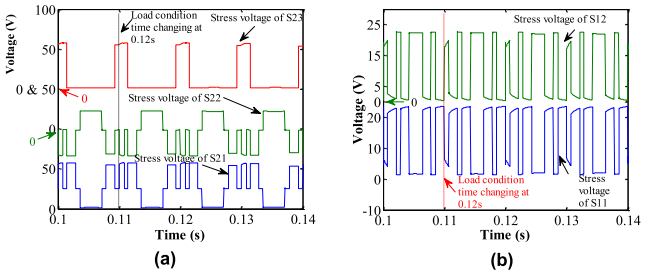

FIGURE 23. Stress voltage of (a) S21, S22, S23, (b) S11, S12.

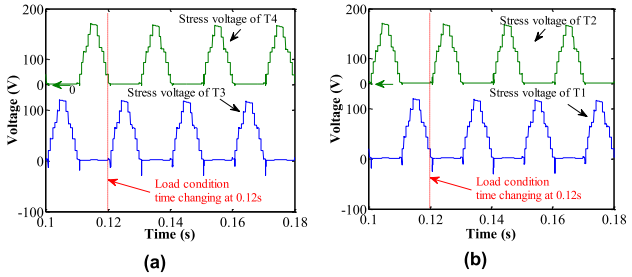

FIGURE 24. Stress voltage of H-bridge switches, (a) T3 and T4, (b) T1 and T2.

current drawn to charge capacitor C21 resembles an impulse response. When the voltage across the load is zero, three switches of the H-bridge were turned on and let the current flow. The stress voltage of the module switches is shown in Figure 23. The TSV of the switches S11 and S12, S22, and S23 and S21 was about $1V$dc, $2V$dc, and $3V$dc, respectively. Figure 15 shows the H-bridge switch voltages. It can be observed that the TSV is about $6V$dc. Figure 25 illustrates the waveforms of the output voltage and current and the voltages of C21 and C11 at the time when the load changed from 50 Ω+10 mH to 25 Ω+10 mH. The current was multiplied by 20 in this plot. Once the output resistance was reduced and thus the power was increased to a required value, the current increased accordingly while the voltage waveform remained unchanged.

The voltage ripple in C11 and C21 increased from 2.6 V to 3.5 V and 2.5 V to 3V, respectively. The value of this increase in voltage ripple is shown in Figure 27(a) for both capacitors. The ripple occurs when high currents are drawn from the capacitor. Figure 27 (b) shows the voltages of C11 and C21 for two different loads. When the power demand was increased, the current drawn from the capacitor, the value of the voltage droop, and the voltage ripple increased accordingly. The currents through C21 and C11 are shown in Figure 27 (c) and Figure 27(d) for two different loads. The Figures show that large amounts of current drawn immediately cause large changes in the capacitor voltage. Similarly, there was a sudden change in voltage when large currents flowed into the capacitor in a short time.

The Total Harmonic Distortion (THD) of the voltage and current is shown in Figure 26 for two different loads. After

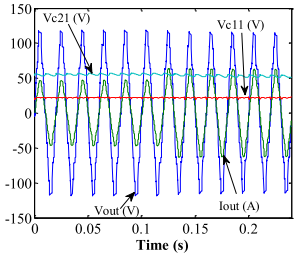

FIGURE 25. Voltage and current of C21 and C11 at the instant of the load changing.

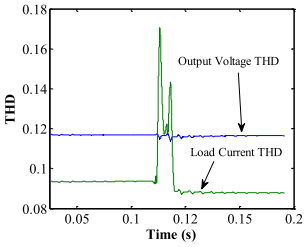

FIGURE 26. Voltage and current THD for two different loads.

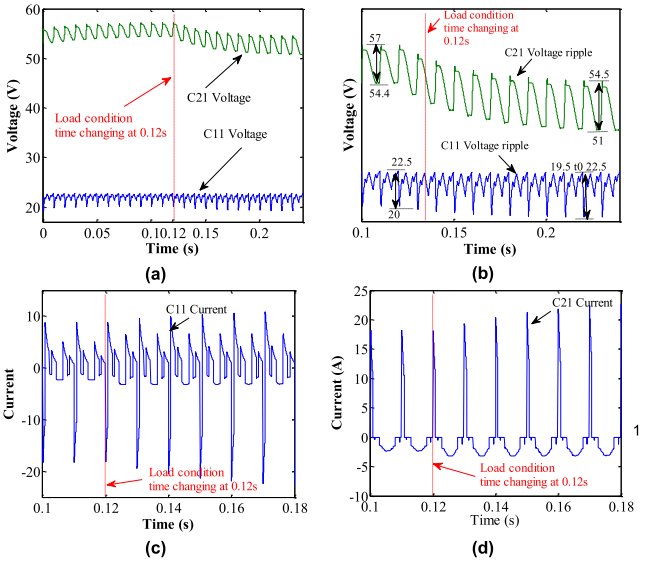

FIGURE 27. (a) The ripple voltages of C11 and C21, (b) The voltages of C11 and C21, (c) The current through C21 for two different loads, and (d) The current through C11.

the power was increased, the THD of both voltage and current improved.

V. EXPERIMENTAL RESULTS

A. EXPLANATIONS OF CONSTRUCTED MLI

The proposed inverter was realized with the components whose specifications are listed in Table 11. A 50 Ω resistor and a 10 mH inductor were used as loads. Figure 29 shows the experimental prototype of the proposed multi-level inverter. In this figure, two of the DC power supplies are used as DC sources and the others are DC-isolated adapters used

TABLE 9. Formula based on N-level and factor.

Ref.	N_{SW}	N_{sem}	N_{dc}	N_C
[3]-2020	$n_{level}-1$	$\frac{1}{2}(3n_{level}-7)$	1	$\frac{1}{2}(n_{level}-5)$
[27]-2019	$\frac{3}{4}(n_{level}+3)$	$\frac{3}{4}(n_{level}+3)$	1	$\frac{1}{4}(n_{level}+3)$
[37]-2021	$n_{level}+1$	$n_{level}+3$	2	$\frac{1}{2}(n_{level}-5)$
[40]-2019	$\frac{7}{6}(n_{level}-1)$	$\frac{7}{6}(n_{level}-1)$	$\frac{1}{7}(n_{level}-1)$	$\frac{1}{7}(n_{level}-1)$
[41]-2018	$n_{level}-3$	$n_{level}-3$	$\frac{1}{2}(n_{level}-1)$	No data
[42]-2019	$\frac{4}{3}(n_{level}-1)$	$\frac{10}{6}(n_{level}-1)$	$\frac{1}{6}(n_{level}-1)$	$\frac{1}{3}(n_{level}-1)$
[43]-2019	$\frac{10}{12}(n_{level}-1)$	$\frac{10}{12}(n_{level}-1)$	$\frac{2}{12}(n_{level}-1)$	$\frac{2}{12}(n_{level}-1)$
[44]-2019	$n_{level}+11$	$n_{level}+11$	1	$\frac{1}{2}(n_{level}-9)$
[46]-2019	$\frac{1}{6}(5n_{level}+7)$	$\frac{1}{6}(7n_{level}+11)$	$\frac{1}{6}(n_{level}-1)$	$\frac{1}{6}(n_{level}-1)$
[48]-2020	$\frac{1}{6}(5n_{level}+13)$	$\frac{1}{6}(5n_{level}+25)$	1	$\frac{1}{6}(n_{level}+5)$
Proposed	$\frac{3}{8}(n_{level}+11)$	$\frac{1}{2}(n_{level}+9)$	$\frac{1}{8}(n_{level}+3)$	$\frac{1}{8}(n_{level}+3)$

TABLE 10. Simulation parameters.

	Parameter	Abbreviation	Value	Unit
1	Diodes Forward Voltage	V_f	0.8	V
2	Diodes Internal Resistance	R_d	0.001	Ω
3	Switches On-State Resistance	R_{on}	0.3	Ω
4	Capacitors	C11 Capacitance	4000	μF
5		C11 ESR	0.01	Ω
6		C21 Capacitance	1333	μF
7		C21 ESR	0.03	Ω
8	Input DC Sources	Vdc1 & Vdc2	24	V
9	Output Frequency	f	50	Hz
10	Load	50 Ω+10 mH and	25 Ω+10 mH	

TABLE 11. Component specifications of the MLI.

Item	Parameter	Part Number
1	Diodes	SFAF1606G
2	Regulators	L7805CV, REF02AU, LF33CPT
3	Switches	IRFP450
4	Drivers	TC4426COA, 6N137
5	Capacitors	C1000uF50v
6	Processor	ATMEGA32A-PU
7	Buffers	SN74HCT240N
8	Current sensors	MAX4080
9	Voltage sensors	ACPL-C87A
10	Op Amp	OP37GP
11	Load	50Ω+10mH

for driving MOSFETs. Table 12 shows the tested inverter specifications. The waveform of the current generated by the modules is shown in Figure 30 which includes the total both

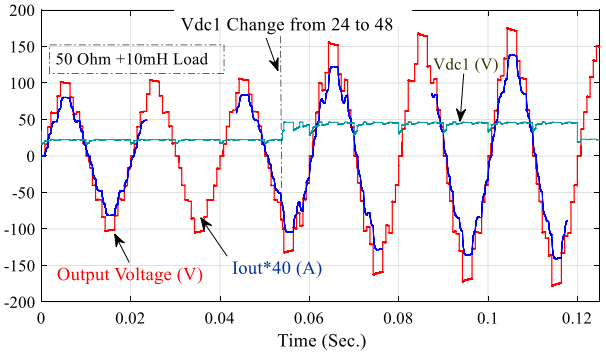

FIGURE 28. Effects of changing Vdc1 DC source on the output voltage and current.

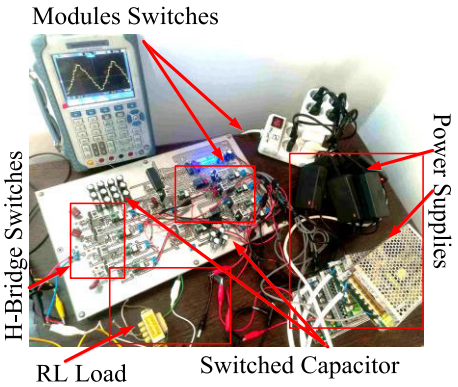

FIGURE 29. The experimental prototype.

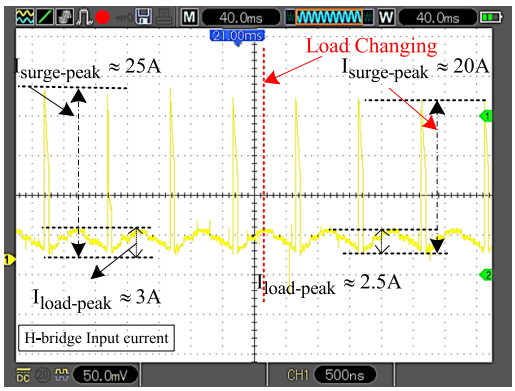

FIGURE 30. Current flowing through the H-bridge including the surge current under load change.

of the load current and the charging current of the capacitors under sudden load change. The sinusoidal half-wave current is the load current and the peak-shaped current is the charging current of the capacitors.

Figure 31, and Figure 32 show the output voltage and current under the sudden load change, respectively. As the energy of the capacitor is discharged, the levels of the waveform across the load experience the droop. The waveform of the load current also becomes slightly more sinusoidal due to the presence of the load inductance. By constructing the proposed inverter, the following goals were achieved: a) power

TABLE 12. Tested inverter specifications.

Item	Specifications	Values	Unit
1	Number of Levels	13	level
2	Input Voltages	2×24	V
3	Peak Output Voltage	119	V
4	Output Power	178	VA
5	THD	12	%
6	Peak Efficiency	96.45	%

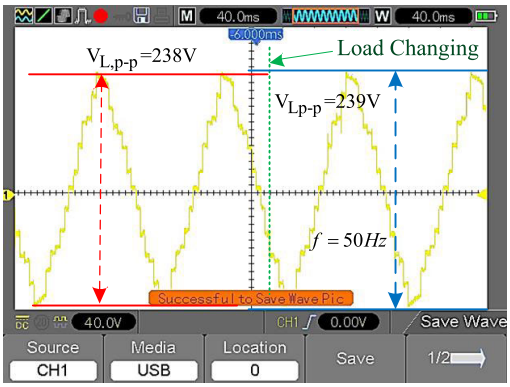

FIGURE 31. The output voltage under the load change.

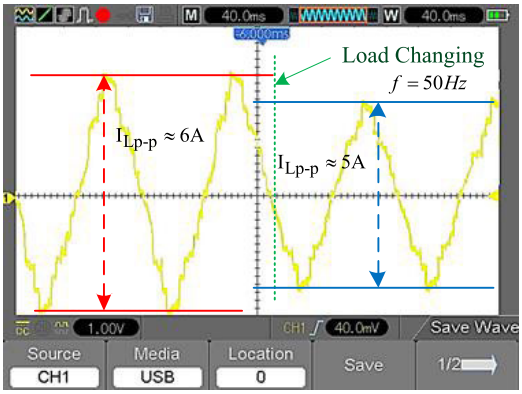

FIGURE 32. The output current under load change.

supplies could provide the needed energy from capacitors, and b) switched capacitors could provide the required energy to shape the waveform, c) power supplies could provide the needed energy from capacitors, and d) switched capacitors could provide the required energy to shape the waveform.

To evaluate the appropriate behavior and correct performance of the presented topology, the mentioned multi-level inverter was constructed and tested on a smaller scale. The required pulses were generated by an ATMEGA32 microcontroller. Although the inverter was tested at 50 Hz, the supplied inverter is easily capable of operating at 400 Hz or higher frequencies. This inverter is independent of the power factor and can supply more power if it uses a capacitor bank with sufficient capacitance. Another advantage of this inverter is that the capacitors charge in a self-balancing manner. Looking at the voltage waveform across the load, the TSV value also matches the simulation.

The modules' switch TSVs are fixed at a maximum of $3V$dc, so higher voltages can easily be generated with this topology. As the voltage across the load increases, only the TSV of the H-bridge switches increases, and due to the low switching frequency of the H-bridge switches, even a relay or thyristor can be used in this section to create a high-voltage sine waveform with commercially available and inexpensive components.

B. DISCUSSION OF THE PROPOSED CSCMLI

One of the differences between H-bridge switches in the proposed topology compared to conventional PWM inverters is the switching frequency. In the proposed structure, the switching frequency of T1 to T4 switches in the H-bridge circuit is twice the load frequency. the switching frequency of the H-bridge switches at 50 Hz load frequency, is equal to 100 Hz, and at 400 Hz operating frequency, is equal to 800-Hz. Figure 34 shows the application of different switches at different frequencies, currents, and voltages [50]. The maximum operating frequency of the Thyristor is about 1kHz, and the GTO's is almost equal to 2 kHz, respectively. Also, the GTO and Thyristor have a higher current capacity and can conduct the capacitor charging current through them. Therefore, it is possible to include GTO, thyristor, and even relays in the H-bridge circuit switches. This means that it will have more capability in electronic systems than conventional inverters, even without the use of transformers in the output.

One problem of conventional PWM inverters is the simultaneous switching of each leg of the H-bridge switches. In the proposed topology, not only is simultaneous switching a problem, but as an advantage, this problem has been used to solve the following two challenges: A) Discharge of the energy stored in the inductor into the H-bridge switches and not allow the reverse current to return to the main circuit, and B) Charging the switched capacitors. Another point in this structure to consider is the inrush current of the switched capacitors. The energy required by the capacitor must be supplied, this energy depends on the inrush current of the capacitor and its duration [23].

The charging time of the capacitors can be extended by extending the zero-voltage time of the inverter, and the maximum incoming current also depends on the DC source.

If the capacitance of the switched capacitors is high and the DC source is not able to supply the inrush current, a Soft Start circuit should be implemented on the DC source's output. However, a balance must be struck between the capacitor charging time and the output current of the power supply so that the THD of the output voltage does not fall victim to the reduction of the delivery power of the DC source.

Another way is to place a high-capacity capacitor at the output of DC sources. Sometimes a soft-start circuit for charging these capacitors needs to be predicted. In the constructed inverter, capacitors with a capacity of 1000 μF are used at the output of the power supplies.

DC sources on their own are not capable of providing the inrush current of the switched capacitors, but the capacitors in the output of the DC sources provide this inrush current. In the provided inverter, the capacitors on the outputs of the DC sources are charged without requiring a soft start circuit.

The proposed CSCMLI MLI is also capable of operating correctly under different DC source voltages. Even when one of the voltages changes temporarily, the inverter is still able to operate properly. Figure 28 validates this. As shown in Figure 28, the voltage Vdc1 suddenly increases from 24 volts to 48 volts at t = 0.055 s.

In the first and second cycles after this voltage change, there is no proper sinusoidal output waveform because capacitors C11 and C21 are not charged yet. In the fourth cycle after this voltage change, the output waveform becomes almost sinusoidal. Figure 28 shows the red voltage curve and the blue current curve. The other color also indicates Vdc1. The voltage variations observed in Vdc1 are due to the current flowing through the switched capacitors.

Also, in the proposed structure, the step voltages will not be equal to the input DC voltages for the following reasons: a) The capacitors must be charged during the operation of the inverter, b) The diodes of the paths will reduce the forward voltage, c) In some situations, the switched capacitors discharge in two steps, thus reducing the voltage, and d) Surge current of switched capacitors during inverter operation [51].

C. COMPARISON OF SIMULATION WITH EXPERIMENTAL RESULTS

Figure 31 and Figure 32 show the measurements of the load voltage and current in the experimental test under the load change, respectively, and Figure 21 displays the simulated CSCMLI voltage and current, respectively. As may be seen, the voltage and current measurements are similar. Some steps of the voltage waveform display drooping due to the voltage droop over the switched capacitors. In both the positive and negative half-cycles, only the first (24 volts) and second (48 volts) surface voltages do not exhibit droop due to the absence of the switched capacitor voltage. The first level of the CSCMLI voltage is the voltage Vdc1 of module 1 in the output, and the second level of the inverter output voltage is the summation of the voltages Vdc1 $+V$dc2 where none of the switching capacitors play a role. The waveforms of the currents are equal to each other. Because of the inductive load, the waveform of the load current is lagged, and the inductive load acts as a low-pass filter, eliminating some harmonics. The waveforms of voltage and current simulated with a real inverter are somewhat different, and as mentioned in the previous section, the reasons are: (a) capacitors must be charged during the operation of the inverter, (b) the diodes of the loops will reduce the voltage equal to their forward voltage, (c) in some situations switched capacitors discharge in two steps, and (d) surge current of switched capacitors during the operation of the inverter [51].

Figure 30 and Figure 22 show the current flowing through the H-bridge in the experimental and simulation tests, respectively. The capacitor is capable of both supplying a large amount of instantaneous current and charging rapidly when it supplies the required current. The fast charging current of the capacitor is called the inrush/surge current. If the capacitance of the switching capacitor is high, and the power supply is unable to supply the required instantaneous current, the input current to the capacitor must be limited using the soft-start circuit. In the designed inverter, the instantaneous current drawn, or the current required by the switching capacitors, is instantaneous high, but the average current is low. Figure 30 and Figure 22 show that the current drawn is about 20 A, but the current drawn by the load is about 2 A. It was stated in the prior section that the instantaneous charge of these switched capacitors is provided by the power supplies Vdc1 and Vdc2.

The amount of energy E_{SC} that would evaporate from the SC bank unit can be expressed as:

$$E_{SC} = \frac{1}{2}C\left(V_i^2 - V_f^2\right). \tag{76}$$

where C is the capacitance of the capacitor; V_i is the primary voltage and V_f is the secondary voltage of the capacitor. The relationship between current and capacitor voltage is also as follows:

$$i_C = C\frac{\mathrm{dV}}{\mathrm{dt}}. \tag{77}$$

The i_C is the capacitor current and dV is the voltage change in time dt. The maximum voltage droop of each switching capacitor in the worst case (peak voltage) is almost seven volts over 700 μs. By inserting these numbers into the (76)-(77)) it is obtained that under the most severe conditions the capacitor must have at least the capacity of 1000 μF; thus, the capacitor placed in the output of each power supply is 1000 μF.

D. METHODS TO REDUCE THE THD OF THE PROPOSED MLI

There are several methods of adjusting the MLI's angular times, resulting in harmonic reduction. Reference [52] uses Select Harmonic Reduction (SHE) to optimize the THD of a similar type of MLI. By including the constraint $t_0 - t_1 > 5\tau$ in the optimization methods like [52], the THD will be improved.

The presented MLI has the ability to employ PWM switching algorithms. By utilizing this switching technique, the current changes (di_l) of (13) will be reduced, resulting in low changes in inductor voltage [53].

Thus, in this situation, the negative effects of the inductor in the MLI will be reduced. While using the PWM switching algorithm, the inverter is capable of driving high inductive loads. Compared to PWM, one of the advantages of the proposed switching technique is the low switching frequency. But this is counterbalanced by the negative effect of the inductor discharge energy problem.

Figure 33 shows the voltage of switched capacitors C11 and C21 under the sudden load change. As the load decreases,

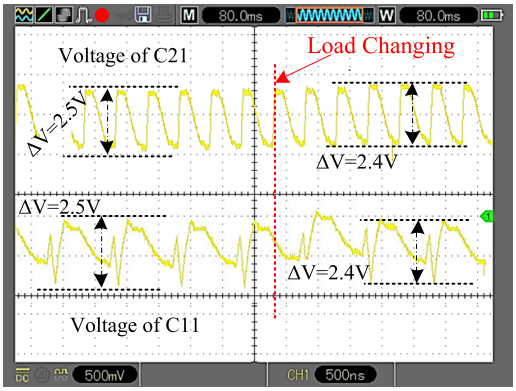

FIGURE 33. Switched capacitor voltages under the sudden load change.

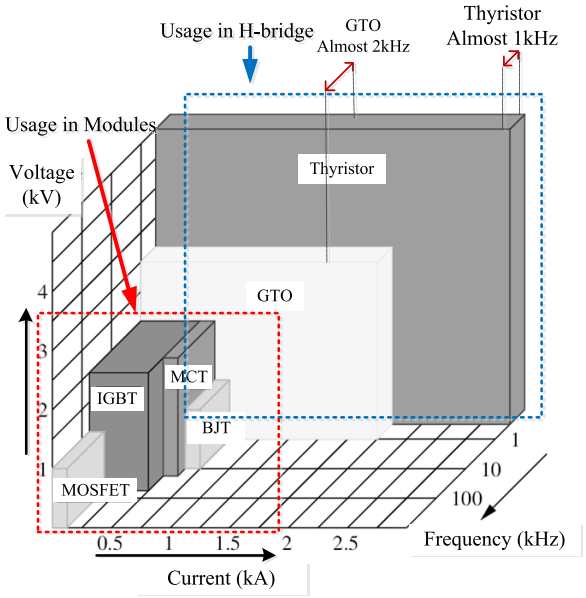

FIGURE 34. Application of different switches in different frequencies, currents, and voltages. Because of the low switching frequency of H-bridge switches, these can be GTO or Thyristor for high voltage applications.

both the average and the peak-peak magnitude of the voltage decrease.

E. BRIEF EXPLANATORY MEMORANDUM FOR THE PROPOSED CSCMLI

All manufacturing information including PCB, schematic of the inverter circuit designed in Proteus software, exported, PDF circuit diagram, simulation of the inverter in MATLAB software, and microcontroller program codes have been attached to the article. Tables 10-13 also give the values of simulation and construction parameters. The main remarks of the presented article are as follows:

1) *The new CSCMLI inverter has the lowest number of switches, the lowest drive and the lowest cost factor compared to all comparable cascaded multi-level inverters.*
2) *In similar multi-level inverters having an H-bridge, closing two switches of one leg at the same time is detrimental, but in the proposed inverter the switches of 2 legs are used to charge the switched capacitor.*
3) *There is limited information about TSV calculation in other articles, but this article fully explains how to calculate TSV.*
4) *As explained, the low switching frequency of the H-bridge allows the presented CSCMLI inverter to operate at high voltages.*
5) *All information about the construction and simulation of the CSCMLI inverter, including the circuit board, microcontroller program code, PCB, circuit diagram, etc. is attached to the article for other researchers to use.*
6) *The structure of the inverter is such that it may be connected to photovoltaic cells and fuel cells and is appropriate for domestic and building use.*
7) *Regarding the inverter design for high and medium voltage applications, the SOA factor in selecting the switch to consider the capacitor inrush current was explained.*
8) *Descriptions of the diode's ability to carry the peak instantaneous inrush current were given.*
9) *A fairly complete description was given of the capability of the maximum pulsed current of the DC source to supply the required peak current of switched capacitors.*

TABLE 13. Values of the experimental design.

Item	Description	Value	Unit
1	Snubber Resistor	10	kΩ
2	Snubber Capacitor	337	μF
3	C11 Capacitor	1333	μF
4	C11 Electrolyte Capacitor	4000	μF
5	Series resistor with gate of MOSFETs	10	Ω
6	Adaptor of Gate-source isolated Voltage	12	V
7	HRP-150N-24, *V*dc Power supplies	24	V

VI. LIMITATIONS OF THE STUDY

The proposed CSCMLI multilevel inverter faces the following limitations:

A. REQUIREMENT OF MORE THAN ONE DC SOURCE IN CASE OF MODULE CASCADE INCREASE

From the perspective of some researchers, using multiple DC sources as an inverter input may exhibit weakness, but in some cases the number of DC power supplies, including photovoltaics, batteries, and photovoltaics, is large and they cannot be connected in parallel or series. For example, it is completely erroneous to connect two DC sources in parallel with even a 0.1-V voltage difference, causing the current to flow back to a power supply of lower voltage. Also, sine or DC voltage may sometimes be up to several kilovolts, and it is not possible to use a typical low-voltage DC source without using a transformer, thus an inverter capable of generating this voltage without a transformer would be quite helpful. Recently, a lot of research has been conducted in this area and

many topologies have been proposed to use more DC sources to generate sinusoidal voltage [1]–[9], [12]–[14], [23]–[24], [34]–[36], [38]–[41], [44]. If the output voltage of the inverter is high, or if more than one isolated DC source exists, the use of the proposed CSCMLI will be useful.

B. INDUCTION LOAD LIMITATION

The proposed topology is not suitable for pure reactive power and high inductance applications. There are limitations in using the proposed CSCMLI to supply demand power to applications. Due to the discharge of inductive load energy in H-bridge switches, it is not possible to connect any type of inductive load to the proposed inverter. The proposed inverter is capable of handling inductive loads more than even 20 Henries, but only if the ohmic resistance is low and the inductive energy can be dissipated into the energy-discharge loop. This limitation does not mean that the presented inverter will not work with inductive loads, but not all types of inductive loads can be connected to the presented CSCMLI inverter. Depending on the type of load, the quantity of ohmic load, and the quantity of inductive load, the relevant mathematical relationships were presented in the following sections.

In ''Section II. Material and methods of Proposed Inverter, Subsections D. Circuit Analysis, E. Role of frequency on inductive load instant time, F. Operation of MLI under the high Inductance Loads'', mathematical calculations were used to express the allowable performance limits of CSCMLI under combined resistance/induction loads. Because of the limitations foreseen, this CSCMLI inverter can be used in Domestic Loads. Loads like lighting, resistive heaters, irons, TV, etc. are resistive loads and sometimes inductive loads, such as a refrigerator require less inductive power compared to other general resistive loads. Therefore, in residential applications which have less inductive loads, the use of this inverter will be acceptable.

Hence, a novel multilevel inverter was designed, simulated, and subsequently manufactured. The proposed CSCMLI inverter utilizes reduced switched capacitors and semiconductors compared to other topologies, elides the requirement of a transformer, and in general, it performs well compared to conventional inverters and similar multilevel topologies. Experimental results validate the possibility of using the proposed CSCMLI inverter in domestic applications incorporating renewable energies as DC input sources.

VII. OPEN QUESTIONS

The proposed CSCMLI inverter is the first one that is being tested experimentally. So far, this topology has not been presented in any journal, thus, there are issues and questions related to this inverter that has not been studied yet, the answer to which may lead to the generation of science and more articles and pave the way for the use of this inverter in the industry. In summary, these Open Questions include:

1) Can this inverter supply high voltage loads such as Klystron and microwave tubes? These tubes are types of pulsed resistive loads that require high voltage to operate. By changing the angles of modules 1 and 2 switches, the required voltage of these tubes can be generated.

2) Is it possible that the proposed CSCMLI inverter be fault-tolerant? In case of failures, the number of voltage levels can be reduced by changing the switching algorithm, but the operation of the inverter continues. This issue will be discussed in more detail in the future.

3) Can relays, thyristors, or GTOs be employed in modules instead of MOSFET and IGBT switches? In this document, in Section V. EXPERIMENTAL RESULTS, Subsection B. Discussion of the proposed CSCMLI, it is stated that relays, thyristors, and GTOs may also be used in the H-bridge. However, it is also possible to use these components instead of the S23 switch. The switching frequency of this switch is low, and if a thyristor or GTO is used, the reliability of the system can be increased or the manufacturing cost reduced. It is also worth studying this issue.

4) Reducing the speed of some induction motors, reducing the light of resistance lights, and reducing the power consumption of the load all can be made by adjusting the output voltage. Since module 2 is capable of generating 1, 2, 3, and 4 times the DC input voltage, the number of output voltage levels can be changed by modifying the switching algorithm. The investigation of this question is also of interest.

5) Despite the constant peak output voltage, the number of voltage levels was increased in article [2] by changing the switching algorithm. The voltage levels number of proposed CSCMLI can also be increased using the technique used in this reference.

VIII. CONCLUSION

In this paper, a new type of MLI topology with switched capacitors is introduced, containing fewer switches but providing the same response compared to similar inverters with two isolated DC sources. Eliminating the harmful reverse flowing currents associated with inductive loads was the purpose of the switch eliminated from the topology. The elimination of the switch was compensated by a novel switching technique. The proposed configuration produced a 13-level voltage with a voltage gain of six by incorporating nine switches including an H-bridge. This topology can be extended in a cascade configuration. The cost function was calculated and compared to similar SCMLIs. Based on data from recently published research on similar inverters, linear equations were derived using level-switch, level-semiconductor, level-DC source, and level-capacitor axes, and the proposed configuration was compared with inverter topologies from the literature. The proposed configuration had the least number of switches, semiconductors, drives, and capacitors and the lowest cost function value at all levels compared to similar topologies using two DC sources.

The role of switched-capacitor inrush current in the selection of switch, diode, and DC source for inverter operation in medium and high voltage applications was presented. Focused on the supply and ability to pass the inrush current required to charge up the switched capacitor, and considering

the availability of the components in the market, the following topics were examined in detail: 1) The role of the SOA parameter in the selection of the switch, 2) The maximum current ratio that the diode passes through, concerning time and its nominal current, and 3) The maximum pulsed power (instantaneous) that may be supplied by the DC power supply to provide the inrush current, considering time. The main advantages of the proposed topology are: a) Due to the low switching frequency of the H-bridge, it is possible to use Thyristor, GTO, IGBT and relays in the H-bridge circuit, and thus this CSCMLI is operable for high voltage applications, b) In other topologies, simultaneous switching of the H-bridge arms causes problems, but the proposed topology uses this simultaneity for charging switched capacitors, c) The energy stored in the inductor load, discharges to the H-bridge circuit instead of current flowing back to the main circuit of the multi-level inverter, and d) This structure has the possibility of using PWM switching algorithm, for having the better performance. Finally, the correct operation of the proposed inverter was verified by the simulation and experimental results. A video demonstrating the experimental test, and all manufacturing data, including PCB, schematics, processor code, etc., are also attached.

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