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Thirteen-Level UXE-Type Inverter With 12-Band Hysteresis Current Control Employing PSO Based PI Controller

DEEPAK UPADHYAY[1], MOHAMMAD ALI[2], (Member, IEEE), MOHD TARIQ[1], (Senior Member, IEEE), SHAHBAZ AHMAD KHAN[1], BASEM ALAMRI[3], (Member, IEEE), AND AHMAD ALAHMADI[3], (Senior Member, IEEE)

[1]Department of Electrical Engineering, ZHCET, Aligarh Muslim University, Aligarh 202002, India
[2]K.A. CARE Energy Research and Innovation Center, King Fahd University of Petroleum and Minerals, Dhahran 31261, Saudi Arabia
[3]Department of Electrical Engineering, College of Engineering, Taif University, Taif 21944, Saudi Arabia

Corresponding authors: Mohd Tariq (tariq.ee@zhcet.ac.in) and Mohammad Ali (mohad_ali92@yahoo.com)

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ABSTRACT This work presents hysteresis control applied to UXE-type inverter topology with a PI (Proportional Integral) controller, where the gains are derived by Particle Swarm Optimization (PSO). The investigated UXE inverter can generate a thirteen-level output voltage waveform, which results in lower switching losses. It can boost the output voltage to 1.5 times the applied input DC source voltage. Satisfactory inverter operation is ensured by employing twelve-band hysteresis current control. The tuning of the PI controller required for the closed-loop hysteresis current control is achieved by nature-inspired PSO algorithm. A comparative analysis is also performed after obtaining the results applying nature-inspired PSO and conventional Ziegler Nichols (ZN) methods. The effectiveness of the control strategy is verified in the MATLAB Simulink and further validated in experiment using TMS320F28379D and also with Typhoon Hardware in Loop Technology.

INDEX TERMS WE-topology, hysteresis control, particle swarm optimization, Ziegler Nichols method, multilevel inverter.

I. INTRODUCTION

Medium voltage multilevel inverters (MLI) have gained popularity in recent years. These are widely used for renewable energy integration because of their better performance. Now their applications have included electric vehicles and power conditioning units [1], [2]. In the MLIs, the switches voltage stress reduces to a considerable level, and the output voltage waveform with reduced THD is achieved [3]. Various popular and established multilevel inverters are NPC (neutral point clamped) [4], CHB (cascaded H bridge) [5] and FC (flying capacitor) multilevel inverter. In CHB-MLI, as the number of voltage levels increase, the number of isolated DC sources increases considerably. Besides, the clamping diodes in NPC-MLI and the flying capacitors in FC-MLI increase with the increase in the number of voltage levels.

Furthermore, to get medium to large voltages, transformers at the load end, or, DC-DC boost converters at the front end are required, which add to the bulk and cost of the system. To overcome this shortcoming of the traditional topologies, multilevel inverters with inherent boosting capabilities are explored. Additionally, these topologies a reduced number of components are required to realize these circuits [6]–[12].

This paper presents hysteresis control of a thirteen-level switched capacitor inverter where the PI controller parameter tuning is performed using metaheuristic particle swarm optimization (PSO). The correct switching pattern is selected with suitable charging and discharging paths to balance the capacitor voltages.

The inverters are controlled by pulse width modulation, hysteresis control, space vector control, model predictive

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control and sliding mode control. Hysteresis current control technique for multilevel inverter is presented in [13] and [14]. There are mainly two types, one with a constant switching frequency [15] and another one with a variable switching frequency [16]. The main principle of hysteresis current control is to limit the reference and load current error by logically creating bands around the reference current. There are two techniques to limit the error: time-locked control and multiband control [17]. These methods apply to multilevel inverters exibiting inherent capacitor voltage balancing [18], [19]. Topologies that do not have inherent balancing of switched capacitors require balancing of the capacitors before implementing the hysteresis bands control. Thus an additional Proportional controller wih integrating factor is required to generate the exact reference current [20]. The PI control balances the capacitor voltages and generates the load reference current.

Conventionally, Zeigler Nichols technique is utilized to tune the gains of the PI controller, but it is a time-consuming process. Further, the time delays, nonlinearities, and the higher-order system makes the process less precise [21]. To overcome these drawbacks, heuristic techniques are used to find the PI gains. These techniques also improve the response of steady-state and the dynamic response of the system [22]. Different optimization techniques like genetic algorithm [23], Particle swarm optimization (PSO) [24], Bee algorithm [25], BAT algorithm [26] and Differential evolution [27] are being employed in obtaining near-to-exact solutions. These techniques give a fast dynamic response within a few iterations and control the inverter more effectively.

In this work, the values of the proportional and integral constants (K_p and K_i) for the closed-loop operation are found by employing the PSO technique. Analysis shows that the PSO converges faster for the problem statement of this work in comparison to GA, Bee and Bat algorithms. The performance of the technique is then compared with the Zeigler-Nichols method.

The structure of the paper is as follows. The thirteen level UXE structure and its states are discussed in the subsequent section. The implementation of twelve band hysteresis control on UXE inverter with PI-controller tuned with PSO and conventional ZN technique is discussed in section III. Simulation results with several tuning methods, hysteresis bands and different load conditions and are shown and analyzed in section IV. In section V, experimental results are presented, and section VI concludes and summarizes the paper.

II. THE UXE-13 TOPOLOGY

A. UXE-13 STRUCTURE AND SWITCHING

Fig. 1 shows the circuit schematic of the 13-level UXE-type inverter. The arrangement comprises of a single DC source, two capacitors, six IGBTs with anti-parallel and four IGBTs without anti-parallel diodes, a DC source that and an AC-switch comprising two antiparallel IGBTs. The switches

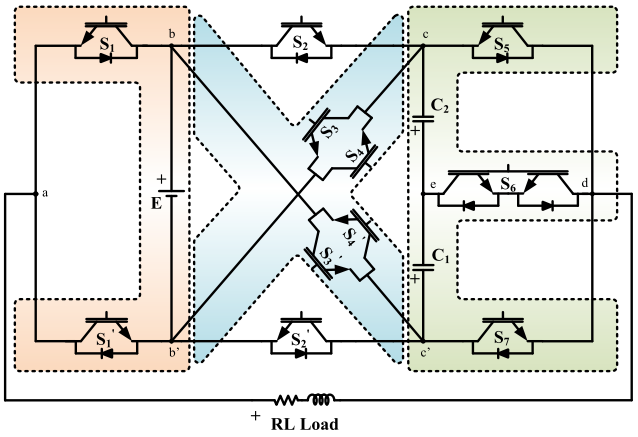

FIGURE 1. Circuit schematic of UXE topology.

TABLE 1. Output voltage states of UXE inverter.

State	S_1	S_1'	S_2	S_2'	S_3	S_3'	S_4	S_4'	S_5	S_6	S_7	V_o
1A.	1	0	0	1	0	0	0	0	1	0	0	1.5E
1B.	1	0	0	1	0	0	0	0	1	0	0	1.5E
2A.	1	0	0	1	0	0	0	0	0	1	0	1.25E
2B.	1	0	0	1	0	0	0	0	0	1	0	1.25E
3A.	1	0	0	1	0	0	0	0	0	0	1	E
3B.	1	0	0	1	0	0	0	0	0	0	1	E
4A.	1	0	0	0	1	0	0	0	0	1	0	0.75E
4B.	1	0	0	0	0	0	1	0	0	1	0	0.75E
5A.	1	0	0	0	1	0	0	0	0	0	1	0.5E
5B.	0	1	0	1	0	0	0	0	1	0	0	0.5E
5C.	0	1	0	1	0	0	0	0	1	0	0	0.5E
5D.	1	0	0	0	0	0	1	0	0	0	1	0.5E
6A.	0	1	0	1	0	0	0	0	0	1	0	0.25E
6B.	0	1	0	1	0	0	0	0	0	1	0	0.25E
7A.	1	0	1	0	0	0	0	0	1	0	0	0
7B	0	1	0	1	0	0	0	0	0	0	1	0
8A.	1	0	1	0	0	0	0	0	0	1	0	-0.25E
8B.	1	0	1	0	0	0	0	0	0	1	0	-0.25E
9A.	1	0	1	0	0	0	0	0	0	0	1	-0.5E
9B.	0	1	0	0	0	0	0	1	1	0	0	-0.5E
9C.	0	1	0	0	0	1	0	0	1	0	0	-0.5E
9D.	1	0	1	0	0	0	0	0	0	0	1	-0.5E
10A.	0	1	0	0	0	1	0	0	0	1	0	-0.75E
10B.	0	1	0	0	0	0	0	1	0	1	0	-0.75E
11A.	0	1	1	0	0	0	0	0	1	0	0	-E
11B.	0	1	1	0	0	0	0	0	1	0	0	-E
12A.	0	1	1	0	0	0	0	0	0	1	0	-1.25E
12B.	0	1	1	0	0	0	0	0	0	1	0	-1.25E
13A.	0	1	1	0	0	0	0	0	0	0	1	-1.5E
13B.	0	1	1	0	0	0	0	0	0	0	1	-1.5E

S_1 and S_1' form a U, S_2, S_2', S_3, S_3', S_4 and S_4' form an X, and, S_5, S_6 and S_7 forms alphabet 'E', and hence the name UXE-type inverter. The circuit is capable of producing a 1.5 times boosted output voltage.

Fig. 2 shows the 13 possible levels of the converter during one cycle of operation. This figure is more explainable in conjunction with Table 1. The condition of charging and discharging depends on the direction of current flowing through the capacitors. If the current is entering the capacitor, it will charge, otherwise it will discharge. With no current flowing into the capacitor, the capacitor voltage will remain unaltered. The condition of $0.5V_{dc}$, has a redundant state. There are two circuit configurations available which are shown by

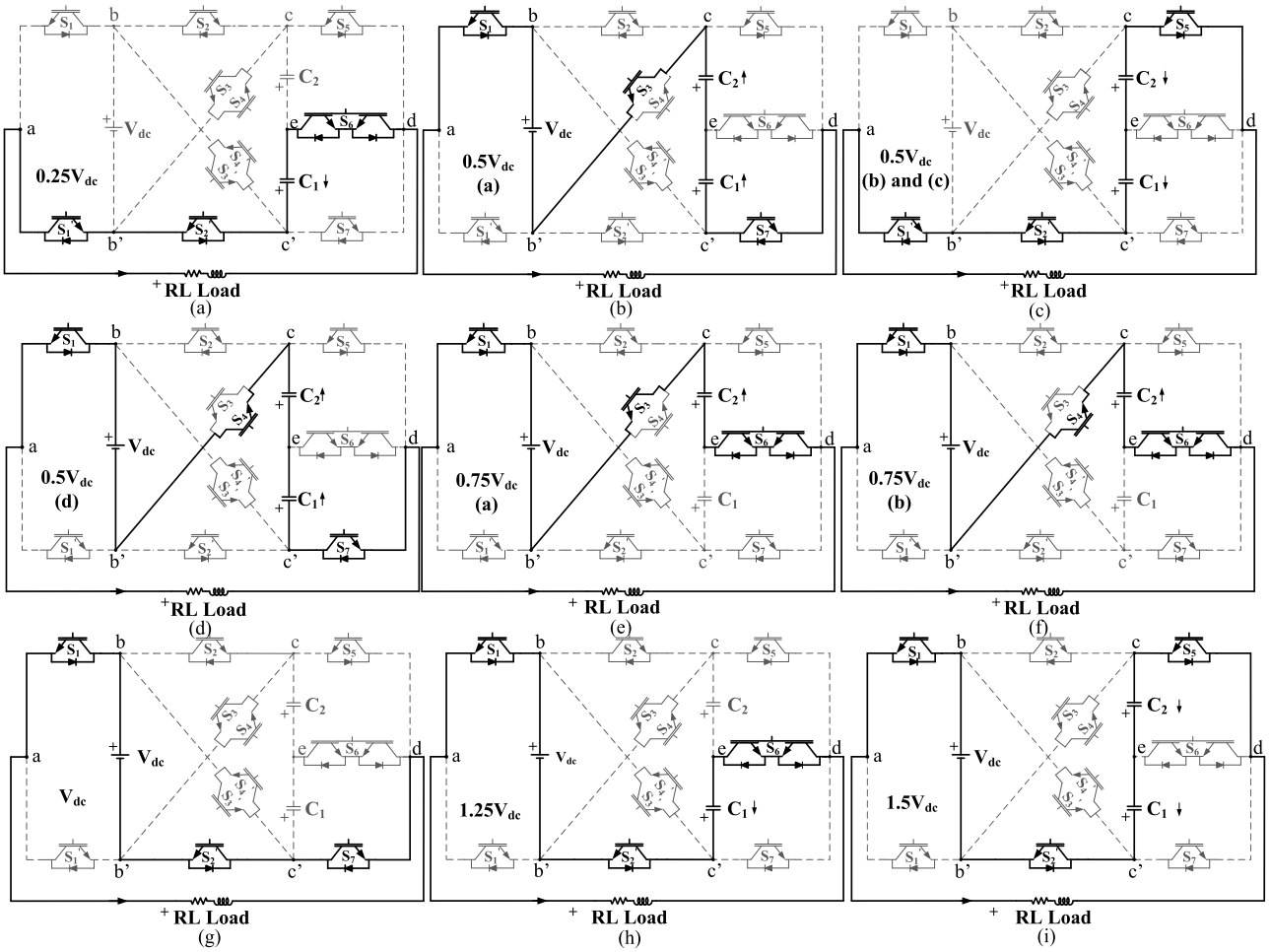

FIGURE 2. Switching state diagrams for positive cycle of 13-level UXE topology.

conditions 5A-5D (for both current directions) in Table 1, and configurations in Fig. 2 (f) an (g) (without consideration of current direction). Similarly, the redundant conditions of $-0.5V_{dc}$ can be understood by 9A-9D from Table 1 and configurations Fig. 2 (n) and (o). Besides, the states of $\pm 1.5V_{dc}$ will also include both capacitors, but will be either in charging or discharging state depending on the direction of current.

For states $\pm 0.75V_{dc}$ different configurations through S_3 and S_4, and S_3' and S_4' as shown in Fig. 2 (d), (e), (p) and (q), are chosen. During these conditions only one capacitor is affected. The rest of the states have single switch configuration and can be seen in Table 1 and in Fig. 2. Fig.3 shows the standing voltages of the switches in each state. The maximum standing voltage across the switches is not more than 1.5 V_{dc}, and the total standing voltage is approximately 6 V_{dc}.

B. COMPARISON WITH RECENT 13-LEVEL TOPOLOGIES

A lesser number of components with single source is employed in this topology to achieve a boosting of 1.5 times the DC source. The redundant states are employed to balance the voltage across the DC-link. The structure requires a single source, 12 IGBTs, seven driver circuits, and two capacitors – making it 22 components in all. The cost factor (CF) is lowest at 1.615. The CF is calculated as given in [28]. The comparative assessment of UXE inverter topology with other recently proposed thirteen level inverter topologies is shown in Table 2. The driver circuits are Skyper-based circuits that can drive two complementary switches through a single board. A topology with 24 component shown in [29] which requires 2 sources and 2 capacitors. As the two sources are in a ratio of 1:3, the boosting results in 0.75, and a highest CF of 3.385. A three-times boosting single-source inverter is presented in [30] that employs 16 switches and 3 capacitors making it the largest component topology of 36 and a CF of 2.692. A 13-level topology with 6 times boosting is presented in [31] that requires 30 components including 3 capacitors and has a cost factor of 2.23. A single-source topology is introduced in [32] that employs 14 switches driven by eight driver circuits. A total of 27 components are required to generate a 13-levels with 1.5 boosting.

III. HYSTERESIS CONTROL FOR UXE-TOPOLOGY

One of the current control technique that has proven to be helpful for the high-performance requirement at the expense

TABLE 2. Comparison with recent 13-level topologies.

Topology	N_s	N_{sw}	N_{dr}	N_d	N_c	N_{comp}	CF	BC	Balancing
[29]	2	10	10	0	2	24	3.385	0.75	Self
[30]	1	16	16	0	3	36	2.692	3	Self
[31]	1	14	11	1	3	30	2.23	6	Self
[32]	1	14	8	0	4	27	2	1.5	Self
UXE-13	**1**	**12**	**7**	**0**	**2**	**22**	**1.615**	**1.5**	**Redundant states**

N_s=number of souces, N_{sw}=number of switches, N_{dr}=number of driver circuits, N_d=number of diodes, N_c=number of capacitors, N_{comp}=total components, CF=cost factor, BC=boosting

of switching frequency variation is Hysteresis bases current control. This paper uses twelve band hysteresis control technique to create the 13 level inverter voltage output. The control principle limits the current error (i_e) within the 12 bands created by the mathematical logic. This technique is advantageous over the others as it exhibits good dynamics and a stable operation. The current error is controlled logically within the fixed band of magnitude 'h' and its multiples from h to 6h.

The optimal PI constants K_p and K_i are needed to be found for proper balancing of capacitor voltages and maintaining the desired dynamic response of the system. Tuning this PI controller is a cumbersome task, and if the topology has more than one capacitor, the task becomes more challenging and time-consuming. To overcome these difficulties, attention has been given to metaheuristic approaches to determine the values of K_p and K_i according to the system's dynamic response. In this paper, a competent approach is taken to tune the PI controller automatically, and the controller is capable of controlling and updating the PI values according to load changes.

A. 12-BAND HYSTERESIS CONTROL AND ITS IMPLIMENTAION

Hysteresis current control technique generates the output voltage levels by quantizing the error between and the reference current the load current into multiple bands. The number of bands required for the n level inverter is (n-1). These bands are created on the sinusoidal varying magnitude of the current error. These bands are created using two control parameters: voltage levels as multiple DC source voltages and the change in current error (Δi). These bands are symmetrical to the y-axis, six bands are in the positive axis, and six in the negative axis are called upper and lower bands, respectively. In Fig.4 complete control strategy block diagram is shown. To accommodate the voltage balancing of the capacitor additional PI control loop is used.

The number of capacitors is two (C_1 and C_2). Therefore two separate PI controllers are required to balance the voltages (V_{c1} and V_{c2}) to (1/4)E source voltage. Initially, the voltage references are generated by taking the load voltages across the capacitors. The error generated by voltages across the capacitors and fed to the PI controllers and the constants (K_{p1}, K_{p2}, K_{i1}, K_{i2}) are generated by the metaheuristic based PI tuner, which generates the four PI constant values. The control algorithm used to find the optimal values of constants is PSO which has a high convergence rate. The yield of

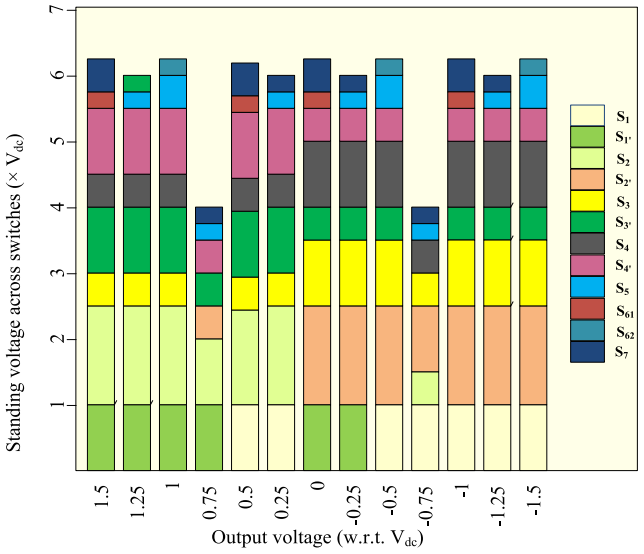

FIGURE 3. Standing voltages of the UXE inverter in each state.

the two PI controllers is added and then multiplied by a sinusoid of unity magnitudeand a frequency of 50Hz. The signal generated after multiplication is the reference current for generating the current error. The current error is fed to the logical block to quantify the signal to 12 bands in the next stage. Each band corresponds to the different voltage levels. When the slope in error is varied, switching between two adjacent levels leads to an inter-level switching. As the current error increases between the bands, the voltage levels are generated to keep the current error within limits. Twelve bands of hysteresis bandwidth 'h' are created, and switching is decided accordingly. These bands are $(0 \rightarrow -h)$, $(-h \rightarrow -2h)$, $(-2h \rightarrow -3h)$, $(-3h \rightarrow -4h)$, $(-4h \rightarrow -5h)$, $(-5h \rightarrow -6h)$ and $(0 \rightarrow h)$, $(h \rightarrow 2h)$ $(2h \rightarrow 3h)$, $(3h \rightarrow 4h)$, $(4h \rightarrow 5h)$, $(5h \rightarrow 6h)$. The width of the hysteresis band is approximately equal to 2-5% of the current error value. Further, the switching is done per the state selected by the hysteresis block, and the input signal is given to the switching function block. In this way, the 13-level is generated in the load voltage.

B. INTRODUCTION TO HEURISTIC-BASED PI CONTROL

The current error needed in the hysteresis band control is generated after processing through the PI control. The primary issue arises in tuning the PI controller to decide the values of K_p and K_i (proportional and integral gain constants). This paper finds the gain constants' values by using the nature-inspired particle swarm optimization (PSO) technique. The performance is compared with the conventional Ziegler-Nichols method. The PSO is also most suited over the GA, Bee and BAT algorithm in terms of convergence to the optimum solution. The meta-heuristic-based nature-inspired optimization techniques can fine-tune the gains of the PI controllers by obtaining optimum solutions.

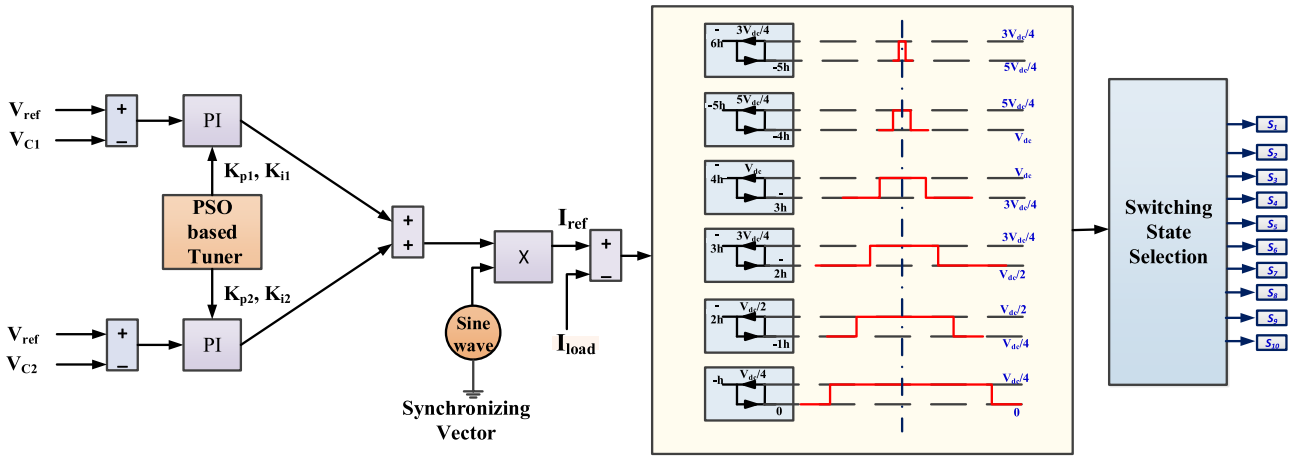

FIGURE 4. Hysteresis band control implementation with PSO based tuning.

C. TUNING OF CONTROLLER

Controller tuning is defined as the selection procedure of the controller parameters to fulfill the desired performance as demanded, attain fast response, and improve stability. ZN method involves tuning of the PID control gains. The other techniques developed after this uses trial and error process As the parameters in this method are tuned multiple times and requires special attention during the application making it herculean task. After large number of iterations there is no guarantee of the optimum solutions.

These demerits encourage trying other developed techniques to get optimum values. One of the most conventional methods used for the tuning of PI controllers is the Ziegler Nichols method.

D. ZIEGLER NICHOLS METHOD

The Ziegler Nichols method is most popular method used for setting PID controller gains. In this method the process starts with making the integral and differential gains to zero and then increasing the proportional value until the system under control becomes stable. Major disadvantage ofemploying this method is its applicability to closed loop systems only. The absolute gain is calculated by determining the value of the proportional gain that causes the loop to oscillate indefinitely in the steady-state. Theother parameter is the ultimate period. In steady state, this parameter is defined as the time taken in one oscillation. These parameters are utilized to calculate the PI controller's gains [21].

E. APPLICATION OF PARTICLE SWARM OPTIMIZATION (PSO)

PSO algorithm replicates the movement of a group of animals. Single individual in set is defined as the particle which is same as fish in a school or a bird in a flock. Each element in the group known as particle are distributed in such a way that the intelligence of single particle and group are considered separate. As the particle gets the food, the whole particle tries to reach to that particle independent of their location. Swarm based optimization techniques are behaviorally inspired rather than GA and DE that are evolution based techniques [33].

In the PSO methodology, initially the particles are considered to be randomly dispersed in the domain [34]. Each elemental particle has two properties – its velocity and position. Every particle have the memory of best enquired position. The velocity and movement is controlled by considering the previous best position and best in all the individual particles [35]–[37]. The main features of PSO are:

- The particle sum up to the velocity vector of other random particles.
- Algorithms that replicate the social relation of the animals have a better rate of convergence compared to evoltionary based algorithms. However, sometimes, an algorithm based on social behavior overcomes the range ofalgorithm due to fast convergence.
- An extra parameter is added in the analysis to consider the effect of overshoot called θ.

1) SIZE OF SWARM

The selection of number o particle is a tradeoff between the complexity and number of iterations. If the number of particles is greater, the computational burden is increased to many folds per iterations. Also, If the number of particles chosen are less, than the required iterations o converge the solution much more. So the best choice for most of the problems is to consider 20-30 particles.

2) SELECTION OF POSITION

Initially, the particles are randomly scattered (similar to chromosomes in GA). These positions update iteration by iteration according to the particle velocity particle:

$$X_j(i) = X_j(1-i) + V_j(i); \quad i = 1, 2, 3 \ldots\ldots n \qquad (1)$$

where, j represents particle number and i represents iteration number.

TABLE 3. Simulation parameters for GA and PSO.

GA & PSO Parameters	*Values*
Population Size	100
Crossover rate	0.9
Mute rate	25%
No. of Iterations	500

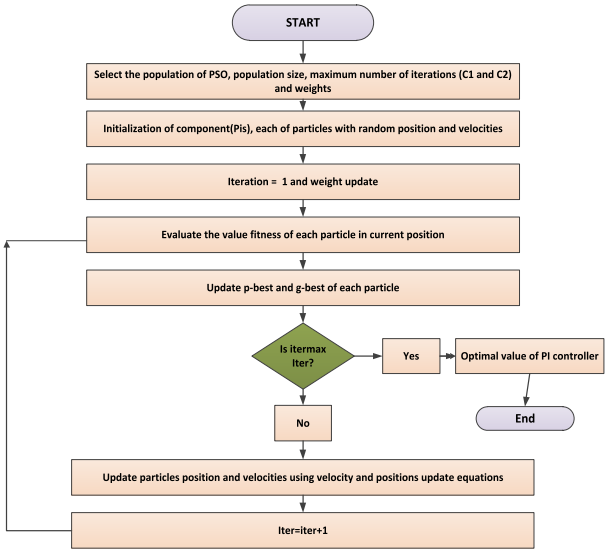

FIGURE 5. Flowchart of PSO implementation.

3) VELOCITY

The rate of varying position of particle in an iteration is denoted by velocity. The velocity parameter is rapidly changing with each iteration. Velocity vector in a particular iteration is calculated by:

$$V_j(i) = V_j(1-i) + C_1 r_1 \left(P_{best,j} - X_j(i-1)\right) + C_1 r_1 \left(G_{best} - X_j(i-1)\right) \quad J = 1, 2, 3 \ldots n \tag{2}$$

Here, C_1 and C_2 are the cognitive (individual) and social (group) learning rates, respectively, and r1 and r2 are uniformly distributed random numbers in the range 0 and 1. C_1 and C_2 signify the relative importance of the memory (position) of the particle itself to the memory (position) of the swarm.

Shi and Eberhart originally introduced the inertia weight θ in 1999 [38] to dampen the velocities over time (or iterations), enabling the swarm to converge more efficiently compared to the original PSO algorithm. Usually, the inertia weight is opted between 0.4 to 0.9, but it is subjective to the problem at hand.

$$\mathrm{V_j(i)} = \theta \mathrm{V_j(i-1)} + \mathrm{C_1 r_1 \left[P_{Best,j} - X_j(i-1)\right]} + \mathrm{C_1 r_1 \left[G_{Best} - X_j(i-1)\right]}; \quad \mathrm{j = 1, 2, 3 \ldots\ldots n} \tag{3}$$

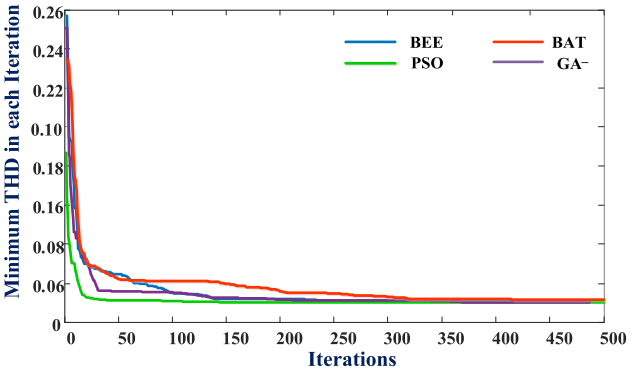

FIGURE 6. Variation of minimum THD value with iterations.

For more insights of particle swarm optimization flowchart illustrating all significant steps is shown in Fig.5. Computational steps are discussed below:

1. Choosing the particle swarm ten times of the design variable in domain of randomly scattered particles.
2. P_{Best} and G_{Best} is calculated in each iteration.
3. Velocity and position vector of all the particles is updated.
4. Stop when convergence criteria meets. Otherwise, repeat from step 2.

F. APPLICATION OF PSO

Output voltage waveform THD depends on fundamental component and the harmonics as:

$$\mathrm{THD} = \frac{\sqrt{\mathrm{V_2^2} + V_3^2 + \mathrm{V_4^2} + \mathrm{V_5^2} \ldots . V_{49}^2}}{V_1}$$

Now,

$$\mathrm{THD} = (\mathrm{THD})_{\min} \tag{4}$$

This equation definesthe objective function of the problem for PSO. The below mentioned equation generates the AC load voltage reference:

$$Van = K_{pl} i_l + Ki_l \int \mathrm{i}_l \mathrm{dt}$$
$$\bar{i_l} = \mathrm{i_l^*} - \mathrm{i}_l \tag{5}$$

where $\mathrm{i_l^*}$ is the referenceload current.

The output voltage levels aredependent of the voltage developed across the capacitors, which is required to be maintained at one fourth of DC source voltage. Futher, the output current is dependent on gain constants. The PI controller is used to control the voltage across the capacitors by maintaining the relation:

$$i_2^* = f(K_{p2}, K_{i2}, K_{p3}, K_{i3}) \tag{6}$$
$$\mathrm{i_l^*} = (\mathrm{K_{p2}} \bar{V_2} + \mathrm{K_{i2}} \int \mathrm{V_2 dt}) + (\mathrm{K_{p3}} \bar{V_3} + \mathrm{K_{i3}} \int \bar{V_3} \mathrm{dt}) \tag{7}$$

$\bar{\mathrm{V}}_2 = \mathrm{V_{c1}^*} - \mathrm{V_{c1}} = \mathrm{V_{c2}^*} - \mathrm{V_{c2}}$, $\mathrm{V_{c2}^*}$ and $\mathrm{V_{c1}^*}$ are capacitor voltage references.

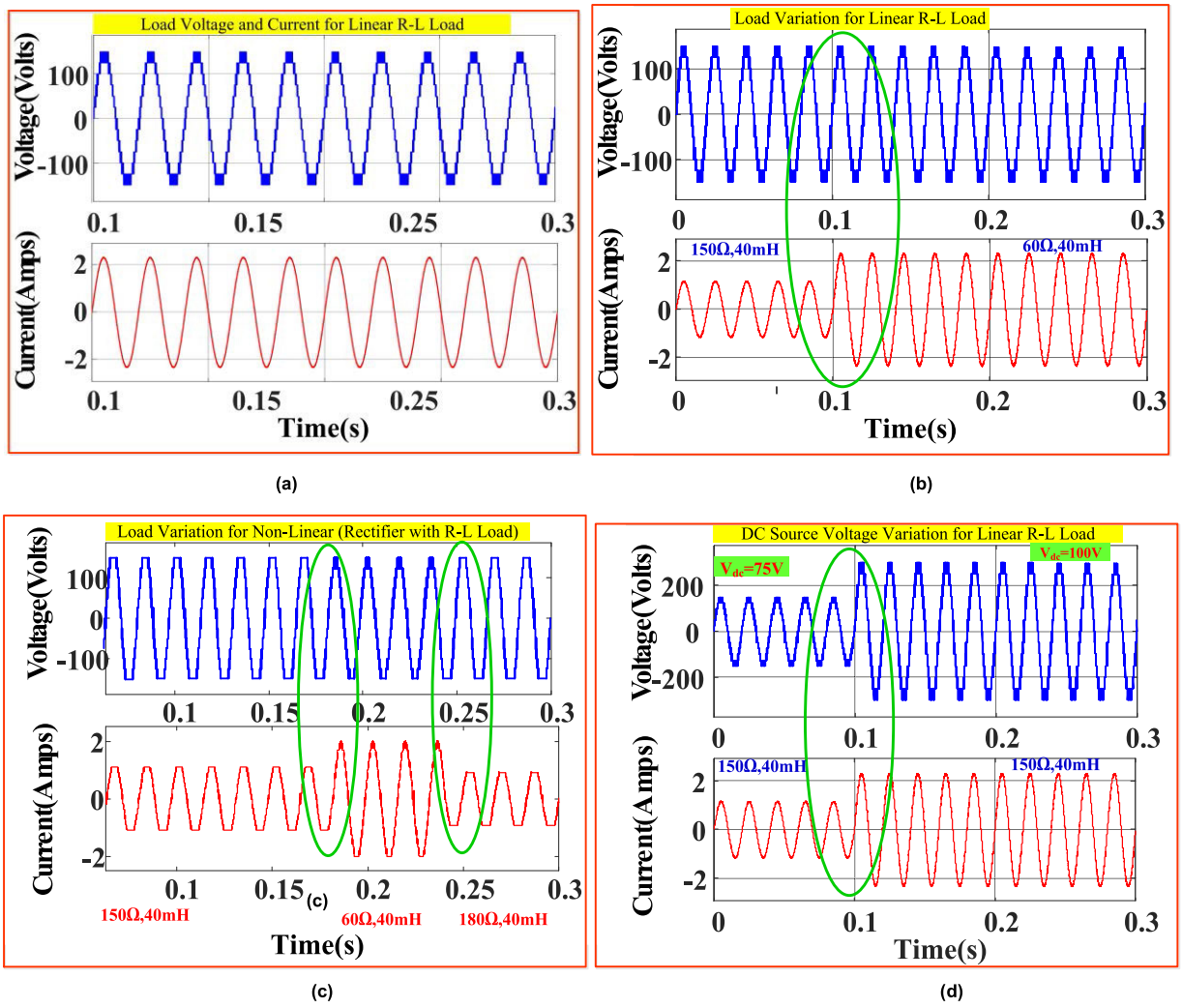

FIGURE 7. Load voltage and load current waveforms at h = 0.02. at various operations.

Limiting condition for capacitor voltage involved (when 100V DC source voltage is applied):

$$48 \leq V_1 - V_2(e) \leq 50 \tag{8}$$

The fitness function is defined by equation (4). The PI controller optimization beginswith random selectionof values from the initial population. The gain constants are calculated at every moment by PSO to balance the voltages across the capacitors, ultimately influencing the THD of the output voltage.

The convergence curve for the PSO, GA, BEE and Bat algorithms have been shown in Fig.6. PSO shows the fastest convergence, and the number of iterations is also less. This makes PSO suitable for applying in the PI tuning controller. The parameters taken for running the PSO and GA is shown in Table 3

IV. SIMULATION RESULTS AND ANALYSIS

Simulation of the proposed control technique is performed on MATLAB 2016a Simulink environment. The source voltage is 100 volts, and the parameters taken for simulation are shown in Table 4. Various dynamic responses were simulated, including topology operation with variable loads and variable DC source voltage. In Fig.7(a), the voltage and current of the thirteen-level UXE inverter are exhibited. It is noticed that the power is approximately unity as the output voltage follow current waveform. The dynamic loading for both linear R-L load and Non-linear R-L load is shown in Fig. 7(b) and 7(c), respectively. It is observed that the number of voltage levels is maintained with the change in load. The switching frequency is constant in the case of linear loads, but a varying switching pattern is seen in the case of non-linear loads. Automatic voltage balancing by PSO based PI controller is depicted in Fig. 6(b) and 6(c). Additionally, the effect of DC source voltage variation on the operation of

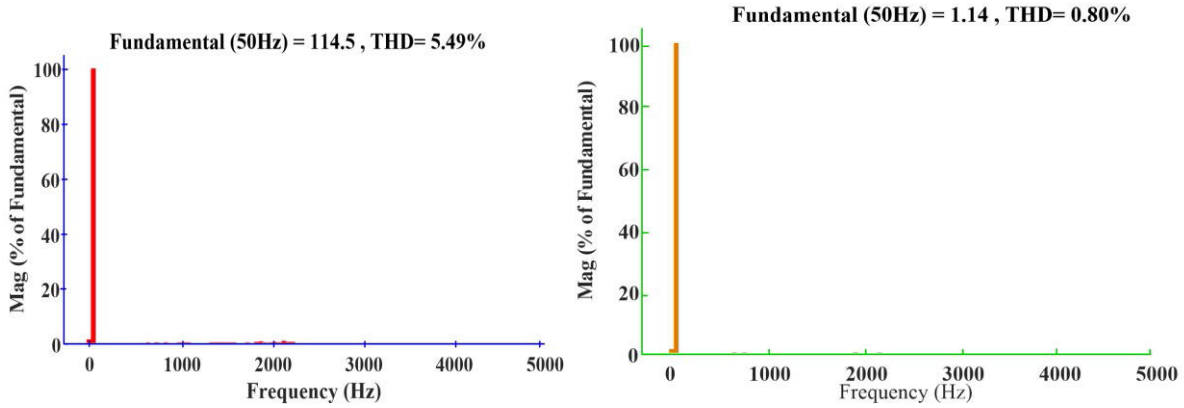

FIGURE 8. Harmonic spectrum of load voltage and current waveforms at h = 0.02.

TABLE 4. Simulation parameters.

S No.	Parameter	Simulation Value	Quantity
1.	DC Source Voltage	100V	1
2.	Peak to Peak Voltage	150V	-
3.	Frequency	50Hz	-
4.	Switching Frequency	5000Hz	-
5.	Capacitors	4700μF,50V	2
6.	Resistive Load	60Ω,80Ω,150Ω	2
7.	Inductive Load	40mH	1

the converter is seen in Fig. 7(d). The controller is working according to the source voltage variations and has maintained desired voltage of 25 volts across the capacitors. Fig.8 shows the harmonic spectrums for load voltages. It can be easily observed that only higher order harmonics are present and can be filtered out using small sized filters.

The THD in the output current and voltage at h = 0.35 are 0.80 and 5.49 respectively. Considering the Fig.9, for low values of h (0.01), the response with ZN is sluggish and oscillatory compared with PSO. For h = 0.02 and h = 0.033, the voltage across the DC link voltage stabilizesearly with K_p and K_i values calculated by PSO. So, it can be observed that the PSO based control results in much precise and exact K_p and K_i, such that the DC link voltagestabilizes much earlier compared to the values generated with ZN method. The main issue faced with hysteresis control is the irregularity of theswitching frequency. With increase in the hysteresis bandwidth (h), this can be limitedwith a compromise in current THD. The DC bus formed by capacitors are regulates at $V_{dc}/2$. K_p and K_i obtained by applying PSO are found to as 0.035 and 0.045, respectively. The hysteresis band is restricted to a small value and simultaneous reduction of the switching frequency and the THD of the load current is not possible as shown in Fig.10. The average switching frequency variation and the variation inthe load current THD with the hysteresis band control is shown in Fig.10.

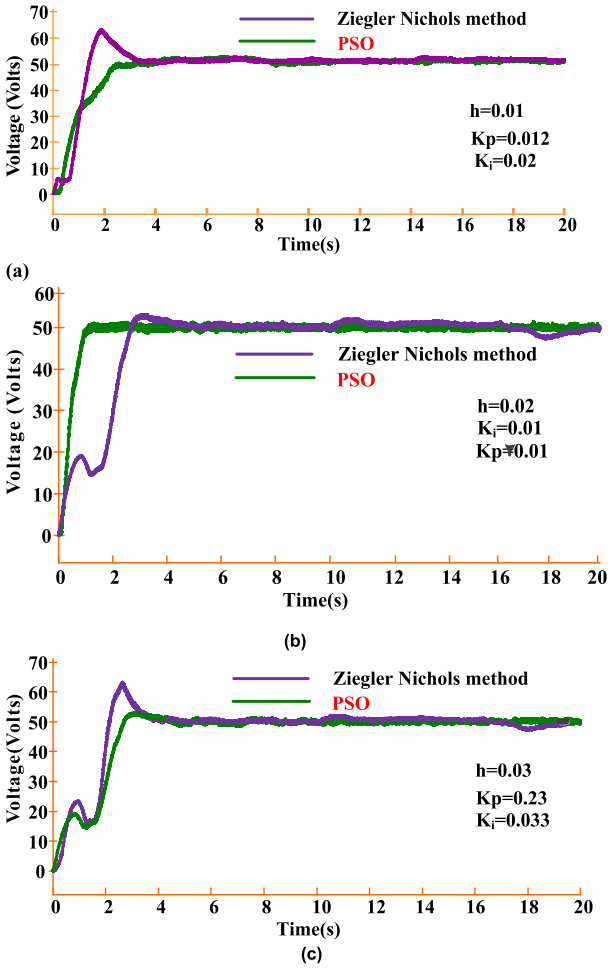

FIGURE 9. Load Voltage and load current waveforms.

In Fig.11, the percentage THD in the load voltage as well as load current decreases considerably with the increase in the hysteresis band width (h) from h = 0.01 to h = 0.3, reaches a minimum value of percentage voltage THD of 4.73 at about h = 0.02 and again with the increment in h, both

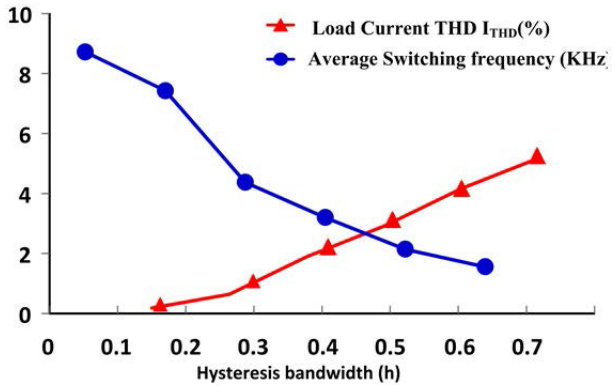

FIGURE 10. Variation of load current THD and average switching frequency with hysteresis bandwidth (h).

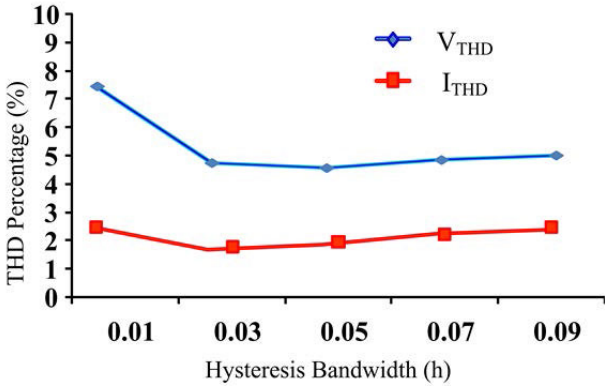

FIGURE 11. Percentage THD variation in load voltage and current at different h.

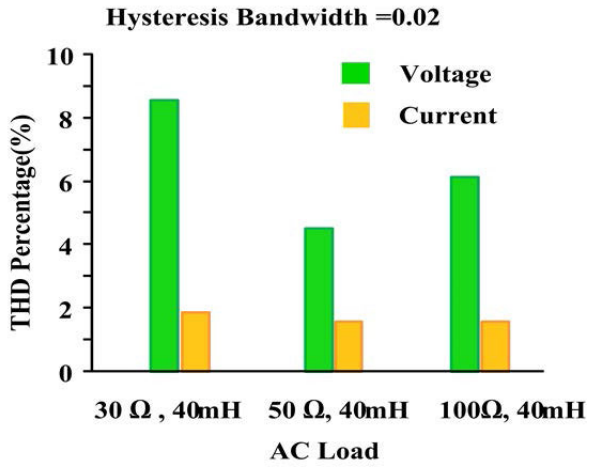

FIGURE 12. Percentage voltage and current THD at different load impedance and at differentbandwidth.

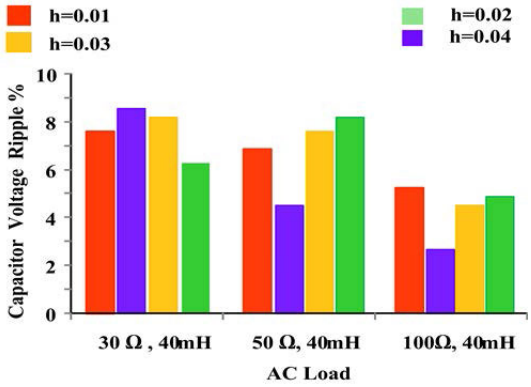

FIGURE 13. Percentage ripple in the capacitor voltage at different load impedance and at different bandwidth (h).

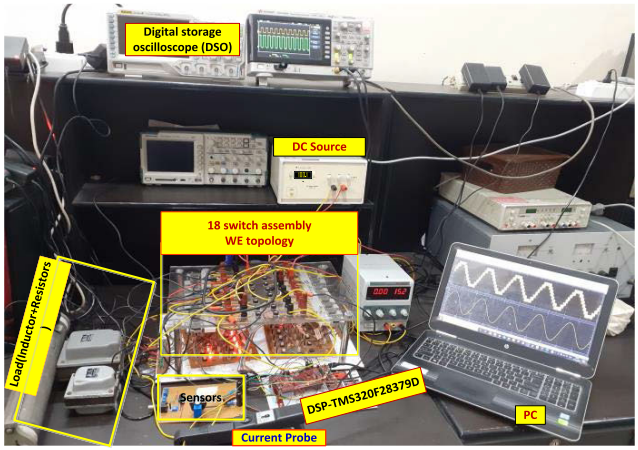

FIGURE 14. Hardware setup for experimental validation.

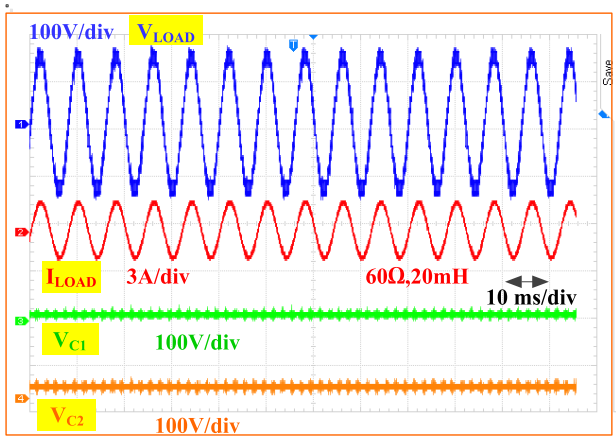

FIGURE 15. Output voltage, current waveforms and voltage across the capacitors C_1 and C_2 during constant load.

the current and voltage THD increase. Percentage THD of voltage and current with three different AC loads have been depicted in Fig.12 at hysteresis bandwidth of 0.02. TheTHD of both load voltage and load current decreases as the load impedance decreaseand increases for low values for load impedance In Fig.13, percentage ripple in the DC-link voltage is shown at four different values h; that is h = .01, h = 0.02, h = 0.03 and h = 0.04. The response isexhibited when K_p and K_i are 0.01 and 0.01 respectively. The DC link voltage is properly maintained by balancing the capacitor voltages at 25 volts each. The analysis of the effect of load voltage

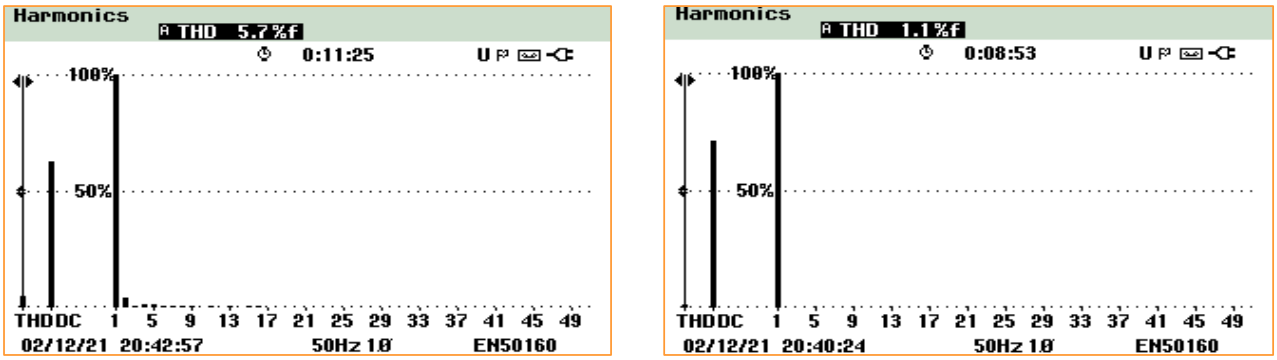

FIGURE 16. Harmonic spectrum for (a) Voltage and (b) Current at h = 0.02

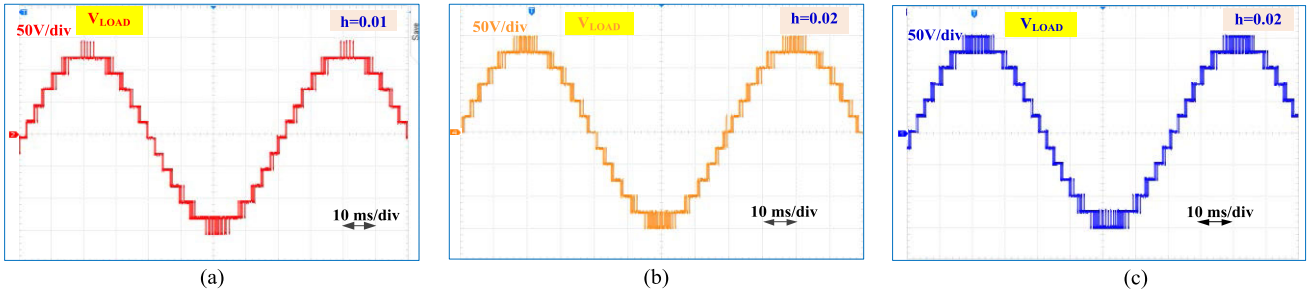

FIGURE 17. Output voltage waveforms at different bandwidth (h)(a)h = 0.04 (b)h = 0.02 (c) h = 0.03.

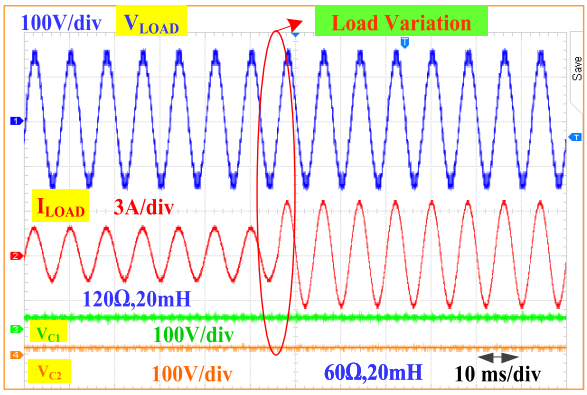

FIGURE 18. Output voltage, current waveforms and voltage across the capacitors C_1 and C_2 during variable load.

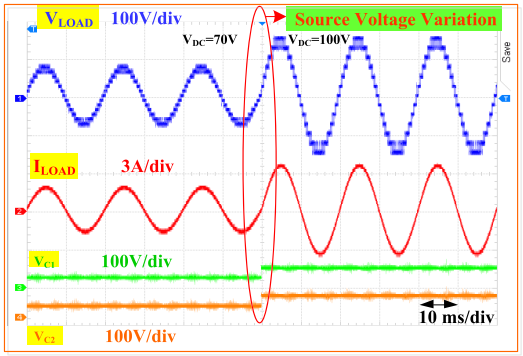

FIGURE 19. Output voltage, current waveforms and voltage across.

and hysteresis bandwidth sows that, for low values of the load impedance, the percentage capacitor voltage ripple is high and maximum at h = 0.04. For medium load impedance (50Ω, 40 mH), the ripple content reduces particularly at h = 0.04. At higher values of load impedance (100Ω, 40mH), the ripple reduces and is minimum at h = 0.04.

V. EXPERIMENTAL RESULTS

Experimental validation of results and analysis for 12-band hysteresis control of UXE-type inverter is done in this section. A 250V-350W prototype has been used for the experimental purpose is shown in Fig.14.

Texas DSP TMS320F28379D generates the gate pulses. Typhoon HIL emulators are used to verify the simulation results and validation of real-time results. The hardware results show that, as the bandwidth is increased, the switching in the output load voltage has been increased. In Fig.15, the output voltage and current with capacitor voltages are shown with the source voltage at 100 Volt. Harmonic spectrums of load voltage and current are shown in Fig.16. These spectrums confirm the results obtained in the simulation. Experimental results for load voltage variation with varying

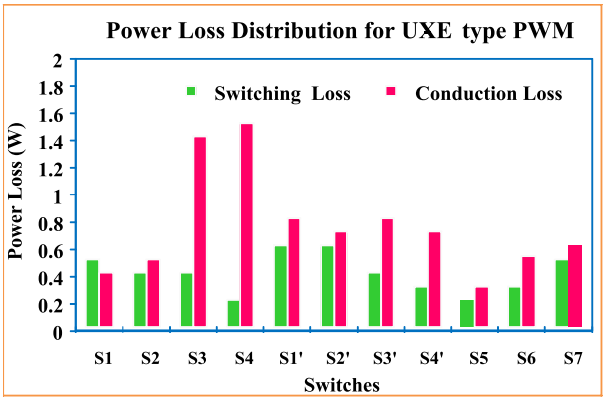

FIGURE 20. Power loss breakup for all the switches at h = 0.02.

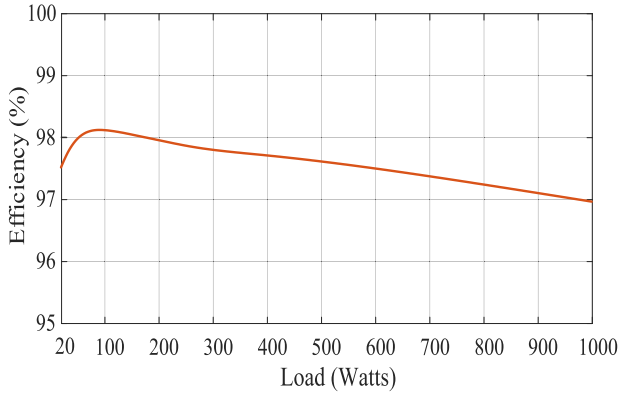

FIGURE 21. Efficiency of UXE with varying output power.

the hysteresis bandwidth from h = 0.01 to h = 0.03 are shown in Fig.17. The output voltage has 13 levels, and capacitor voltages are maintained at 25V each. The dynamic response of the inverter operated by 12-band hysteresis control is analyzed by varying the load impedance to double of the rated value.

The output load voltage is maintained the same, and the load current is increased by two times, confirming the satisfactory operation of UXE-type inverter and PSO based 12-band hysteresis control. Variation of DC source voltage is shown in Fig.19. The DC source voltage is varied from 70V to 100V, and the voltage across the capacitor is also changed and operated satisfactorily. Power loss breakup has been shown in Fig.20. The analysis has been done by the PLECS simulation tool. The total switching loss calculated using PLECS is 10W, and the loss on actual hardware is 12W. The efficiency curve for varying loads is shown in Fig.21. The maximum efficiency is achieved at 90W that is approximately 98.2%, and then starts decreasing with load increment.

VI. CONCLUSION

The twelve-band hysteresis control technique was validated on a thirteen level UXE-type inverter. The voltage across the DC link was successfully maintained at half of the input side DC source voltage using nature-inspired particle swarm optimization (PSO) based PI control. The fast convergence of PSO for finding the most appropriate values for gain constants enables the faster controller's tuning compared to the conventional Ziegler Nichols (ZN) method. The K_p and K_i calculated using PSO resulted in the early settling of DC link voltage. However, this control is effected by the noise in the error signal, thus leads to undesirable voltage levels. The results were compared, analyzed and verified in simulation, on hardware prototype driven by DSP TMS320F28379D and on real-time Typhoon Hardware in Loop emulator.

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DEEPAK UPADHYAY received the B.Tech. degree from the University of Pune, Pune, India. He is currently pursuing the master's degree in power system and drives with Aligarh Muslim University, Aligarh, India. He has published research papers in various journals and international conferences. His research interests include integration of photovoltaic distributed systems, control of multilevel converters, and electric vehicles. He has also received Best Paper Award in ICRP-2020.

MOHAMMAD ALI (Member, IEEE) was born in Tripoli, Libya, in 1983. He received the B.E., M.Tech., and Ph.D. degrees in electrical engineering from Aligarh Muslim University, Aligarh, in 2011, 2013, and 2019, respectively. He is currently working as an Assistant Professor with the Department of Electrical Engineering, Aligarh Muslim University, where he is developing and modulating novel asymmetrical multilevel inverters for renewable energy applications. Aside, he is also working on matrix converters. He has previously worked as a Senior Research Fellow under the sponsored Project Collaborative Research Grant Scheme of Capability Systems Centre, University of New South Wales Canberra, Australia, sanctioned to Dr. Mohd Tariq (as a PI) with the Department of Electrical Engineering, Aligarh Muslim University, and, earlier as an Assistant Professor with the Department of Electrical Engineering for three years, from 2016 to 2019. He has also worked as a Visiting Researcher at Qatar University, in 2018. Furthermore, he has published three new multilevel topologies for patents. He is the author of IEEE TRANSACTIONS/journals and IET journals and several international conference papers. Besides, he is also the author of two book chapters in the *Power Electronics Handbook* (Elsevier). His research interests include AC-AC and DC-AC power converter topologies, their analysis and modulation, and their application in renewable energy systems connected to the grid and stand-alone systems.

MOHD TARIQ (Senior Member, IEEE) received the bachelor's degree in electrical engineering from Aligarh Muslim University, Aligarh, the master's degree in machine drives and power electronics from the Indian Institute of Technology (IIT)—Kharagpur, and the Ph.D. degree in electrical engineering (with focus on power electronics and control) from Nanyang Technological University (NTU), Singapore. He is currently working as an Assistant Professor with Aligarh Muslim University, where he is directing various international and national sponsored research projects and leading a team of multiple researchers in the domain of power converters, energy storage devices, and their optimal control for electrified transportation and renewable energy application. Previously, he has worked as a Researcher with the Rolls-Royce-NTU Corporate Laboratory, Singapore, where he has worked on the design and development of power converters for more electric aircraft. Before joining his Ph.D. degree, he has worked as a Scientist with the National Institute of Ocean Technology, Chennai, under the Ministry of Earth Sciences, Government of India, where he has worked on the design and development of BLDC motors for the underwater remotely operated vehicle application. He also worked as an Assistant Professor with the Maulana Azad National Institute of Technology (MANIT), Bhopal, India. He has authored more than 150 research papers in international journals/conferences, including many articles in IEEE TRANSACTIONS/journals. He is also the inventor of approximately 25 patents granted/published by the patent offices of USA, Australia, U.K., EP, India, and China. He was a recipient of the 2019 Premium Award for Best Paper in *IET Electrical Systems in Transportation* journal for his work on more electric aircraft and also the Best Paper Award from the IEEE Industry Applications Society's (IAS) and the Industrial Electronic Society (IES), Malaysia Section—Annual Symposium (ISCAIE-2016) held in Penang, Malaysia, and many other best paper awards in different international conferences. He is a Young Scientist Scheme Award, in 2019, supported by the Department of Science and Technology, Government of India, a Young Engineer Award, in 2020, by the Institution of Engineers, India, and a Young Researchers Award, in 2021, by the Innovation Council, AMU. He is also the Founder Chair of IEEE AMU student branch and the Founder Chair of IEEE SIGHT AMU.

SHAHBAZ AHMAD KHAN received the Diploma degree in engineering and the Bachelor of Engineering degree in electrical engineering. He is currently pursuing the master's degree in electrical engineering (power systems and drives) with ZHCET, Aligarh Muslim University. He has coauthored various research papers in international journals and international conferences. His research interests include multilevel power electronics converter, electric vehicles, grid integration of distributed energy systems, and battery storage systems.

BASEM ALAMRI (Member, IEEE) received the B.Sc. degree (Hons.) in electrical engineering from the King Fahd University of Petroleum and Minerals (KFUPM), in 2001, the M.Sc. degree (Hons.) in sustainable electrical power from Brunel University, London, U.K., in 2007, the M.Sc. degree (Hons.) in electrical power systems from King Abdulaziz University, Jeddah, Saudi Arabia, in 2008, and the Ph.D. degree in electrical power engineering from Brunel University, in 2017. He is currently an Assistant Professor in electrical engineering with the College of Engineering, Taif University. His research interests include power systems, power quality, power filter design, and smart grids, with a particular emphasis on the integration of renewable energy sources with power grids. He is a member of many international and local professional organizations. He is also a Certified Energy Auditor (CEA ®), Certified Energy Manager (CEM ®), and a Certified Measurement & Verification Professional (CMVP ®) of the Association of Energy Engineers (AEE), USA. He has received many awards and prizes, including a certificate from the Advance Electronics Company (AEC) in recognition of the Outstanding Academic Achievement during the B.Sc. degree with KFUPM. He also received the National Grid (NG) Prize, the Power Grid Operator in the U.K., for being the top distinction student of the M.Sc. degree of the SEP Program with Brunel.

AHMAD ALAHMADI (Senior Member, IEEE) received the Ph.D. degree in nano-electronic devices from the School of Engineering, Ohio University, Athens, OH, USA. Since July 2017, he has been the Vice Dean of the Faculty of Engineering, Taif University, Saudi Arabia, where he is currently an Associate Professor with the Department of Electrical Engineering, Faculty of Engineering. His research interests include control systems and nano-electronic devices.