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Systematic Transistor Sizing of a CNFET-Based Ternary Inverter for High Performance and Noise Margin Enlargement

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ABSTRACT Noise and variation are the two major challenges for the reliability of digital circuits, especially multiple-valued logic (MVL) circuits where the entire voltage range is divided into some narrow zones. In spite of few correct examples, many ternary inverters with reduced noise margins have been presented in the literature. The defect is mainly because of their improperly shaped voltage transfer characteristic (VTC). With proper transistor sizing, we can rectify the problem and provide uniformly wide noise margin values while maintaining power-delay product (PDP) low. As far as we know, none of the previous ternary inverters has been given based on a methodical transistor sizing procedure. In this paper, a systematic transistor sizing through physical equations is suggested for an existing standard ternary inverter (STI), whose original sizes for the carbon nanotube FETs (CNFETs) are inappropriate. This paper includes a comprehensive investigation to determine appropriate values for the physical parameters of the CNFET-based STI. Compared with the original design, with a negligible increase in circuit delay and area, simulation results show that the proposed ternary inverter can increase noise margin and static noise margin by up to 47.7% and 83.3%, respectively.

INDEX TERMS CNFET, inverter, noise margin, reliability, static noise margin, ternary logic, transistor sizing.

I. INTRODUCTION

Multiple Valued Logic (MVL) has a long history. In 1920, Jan Lukasiewicz began to create the first MVL system. Research in MVL, including ternary circuits and systems, also started in the mid-sixties [1]–[3]. There are several ternary CMOS circuits in the literature [2]–[6]. However, with the beginning of the Carbon Nanotube Field Effect Transistor (CNFET) [7], MVL circuitry has revived once again and has been soared in popularity in the recent decade. Multi-threshold transistors are absolutely necessary to construct MVL circuits, in which there are more than two voltage levels. Multi-Threshold CMOS (MTCMOS) devices make it feasible to have transistors with normal, low, and high thresholds [8], [9]. In addition, the emerging CNFET technology provides high flexibility in tuning the threshold voltage by adjusting the diameter of Carbon Nanotubes (CNTs) [7], [10].

Despite several advantages, vulnerability against noise is the Achilles' heel of MVL circuits and systems, especially in today's ongoing reduced voltage. Several ternary [11]–[30], quaternary [29]–[31], and quinary [25] inverters with reduced noise margins (NMs) have been presented in the literature. They seriously suffer from unreliability and vulnerability to noise and voltage variation because of their improper Voltage Transfer Characteristic (VTC) shape and non-uniform NMs. There are some examples of ternary inverters with uniform NMs in the literature a well. The VTC curves in [32]–[35] are properly shaped. However, the ones in [32]–[34] have more transistors than other well-known competitors. Besides, the structures of [33] and [34] are based on dynamic logic and Differential Cascode Voltage Switch Logic (DCVSL), respectively, whose applications are somehow limited in digital electronics. Additionally, [34] needs an extra power supply rail of $1/2V_{DD}$ to be able to produce logic '1'.

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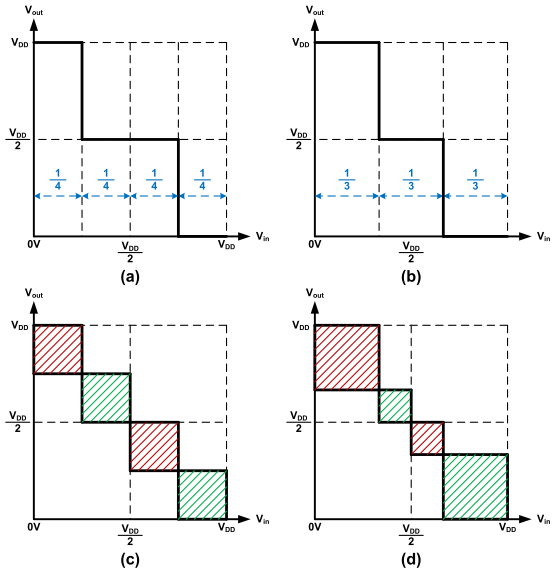

FIGURE 1. VTC of a ternary inverter with ideal steep slopes and sharp corners, (a) Properly divided in 4 equal parts, (b) Improperly divided in 3 equal parts, (c) Proper VTCs form uniform NMs, (d) Improper VTCs form non-uniform NMs.

In spite of NM uniformity, the selected threshold voltages in [35] cause performance degradation and high sensitivity to variations. Finally, none of the papers has suggested a methodical transistor sizing procedure.

Similar to Fig. 1(a), the VTC curve of a ternary inverter must be divided into four equal parts from the x-axis (V_{in}-axis) [36]. Several papers have incorrectly considered Fig. 1(b) as the ideal VTC curve for a Standard Ternary Inverter (STI). As a result of this false presumption, the VTCs of [11]–[30] have been wrongfully divided into three parts (Similar to Fig. 1(b)). Furthermore, the worst-case noise condition happens when there are noise sources on all inputs of an infinite chain of logic gates that intensify false voltage levels [37]. The scenario is equivalent to two back-to-back inverters, like inside an SRAM cell. Figs. 1(c) and 1(d) visually show how the proper and improper VTC curves form uniform and non-uniform NMs, respectively. Additionally, VTC curves with sharp corners and steep slopes are always preferred.

A proper transistor sizing can make NMs uniformly wide. For example, the ternary inverters in [15] and [38] have the same structure. Nevertheless, the latter has wider NMs because of having transistors with more appropriate sizes. The same thing is also true for the STIs in [16] and [35]. Therefore, transistor sizing has a significant impact on the suitability and practicality of ternary circuits and should carefully be considered. To the best of our knowledge, a systematic transistor sizing procedure has never been presented before. The size of transistors for ternary inverters has previously been determined by the trial and error method with the aim of reducing Power-Delay Product (PDP). Even though the optimization of PDP is crucial, circuit designers

TABLE 1. Truth tables of STI, NTI, and PTI.

a	$\bar{a}$	$\bar{a}-$	$\bar{a}+$
0	2	2	2
1	1	0	2
2	0	0	0

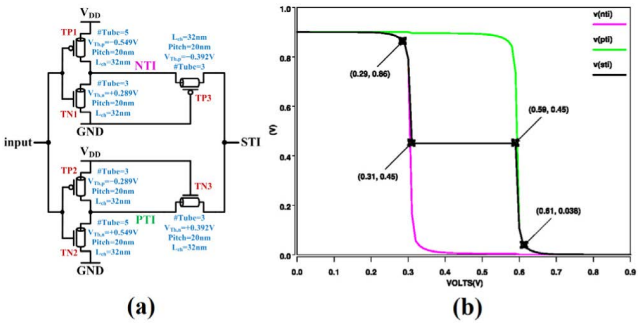

FIGURE 2. STI presented in [16], (a) Circuit, (b) VTC.

are indeed obliged to pay careful attention to NM as well. Otherwise, ternary circuits might lose their appropriateness.

In this paper, we thoroughly discuss the correct size of transistors for one of the previously presented ternary inverters through physical equations. The steps toward an efficient STI are given in details, considering the fact that NM and circuit performance are equally important. The rest of the paper is organized as follows: Background information is briefly reviewed in Section 2. Section 3 presents the proposed transistor sizing procedure. Simulation results in Section 4 verify the suitability of the transistor sizing procedure. Limitations of the study are mentioned in Section 5. Finally, Section 6 concludes the paper.

II. BACKGROUND INFORMATION

A. REVIEW OF TERNARY INVERTER IN [16]

Among several different STIs, the one in [16] (Fig. 2(a)) has a straightforward structure with some great advantages. This ternary inverter, whose VTC is plotted in Fig. 2(b), is composed of six CNFETs. It consists of a Negative Ternary Inverter (NTI), a Positive Ternary Inverter (PTI), and a couple of voltage dividers (TN3 and TP3, which are constantly ON) to produce the standard ternary output on the basis of (1). The truth tables of STI, NTI, and PTI are depicted in Table 1. There are three ternary logic values, '0', '1', and '2', represented by $0V$, $1/2V_{DD}$, and V_{DD} in digital electronics, respectively. The VTC curves of NTI and PTI, which are binary inverters, are respectively shifted to left and right so that $NTI('1')='0'$ and $PTI('1')='2'$ (Fig. 2(b)).

$$STI = \frac{NTI + PTI}{2} \tag{1}$$

The VTC curve shows the logical behavior of an inverter and reveals NM values. In ternary logic, NMs need to be calculated four times by (2) to (5) [39]. The equations are the extended versions of the ones required for binary NM

calculations. According to Fig. 2(b) and based on (2) to (5), $NM_0 = 290mV$, $NM_{1-} = 140mV$, $NM_{1+} = 140mV$, and $NM_2 = 290mV$. Their minimum amount is considered the final NM of the circuit (6). Since the VTC curve is almost divided into three equal parts from the V_{in}-axis (Fig. 2(b)), NM values are not uniform, meaning that NM_0 and NM_2 are 150mV wider than NM_{1-} and NM_{1+}. As a result, this ternary inverter suffers from reduced NMs. However, its VTC curve has steep slopes and sharp corners around logic '1'. These great advantages are not available in many other ternary inverters.

$$NM_0 = |V_{I0} - V_{O0}| \tag{2}$$
$$NM_{1-} = |V_{O1} - V_{I1-}| \tag{3}$$
$$NM_{1+} = |V_{I1+} - V_{O1}| \tag{4}$$
$$NM_2 = |V_{O2} - V_{I2}| \tag{5}$$
$$NM = \min(NM_0, NM_{1-}, NM_{1+}, NM_2) \tag{6}$$

B. REVIEW OF CNFET TECHNOLOGY

Graphene is a two-dimensional form of carbon allotrope. It is rolled up along a chiral vector to build a hollow cylinder, called CNT. The chiral vector is defined by (7), where n_1 and n_2 are non-negative integers that indicate the conductivity of single-wall CNTs (Fig. 3(a)). Depending on the values of n_1 and n_2, the obtained CNT might be armchair (Fig. 3(b)) where $n_1 = n_2$, zigzag (Fig. 3(c)) where $n_1 = 0$ or $n_2 = 0$, or chiral (Fig. 3(d)). If $|n_1 - n_2| = 3K$ for $K=0, 1, 2, \ldots$, the obtained CNT is metallic. Otherwise, it has semiconducting characteristics. The diameter of CNT (D_{CNT}) can be calculated by (8) [10], where a_0 (≈ 0.142nm) is the intra-atomic carbon-to-carbon distance.

$$\overrightarrow{Chiral} = n_1 \times \vec{a_1} + n_2 \times \vec{a_2} \tag{7}$$
$$D_{CNT}(nm) = \frac{\sqrt{3} \times a_0}{\pi}\sqrt{n_1^2 + n_2^2 + n_1 n_2} \approx 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1 n_2} \tag{8}$$

One or more semiconducting CNTs are used as the channel of transistors. Figure 4 shows the structure of the MOSFET-like CNFET device, where L_{ch}, L_{dd}, and L_{ss} are the lengths of the undoped CNT channel, doped CNT drain-side extension, and doped CNT source-side extension regions, respectively. The total transistor width (W_{Gate}) is calculated by (9) [40], in which W_{min} is the minimum gate width, N is the number of CNTs, and $Pitch$ is the distance between the centers of two neighboring CNTs. Moreover, the threshold voltage of the transistor (V_{Th}) is a function of D_{CNT}, and is calculated by (10), where E_g is the bandgap energy, V_π (≈ 3.033eV) is the carbon $\pi - \pi$ bond energy, and e ($\approx 1.6 \times 10^{-19}$C) is the unit electron charge. As it is evident in (10) [10], it is possible to tune V_{Th} by altering D_{CNT} since there is an inverse correlation between these two parameters.

$$W_{Gate} = \max(W_{\min}, N \times Pitch) \tag{9}$$
$$V_{Th} = \frac{E_g}{2 \times e} = \frac{\sqrt{3}}{3} \times \frac{a \times V_\pi}{e \times D_{CNT}} \approx \frac{0.43}{D_{CNT}(nm)} \tag{10}$$

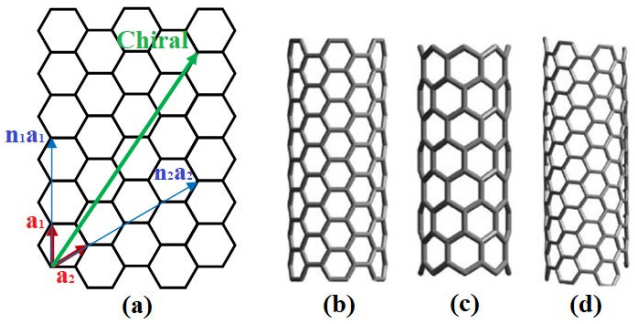

FIGURE 3. Carbon Nanotube, (a) Graphene, (b) Armchair CNT, (c) Zigzag CNT, (d) Chiral CNT.

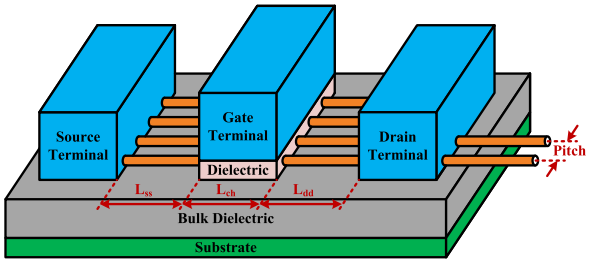

FIGURE 4. MOSFET-like CNFET device [10].

CNFETs follow the same voltage and current equations of MOSFETs [41]. The I-V characteristics for an nCNFET and a pCNFET with the same device parameters are plotted in Figs. 5 and 6, respectively. Both transistors have three CNTs with the diameter of 1.8009nm. Figs. 5(a) and 6(a) show I_{ds} (I_{sd}) versus V_g. As the gate voltage increases, the n-type transistor switches on whereas the p-type one turns off. Furthermore, Figs. 5(b) and 6(b) display I_{ds} (I_{sd}) versus V_d for different V_{gs}s. Regarding Figs. 5 and 6, the following observations are made:

1. In general, CNFET and MOSFET technologies have similar I-V characteristics.
2. The same amount of current flows through the channels of nCNFET and pCNFET under identical physical and electrical conditions. For example in Figs. 5(b) and 6(b), both transistors conduct the identical amounts of current, i.e. $I_{ds,n} = I_{sd,p} = 22.1\mu A$, in $|V_{ds}| = |V_{sd}| = 0.45V$ and $V_{gs} = 0.5V$. The same phenomenon is also observed in Figs. 5(a) and 6(a), where the same amounts of current flow in the corresponding voltage points, e.g. $I_{ds,n} = I_{sd,p} = 16.6\mu A$ when $V_g = 0.45V$. This is due to the identical carrier mobility, μ, of the n-type and p-type CNFETs ($\mu_n = \mu_p$). It is in contrast with MOS transistors where $\mu_n \approx 2 \times \mu_p$.
3. While the saturation current of an MOS transistor is influenced by its effective channel length, the amount of saturation current remains constant for a CNFET device. For example, according to Figs. 5(b) and 6(b), when $V_{gs} = 0.5V$, I_{ds} (I_{sd}) is always equal to 22.1μA in the saturation region despite increasing V_d. This is in contrast to what

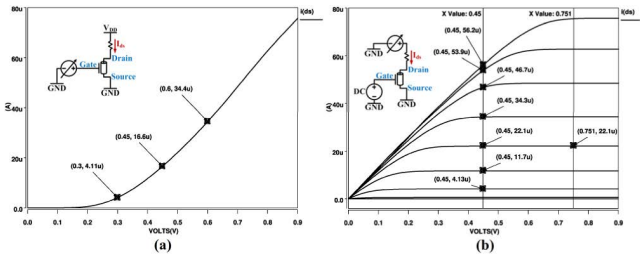

FIGURE 5. I-V characteristics of nCNFET, (a) I_{ds} vs. V_g, (b) I_{ds} vs. V_d per V_{gs}s.

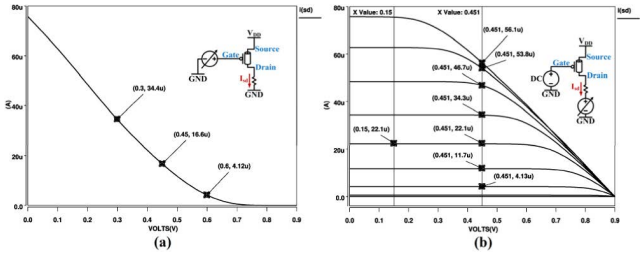

FIGURE 6. I-V characteristics of pCNFET, (a) I_{sd} vs. V_g, (b) I_{sd} vs. V_d per V_{gs}s.

happens in MOS transistors, where the saturation current enlarges gradually as V_d increases. As a result, CNFETs are needless of channel-length modulation.

III. PROPOSED TRANSISTOR SIZING

The primary target of transistor sizing is to achieve uniform NMs, where all of the NM values are almost equal. In binary logic, V_M is the point on the VTC curve where $V_{out} = V_{in}$. To make NM_L and NM_H identical, V_M must be equal to $1/2V_{DD}$ (Fig. 7(a)). In ternary logic, we consider that there are rationally two V_Ms, V_{M1} and V_{M2}, which are illustrated in Fig. 7(b). The main goal is to achieve a VTC curve that almost perfectly resembles the ideal one, depicted in Fig. 1(a). Thus, to divide the VTC curve into four equal parts, V_{M1} and V_{M2} must be on the points ($1/4V_{DD}$, $1/2V_{DD}$) and ($3/4V_{DD}$, $1/2V_{DD}$), respectively. In fact, V_{M1} is the point on the VTC curve where $V_{out} = 2V_{in}$, and V_{M2} is the point on the VTC curve where $V_{out} = 2/3V_{DD}$. In addition, these points are respectively on the VTCs of NTI and PTI as well.

First, we solely consider NTI. The aim is to shift its VTC curve onto V_{M1}, where $V_{in} = 1/4V_{DD}$ and $V_{out} = 1/2V_{DD}$. The operating regions of the NTI transistors must initially be determined. According to (11) to (14), both transistors operate in the saturation mode. Note that there are two different ways to shift a VTC:

1. By adjusting the channel width and channel length of transistors.
2. By adjusting the threshold voltage of transistors.

As a possible third solution, a combined method can be utilized as well. Nonetheless, all of the presented ternary circuits so far, including the one in [16], rely on multi-threshold transistors. Resembling TN1 and TP1 in

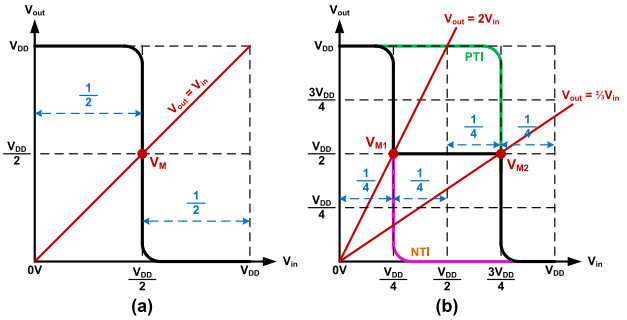

FIGURE 7. V_M in VTC curve, (a) There is one V_M in binary logic, (b) There are two V_Ms in ternary logic.

Fig. 2(a), we consider $V_{Th,n}$ (which is intrinsically positive; $V_{Th,n} > 0$) and $V_{Th,p}$ (which is intrinsically negative; $V_{Th,p} < 0$) to be *Low-*V_{Th} and *High-*V_{Th}, respectively. Additionally, with simultaneous consideration of $V_{out} = 2V_{in}$, we reach the conclusion that both transistors operate in the saturation mode. In this regard, (11) and (13) impose two constraints: *i)* $V_{Th,n} < 1/4V_{DD}$, and *ii)* $|V_{Th,p}| < 3/4V_{DD}$.

$$V_{gs,n} = \underbrace{V_{in}}_{\frac{V_{DD}}{4}} - 0 > \underbrace{V_{Th,n}}_{Low\ V_{Th}} \tag{11}$$

$$V_{gs,n} - V_{Th,n} = V_{in} - V_{Th,n} < V_{ds,n} = V_{out} = 2V_{in}$$

$$\Rightarrow \underbrace{-V_{Th,n}}_{-} < \underbrace{V_{in}}_{+} \tag{12}$$

$$V_{gs,p} = \underbrace{V_{in}}_{\frac{V_{DD}}{4}} - V_{DD} < \underbrace{V_{Th,p}}_{High\ V_{Th}} \tag{13}$$

$$V_{gs,p} - V_{Th,p} = V_{in} - V_{DD} - V_{Th,p} > V_{ds,p} = 2V_{in} - V_{DD}$$

$$\Rightarrow \underbrace{-\underbrace{V_{Th,p}}_{High\ V_{Th}}}_{\gg 0} > \underbrace{V_{in}}_{>0} \tag{14}$$

When an NTI is individually dealt with, $I_{ds,n} = I_{sd,p}$ and consequently we have (15):

$$\frac{K_n}{2}\left(V_{gs,n} - V_{Th,n}\right)^2 = \frac{K_p}{2}\left(V_{gs,p} - V_{Th,p}\right)^2 \tag{15}$$

Afterward, $V_{gs,n}$ and $V_{gs,p}$ in (15) are quantified as in (16):

$$\frac{K_n}{K_p}\left(V_{in} - V_{Th,n}\right)^2 = \left(V_{in} - V_{DD} - V_{Th,p}\right)^2$$

$$\Rightarrow \underbrace{\sqrt{\frac{K_n}{K_p}}}_{+}\underbrace{\left(V_{in} - V_{Th,n}\right)}_{+} = \pm\underbrace{\left(V_{in} - V_{DD} - V_{Th,p}\right)}_{-} \tag{16}$$

Since the left-side of the equation is positive and the right-hand side parenthesis is negative, we accept the minus sign in the right-side of the equation to maintain equality. After

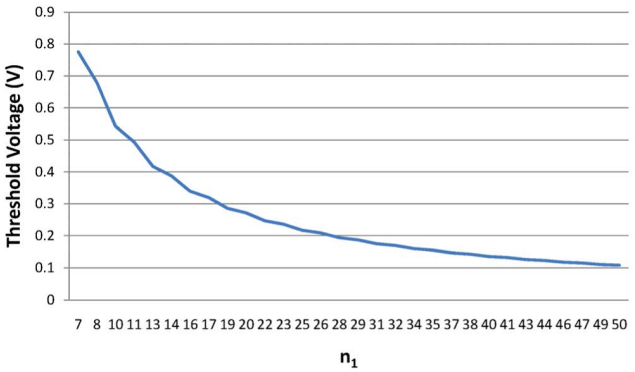

FIGURE 8. Threshold voltage vs. n_1 for a CNFET device with zigzag CNTs (n_1 values which are multiples of 3 are excluded).

some algebraic simplifications, (17) is procured:

$$V_{in} = \frac{V_{DD} + V_{Th,p} + \sqrt{\frac{K_n}{K_p}} V_{Th,n}}{1 + \sqrt{\frac{K_n}{K_p}}} \tag{17}$$

If we aim for $V_{in} = 1/4V_{DD}$, the first condition is that the proportion of K_n to K_p has to be 9X. It leads us to (18):

$$V_{in} = \frac{V_{DD} + V_{Th,p} + 3V_{Th,n}}{4} \tag{18}$$

Table 2 shows the required considerations for NTI. The threshold voltage of a CNFET device is determined by its chiral indices, n_1 and n_2. Regarding (8) and (10), the second condition, i.e. $|V_{Th,p}| = 3 \times V_{Th,n}$, leads to the deduction that the proportion of $n_{1,n}$ to $n_{1,p}$ must equal 3 for zigzag CNTs, where $n_2 = 0$ (19). However, in this situation, $n_{1,n}$ becomes multiple of 3, and the corresponding CNT becomes metallic. Therefore, if $n_{1,p} = 10$, $n_{1,n}$ is assumed to be 29 instead of 30. As it is plotted in Fig. 8, threshold voltage variations for higher values of n_1 are negligible; hence, our supposition does not have a considerable effect on the final outcome. The chiral indices of (10, 0) and (29, 0) lead to 0.549V and 0.189V threshold voltages, respectively, which are in accordance with the existing constraints in Table 2 in 0.9V power supply. Since D_{CNT} is subject to variation, according to Fig. 8, the threshold voltage variation becomes significant if chiral indices smaller than (10, 0) are selected. On the other hand, larger chiral indices result in extremely low threshold voltages, which, in turn, lead to more leakage and sub-threshold power dissipation [42].

$$\frac{|V_{Th,p}|}{V_{Th,n}} = 3 \Rightarrow \frac{\frac{0.43}{\frac{a}{\pi} \times n_{1,p}}}{\frac{0.43}{\frac{a}{\pi} \times n_{1,n}}} = 3 \Rightarrow \frac{n_{1,n}}{n_{1,p}} = 3 \tag{19}$$

Furthermore, since $\mu_n = \mu_p$, there are three possible options to satisfy the first condition in Table 2, whose extended version is shown in (20). These options are $N(nCNFET) = 9\times N(pCNFET)$, $L_{ch}(pCNFET) = 9\times L_{ch}(nCNFET)$, and $Pitch(nCNFET) = 9\times Pitch(pCNFET)$. However, the first option leads to considerable power dissipation. As it is

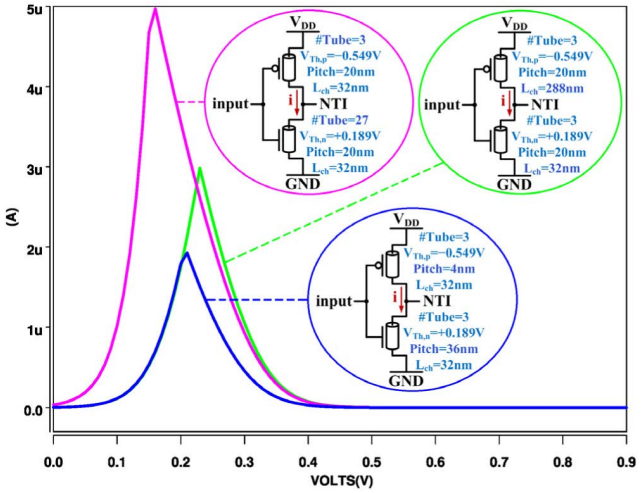

FIGURE 9. The amount of current in NTI vs. V_{in}.

demonstrated in Fig. 9, the peak power of the first option compared to the second and third ones is approximately 1.66X and 2.5X, respectively. On the other hand, the third option might weaken driving capability of the cell. This leads us to the second alternative, whose amount of current stands in the middle in Fig. 9 (the green curve). However, this option is also somewhat inappropriate because a significant increase in channel length will cause a major circuit delay. Thus, a middle-ground solution is taken into account in this paper by considering $L_{ch}(nCNFET) = 32nm$, $L_{ch}(pCNFET) = 96nm$ ($=3\times L_{ch}(nCNFET)$), $Pitch(pCNFET) = 10nm$, and $Pitch(nCNFET) = 30nm$ ($=3\times Pitch(pCNFET)$). In fact, a combination of the second and third options is utilized.

$$\frac{K_n}{K_p} = 9 \Rightarrow \frac{\mu_n \times C_{OX} \times \left(\frac{N \times Pitch}{L_{ch}}\right)_n}{\mu_p \times C_{OX} \times \left(\frac{N \times Pitch}{L_{ch}}\right)_p} = 9 \tag{20}$$

The required conditions depicted in Table 2 are only one possible way to satisfy $V_{in} = 1/4V_{DD}$ in (17). Mathematically, there are infinite ways to do so. By applying $V_{in} = 1/4V_{DD}$ in (17), we reach (21):

$$\frac{V_{DD}}{4} \times \left(1 + \sqrt{\frac{K_n}{K_p}}\right) = V_{DD} + V_{Th,p} + \sqrt{\frac{K_n}{K_p}} V_{Th,n}$$
$$\Rightarrow V_{Th,p} = V_{DD} \times \left(\sqrt{\frac{K_n}{K_p}} - 3\right) - \sqrt{\frac{K_n}{K_p}} V_{Th,n} \tag{21}$$

- If $\sqrt{(K_n/K_p)} = 3$, then $V_{Th,p} = -3\times V_{Th,n}$ is an acceptable equation. For instance, ($V_{Th,n} = 0.15V$, $V_{Th,p} = -0.45V$) and ($V_{Th,n} = 0.2V$, $V_{Th,p} = 0.6V$) are satisfactory pairs of threshold voltages.
- If $\sqrt{(K_n/K_p)} = 2$, then $V_{Th,p} = -V_{DD} - 2\times V_{Th,n}$ does not lead to an acceptable value for $V_{Th,p}$. For different values of $V_{Th,n}$, $|V_{Th,p}| > V_{DD}$, which is wrong. Any

TABLE 2. Transistor sizing considerations for NTI.

Constraints	Required Conditions
$V_{Th,n} < \frac{V_{DD}}{4}$	$K_n = 9\times K_p$
$\lvert V_{Th,p}\rvert < \frac{3V_{DD}}{4}$	$\lvert V_{Th,p}\rvert = 3\times V_{Th,n}$

TABLE 3. Transistor sizing considerations for PTI.

Constraints	Required Conditions
$V_{Th,n} < \frac{3V_{DD}}{4}$	$K_p = 9\times K_n$
$\lvert V_{Th,p}\rvert < \frac{V_{DD}}{4}$	$V_{Th,n} = 3\times\lvert V_{Th,p}\rvert$

other numbers smaller than 2 would lead to a wrong result too.

- If $\sqrt{(K_n/K_p)} = 4$, then $V_{Th,p} = V_{DD} - 4\times V_{Th,n}$ does not lead to an acceptable value for $V_{Th,p}$ either. For small values of $V_{Th,n}$, like 0.15V or 0.2V, $V_{Th,p}$ becomes positive in 0.9V power supply, which is again incorrect. Any other numbers greater than 4 would lead to a wrong result as well.

Therefore, $K_n = 9\times K_p$ is the only acceptable condition, and other correlations between K_n and K_p do not result in any meaningful values for $V_{Th,n}$ and $V_{Th,p}$ although it is mathematically feasible to achieve other results.

After dealing with NTI, it is time to cope with PTI, whose VTC must be shifted onto V_{M2}, where $V_{in} = 3/4V_{DD}$ and $V_{out} = 1/2V_{DD}$. At first, we have to settle the operating regions of the transistors. According to (22) to (25), both transistors operate in the saturation mode. Resembling TN2 and TP2 in Fig. 2(a), we consider $V_{Th,n}$ and $V_{Th,p}$ to be *High-*V_{Th} and *Low-*V_{Th}, respectively. Furthermore, with simultaneous consideration of $V_{out} = 2V_{in}$, we conclude that both transistors operate in the saturation mode. In this regard, (22) and (24) impose two constraints: *i)* $V_{Th,n} < 3/4V_{DD}$, and *ii)* $|V_{Th,p}| < 1/4V_{DD}$.

$$V_{gs,n} = \underbrace{V_{in}}_{\frac{3V_{DD}}{4}} - 0 > \underbrace{V_{Th,n}}_{High\ V_{Th}} \quad \underbrace{\ll 0}\ \ \underbrace{<0} \tag{22}$$

$$V_{gs,n} - V_{Th,n} = V_{in} - V_{Th,n} < V_{ds,n} = V_{out} = \frac{3V_{in}}{4}$$

$$\Rightarrow \underbrace{-\underbrace{V_{Th,n}}_{High\ V_{Th}}}_{\ll 0} < \underbrace{-\frac{V_{in}}{4}}_{<0} \tag{23}$$

$$V_{gs,p} = \underbrace{V_{in}}_{\frac{3V_{DD}}{4}} - V_{DD} < \underbrace{V_{Th,p}}_{High\ V_{Th}} \quad \underbrace{\ll 0}\ \ \underbrace{<0} \tag{24}$$

$$V_{gs,p} - V_{Th,p} = V_{in} - V_{DD} - V_{Th,p} > V_{ds,p} = \frac{3V_{in}}{4} - V_{DD}$$

$$\Rightarrow \underbrace{-V_{Th,p}}_{+} > \underbrace{-\frac{V_{in}}{4}}_{-} \tag{25}$$

In a similar way to NTI, V_{in} will again resemble (17). The repetitive calculations are eliminated here for the sake of brevity. If we aim for $V_{in} = 3/4V_{DD}$, the first condition is that the proportion of K_p to K_n has to be 9X. It results in (26):

$$V_{in} = \frac{V_{DD} + V_{Th,p} + \frac{V_{Th,n}}{3}}{\frac{4}{3}} \tag{26}$$

Again, if we aim for $V_{in} = 3/4V_{DD}$, $V_{Th,n}$ must equal $3\times|V_{Th,p}|$. Table 3 shows the required considerations for PTI. In order to satisfy the conditions in Table 3, we suppose:

1. $|V_{Th,p}| = 0.189V$
2. $V_{Th,n} = 0.549V$ ($\approx 3\times|V_{Th,p}|$)
3. $L_{ch}(pCNFET) = 32nm$
4. $L_{ch}(nCNFET) = 96nm$ ($= 3\times L_{ch}(pCNFET)$)
5. $Pitch(nCNFET) = 10nm$
6. $Pitch(pCNFET) = 30nm$ ($= 3\times Pitch(nCNFET)$)

In the last step, TN3 and TP3, which are responsible for voltage division, are thoroughly examined. Among different physical parameters of these transistors, only the chiral indices, which settle D_{CNT}, might reshape the VTC curve of STI (Fig. 10(a)). Nevertheless, VTC remains unchanged for the n_1 values from 8 to 14, and starts to deform for higher values of n_1. Additionally, according to Fig. 10(b), $n_1 = 14$ results in the highest performance in terms of PDP (27), which is a crucial evaluating factor in digital electronics. Therefore, the chiral indices of (14, 0), which correspond to 0.392V threshold voltage, is selected for TN3 and TP3.

$$PDP = \max(Delay) \times \text{avg}(Power) \tag{27}$$

The channel length of TN3 and TP3 is set to the minimum feature size, i.e. 32nm, not to lengthen the critical path of the cell. Furthermore, Figs. 11(a) and 11(b) show how delay and power consumption vary with respect to N and $Pitch$, respectively. The intersection of delay and power diagrams reveals the optimum value of these physical parameters.

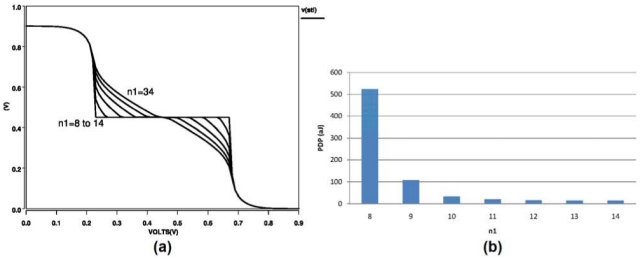

FIGURE 10. Variations vs. different values of n_1 ($n_2 = 0$) for TN3 and TP3, (a) Variations in VTC curves; $n_1 > 14$ causes VTC deformation, (b) Variation in PDP of STI; $n_1 = 14$ leads to the lowest PDP.

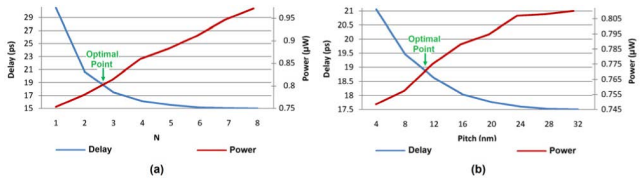

FIGURE 11. Delay and power variations vs.: (a) The number of CNTs for TN3 and TP3; The optimal point is closer to N = 3, (b) Pitch for TN3 and TP3; The optimal point is on Pitch = 11nm.

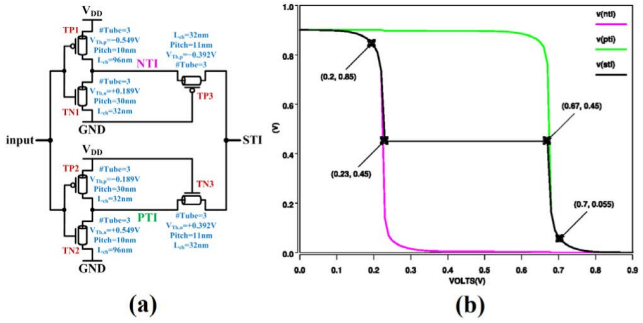

FIGURE 12. STI presented in [16] with the proposed transistor sizes, (a) Circuit, (b) VTC.

Therefore, we choose *pitch* = *11nm* and $N = 3$ (since N is a whole number) for TN3 and TP3. Eventually, based on our analytical method, the proper transistor sizes for the STI given in [16] in CNFET technology are shown in Fig. 12(a). The VTC curve is also plotted in Fig. 12(b).

IV. SIMULATION RESULTS AND COMPARISONS

The ternary inverter in [16] with the original transistor sizes (Fig. 2(a)) and proposed transistor sizes (Fig. 12(a)) are simulated by Synopsys HSPICE with 32nm Stanford CNFET model [43]–[45]. This model supports unipolar MOSFET-like CNFETs, where each transistor can have one or more CNT(s) under its gate electrode. Verified by experimental results, it includes non-idealities associated with CNFETs and provides a precise explanation of the electrical behavior of the intrinsic and additional doped CNTs [46]. All simulations are performed in 0.9V at room temperature.

NM values are often calculated from the VTC critical points. Ternary NM equations were previously presented in (2) to (6). However, there is another method of measuring NMs in practice, where two inverters are cascaded (Fig. 13). Along the linking wire in the middle, noise might alter the amount of voltage. Voltage variation is tolerable as long as the transmitted logic is not violated, and the second inverter receives the correct logic value. In brief:

- When the first inverter generates '0' (Fig. 13(a)), NM_0 is the maximum acceptable voltage increment to V(0) for the second inverter to still receive logic '0'.
- When the first inverter produces '1' (Fig. 13(b)), NM_{1-} is the maximum acceptable voltage drop from V(1) for the second inverter to still receive logic '1'.

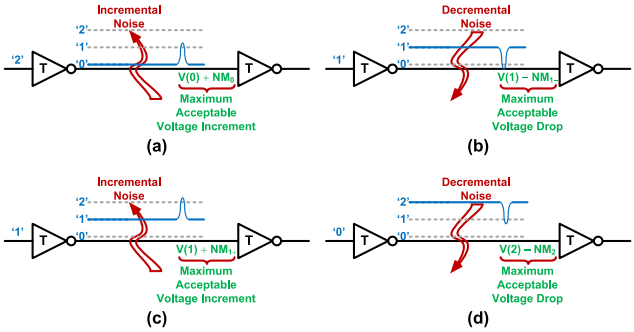

FIGURE 13. Ternary NM explanations in practice, (a) NM_0, (b) NM_{1-}, (c) NM_{1+}, (d) NM_2.

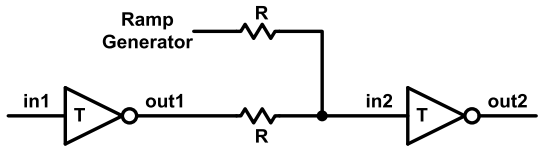

FIGURE 14. Simulation setup for ternary NM measurements in practice.

- When the first inverter generates '1' (Fig. 13(c)), NM_{1+} is the maximum acceptable voltage increment to V(1) for the second inverter to still receive '1'.
- Finally, when the first inverter produces '2' (Fig. 13(d)), NM_2 is the maximum acceptable voltage drop from V(2) for the second inverter to still receive logic '2'.

The simulation setup is shown in Fig. 14, where two ternary inverters are put in series. In the middle, there is a ramp generator which acts as a kind of noise source. The first inverter produces 0.9V for V(2), 0.45V for V(1), and 0V for V(0). Then, the ramp generator progressively adds positive or negative voltage values to the existing input voltage of the second inverter. If the incremental or decremental voltage is more than the tolerable amount, the second inverter starts to generate wrong output values. The time at which *out2* starts to diverge from its expected voltage level is mapped onto *in2* to achieve the amount of input voltage which has caused malfunction.

Simulation results for the STI presented in [16] with the original transistor sizes and the proposed transistor sizes are depicted in Figs. 15 and 16, respectively. Moreover, Table 4 shows the simulation results, which demonstrate how much the proposed systematic transistor sizing can be influential in making NM_0, NM_{1-}, NM_{1+}, and NM_2 uniform. With the proposed transistor sizes, NMs are almost uniformly distributed whereas the original design causes a considerable gap between the NM values. As a result, the proposed method improves NM by approximately 42.8% and 47.7% when they are achieved through the VTC curves and the practical simulations, respectively. Besides, the nominal NM values, measured by (2) to (5), and the experimental NM values, measured by simulation, are quite close and confirm each other's validity. (28), as shown at the bottom of the next page. Table 5 compares the NM values of the proposed design

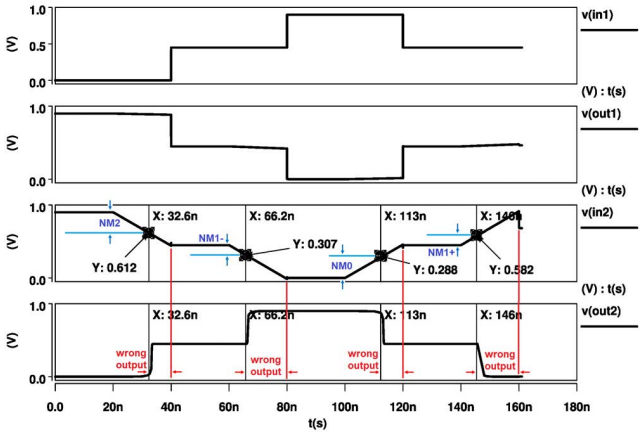

FIGURE 15. Simulation results for the STI with the original transistor sizes in [16].

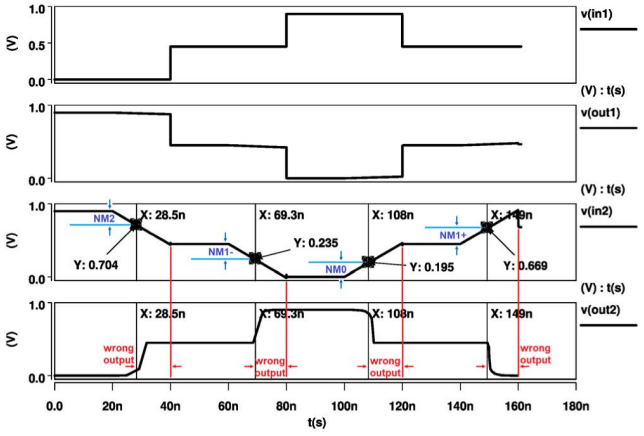

FIGURE 16. Simulation results for STI with the proposed transistor sizes.

(Fig. 12(a)) with some state-of-the-art ternary inverters. Among the competitors, STIs based on CNFET (and its integration with memristor), Graphene Nano-Ribbon Field Effect Transistor (GNRFET), and graphene barristor exist. No matter what technology is used, the closer the VTC curve is to the ideal form (Fig. 1(a)), the larger NMs with uniform distribution are. The one in [35] has completely uniform NMs. The STI with the proposed transistor sizes is the second-best design. It enhances NM by at least 25% in comparison with other designs, except [35]. In order to demonstrate the discrepancies of the NM values in a quantitative manner, the variance (S^2) of NMs are calculated by (28), where $\overline{NM}$ is the mean value of NM_0, NM_{1-}, NM_{1+}, and NM_2. After the design in [35], whose $S^2 = 0$, the proposed design with $S^2 = 133$ has the most uniform NMs.

Static Noise Margin (SNM) indicates the maximum tolerated amount of noise by which the cross-coupled inverters inside an SRAM do not flip the cell [47]. The VTC curves of the cross-inverters affect the SNM value. SRAMs with reduced SNMs do not provide sufficient reliability and stability [47], [48]. The overlapped VTCs of the cross-coupled STIs with the original and the proposed transistor sizes are plotted in Figs. 17(a) and 18(a), respectively. They are called butterfly diagrams. The same diagram for the STIs with the threshold voltages indicated in [35] is also plotted in Fig. 19(a). The four maximum nested squares/rectangles between the normal and mirrored VTCs of two STIs indicate eight SNMs (Fig. 18(a)) [37], [49], whose minimum amount

TABLE 4. Comparison of noise margin values between the STIs with original transistor sizes in [16] and proposed transistor sizes.

Designs		NM_0 (mV)	NM_{1-} (mV)	NM_{1+} (mV)	NM_2 (mV)	NM (mV)
STI with original transistor sizes in [16]	NM values achieved through VTC curve (Fig. 2(b))	290	140	140	290	140
	NM values achieved through simulation (Fig. 15)	288	143	132	288	132
STI with proposed transistor sizes	NM values achieved through VTC curve (Fig. 12(b))	200	220	220	200	200
	NM values achieved through simulation (Fig. 16)	195	215	219	196	195

TABLE 5. Comparison of noise margin values (mV) with state of the art in 0.9V power supply.

Designs	Tech.	NM_0	NM_{1-}	NM_{1+}	NM_2	S^2	NM
Proposed	CNFET	200	220	220	200	133	200
[19] 2018*§	Graphene Barristor	310	185	110	300	9222	110
[27] 2020§	GNRFET	190	160	160	190	300	160
[24] 2020§	GNRFET	290	145	150	285	6541	145
[30] 2018§	CNFET	300	125	125	300	10208	125
[25] 2020§	CNFET	305	120	150	170	6689	120
[35] 2020§	CNFET	220	220	220	220	0	220
[26] 2020†	CNFET	229	146	142	241	2787	142
[28] 2018§	CNFET + Memristor	185	165	190	160	216	160

* Power Supply = 1V
§ NM values have been extracted from the VTC curve inside the original paper and NM equations in (2) to (5).
† The same NM values in the original paper have been reported here since there is no illustration of the VTC curve inside the paper.

$$S^2 = \frac{(NM_0 - \overline{NM})^2 + (NM_{1-} - \overline{NM})^2 + (NM_{1+} - \overline{NM})^2 + (NM_2 - \overline{NM})^2}{3} \quad (28)$$

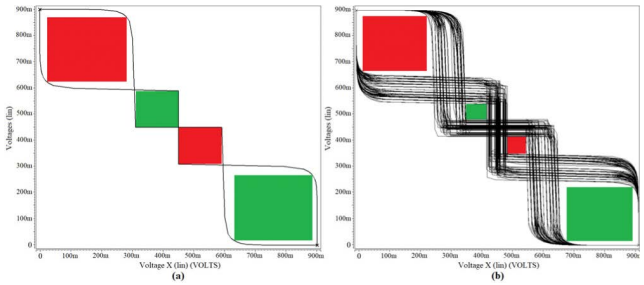

FIGURE 17. SNM for STIs with the original transistor sizes in [16], (a) Without process variation, (b) With process variation.

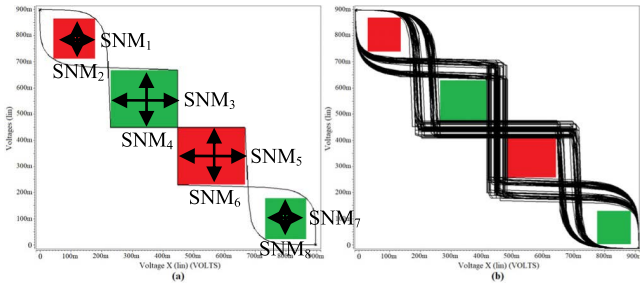

FIGURE 18. SNM for STIs with the proposed transistor sizes, (a) Without process variation, (b) With process variation.

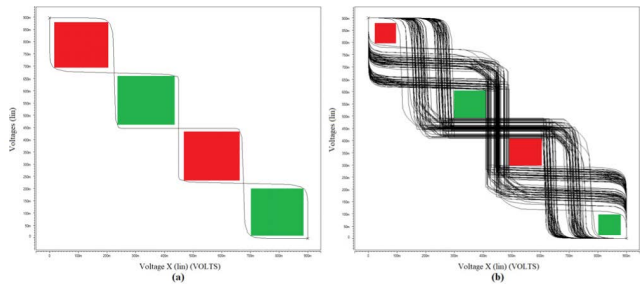

FIGURE 19. SNM for STIs with the threshold voltages in [35], (a) Without process variation, (b) With process variation.

equals SNM (29).

$$SNM = \min(SNM_1, SNM_2, \ldots, SNM_8) \tag{29}$$

In spite of its several great advantages, CNFET is still in development and suffers from imperfect fabrication [50], [51]. Some of the manufacturing issues are metallic and misaligned CNTs, chirality drift, CNT doping variations, and density fluctuations [50]. One of the most problematic issues affecting circuit design is that D_{CNT} is subject to 0.04nm to 0.2nm variations [52]. This impact on the SNM of the cross-coupled STIs is studied in this paper as well.

Process Variation (PV) analysis for our target STIs is performed by 100 Monte Carlo runs, in which the distribution of diameters is assumed to be Gaussian with 6-sigma distribution. In addition, we consider the highest expected variability for each mean diameter, i.e. 0.2nm. The butterfly diagrams with process variations are plotted in Figs. 17(b) to 19(b).

TABLE 6. Comparison of static noise margin values.

Designs	STIs with original transistor sizes in [16]		STIs with threshold voltages indicated in [35]		STIs with proposed transistor sizes	
	without PV (Fig. 17(a))	with PV (Fig. 17(b))	without PV (Fig. 19(a))	with PV (Fig. 19(b))	without PV (Fig. 18(a))	with PV (Fig. 18(b))
SNM	135mV	60mV	185mV	80mV	140mV	110mV

Table 6 shows SNM values with and without process variation. Without process variation, the STI with the proposed transistor sizes have 3.7% higher SNM than the original one [16]. It is worthwhile it to mention that if all of the corners had been sharp enough, the improvement percentage would have been more considerable. It signifies the importance of having sharp corners and steep slopes within VTC curves. Once PV is also taken into account, the proposed STI improves SNM by nearly 83.3%. In addition, since the VTC curve in [35] is almost perfectly shaped, it has the highest SNM. However, in the presence of process variation, its SNM drops dramatically because, as shown in Fig. 8, the threshold voltage variation becomes significant if smaller chiral indices are used. While [35] utilizes (8, 0), the new design employs chiral indices of (10, 0) for the same transistors. As a result, the proposed STI is less sensitive to PV, and improves SNM by 37.5%. In addition to narrow voltage zones in MVL systems, sensitivity to process variation is another reason why appropriate transistor sizing is an absolute necessity for designing ternary circuits. The obtained results show that how much uniform noise margins can alleviate the negative effects of process variation.

The diameter of a CNT is not the only parameter which is subject to fluctuation, and other physical parameters might vary in the fabrication process of CNFETs as well. The butterfly diagrams for the proposed STI in the presence of N (± 2), $Pitch$ ($\pm 10\%$), and L_{ch} ($\pm 10\%$) variations are plotted in Figs. 20(a), 20(b), and 20(c), respectively. As it is clear, the level of sensitivity to N, $Pitch$, and L_{ch} variations in comparison with the level of sensitivity to D_{CNT} variation (Fig. 18(b)) is negligible.

The proposed transistor sizing significantly improves the tolerance of the ternary inverter against noise. However, we have to mention that the presented method might on the other hand impose an adverse effect on the other circuit evaluating factors such as delay, power consumption, and area. Therefore, it is essential to study these parameters in parallel with NM measurements. All of the three STIs are simulated in a real test-bed with input buffers and output loads of fan-out of four ternary inverters (ternary FO4).

Before presenting the results, it is necessary to mention that unwanted metallic CNTs can seriously degrade NM in VLSI circuits. In their presence, inverters do not produce full rail-to-rail outputs, excessive leakage power dissipates, and Noise Margin Violation (NMV) occurs. It has been shown in [49] that 33% metallic CNTs can lead to zero SNM. Some

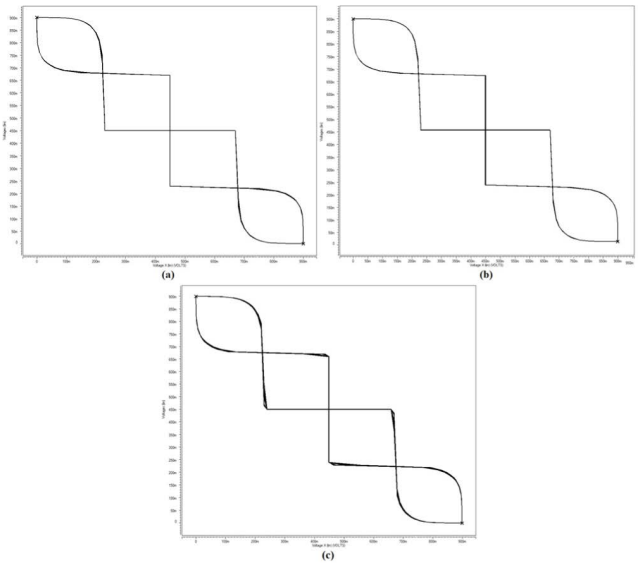

FIGURE 20. Butterfly diagrams for STIs with the proposed transistor sizes in the presence of the process variation of physical parameters, (a) N (±2), (b) Pitch (±10%), (c) L_{ch} (±10%).

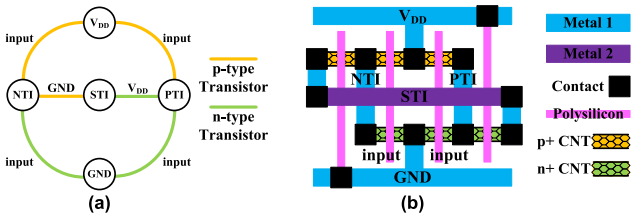

FIGURE 21. Layout schema, (a) Euler graph, (b) Stick diagram.

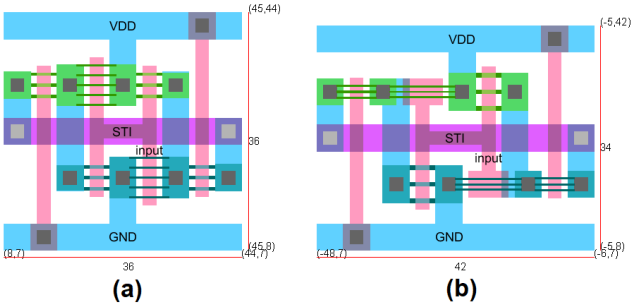

FIGURE 22. Layout, (a) STI with the original transistor sizes in [16] occupies 36λ × 36λ chip area, (b) STIs with the proposed transistor sizes and with the threshold voltages in [35] occupy 34 λ × 42λ chip area.

metallic-CNT-tolerant layout strategies have been proposed in the literature. For instance, the impact of various layout styles on the VTC curves of two cross-coupled binary inverters has been investigated in [53]. It has been shown that how a correlated layout style, where the same CNTs pass under the gate regions of both nCNFET and pCNFET in an inverter, brings about VTC symmetry and small NMV. Moreover, CNT density variation can cause noise margin and delay variations in CNFET-based circuits. For example in [54], at the cost of 7.5X area overhead, the functional yield of CNFET VLSI circuits has been improved by deploying redundant transistors in the series and parallel structures. The impact of lithographic and chemical imperfections on the CNT density variation has also been presented in [55].

The main focus of the current study is on the amount of overhead that the proposed transistor sizing imposes on area. Therefore, the focus is shifted from immunity against metallic CNTs to compactness. It is worth mentioning that, as it is illustrated in Fig. 7(b), we do not actually aim for symmetry in the VTC curves of PTI and NTI at all. In order to reach a compact layout, where n-type (p-type) transistors are placed alongside one another, the concept of Euler graph (Fig. 21(a)) is utilized in this paper. The layout views, sketched by the Electric CAD tool [56], are demonstrated in Fig. 22. Both layouts are in accordance with the stick diagram presented in Fig. 21(b). They have successfully passed Design Rule Check (DRC) and Layout Versus Schematic (LVS) checks.

Table 7 compares the ternary inverters in terms of delay, power consumption, PDP, and area. Compared to the original version, the STI with the proposed transistor sizes increases delay by only 2.297ps in the rigorous situation setup where the Unit Under Test (UUT) confronts FO4 output loads. Instead, it reduces the average power consumption by

TABLE 7. Comparison of simulation results.

Designs	STI with original transistor sizes in [16]	STI with threshold voltages in [35]	STI with proposed transistor sizes
Delay (ps)	15.593	45.128	17.890
Power (μW)	0.7960	0.7207	0.7893
PDP (aJ)	12.412	32.522	14.120
Area (μm^2)	0.3318	0.3656	0.3656

6.7nW. Furthermore, the overall area overhead equals only 10.2%. In comparison with the outstanding achievements in increasing NM values, these expenses are insignificant. Although the original ternary inverter in [16] might operate a bit faster and occupy a smaller area, its reduced NMs make the cell useless in a practical environment. Furthermore, compared to [35], the new ternary inverter operates with 60.4% higher speed and 56.6% higher performance in terms of PDP.

Eventually, the sensitivity of the ternary inverters against simultaneous voltage and temperature variations is measured. For this purpose, the circuits are simulated in three different power supplies (1V, 0.9V, and 0.8V) and at various ambient temperatures (ranged from 0°C to 100°C). The simulation results are plotted in Fig. 23. According to this analysis, the maximum PDP variation for the ternary inverters in [16] and [35] is equal to 45.1724aJ and 97.085aJ, respectively. The proposed design with the maximum PDP variation of 63.7549aJ stands in the middle.

V. LIMITATIONS OF THE STUDY

We have to mention that experimental results, in the sense of physical implementation, are certainly required to validate

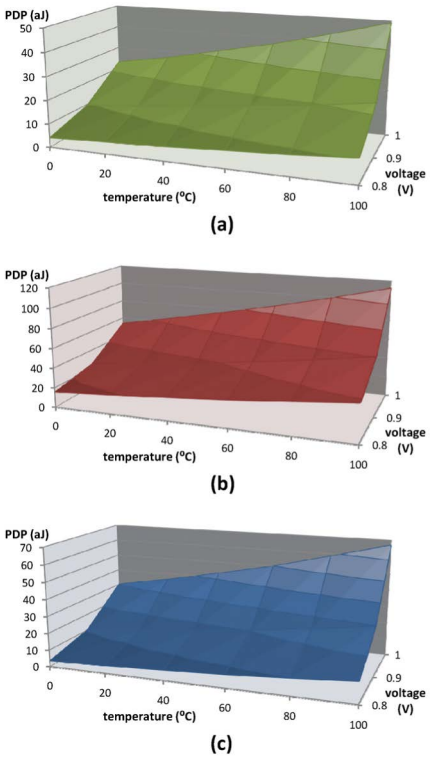

FIGURE 23. PDP versus simultaneous voltage and temperature variations, (a) STI with the original transistor sizes in [16], (b) STI with the proposed transistor sizes, (c) STI with the threshold voltages in [35].

the work. However, one of the major limitations of the current study was lack of the facilities for fabricating or building a prototype of the proposed work.

Although experimental results are not given, the CNFET model developed by the Stanford University for HSPICE simulations [43] takes all of the non-idealities such as Schottky barrier effects, carrier scattering, screen effect, transcapacitance network for intrinsic and doped CNTs, source/drain/gate parasitic resistances/capacitances, and so forth into account. Therefore, it provides high accuracy with respect to experimental results obtained from the fabricated CNFETs [44], [45]. The VTC curves and the results achieved by the HSPICE simulations in this paper confirm the usefulness of our theoretical transistor sizing procedure.

VI. CONCLUSION AND FUTURE WORKS

Transistor sizing has significant effects on the NM of ternary circuits. A systematic transistor sizing with the aim of NM enlargement has been suggested in this paper for an existing ternary inverter [16]. Unlike the VTC of a binary inverter with a single V_M, there are two V_Ms on the VTC curve of an STI. To get close to the ideal form (Fig. 1(a)), the VTC curves of NTI and PTI have shifted in such a way that V_{M1} and V_{M2} are situated on ($1/4V_{DD}$, $1/2V_{DD}$) and ($3/4V_{DD}$, $1/2V_{DD}$) points, respectively.

The acquired results are very promising. Our comprehensive investigations show that the proposed method can considerably improve the NM and SNM of the previous STI in [16]. Higher reliability comes at a price indeed. Nonetheless, the degradation of other circuit evaluating factors is insignificant. Based on our observations, we also reach the following conclusions:

1. The steepness of the VTC curve as well as the sharpness of its corners has direct influence on NMs of a ternary inverter. Further investigations into this issue and their effects on the transistor sizing procedure can be carried out in future studies.
2. Noise margin and circuit performance are equally important, and circuit designs should not sacrifice one of them for the improvement of the other one. With the main focus on performance, the ternary inverter in [16] has the lowest PDP. However, it suffers from reduced, non-uniform NMs. On the other hand, with total concentration on NM, NMs of the STI with the threshold voltages in [35] are perfectly uniform. Nevertheless, its PDP increases dramatically. In-between these two designs, the proposed STI makes an excellent compromise between NM and PDP; with 42.8% higher NM than [16], and 56.6% lower PDP than [35].
3. Amongst the physical parameters of a CNFET, variations in D_{CNT} distort the VTC curve critically. Compared to D_{CNT}, the variations of other physical parameters do not affect the VTC shape significantly.

Finally, for future works, we suggest that:

1. The proposed transistor sizing procedure (or a similar version) can be applied to other ternary inverters with different structures with the aim of improving their reliability and practicality.
2. Experimental results can be achieved to validate the work with a higher degree of certainty.
3. The impact of metallic CNTs and different layout styles on the shape of VTC curve and NM values can further be investigated.

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