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Low-Noise Resistive Bridge Sensor Analog Front-End Using Chopper-Stabilized Multipath Current Feedback Instrumentation Amplifier and Automatic Offset Cancellation Loop

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ABSTRACT Resistive bridge sensors are used in many application areas to measure changes in physical parameters. To amplify the resistive changes from sensing elements with high precision, various offset contributors in the resistive bridge and amplifiers should be minimized. This study proposes a low-noise resistive bridge sensor analog front-end (AFE) using a chopper-stabilized multipath current feedback instrumentation amplifier (CFIA) and an automatic offset cancellation loop. The proposed circuit exploits a multipath chopper-stabilized architecture for obtaining low noise performance and wide bandwidth characteristics. This circuit can minimize the offsets in the bridge and the high frequency and low frequency amplifiers, while achieving high precision resistive signal acquisition. The high frequency path of the multipath amplifier uses the CFIA topology with class-AB output stage. The offset in the high frequency path is stabilized by the low frequency path amplifier with a high gain and low noise chopper amplifier. The up-modulated offset in the low frequency chopper amplifier path is reduced by the AC-coupled ripple reduction loop (RRL). An automatic offset calibration loop (AOCL) circuit was designed to calibrate the offset due to the bridge mismatch. The AOCL reduces the bridge offset using a successive approximation register (SAR)-based binary-search algorithm. The gain of the proposed circuit is adjustable from 15.56 dB to 44.14 dB. The AFE is implemented in a 0.18 μm CMOS process and draws 123 μA current from a 3.3 V supply. The input referred noise and noise efficiency factor (NEF) are 14.6 nV/$\sqrt{}$Hz and 6.1, respectively.

INDEX TERMS Resistive analog front-end, current feedback instrumentation amplifier (CFIA), multipath amplifier, automatic offset calibration loop (AOCL).

I. INTRODUCTION

Resistive microelectromechanical system (MEMS) sensors are in the spotlight for detecting various environmental changes such as force, acceleration, pressure, and humidity owing to their advantages such as reliability and low price based on their simple structure and long-lasting durability [1]–[5]. As sensors become smaller and thinner to meet the stringent requirements of new mobile and wearable platforms, the resistive change needed to detect an amount of

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physical change is also decreased [6]. Moreover, the MEMS sensors suffer from the severe process variations, and these process variations are getting worse because the process variations are inversely proportional to the square-root of the area [7]. The output variations due to these process variations result in increased manufacturing costs. Various attempts to compensate for these errors with low cost have been reported [8]–[10].

A good solution for high-end resistive sensors is an analog front-end (AFE) circuit with high precision low noise signal acquisition, high programmability, and automatic offset cancellation capability. An instrumentation amplifier (IA) is a key building block for amplification of the small voltage input from the resistive bridge sensors [11], [12]. The implementation of IAs with low noise, high input impedance, and low power is the main focus of the recent IA research [13]. To evaluate the design tradeoffs between the noise, power, and bandwidth, the noise efficiency factor (NEF) is widely used as the figure of merit (FoM) [14]. The NEF is calculated as (1)

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \tag{1}$$

where $V_{ni.rms}V_{ni,rms}$ is input referred noise voltage from the circuit, $I_{tot}I_{tot}$ is current usage in the circuit summed from ground, and BW is bandwidth of system.

The popular topologies for implementing IA include the 3-opamp IA, the capacitively coupled IA (CCIA), and the current feedback IA (CFIA). The 3-opmap IA can achieve a high input impedance, however, the large power and area consumptions are main drawbacks. Also, the CMRR of the three-op amp IA is degraded by resistive mismatches [15]. The CCIA has better low power and low noise characteristics. In addition, it can be implemented in a relatively small area compared to the 3-opamp IA [16]. However, the input impedance is low due to the input capacitance, thus an input impedance boosting circuit with positive feedback is needed [17]. An input impedance boosting circuit based on positive feedback can increase the input impedance of the CCIA, but can damage the stability of the circuit. The CFIA is widely used in resistive bridge sensors because it can achieve a high input impedance, low noise, and low power characteristics [18], [19]. A general topology of the CFIA is shown in Fig. 1. The circuit consists of three amplifier stages, and current components from the resistors at the output are fed back to the input. The voltage V_o at the output can be described as

$$\begin{aligned} V_o &= \frac{G_{m1} \cdot G_{m3}}{1+\frac{R_1}{2R_2+R_1}G_{m2}G_{m3}} \cdot V_{DM} + \frac{\Delta G_{m1}}{1+\frac{R_1}{2R_2+R_1}G_{m2}G_{m3}} \cdot V_{CM} \\ &\cong \left(1+\frac{2R_2}{R_1}\right) \cdot V_{DM} \end{aligned} \tag{2}$$

where assuming that G_{m3} is large. The gain of the CFIA can be controlled by changing the ratio between R_1 and R_2. To obtain high gain accuracy, G_{m1} and G_{m2} should be matched, and the high open loop gain of $G_{m1} \cdot G_{m3}$ are required.

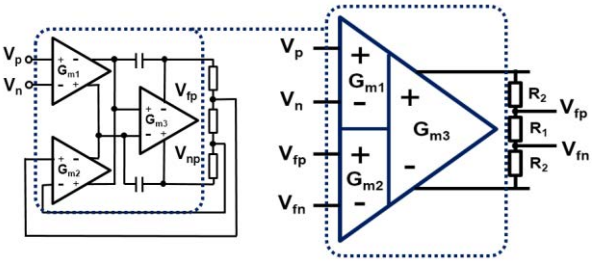

FIGURE 1. Topology of current feedback IA (CFIA).

Recently, the offset stabilized amplifier to suppress the low frequency noise including offset, 1/f noise and long-term drift have been extensively reported [20]. The offset stabilized amplifier is implemented using multipath topology. The main path (high frequency path, HFP) is generally a low-gain and wide-bandwidth amplifier. The offset of the main path is stabilized by the low noise and high gain auxiliary amplifier (low frequency path, LFP) with various dynamic offset cancellation (DOC) techniques.

The popular DOC techniques for the LFP implementation include auto zeroing (AZ) and a chopper amplifier [20]–[22]. The AZ scheme can implement a smaller circuit size; however, the thermal noise level is increased because of noise folding. In addition, the AZ operates in discrete-time and a ping-pong architecture with doubled circuit size and power is used to obtain continuous-time output [18]. The chopper amplifier is another popular DOC technique. In a chopper amplifier, the input signal is modulated to the high frequency chopper band, amplified, and demodulated to the baseband. The low frequency noise and offset of the amplifier is up-modulated by the demodulation chopper. Thus, the signal band and the noise band can be separated. In the chopper amplifier, the aliasing due to the sampling operation does not occur, and a low thermal noise level can be achieved. However, the up-modulated offsets, called ripple, should be attenuated. To attenuate the ripple, a high order low-pass filter (LPF) is required. To relax the LPF requirements, many ripple reduction loop (RRL) techniques have been reported, including the AC-coupled RRL [18], synchronous switched-capacitor notch filter [23], and auto correction feedback [24].

This paper proposes a low-noise resistive bridge sensor analog front-end (AFE) using a chopper-stabilized multipath current feedback instrumentation amplifier (CFIA) and an automatic offset cancellation loop. The block diagram of the proposed IA with offset cancellation is shown in Fig. 2 In the resistive AFE with multipath IA, the main offset sources can be categorized into three parts: the offset due to the mismatch of the resistive bridge (V_{os1}), the offset in the main high frequency path (V_{os2}), and the offset in the auxiliary low-frequency path (V_{os3}). In this design, we tried to reduce these three offsets to achieve high precision resistive signal acquisition performance. The V_{os1} is reduced by the automatic offset

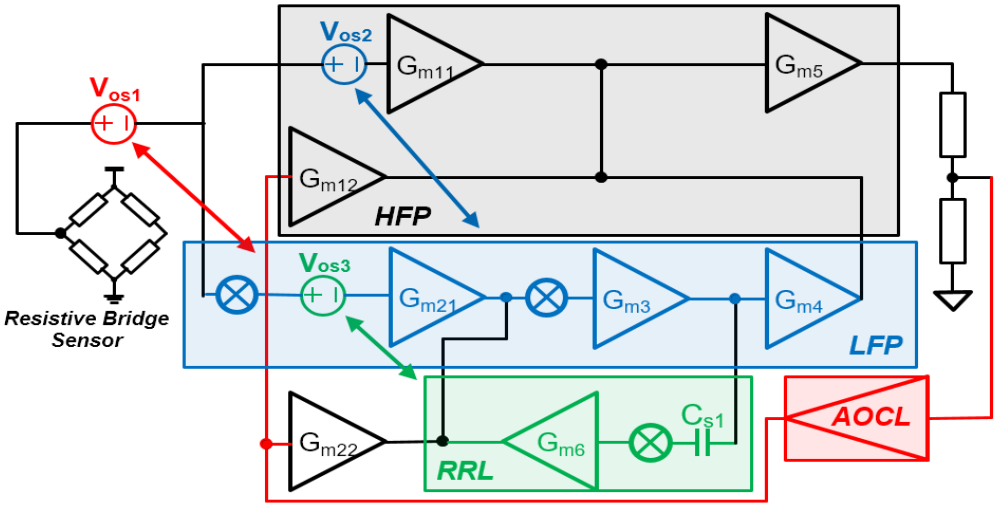

FIGURE 2. Simplified diagram of offset stabilizing multipath circuit.

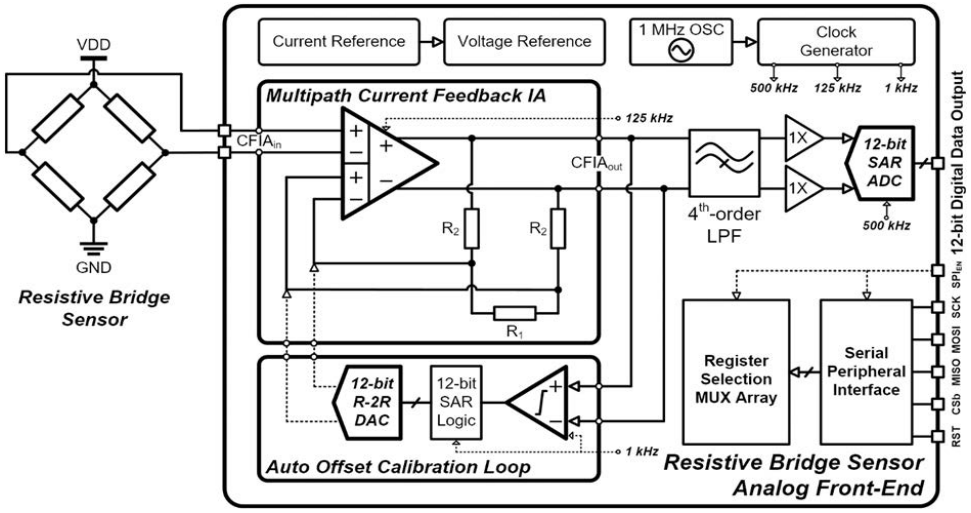

FIGURE 3. Block diagram of low-noise resistive bridge sensor AFE.

calibration loop (AOCL). The offset can arise not only from mismatching of the elements inside the CFIA circuit, but also from resistive bridge sensors. In this case, the offset needs to be calibrated outside the CFIA by AOCL block.

II. PROPOSED LOW NOISE ANALOG FRONT-END

A. OVERALL CIRCUIT DESIGN

In this work, we propose a low-power, low-noise AFE for resistive bridge sensors. Fig. 3 shows the block diagram of the proposed AFE circuit for resistive bridge sensor. The main block consists of fully differential multipath CFIA, 4th order LPF, buffer, 12-bit SAR ADC, and AOCL. The current reference, voltage reference, relaxation oscillator, clock generator, and serial peripheral interface (SPI) are fully integrated. The circuit exploits a multi-path chopper stabilized architecture for obtaining low noise performance while keeping wide bandwidth characteristics.

The proposed circuit can minimize the offsets in the bridge and in the high and low frequency amplifiers. Therefore, it can achieve high-precision resistive signal acquisition performance. For the high frequency path of the multipath amplifier, a CFIA topology with class-AB output stage is used. The offset in the high frequency path is stabilized by the high-gain low frequency path amplifier and a low noise chopper amplifier. The up-modulated offset in the low frequency chopper amplifier path is reduced by an AC-coupled RRL. To calibrate the offset due to the bridge mismatch, an automatic offset calibration loop (AOCL) circuit was designed. The AOCL can operate once when power-up, or can operate periodically. The AOCL reduces the bridge offset using successive approximation register (SAR)-based binary-search algorithm. The input voltage signal from the resistive bridge is amplified by the CFIA, and the gain of CFIA can be adjusted from 15.56dB to 44.14dB with a programmable 5-bit register.

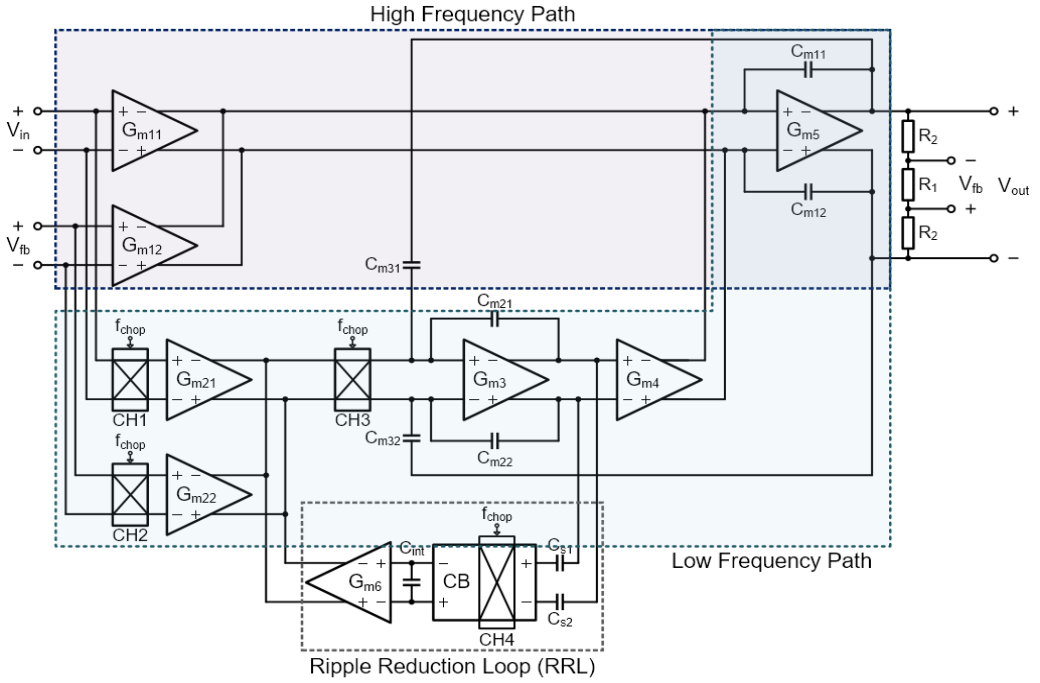

FIGURE 4. Multipath current feedback instrumentation amplifier circuit.

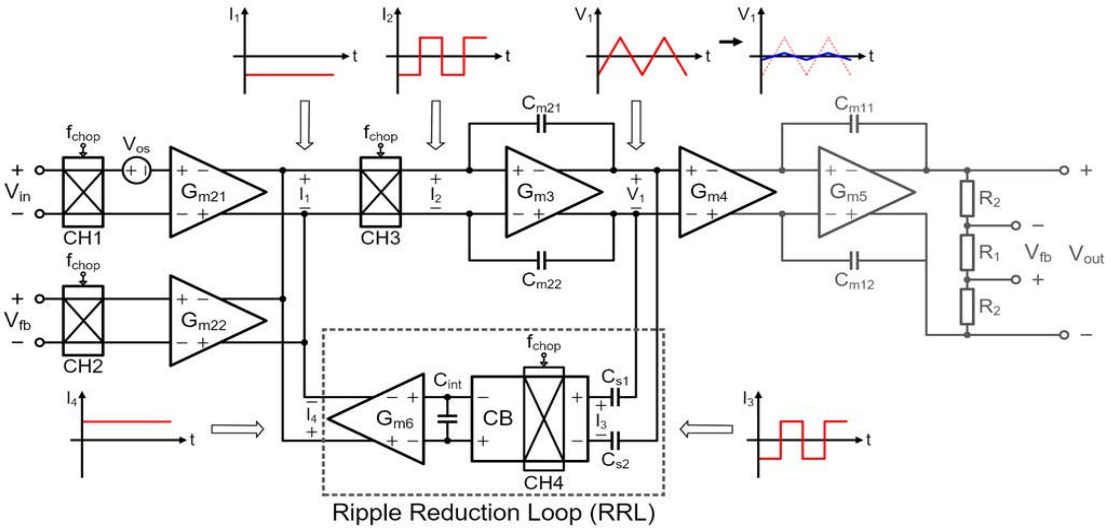

FIGURE 5. Block diagram and operating principle of LFP including RRL.

The CFIA output is band-limited by 4th-order LPF with 1 kHz cutoff-frequency and a 12-bit SAR ADC converts it into 12-bit digital values.

B. MULTIPATH CURRENT FEEDBACK IA

The multipath CFIA block diagram is shown in Fig. 4. The multipath CFIA has two main signal paths: the low frequency path (LFP) and the high frequency path (HFP). The low frequency path consists of 5 stages (G_{m21}, G_{m22}, G_{m3}, G_{m4}, and G_{m5}) and the high frequency path consists of two parallel stages (G_{m11}, G_{m12}) and a class-AB output stage (G_{m5}) that is shared with the LFP. In the LFP, the chopper technique was used to achieve low noise characteristics at low frequencies. To reduce the up-modulated ripple, a AC-coupled RRL is implemented [18]. To stabilize the offset of the HFP, the gain of the LFP should be much higher than HFP. In this design, the gain of LFP is $G_{m21} \cdot G_{m3} \cdot G_{m4} \cdot G_{m5}$, and the gain of HPF is $G_{m12} \cdot G_{m5}$.

The LFP dominates the low frequency response, the RRL acts as notch filter at chopper frequency, and the HFP dominates the high frequency band, resulting in an overall smooth frequency response. To compensate for the frequency

TABLE 1. Amplifier performances and comparisons.

Parameter	**This work**	[18] JSSC 2012	[28] ICICM 2019	[29] TCAS-I 2017	[30] JSSC 2021	[31] JSSC 2020
Technology (um)	**0.18**	0.7	0.18	0.32	0.18	0.18
Architecture	**CFIA**	CFIA	CFIA	Indirect CFIA	CFIA	Current-balanced IA
DOC Techniques	**Multipath +CH + RRL**	Multipath + CH + RRL	CH + RRL	CH + DEM*	Multipath +AZ +CH +Fill-in	CH
f_{chop} or f_{AZ} (kHz)	**125**†	30†	20†, 200†	20†	20†§	260†
Supply Voltage (V)	**3.3**	5	3.3	3.3	5	1.2
Current Consumption (μA)	**123**	143	200	170	550	21
Gain Bandwidth (Hz)	**1.92 M**	900 k	-	40 k	4.2 M	10 k
Input Referred Noise (nV/√Hz)	**15**	21	23	18	14	16
CMRR (dB)	**> 100**	137	130	> 120	-	66
PSRR (dB)	**>90**	120	-	115	124	-
Input Referred Offset (μV)	**1.0**	<2.0	5.0	2.0	0.8	-
Active Area (mm^2)	**1.28**	1.8	-	0.57	-	<0.7
NEF	**6.1**	9.6	6.1	10.6	15.4	11.8
Automatic Offset Calibration	**Yes**	No	No	No	No	No

*Dynamic element matching (DEM)
†Chopper operating frequency (f_{chop})
§Auto-zeroing operating frequency (f_{AZ})

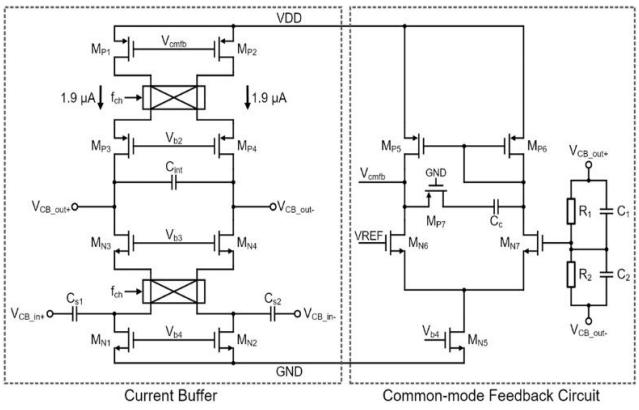

FIGURE 6. Current buffer and common-mode feedback circuit.

response, the compensation capacitors, C_{m11}, C_{m12}, C_{m21}, C_{m22}, C_{m31}, C_{m32} are added. The value of C_{m31} and C_{m32} are selected so that the overall frequency response becomes almost a first-order system. Fig. 5 depicts the LFP circuit including the RRL and the more detailed operation of the circuit. The choppers *CH1*, *CH2*, *CH3*, and *CH4* are operated with the same non-overlapping clocks of 125 kHz.

The operation of the RRL is as follows. The offset voltage, V_{os}, is converted to offset current (I_1) by G_{m21}, and up-modulated by *CH3*. The square-wave ripple current (I_2) is converted to a triangular-wave voltage (V_1) by a Miller integrator which consists of G_{m3} and C_{m21}. The high frequency components of V_1 are filtered by AC-coupling ripple sensing capacitors, C_{s1} and C_{s2}, and are demodulated into the baseband by *CH4*. The high output impedance of current buffers (CB) and C_{int} form the low pass filter, and the output current of G_{m6} (I_4) is negatively fed back to the summation node of the G_{m21} and G_{m22} outputs.

The design of CB in RRL, common-mode-feedback (CMFB), and sensing capacitors C_{s1} and C_{s2} are shown in Fig. 6. The bias current of CB is 1.9 μA. The C_{s1} and C_{s2} and input resistances of CB form high pass filters. The high-pass filtered currents from V_{CB_In+}, V_{CB_In-} are demodulated by the chopper and are buffered by common gate amplifiers, M_{N3} and M_{N4}. The output common-mode of V_{CB_OUT+}, V_{CB_OUT-} is detected through parallel resistors and capacitors, R_1, R_2, C_1, C_2. The single-stage error-amplifier forms CMFB.

Fig. 7 shows the main HFP amplifier design. The two input transconductors, G_{m11} and G_{m12} converts the input voltage signal and feedback voltage signal to output current. The G_{m4} converts the input voltage from LFP to the output current. These currents are summed by the cascode summation stage. In the current summation cascode stage, four transistors, M_{N5}, M_{N6}, M_{P17} and M_{P18} are added for class-AB biasing with the Monticelli style [25]. The output stage, G_{m5}, is in a class-AB amplifier configuration.

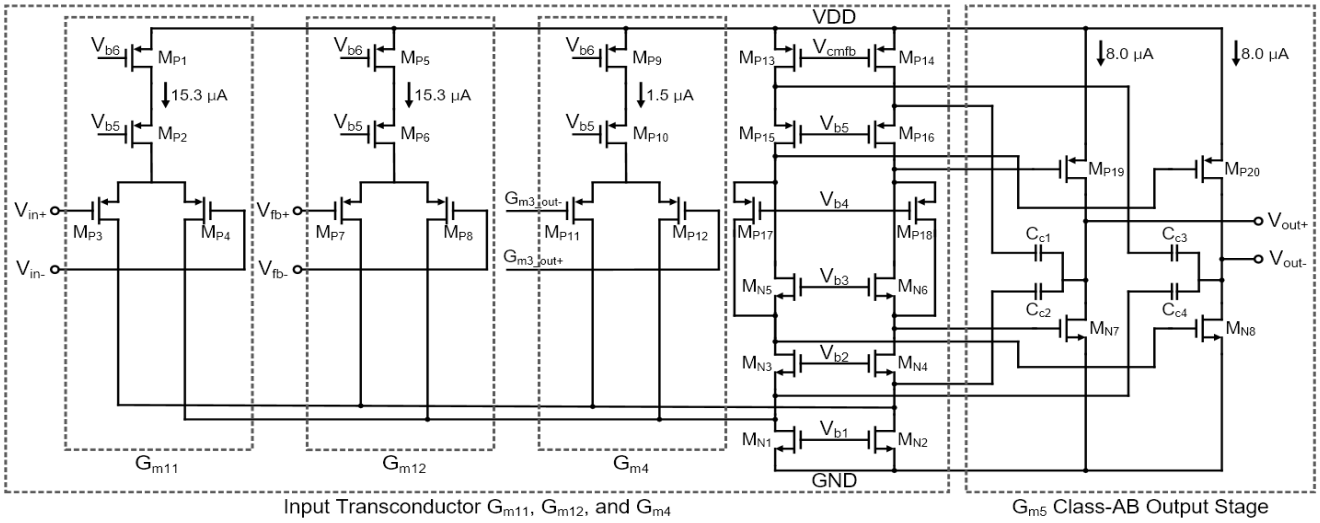

FIGURE 7. High frequency path circuit in multipath current feedback instrumentation amplifier.

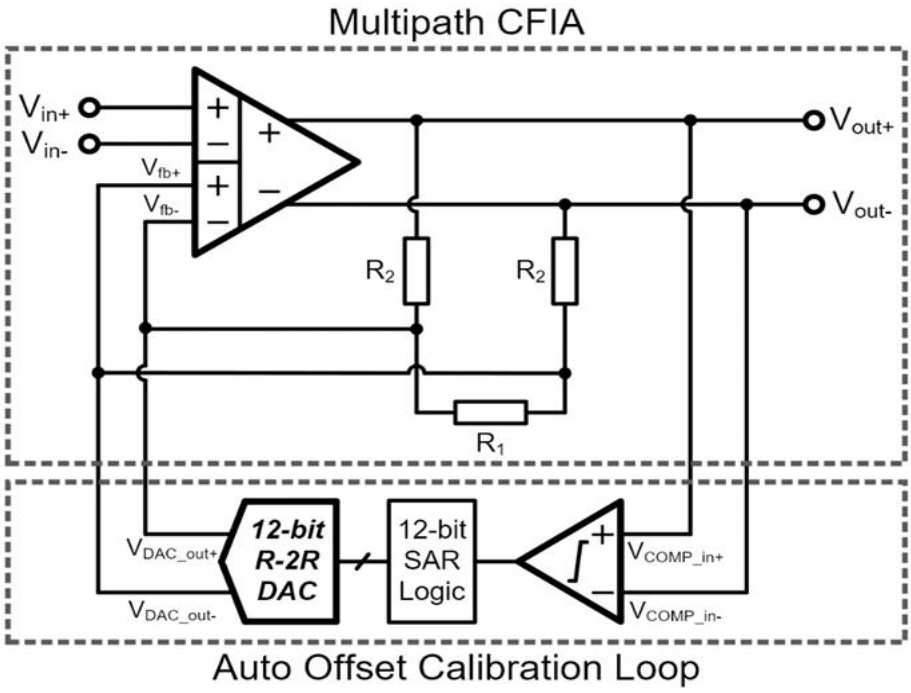

FIGURE 8. Proposed multipath CFIA and auto offset calibration loop (AOCL) circuit block diagram.

To enhance the frequency stability and the CMRR with smaller capacitances, the compensation capacitors, C_{c1}, C_{c2}, C_{c3}, and C_{c4} are placed in a nested-Miller compensation scheme.

C. AUTO OFFSET CALIBRATION LOOP

In this design, the offsets in the main HPF amplifier and auxiliary LFP amplifier are canceled by chopper stabilization and RRL techniques, respectively. However, the offset in the resistive bridge still remains. To adjust the offset in the bridge, the automatic offset calibration loop circuit (AOCL) is designed [26], as shown in Fig. 8. The AOCL includes a comparator, 12-bit SAR logic block, and 12-bit R-2R digital-to-analog converter (DAC). The AOCL can be activated for a one-time use at power-up with a zero-input condition, or it can be activated when calibration is needed. During the AOCL sequences, the amplified offset from the bridge is compared by the comparator. The 12-bit SAR logic generates the DAC control signal using a binary-search algorithm. The 12-bit digital output controls the 12-bit R-2R DAC, and the DAC generates the compensation feedback voltage. The output voltage including the compensation voltage of DAC can be

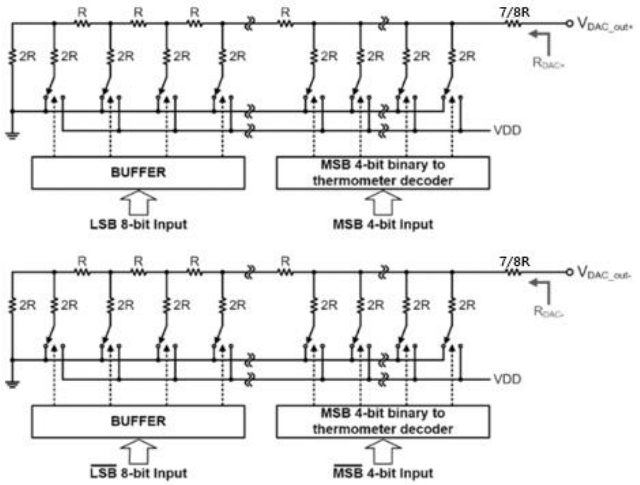

FIGURE 9. 12-bit R-2R DAC circuit in AOCL.

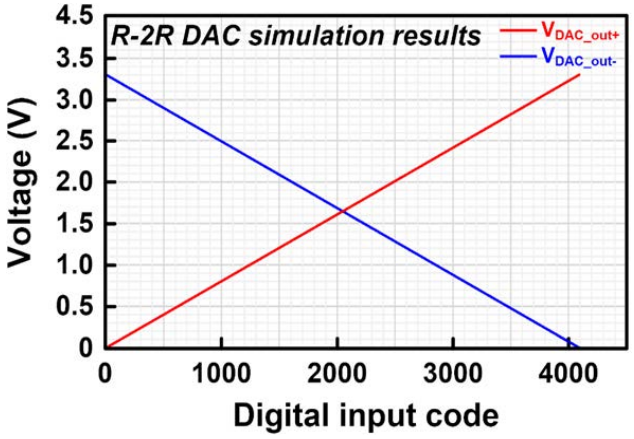

FIGURE 10. Simulation results of differential R-2R DAC.

expressed as (3).

$$V_{out+} - V_{out-} = (1 + 2 \cdot \frac{R_2}{R_1}) \cdot (V_{in+} - V_{in-}) + \frac{R_2}{R_{DAC}} \cdot ((V_{in+} - V_{in-}) - (V_{DAC_out+} - V_{DAC_out-})) \quad (3)$$

where R_1, R_2 are feedback resistors of CFIA, V_{in} is the input signal to the comparator, and V_{DAC_OUT} is the output signal of the DAC.

The implementation of the differential R-2R DAC is shown in Fig. 9. The R-2R DAC is segmented to the MSB (most significant bits) part and LSB (least significant bits) parts. The 15 resistors are selected by the thermometer code of the MSB control bits for better matching. The 16 parallel connection of *2R* generates *1/8R*. The series-connected *7/8R* makes the output resistance of the DAC to be R.

The differential DAC outputs with varying input code are shown in Fig. 10.

The two-stage comparator in AOCL is shown as Fig. 11. The comparator consists of pre-amplifier stage with NMOS latch load and positive-feedback full latch stage. The latch

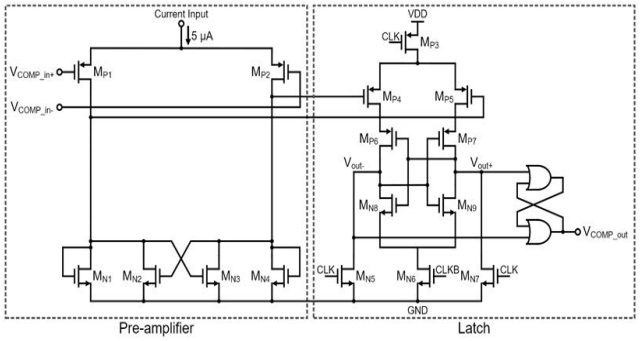

FIGURE 11. 2-stage comparator in AOCL.

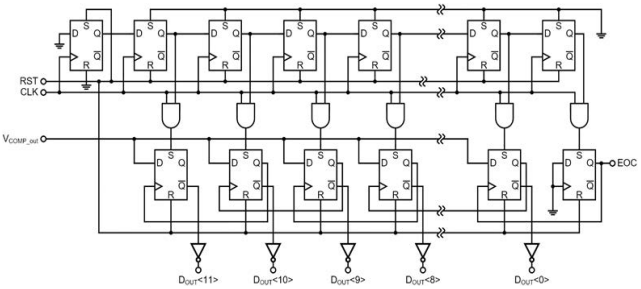

FIGURE 12. 12-Bit SAR control logic in AOCL.

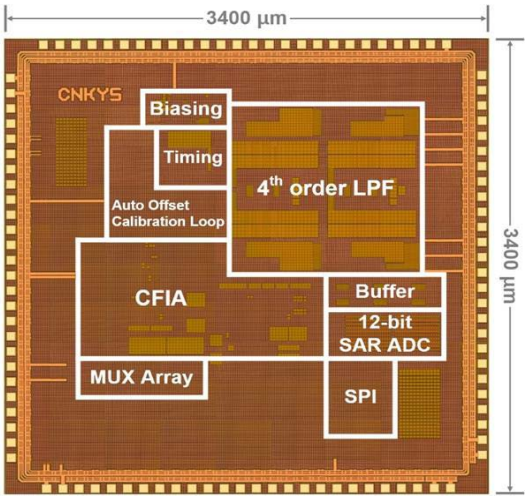

FIGURE 13. Die photograph of AFE.

stage is reset when CLK = H. The input signal of the latch stage is regenerated when CLK transits from L to H. The differential outputs of the latched stage, V_{out+} and V_{out-}, are latched using SR-latch, and generate V_{COMP_OUT}. The operating clock of the comparator is 1 kHz. Because the comparator evaluates the amplified bridge offset at the CFIA output node, in the point of the input referred noise of CFIA, the input offset of the comparator is divided by the gain of CFIA. In this design, the additional offset cancellation scheme for comparator stage is not applied.

The SAR logic is shown in Fig. 12 [27]. The SAR logic block is made up with 2-column and 14-row flip-flops. The first column flip flops operate as shift register that receives

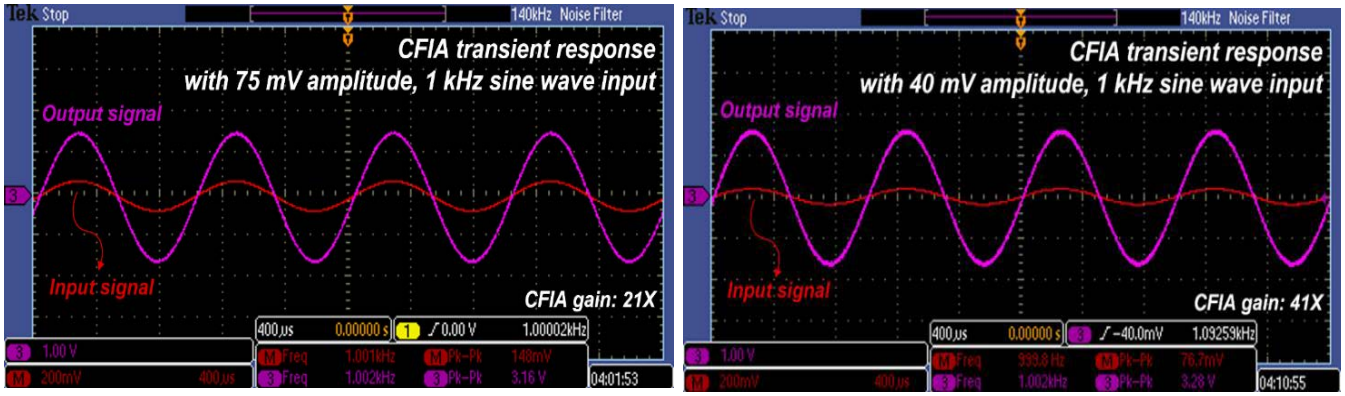

FIGURE 14. Transient response measurement result of CFIA.

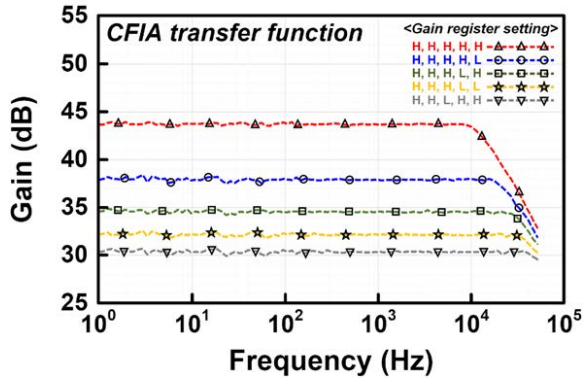

FIGURE 15. Transfer function measurement results of the CFIA.

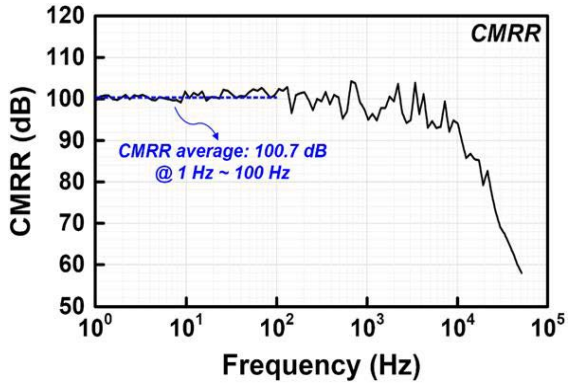

FIGURE 17. CMRR of the CFIA.

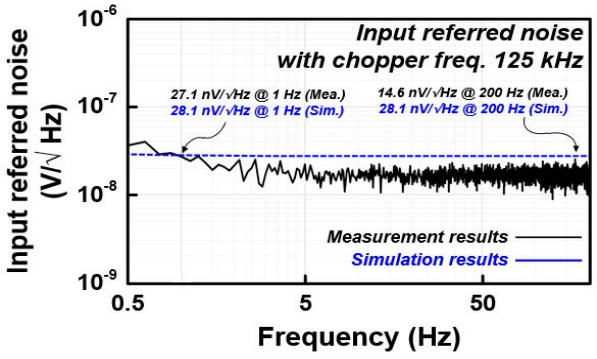

FIGURE 16. Input referred noise of the CFIA.

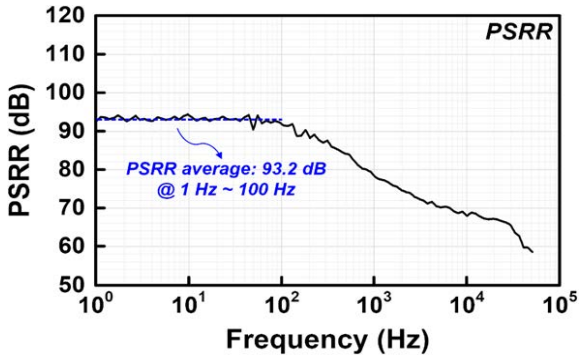

FIGURE 18. PSRR of the CFIA.

data from the comparator. The second column's flip flops store data from first column, update the comparator outputs, and generate the DAC control input.

Initially the MSB of the DAC input is set to H, and the LSBs are set to L. After the output offset is evaluated by comparator, the comparator output is updated to MSB. This operation is repeated to LSB successively. After completing the successive output of data, the end of conversion flag is set to high and the AOCL operation is finished.

III. EXPERIMENTAL RESULTS

A die photograph of the proposed low noise AFE for the resistive bridge sensor is shown Fig. 13. The circuit was implemented on a 3.4 mm $\times$ 3.4 mm die, using a 0.18 μm 1 p6m CMOS process. The active area of the circuit is 5.87 mm^2. The supply voltage and current consumption are 3.3V and 123 μA. The chopper frequency is 125 kHz.

The DC gain of the CFIA is programmable with a 5-bit register, from 15.56 dB to 44.14 dB. The gain-bandwidth product is 1.92 MHz. The time domain measurement results with 26.44 dB and 32.25 dB gain are shown in Fig. 14.

Fig. 15 shows the measured transfer function of CFIA. An input sinusoidal signal of 10mV amplitude with 1.65V DC using a dynamic signal analyzer (Agilent 35670A) was applied.

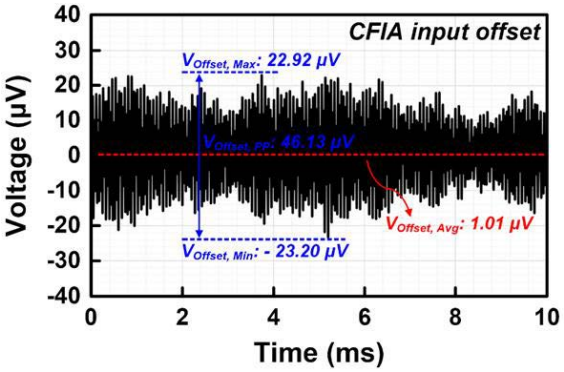

FIGURE 19. Input-referred offset voltage of the CFIA.

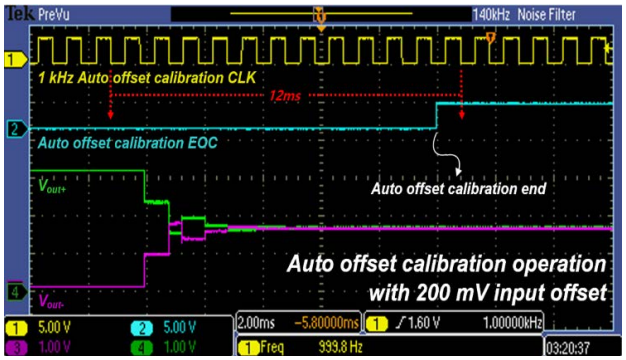

FIGURE 20. Measurement result of auto offset calibration loop process.

The measured input referred noise is shown in Fig. 16. The blue and black lines represent the simulated and measured results, respectively. The simulated and measured input referred noise are 28.1 nV/$\sqrt{}$Hz and 14.6 nV/rtHz, respectively.

The measured common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) of the chip are shown in Fig. 17 and Fig. 18, respectively. Around DC frequency (averaged from 1 Hz to 100 Hz), a high CMRR of 100.7 dB and a high PSRR of 93.2 dB are achieved. The measured input offset of the CFIA is shown in Fig. 19. The peak-to-peak input referred offset ranges from -23.20 to 22.92 μV. The averaged input referred offset is 1.01 μV.

The measured results of the AOCL operation are shown in Fig. 20. The yellow, cyan, green, and purple waveforms represent the 1 kHz AOCL clock, end-of-conversion (EOC) output of AOCL, positive output of CFIA (VOUT+), and negative output of CFIA (VOUT-), respectively.

The differential input signals with 200 mV differential offset and 1.65 V (= VDD/2) common mode were applied. After the AOCL operation, the output offset is reduced to around 1 LSB (0.8 mV = 3.3 V/4096). The calibration time for AOCL operation is 12 ms.

IV. CONCLUSION

In this study, we designed a low noise and low power AFE for resistive bridge sensors. The system consists of a multipath CFIA, 12-bit SAR ADC, 4th order LPF, buffer and SPI block. The AFE is designed as a multipath amplifying circuit based on chopper stabilization. To reduce the ripple signal from the up-modulated offset through the chopper, we exploited an RRL scheme.

The multipath configuration of the CFIA covers the notch characteristic of RRL. To calibrate the offset caused by the resistive bridge sensor, an AOCL using a binary search algorithm is utilized. The AFE operates with a 3.3V supply voltage and a chopper frequency of 125 kHz. Table 1 shows the performances of proposed scheme and existing designs. Compared to the recent state-of-the-art results, the AFE achieved a low NEF of 6.1 with low input referred noise (15 nV/$\sqrt{}$Hz) and low current consumption (123 μA). The proposed circuit can minimize the offsets in the bridge, and the high and low frequency amplifiers. The experimental performance demonstrates that this design can achieve a high precision resistive-signal acquisition performance than that of the current state-of-the-art designs.

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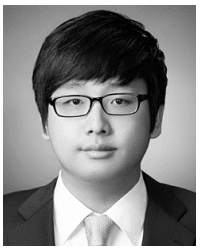

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