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Improved Circuit Design and Adaptive Burst Mode Control in PSFB Converters for Higher Efficiency Over a Wide Power Range

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ABSTRACT This paper presents an improved circuit design of Gallium Nitride (GaN) based phase shifted full bridge (PSFB) converters along with a new adaptive burst mode control strategy, to achieve high efficiency over a wide power range, including light loads. The main challenges of PSFB converters addressed in this paper are: load-dependent zero-voltage switching (ZVS), transformer saturation, and secondary side ringing. Since switching losses of GaN FETs are dominant at light loads, adaptive burst mode control can be employed to improve the efficiency at lower output power. By periodically switching output current between 0 A and minimum ZVS current, adaptive burst mode control can enable both smaller effective switching frequency and lower switching losses. A correction factor 'k' is adopted in the adaptive burst mode control's current loop PI calculation so that the output current can switch fast without any overshoot that increases switches' current stress. To verify the effectiveness of the proposed circuit and controller design, a 375 V input, 70 V output, 800 W PSIM simulation model as well as experimental prototype are developed and tested. The experimental results demonstrate the practical benefits of the proposed adaptive burst mode control.

INDEX TERMS Phase shifted full bridge (PSFB), zero-voltage switching (ZVS), burst mode control, Gallium Nitride (GaN) FETs, wide range efficiency improvement.

I. INTRODUCTION

Due to the benefits of zero-voltage switching (ZVS), phase shifted full bridge (PSFB) isolated converters are widely used in many modern industrial applications, such as renewable energy conversion [1], electric vehicle charging [2], [3], and telecommunication systems' power supply [4], [5]. PSFB converter has the benefits of wide gain range and fixed switching frequency over LLC resonant converter [6], has lower switch voltage rating compared to active clamp converter [7], and lower complexity than dual active bridge (DAB) converter [8], for unidirectional power flow.

Using fast Gallium Nitride (GaN) devices, the PSFB converter can operate at higher frequencies, which increases power density and response speed [9], [10]. However, a higher switching frequency also makes the PSFB converter's inherent drawback, load-dependent ZVS, more prominent [11]. At high switching frequencies, a smaller transformer leakage inductance is needed to reduce the duty loss issue for maintaining sufficient voltage gain, but this will lead to ZVS failure at light loads. When using GaN devices at relatively higher voltages and frequencies, since switching losses are dominant under light load operation due to the C_{oss} capacitance [12], the total light load efficiency becomes very poor under ZVS failure. Several techniques have been proposed to improve the light load efficiency of PSFB converters and they can be overall classified into two types: (i) extending the PSFB converter's ZVS range and (ii) reducing equivalent switching frequency at light loads.

Under the first classification, many auxiliary circuits have been proposed in [13]–[17], but they increase the current stress of the device and cause extra auxiliary circuit loss. Meanwhile, several topology variants are proposed to overcome PSFB's load-dependent ZVS issue, such as triple converter with shared leading legs [18], converter adopting two series-connected transformers [19], [20], and the

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combination of two different PSFB converters [21], [22]. These variants generally have limitations of application scenarios and are not widely used in consideration of system complexity and reliability.

For the second classification, burst mode control is utilized in [23], [24]. By forcing the converter to switch in a few large duty cycles by default and then skip some switching cycles, the burst mode control can effectively reduce the overall equivalent switching frequency, thereby reducing the switching losses at light loads. However, this burst mode can only be applied to very light load conditions, since the output current is not actively controlled and continuous large duty cycles may produce high peak currents, damaging the devices.

This paper proposes an adaptive burst mode control strategy that combines the benefits of the above-mentioned approaches. The proposed strategy forces the converter to periodically switch output current between 0 A and the minimum ZVS current, but at the same time, the average output current still matches with the load requirement. The equivalent switching frequency decreases due to the presence of converter disabled time slots (0 A current) and the converter maintains the minimum ZVS output current in most switching cycles. It is noteworthy that not all switching cycles can achieve ZVS due to the rising time needed by the output current. To reduce the output current rising time as much as possible, an adaptive current loop PI calculation is also adopted in this paper. It can also ensure that no current overshoot occurs during the output current transients (0 A to minimum ZVS), which helps to protect the devices from damage due to over-currents.

The main advantages of the proposed concepts can be summarized as follows:

- The proposed adaptive burst mode control strategy can extend PSFB converter's ZVS range and reduce the effective switching frequency concurrently at light load; thereby increasing the light load efficiency drastically.
- The new proposed correction factor 'k' can help adaptive burst mode controller to switch output current between 0 A and minimum ZVS current, quickly and smoothly.
- The developed methods can be extended to other types of DC-DC converters with current control as well, such as buck, boost, etc.

This paper is organized as follows. In section II, the circuits and operating principle of PSFB will be firstly described and the related reason for light load ZVS failure will be explained. Then, other practical concerns (such as transformer saturation and secondary side ringing) aggravated by GaN-based high switching frequency and their corresponding solutions are discussed. In section III, the proposed adaptive burst mode control and the internal current loop PI calculation are designed. Section IV provides the experiment results to confirm the mathematical analysis and verify the effectiveness of the proposed adaptive burst mode control. Section V will be the conclusion.

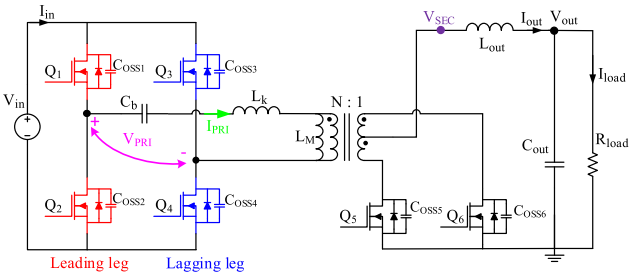


FIGURE 1. Phase shifted full bridge (PSFB) converter schematic.

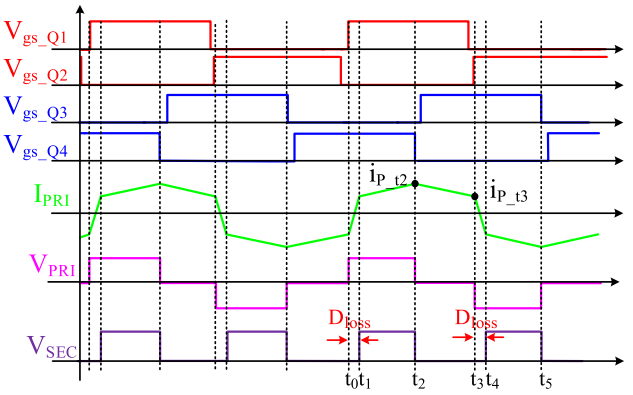


FIGURE 2. PSFB converter's main operational waveforms.

II. GaN-BASED PSFB CONVERTER DESIGN

The schematic of the PSFB converter is shown in Fig. 1. L_k is the leakage inductance of the transformer, designed to achieve an extended ZVS range; this can be a separate inductor as well if the transformer leakage inductance is not sufficient. C_b is the blocking capacitor to prevent DC current saturating the transformer. It is noteworthy that a GaN device does not have a parasitic reverse body diode, but itself can operate similar to a diode when the reverse voltage is applied [25]. This property is indicated as 'equivalent' reverse diodes in Fig. 1. C_{oss} represent FET output capacitance.

The operating principle of PSFB can be explained with the main waveforms shown in Fig. 2. Q_1 and Q_2 in the leading leg turn on alternately with fixed 50 % pulse width. The lagging leg operates the same as the leading leg, but a specific phase shift is applied between the two legs. By adjusting the phase shift value, the duty cycle of bipolar square wave V_{PRI} can be modified. After the synchronous rectification of secondary side devices Q_5 and Q_6, V_{sec} with a specific duty cycle can be applied to achieve the appropriate output voltage regulation.

A. LEAKAGE INDUCTANCE (L_k) DESIGN

Once a certain device turns off, the current stored in the inductor L_k needs to fully discharge two C_{oss} in the same leg within the deadtime, so that the other device can turn on with ZVS. For leading and lagging legs, the leakage inductor

currents at switching time can be represented as i_{P_t2} and i_{P_t3}, respectively. As shown in Fig. 2, the leading leg utilizes a smaller current to achieve ZVS ($i_{P\_t3} < i_{P\_t2}$). Therefore, L_k should meet the requirement as in (1).

$$\frac{1}{2}L_k i_{P\_t3}^2 \geq \frac{1}{2}\left(C_{oss1} + C_{oss2}\right)V_{in}^2 \tag{1}$$

After simplification,

$$L_k \geq \frac{\left(C_{oss1} + C_{oss2}\right)V_{in}^2}{i_{P\_t3}^2} \approx \frac{N^2\left(C_{oss1} + C_{oss2}\right)V_{in}^2}{i_{out}^2} \tag{2}$$

where, V_{in} is the input voltage, i_{out} is the output current and N is the transformer turns ratio. In the consideration of a wide load range, L_k should be as large as possible to meet the requirement of (2) for ZVS. However, large L_k will bring an obvious duty loss issue to the secondary side since it will take a longer time for L_k to change the current to the opposite direction as shown in $t_0 \sim t_1$ and $t_3 \sim t_4$ time slots of Fig. 2. The duty loss can be defined approximately as in (3) [7].

$$D_{loss} \approx \frac{4I_{out}L_k f_s}{N \cdot V_{in}} \tag{3}$$

where, f_s is the converter switching frequency. To obtain sufficient converter voltage gain, the maximum acceptable duty loss D_{loss} can be defined as in (4).

$$D_{loss\_max} = D_{ctrl\_max} - \frac{N \cdot V_{out}}{V_{in}} \tag{4}$$

where, D_{ctrl_max} is the maximum duty cycle that can be achieved by a practical controller, which is related to the controller's processing speed. In this paper, D_{ctrl_max} is set as 0.9 to be compatible with various performance processors. Then, by combining (3) and (4), (5) and (6) can be deduced.

$$0.9 - \frac{N \cdot V_{out}}{V_{in}} \geq \frac{4I_{out}L_k f_s}{N \cdot V_{in}} \tag{5}$$

After simplification,

$$L_k \leq \frac{N \cdot V_{in}}{4I_{out}f_s} \cdot \left(0.9 - \frac{N \cdot V_{out}}{V_{in}}\right) \tag{6}$$

Therefore, the L_k range can be identified by (2) and (6). Since GaN based PSFB converters are switching at high frequencies, the L_k range is becoming increasingly smaller, limited by (2) and (6). Even if there are multiple L_k values possible, there will still be a trade-off on choosing relatively larger or smaller L_k, in which a smaller L_k value leads to a narrower ZVS load range and a larger L_k value results in more inductor AC core losses. In this paper, a relatively smaller L_k value is preferred, and an adaptive burst mode control is employed to increase the efficiency for the overall load range.

B. BLOCKING CAPACITOR (C_b) DESIGN

The simplified PSFB convert circuit and the corresponding AC signal model are shown in Fig. 3. If switches are ideally the same, the bipolar square wave V_{PRI} will be symmetrical and there will not be any DC component. However, in practice, the on/off time of every switch can be different due to

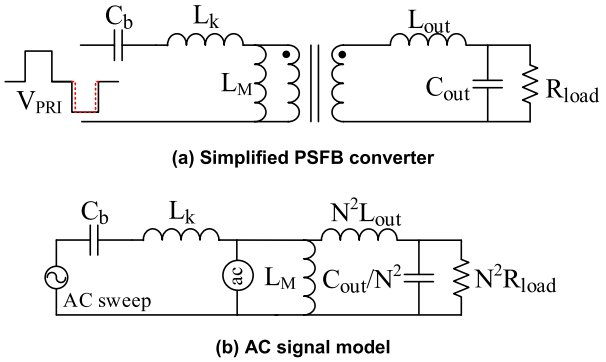


FIGURE 3. Simplified PSFB converter circuit with AC signal model.

the mismatch of the gate driver, gate resistance, and switch input capacitance. Thus, the waveform may be asymmetrical as shown in Fig. 3 (a), with a minor DC component that can saturate the transformer over time. This saturation issue is more serious in GaN-based PSFB converter due to its higher switching frequency. Therefore, a blocking capacitor C_b is added in series with the transformer to form a high pass filter that can block the DC components.

Based on Fig. 3 (b), the transfer function from V_{PRI} to the transformer can be represented as (7).

$$H(s) = \frac{sL_M \| Z_{SEC}}{\frac{1}{sC_b} + sL_k + sL_M \| Z_{SEC}} \tag{7}$$

where, Z_{SEC} is the secondary side impedance and can be defined as (8).

$$Z_{SEC} = sN^2L_{out} + \frac{\frac{N^2}{sC_{out}} \cdot N^2R_{load}}{\frac{N^2}{sC_{out}} + N^2R_{load}} \tag{8}$$

Then, it can be approximately simplified as (9).

$$Z_{SEC} = sN^2L_{out} + \frac{N^2}{sC_{out}} \tag{9}$$

After substituting (9) into (7) and simplifying (7) by ignoring a 'large' L_M, the transfer function can be approximated as (10).

$$\begin{aligned} H(s) &= \frac{sN^2L_{out} + \frac{N^2}{sC_{out}}}{\frac{1}{sC_b} + sL_k + sN^2L_{out} + \frac{N^2}{sC_{out}}} \\ &= \frac{s^2N^2L_{out}C_bC_{out} + N^2C_b}{N^2C_b + C_{out} + s^2\left(L_k + N^2L_{out}\right)C_bC_{out}} \\ &= \frac{N^2C_b}{N^2C_b + C_{out}} \cdot \frac{1 + s^2L_{out}C_{out}}{1 + \frac{s^2\left(L_k + N^2L_{out}\right)C_bC_{out}}{N^2C_b + C_{out}}} \end{aligned} \tag{10}$$

Based on (10), the high pass filter can be represented as (11).

$$\begin{cases} H(0) = \dfrac{N^2C_b}{N^2C_b + C_{out}} \\ f_{zero} = \pm\dfrac{1}{2\pi\sqrt{L_{out}C_{out}}} \\ f_{pole} = \pm\dfrac{1}{2\pi}\sqrt{\dfrac{N^2C_b + C_{out}}{\left(L_k + N^2L_{out}\right)C_bC_{out}}} \end{cases} \tag{11}$$

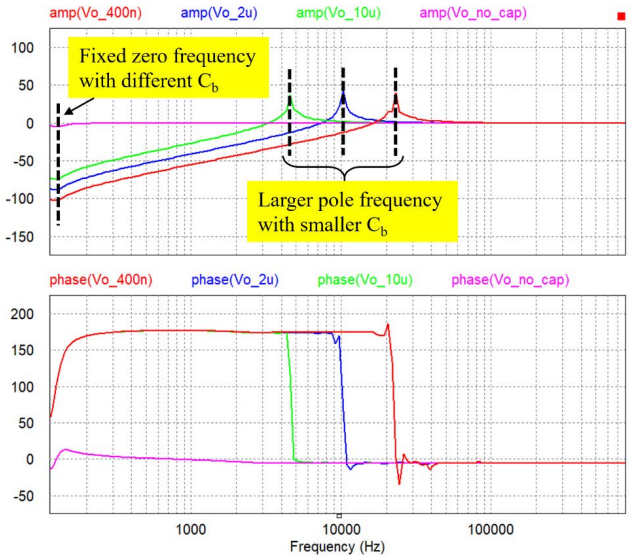


FIGURE 4. AC sweep results with different C_b (red- C_b = 400nF, Blue-C_b = 2 μF, Green-C_b = 10 μF and Pink-C_b = 0 μF) from simulation.

Thus, to achieve enough attenuation for the DC component, C_b should be as small as possible. However, small C_b will simplify f_{pole} as in (12).

$$f_{pole} = \pm\frac{1}{2\pi}\sqrt{\frac{1}{\left(L_k + N^2 L_{out}\right) C_b}} \tag{12}$$

Based on (12), it can be concluded that too small a value for C_b will increase pole frequency. When this value gets close to the switching frequency, it will distort the normal V_{PRI} signal. Therefore, C_b should be designed such that pole frequency is $1/5^{th}$ of switching frequency to avoid V_{PRI} distortion.

The AC sweep results with different C_b values shown in Fig. 4 verifies the effectiveness of (11) and (12) as frequency of the 'zero' remains the same with different C_b values. Smaller values of C_b lead to lower DC attenuation but lead to higher pole frequencies.

C. CLAMPING CIRCUIT DESIGN FOR REDUCED RINGING

In PSFB converters, it is common to observe high frequency ringing and peak overshoot across the switching devices. However, the ringing issue becomes worse in GaN FET-based PSFB converters due to the devices' small C_{oss} and fast di/dt. As shown in Fig. 5, when Q_6 turns off, the sudden voltage step change across the drain-source of Q_6 (V_{ds_Q6}) causes the leakage inductance 'L_k/N^2' to resonate with C_{oss6}, which causes ringing/overshoots at the drain of Q_6 (V_{d_Q6}). This will also appear on V_{d_Q5} when Q_5 turns off. The ringing frequency and overvoltage peak can be given by (13) and (14) [8].

$$f_{ringing} = \frac{1}{2\pi\sqrt{\frac{L_k C_{oss}}{N^2}}} \tag{13}$$

$$V_{ov} = \frac{L_k}{N^2}\cdot\frac{di}{dt} \tag{14}$$

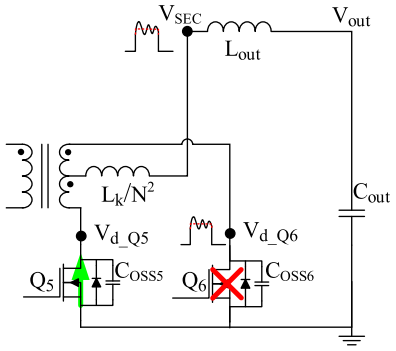


FIGURE 5. The ringing equivalent circuit referred to the secondary side.

It can be noticed that compared to Si devices, GaN devices have smaller C_{oss} and faster di/dt, which lead to more frequent ringing and higher over-voltage peaks. To reduce this ringing, a diode clamping circuit is adopted as shown in Fig. 6. The ringing starts at the drain voltages of Q_5 and Q_6 and can be reflected to the primary side by the transformer. Thus, introducing D_1 and D_2 shown in Fig. 6 to clamp the voltage V_T, can reduce the ringing issue. Its performance is shown in Fig. 7 (b) based on the simulation of a 375 V input, 70 V output GaN-based PSFB converter. Operating waveforms without clamping circuits are also included in Fig. 7 (a) as a reference.

Based on the waveforms shown in Fig. 7 (b), it can be noticed that diodes D_1 and D_2 can clamp the voltage after the external leakage inductor L_{ke}. However, the transformer's integrated leakage inductance L_{ki} still causes minor ringing, which requires the secondary side devices to have reasonable headroom for their voltage ratings. Since the ringing energy is transferred back to the input source, the power loss here is primarily due to the conduction loss of D_1 and D_2, which are also presented as I(D1)∗V(D1) and I(D2)∗V(D2) in Fig. 7 (b).

RCD clamping methods to directly clamp the voltage on the secondary side were proposed in [26]. In this research, this technique was explored analytically and via simulations. However, since it needs a resistor to release the absorbed ringing energy, it caused more power loss. Since Tagore Technology's 650 V GaN devices were adopted on the secondary side as well (due to their integrated gate drivers), there was enough headroom for the voltage and hence the more efficient method (only the clamping diodes) was chosen. It was also experimentally verified that the ringing does not affect the noise performance of the RF system.

III. ADAPTIVE BURST MODE DESIGN

The GaN FET devices' switching losses become an increasingly dominant part of the total power loss when the load decreases from 100 % to 0 %. However, based on the analysis in section II (part A), it can be seen that L_k can only achieve ZVS when the load is higher than a certain value, say 50 %, which causes increasingly poor efficiency at lower power. The main principle of a traditional burst mode control is to

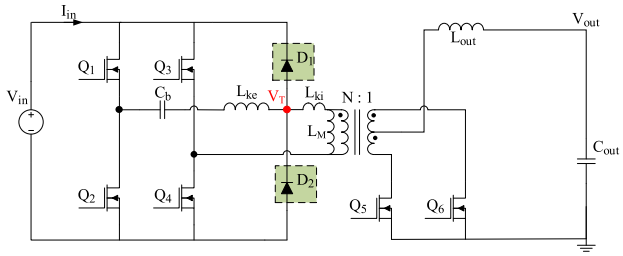


FIGURE 6. Diode clamping circuits for reducing the ringing issue.

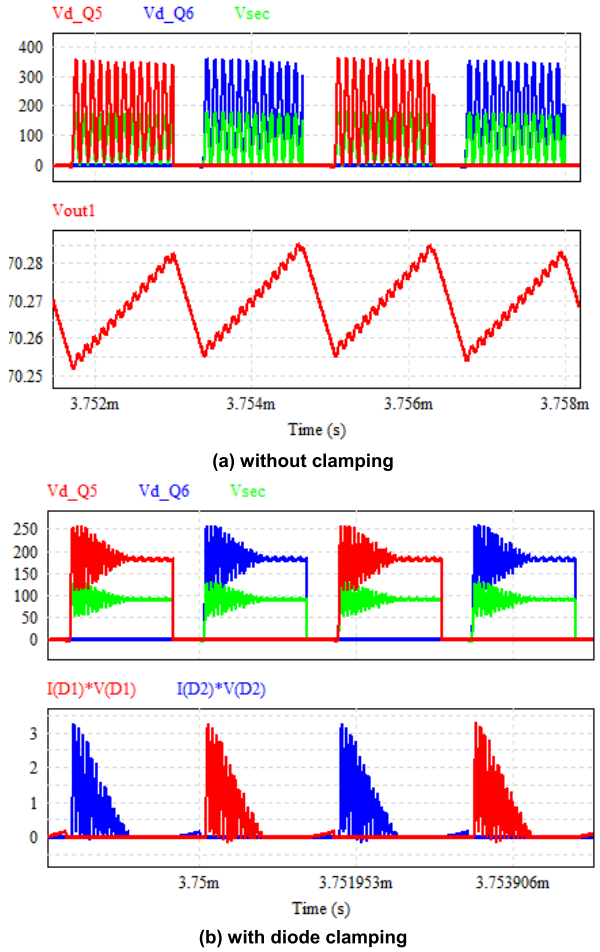


FIGURE 7. Secondary side main operating waveforms with and without diode clamping from simulation.

make the converter operate in a larger than desired duty cycle during the first N switching cycles and skip the next M-N (M>N) cycles, so that the average output current over M cycles still matches with the load requirement. Therefore, switching loss can reduce to N/M. But this technique can only be applied at no load or very light load (typically 0 % to 20 % load [24]), otherwise, its uncontrolled default duty ratio will cause over-currents that can damage the devices. An adaptive burst mode control is designed in this section to overcome this issue, so that burst mode can operate in a wider load range.

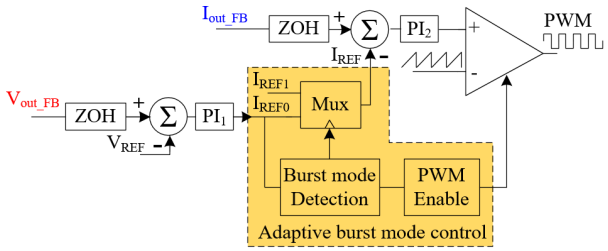


FIGURE 8. Adaptive burst mode control loop.

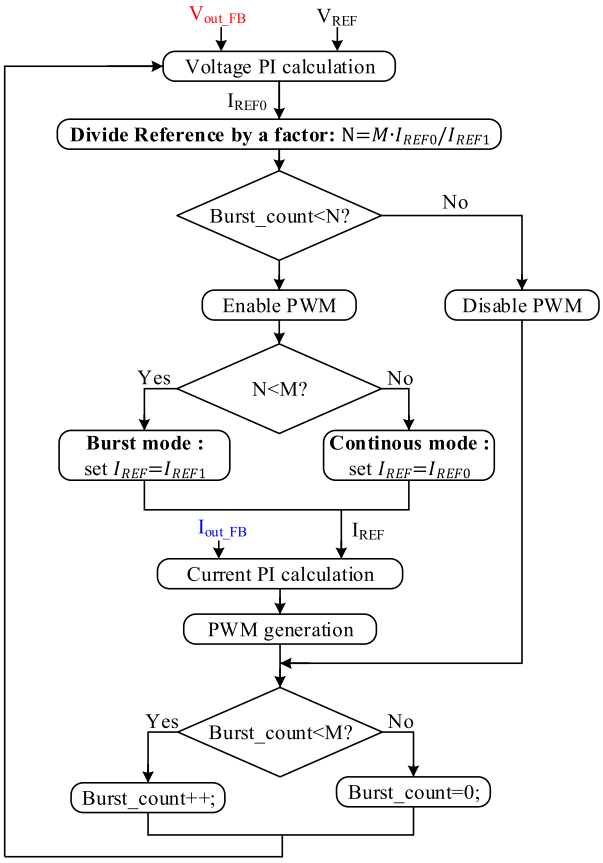


FIGURE 9. Controller flowchart of adaptive burst mode control loop.

A. CONTROL LOOP DESIGN

The proposed adaptive burst mode control diagram and its detailed flowchart are shown in Fig. 8 and Fig. 9, respectively. V_{out_FB} and I_{out_FB} are the feedback from output voltage and current, respectively. ZOH blocks represent the zero-order holds inside the microcontroller for sampling the feedback signals. The ZOH blocks are set at converter's switching frequency, so that the PI values can be calculated and PWM signals can be updated in every switching cycle. *Burst_count* in Fig. 9 is a counter to indicate which number of the cycle is the current cycle in the single burst mode period.

At the beginning of each cycle, based on the error between V_{out_FB} and voltage reference, V_{REF}, the outer voltage loop produces a current reference, I_{REF0} that indicates the real

required output current. Then, N (the number of PWM enable cycles in a single burst mode period), is calculated by (15)

$$N \cdot I_{REF1} = M \cdot I_{REF0} \tag{15}$$

where, M is the total number of the cycles in a single burst mode period and I_{REF1} is the minimum current reference that can achieve ZVS.

If I_{REF0} is larger than I_{REF1}, N will be larger than M. Then *Burst_count* will always be smaller than N since *Burst_count* is smaller than M. Therefore, the controller will operate in continuous mode and the inner current loop will modify the PWM signal to control the output current to follow the current reference, I_{REF0}. If I_{REF0} is less than I_{REF1}, N will be less than M. Then, for the first N cycles, burst mode will be active and will force the inner current loop to control the output current as I_{REF1} indicates. During the rest of the *'M-N'* cycles, the current loop PI calculation will be skipped, PWM will be disabled, and the converter will stop switching.

Since I_{REF0} is updated by voltage PI every cycle, the burst mode controller can adaptively calculate the N value such that the average output current of the whole burst mode period (M cycles) can match with the real load current.

Since the converter switches for only N cycles in every M cycles, the switching loss is reduced. Besides, these N cycles are under current control with the reference I_{REF1}, so that ZVS can be achieved, and the overcurrent issue can be avoided.

B. ADAPTIVE CURRENT LOOP PI CALCULATION DESIGN

In adaptive burst mode control, the current loop's PI calculation is directly responsible for the control of output current. Since the current reference always has a step change at the beginning of every burst mode period, an adaptive current loop PI calculation is proposed to optimize the step response of the corresponding PI calculation.

The conventional current loop's PI calculation and output current waveform are shown in Fig. 10 (a). The current reference I_{REF} can be defined as in (16).

$$I_{REF} = \begin{cases} I_{REF1}, & 0 < t \le N \cdot T_S \\ 0, & N \cdot T_s < t \le M \cdot T_S \end{cases} \tag{16}$$

where, I_{REF1} is the minimum current reference to ensure ZVS and T_S is the converter switching period. It needs to be mentioned that output current frequency is the double of the converter switching frequency in the PSFB converters.

When the converter starts working in the burst mode, current reference I_{REF} will have a step change at the beginning of the burst mode period, t_0. Then, the conventional current PI controller needs the $t_0 \sim t_1$ time slot to increase output current to the minimum ZVS current that I_{REF1} indicates, which results in hard switching at $t_0 \sim t_1$. After t_2, the PI value is reset to 0 and the same calculation repeats from t_3 to t_5. This method loses a lot of ZVS benefits as shown in $t_0 \sim t_1$ and $t_3 \sim t_4$ time slots and increases the N value due to the long start-up time of conventional PI calculation. The conventional current loop PI calculation can be represented as in (17) and (18).

$$PI_2(t) = k_P \cdot error(t) + k_I \cdot \int_{t_0}^{t} error(t) \cdot dt \tag{17}$$

$$error(t) = I_{REF}(t) - I_{out\_FB}(t) \tag{18}$$

where the k_P is the proportional gain and k_I is the integral gain. Based on (17), it can be noticed that the integration calculation depends on the accumulation of transient error, which causes a long start-up time because the integration value is relatively small at the very beginning, around t_0.

To reduce the start-up time of conventional PI calculation, the integration value at the previous burst mode period can be added to the beginning of the next burst mode period, which can shorten the accumulation time of the transient error. Meanwhile, since the current PI output is stable from t_1 to t_2 as shown in the first burst mode period in Fig. 10 (a), the error between I_{REF} and output current feedback I_{out_FB} can be assumed to be infinitesimally close to 0 during the stable state. Here, the current loop PI can be represented as in (19).

$$PI_2(t) = k_I \cdot \int_{t_0}^{t} error(t) \cdot dt, \quad t_1 < t \le t_2 \tag{19}$$

where, the integration of error(t) is equivalent to A_{S1} (area of S1, same naming method for A_{S2} and A_{S3}), shown in Fig. 10 (a). Thus, (19) can be simplified to (20).

$$PI_2(t) = k_I \cdot A_{S1}, \quad t_1 < t \le t_2 \tag{20}$$

By adding the integration value at t_2 to the second burst mode period, the fast current loop PI calculation as shown in Fig. 10 (b) can be represented by (21).

$$PI_2(t) = k_P \cdot error(t) + k_I \cdot \left[A_{S1} + \int_{t_3}^{t} error(t) \cdot dt \right] \tag{21}$$

A_{S1} in (21) helps current PI to output a higher value, which produces a larger duty cycle after the PWM generator and causes the output current to increase faster than it was in the first burst mode period. When the output current increases to I_{REF1} at t_{4a}, the current PI output is given by (22).

$$PI_2(t_{4a}) = k_P \cdot 0 + k_I \cdot \left[A_{S1} + \int_{t_3}^{t_{4a}} error(t) \cdot dt \right] \tag{22}$$

where, $\int_{t_3}^{t_{4a}} error(t) \cdot dt$ can be equivalent to the area of S2. Thus, (22) can be simplified to (23).

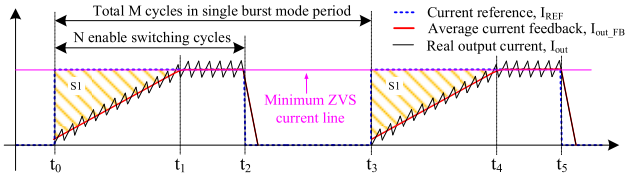
$$PI_2(t_{4a}) = k_I \cdot (A_{S1} + A_{S2}) \tag{23}$$

However, based on (20), the stable state current PI output should be $k_I \cdot A_{S1}$. Therefore, the current overshoot will appear from t_{4a}. When the current recovers to I_{REF1} at t_{4b}, the current PI output can be given by (24).

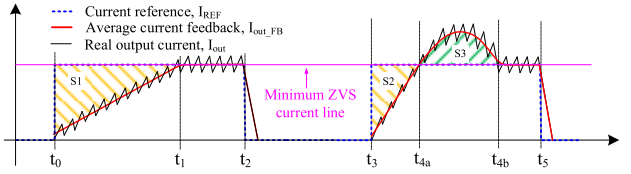
$$PI_2(t_{4b}) = k_I \cdot \left[A_{S1} + A_{S2} + \int_{t_{4a}}^{t_{4b}} error(t) \cdot dt \right] \tag{24}$$

Since error(t) is negative at the $t_{4a} \sim t_{4b}$ slot, $\int_{t_{4a}}^{t_{4b}} error(t) \cdot dt$ is equivalent to $-A_{S3}$. Thus, (24) can be simplified to (25).

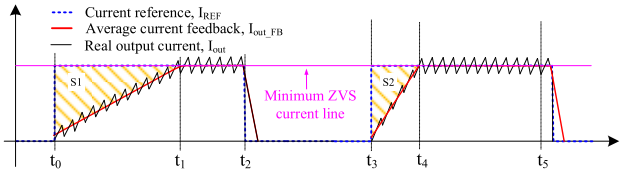
$$PI_2(t_{4b}) = k_I \cdot (A_{S1} + A_{S2} - A_{S3}) \tag{25}$$



(a) Conventional current loop PI calculation (slow output current increasing)



(b) Fast current loop PI calculation (fast output current increasing but inherent current overshoot S3)



(c) Adaptive current loop PI calculation (fast output current increasing and no inherent current overshoot)

FIGURE 10. Ideal output current waveforms of different current loop PI calculations.

To avoid further under/overshoot, $PI_2(t_{4b})$ should be equal to the stable state current PI output as in (26).

$$k_I \cdot A_{S1} = PI_2(t_{4b}) = k_I \cdot (A_{S1} + A_{S2} - A_{S3}) \tag{26}$$

Therefore, A_{S2} should be equal to A_{S3}, which means that the amplitude of overshoot depends on the area of S2. If the current overshoot is too large, the GaN device can get damaged due to thermal failure. Thus, A_{S2} should be as small as possible. The minimum A_{S2} can be approximated as in (27).

$$A_{S2} = \frac{1}{2} \cdot I_{REF1} \cdot (t_{4a} - t_3)_{min} \tag{27}$$

where, t_{4a}-t_3 is calculated by (28).

$$\begin{aligned} t_{4a} - t_3 &= \frac{I_{REF1}}{D\frac{V_{in}}{N \cdot L_{out}} - (1-D)\frac{V_{out}}{L_{out}}} \\ &= \frac{I_{REF1}}{D\left(\frac{V_{in}+N \cdot V_{out}}{N \cdot L_{out}}\right) - \frac{V_{out}}{L_{out}}} \end{aligned} \tag{28}$$

Since input voltage V_{in}, transformer turns ratio N, output inductor L_{out}, and output voltage V_{out} are fixed by converter specifications, only increasing duty cycle D can reduce A_{S2}. In consideration of duty loss from the primary side to the secondary side and practical application in digital control, maximum duty cycle (*less than 0.9*, which is based on the discussion in section II, part A) may not sufficiently reduce t_{4a}-t_3 for certain converter specifications. Therefore, the fast

TABLE 1. Experimental protype – specifications and parameters.

Parameters	Values
Input voltage, V_{in}	375 V
Output voltage, V_{out}	70 V
Output current, I_{out}	0 ~ 12 A
Switching frequency, f_s	300 kHz
Blocking capacitor, C_b	2 µF
External Leakage inductor, L_{ke}	3.3 µH
Output inductor, L_{out}	10 µH
Output capacitor, C_{out}	4*68 µF
Primary side GaN devices' output capacitor, C_{oss}	30 pF
Turns ratio of the transformer, N:1	4:1
Magnetic inductor of the transformer, L_M	245 µH
Internal leakage inductor of the transformer, L_{ki}	0.8 µH
Total number of switching cycles in single burst mode period, M	15
Minimum current reference to achieve ZVS, I_{REF1}	7.5 A
Correction factor of adaptive current loop PI calculation, k	0.86
Clamping diodes part number	CSD01060E-TR
Microcontroller part number	dsPIC33CH128MP208

PI calculation cannot be generally applied to different specifications, without making certain further improvements.

The root cause of failure of fast PI calculation is that it adds total A_{S2} to the next period's integration calculation, which makes overshoot area 'S3' inevitable. A correction factor k is adopted in the adaptive current loop PI calculation as shown in Fig. 10 (c). k is multiplied to A_{S2} before it is added to the integration calculation in the second period. Then, (23) in fast PI calculation can be changed to (29).

$$PI_2(t_4) = k_I \cdot (k \cdot A_{S1} + A_{S2}) \tag{29}$$

To avoid any overshoot, $PI_2(t_4)$ should be equal to stable state current PI's output value, which is given by (30).

$$k_I \cdot A_{S1} = PI_2(t_4) = k_I \cdot (k \cdot A_{S1} + A_{S2}) \tag{30}$$

Since there is 0 error at the stable state, (31) will be true.

$$k_I \cdot A_{S1} = I_{REF1} \tag{31}$$

Then, by combining (27), (28), (30), and (31), k can be identified as in (32).

$$k = 1 - \frac{1}{2} \cdot \frac{I_{REF1} \cdot k_I}{D\left(\frac{V_{in}+N \cdot V_{out}}{N \cdot L_{out}}\right) - \frac{V_{out}}{L_{out}}} \tag{32}$$

Fig. 11 shows the output current results of different current loop PI calculations, where $k = 0$ is equivalent to conventional PI calculation and $k = 1$ is equivalent to fast PI calculation. The $k = 0.86$ in the adaptive current loop PI calculation is deduced from (32).

It can be further noticed that conventional PI calculation responds too slowly to the current reference step change. When M is small enough, output current cannot even rise to the minimum ZVS current in a single burst mode control period. (M is chosen based on the condition that f_s/M is >20 kHz to avoid audile noise). Regardless of the type of

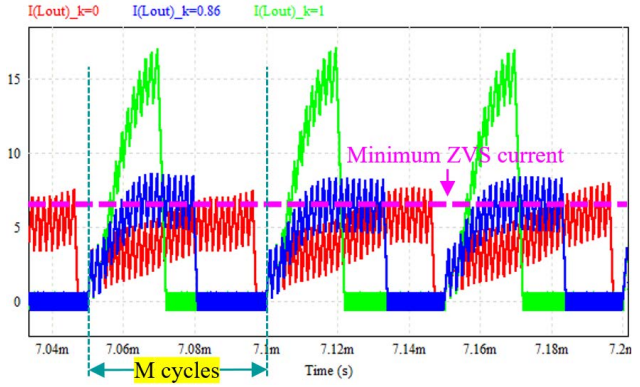


FIGURE 11. Simulation results comparison of different current loop PI calculations. (k=0: conventional PI calculation; k=1: fast PI calculation; k=0.86: adaptive current loop PI calculation)

current loop PI calculation, the proposed burst mode control can adaptively calculate the N value to meet the average output current requirement in (15), which further proves its effectiveness.

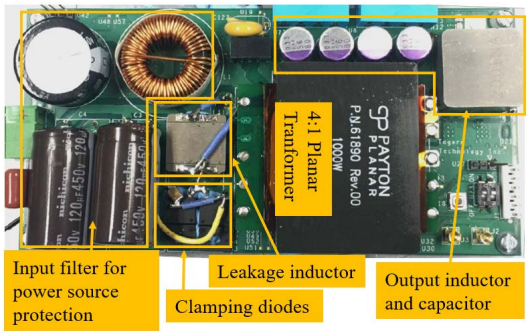
IV. EXPERIMENTAL PROTOTYPE, RESULTS AND DISCUSSION

A PSFB converter prototype has been developed to verify the proposed design methods and adaptive burst mode control. The pictures of the hardware and full load thermal image are shown in Fig. 12 and the specifications of the converter and system parameters are given in Table 1. The overall board size is 145 mm × 72 mm and the PCB has 4 layers.

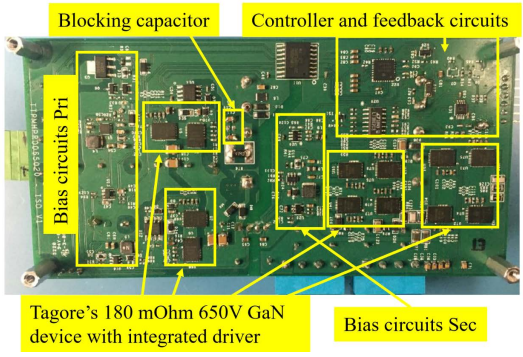
The hardware of the controller and feedback circuits are shown on the top-right side of Fig. 12 (b), and their main schematic is shown in Fig. 12 (d). The output current, I_{out}, is sensed using a 2.5 mΩ resistor, and a high common-mode rejection ratio (CMRR) amplifier (AD8274), is adopted to reduce the common mode voltage from I_{out}. Then, the sensed I_{out} signal, I_{out_sense}, is amplified and level-shifted by operational amplifiers, LT1802, to fit the microcontroller's input range (0 to 3.3 V). The output voltage feedback is realized using the resistor divider and the operational amplifier, LT1802. The microcontroller has 6 PWM outputs, so all GaN devices (Q_1~Q_4 on primary side and Q_5~Q_6 on secondary side) have independent PWM signals. All the PWM signals are inherently synchronized inside the microcontroller. Since it is placed on the secondary side, a digital isolator, SI8645BD-B-IS, is adopted to transfer the PWM signals from the microcontroller to the primary side. The GaN devices are gate integrated, hence no separate gate drivers were needed.

The microcontroller's clock frequency is set as 90 MHz. Since the N value needs to be updated once for every switching cycle, the N is updated at 300 kHz. To achieve such a high updating frequency, all data calculations inside the microcontroller are in integer type.

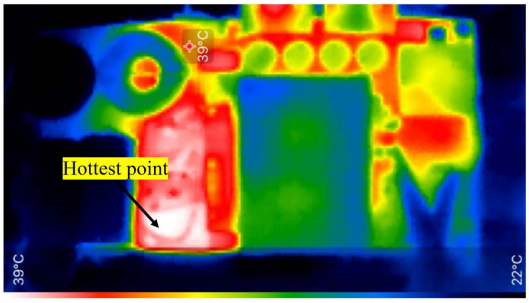
It is noteworthy that based on (2) and information on Table 1, the minimum current reference I_{REF1} to achieve ZVS is supposed to be calculated as 5.76 A. However, considering the effect of the operating temperature on the leakage inductance and GaN devices' output capacitor (C_{oss}), a 30 %



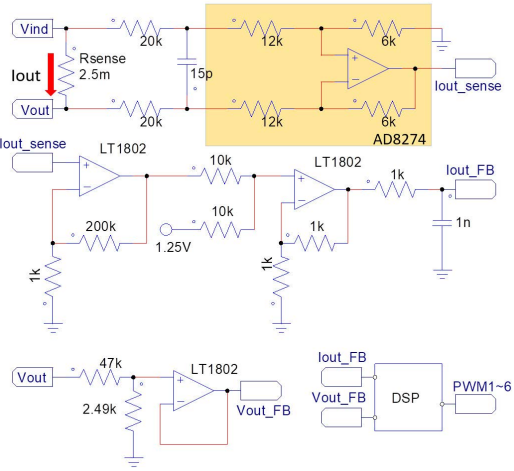
(a) Experimental prototype: top view



(b) Experimental prototype: bottom view



(c) Full load operating thermal image (160 CFM air cooled)



(d) Schematic of the practical controller and feedback circuits (the default units of resistors and capacitors are Ω and F respectively)

FIGURE 12. Hardware photographs, thermal image and partial schematic of experimental prototype.

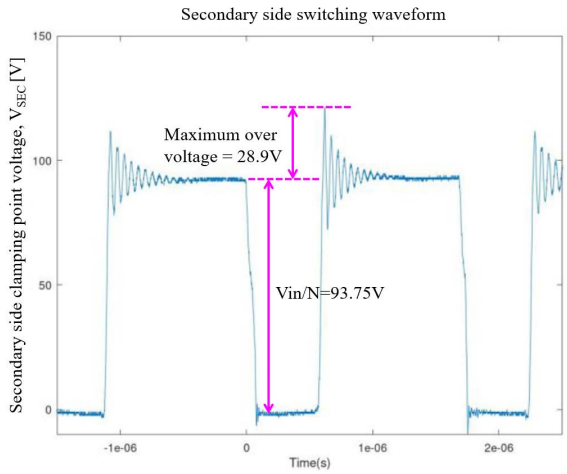


FIGURE 13. Experimental waveform of secondary side clamping point, V_{SEC}.

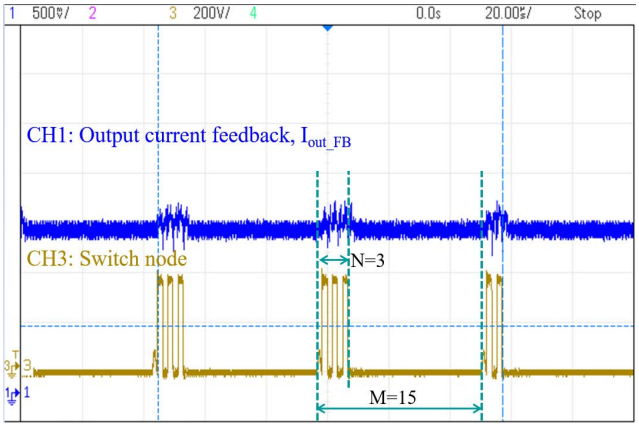
margin is adopted to I_{REF1}. Therefore, the final I_{REF1} in Table 1 is listed as 7.5 A. In addition, M is set as 15 in this prototype controller, otherwise, a larger M value will produce audible switching noise (300 kHz/15 = 20 kHz, within the audible range).

Tagore Technology's 180 mΩ, 650 V, GaN FETs (TP44200NM.) are adopted as both primary side and secondary side switches in this prototype. Integrated driver reduces the noise on the gate driver and results in smoother turning on/off. The secondary side switching waveform is shown in Fig. 13, which proves that diode clamping effectively clamps the V_{SEC} voltage and matches with the simulation result in Fig. 7 (b). The full load operating thermal image shown in Fig. 12 can visually prove that the diode clamping does not lead to significant power loss since the hottest point is only 39 ^{o}C under fan cooling.

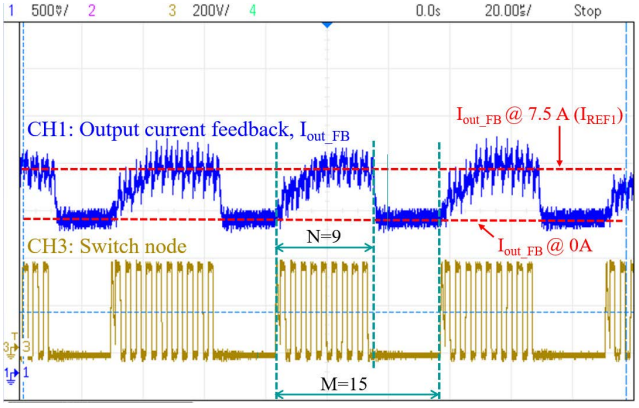
The steady state operating waveforms with the adaptive burst mode control strategy for different load conditions are shown in Fig. 14. Since the output current cannot be directly probed, the output current I_{out} (before output capacitor as shown in Fig. 1) feedback signal I_{out_FB} is used to linearly reflect the change in output current. The primary side leading leg's switch node waveform is also included in Fig. 14 to indicate the number of switching cycles.

At very light load condition, the waveforms in Fig. 14 (a) shows that the adaptive burst mode control operates similar to the conventional burst mode control, since the N value (number of PWM enabled switching cycles in a single burst mode period) is too small for the controller to increase the output current to the minimum ZVS current I_{REF1}.

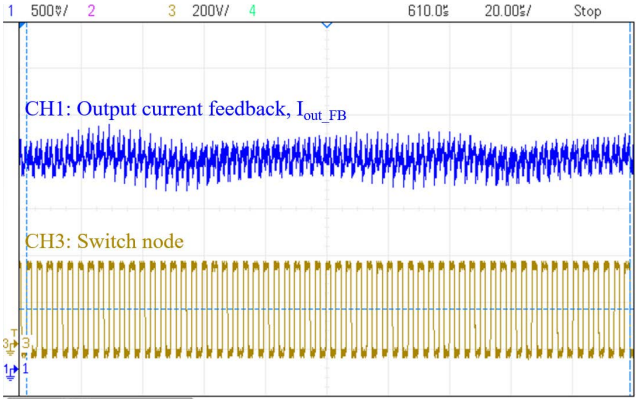
At light load condition, the waveforms in Fig. 14 (b) show that the adaptive burst mode control can control the output current as I_{REF1} indicates. Most switching cycles can achieve ZVS to reduce switching loss which is the dominant power loss at light loads. A very small current overshoot, caused by the calculation errors resulting from integer data-type conversions inside the microcontroller, can be noticed when



(a) Burst mode operation with 300 mA load current (single burst mode period consists of M switching cycles and N cycles are enabled)



(b) Burst mode operation with 3.5 A load current (single burst mode period consists of M switching cycles and N cycles are enabled)



(c) Continuous mode operation with 8 A load current

FIGURE 14. Prototype converter's steady state experimental waveforms by adaptive burst mode control with different load conditions. (7.5 A is set as minimum ZVS current reference I_{REF1} to help burst mode operating to achieve ZVS and correction factor k of adaptive current loop PI calculation is set as 0.86).

the output current increases. However, this overshoot does not cause any GaN device failure since it is well within the rating.

In the ideal case assumption that output current's rising time is infinitesimally small, N is supposed to be 7 to meet this 3.5 A load requirement as $7 \times 7.5\ A = 15 \times 3.5\ A$. However, in a practical application, the output's rising time cannot be ignored. Therefore, N is shown as 9 in Fig. 14 (b),

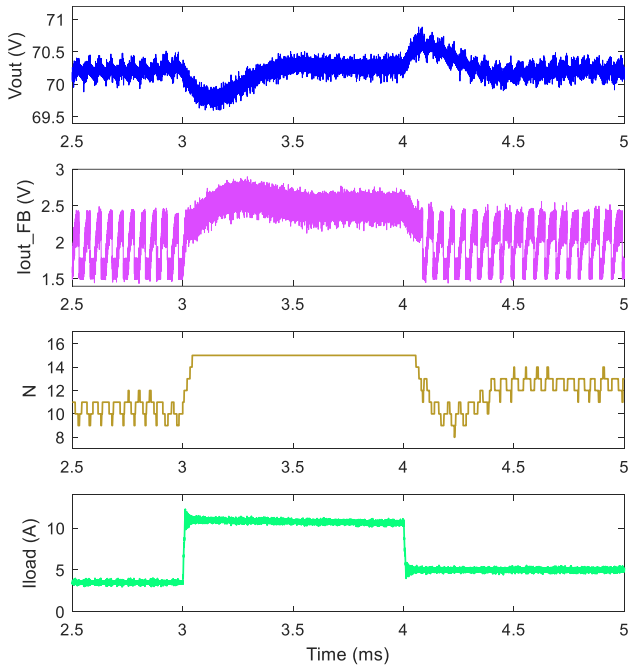


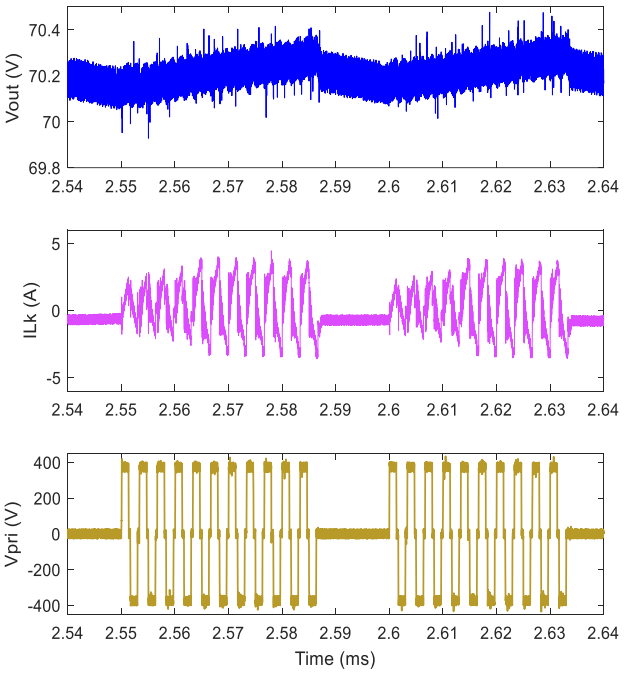
FIGURE 15. Prototype converter load transients (3.5 A to 11 A to 5 A) experimental waveforms with adaptive burst mode control. (*N* waveform is the real time value calculated in the microcontroller, $N = 15$ means prototype operates in continuous mode, 7.5 A is set as minimum ZVS current reference I_{REF1} to help burst mode operating to achieve ZVS and correction factor *k* of adaptive current loop PI calculation is set as 0.86).

which proves that the N value is adaptively calculated by the proposed burst mode controller.

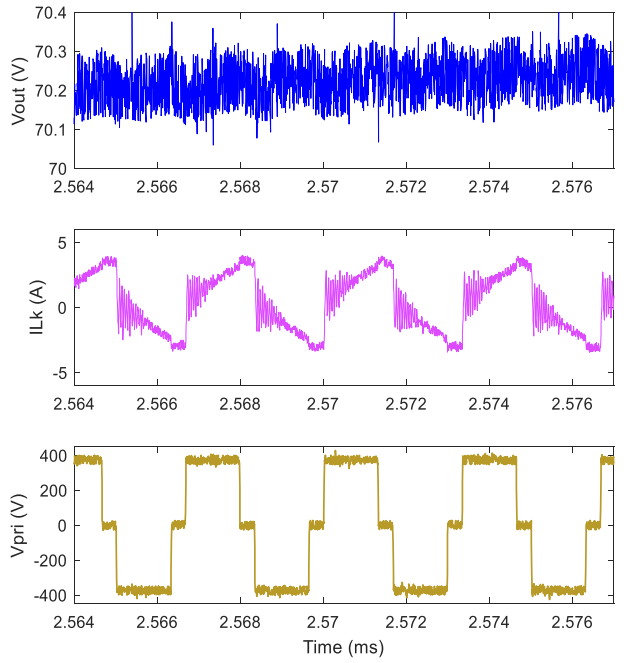
At the heavy load condition (over 7.5 A in this prototype), the converter can achieve ZVS naturally. Adaptive burst mode control calculates that $N>M$. Since the control forces the converter to switch N cycles for every M cycles, $N>M$ can make it operate in continuous mode. The continuous mode operating waveforms are shown in Fig. 14 (c).

The prototype converter's load transient waveforms under adaptive burst mode control are shown in Fig. 15. It may be noted that the waveforms shown in Fig. 13, Fig. 15 and Fig. 16 have been plotted using MATLAB based on experimental data captured using oscilloscopes, to combine with other real time data such as N value from the microcontroller to indicate the converter's real time operation. As shown in Fig. 15, the proposed burst mode control can adaptively change the N value based on the different load conditions and can smoothly switch from burst mode to continuous mode by increase N to 15 (M's value). In every burst mode period, output current (reflected by I_{out_FB}) can smoothly switch between 0 A and minimum ZVS current without any overcurrent. Less than 1 V output voltage under/overshoots are achieved during the load transients.

The primary side operating waveforms under adaptive burst mode control are shown in Fig. 16, which indicates that the blocking capacitor does not distort the transformer current and the proposed control strategy does not affect the



(a) Primary side operating waveforms for continuous two burst mode periods. (I_{Lk} is the leakage inductor current and Vpri is the voltage difference between the switching nodes of two legs)



(b) Zoomed in waveforms of primary side operating. (I_{Lk} is the leakage inductor current and Vpri is the voltage difference between the switching nodes of two legs)

FIGURE 16. Primary side experimental waveforms during burst mode.

normal operating of the PSFB converter. The output voltage waveform also proves that adaptive burst mode control does not produce large output voltage ripple.

Fig. 17 compares the efficiency of the prototype converter with/without adaptive burst mode control under different load

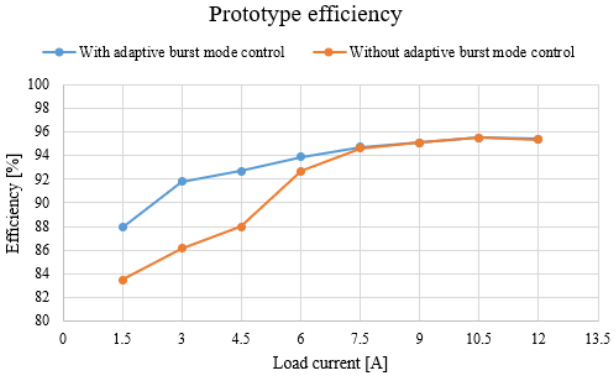


FIGURE 17. Prototype efficiency with and without adaptive burst mode control. (DC biasing power loss is 9 W at no load condition).

conditions. From the comparison in Fig. 17, it is obvious to conclude that adaptive burst mode can effectively increase the power efficiency when the prototype converter cannot naturally achieve ZVS (load current less than 7.5 A in this prototype). A significant efficiency improvement of up to 5 % is possible when the load current is less than 4.5 A. Moreover, Fig. 17 also shows that adaptive burst mode control has the benefit of a wider efficiency-improved load range, compared to the conventional burst mode control. Conventional burst mode is typically applied from no load to 20 % load (0 A to 2.4 A in this prototype) to prevent continuous uncontrolled duty cycle, producing high peak currents that can damage the devices.

V. CONCLUSION

The main issues faced by GaN-based PSFB converters, such as load-dependent ZVS, transformer saturation, and secondary side ringing, were analyzed in detail and solved in this paper. An adaptive burst mode control was proposed to improve the power efficiency at light load. This adaptive burst mode control could achieve both smaller equivalent switching frequency and smaller single switching loss (ZVS for most switching cycles) at the light load condition, which dramatically improved the light load efficiency. A correction factor 'k' was designed in the current loop PI calculation to ensure that the adaptive burst mode smoothly switches the output current between 0 A and minimum ZVS current. A 375 V input 70 V output 800 W prototype was built, and the test results verify the effectiveness of the proposed approach. The efficiency comparison also shows a big improvement from 88 % to 92.5 % at around 3 A load current. The proposed approach can be very effective in applications such as laboratory power supplies, telecom/server power supplies, etc., which usually face a wide range of load conditions.

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