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Time-Domain Protection of Superconducting Cables Based on Artificial Intelligence Classifiers

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ABSTRACT Fault detection and protection of Superconducting Cables (SCs) is considered a challenging task due to the effects of the quenching phenomenon of High Temperature Superconducting (HTS) tapes and the prospective magnitude of fault currents in presence of highly-resistive faults and converter-interfaced generation. This paper presents a novel, time-domain method for discriminative detection of faults in a power system incorporating SCs and high penetration of renewable energy sources. The proposed algorithms utilizes feature extraction tools based on Stationary Wavelet Transform (SWT), as well as artificial intelligence (AI) classifiers to discriminate between external and internal faults, and other network events. The performance of the proposed schemes has been validated in electromagnetic transient simulation environment using a verified model of SC. Simulation results revealed that the proposed algorithms can effectively and within short period of time discriminate internal faults occurring on SC, while remain stable to external faults and other disturbances. The suitability of the proposed algorithms for real-time implementation has been verified using software and hardware in the loop testing environment. To determine the best options for real-time deployment, two different artificial intelligence classifiers namely Artificial Neural Network (ANN) and Support Vector Machine (SVM) have been deployed. The extensive assessment of their performance revealed that the ANN classifier is advantageous in term of prediction speed.

INDEX TERMS Superconducting cables, fault detection, artificial intelligence.

I. INTRODUCTION

In recent years, the deployment of multi-layer Superconducting Cables (SCs) with High Temperature Superconducting (HTS) tapes with inherent fault current limiting capability has been considered as a promising solution towards the modernization of power systems [1]–[3]. As opposed to conventional copper power cables, SCs are characterized by a plethora of technically-attractive features such as compact structure, higher current-carrying capability [4], lower losses, higher power transfer at lower operating voltages and over longer distances [5] and reduced environmental impact [6]. Nevertheless, the integration of SCs with fault current limiting capability within power grids, poses a wide range of fault-related challenges accounting for detection, discrimination and relay coordination, emanating mainly from the quenching phenomenon of the HTS tapes.

The performance of SCs is mainly determined by the electro-magneto-thermal properties of the HTS tapes such as the critical current I_C, critical temperature T_C, critical magnetic field H_C and the structure of the cable and the operating conditions of the system [4]. During steady state conditions, HTS tapes operate in superconducting mode, introducing a current-flowing path with approximately zero resistance. Under certain transient conditions (e.g. electric faults), when the current flowing through the HTS tapes exceeds the value of critical current I_C value, HTS tapes start quenching. During the quenching process, as the fault current increases, the resistance of the HTS tapes and the temperature of the SC increase dramatically, the HTS tapes switch to resistive state and the parallel-connected copper layer (also known as stabilizer layers) provides an alternative, resistive path for the fault current.

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Consequently, the transition to the resistive state, imposes a dynamic change to the equivalent impedance of the system which may introduce an adverse impact on well-established protection schemes, such as overcurrent and distance relays. Furthermore, fault analysis of a SC with second generation (2G) HTS tapes and copper stabilizer layer conducted in [7], [8], revealed that during highly-resistive faults, the quenching process is jeopardized as the fault current is predominately limited by the fault resistance, making the fault detection more challenging. Therefore, the protection of SCs against electric faults is becoming an emerging challenging research area due to the particularities of this technology. Consequently, there is a need for novel and efficient protection schemes which will consider features such as the variable resistance, reduced fault currents and the electrical characteristics of SCs during transient conditions. A coordinated protection scheme based on differential relays, overcurrent and directional overcurrent relays is proposed in [9] for a coaxial HTS cable, integrated in meshed network. A decision-making algorithm was investigated in [10] to improve the performance of differential and overcurrent relays. In [11], a real-time protective algorithm using symmetrical coordinate method and vector analysis during fault conditions, was investigated for protection of a triaxial HTS power cable. In [12] a method based on transmission characteristics is proposed for detection of series faults on DC SCs during which one or more conductors are damaged or disconnected, while a Machine Learning (ML) model was developed to predict the fault type. All the aforementioned protection schemes have enhanced the reliability of the SCs in power system applications. Nevertheless, there are still challenges to resolve in order to improve the fault detection methods on SCs, especially for highly-resistive faults and converter-dominated grids to ensure the reliable protection operation during quenching.

The last few years, there has been an increasing interest in the applications of Artificial Intelligence (AI) based methods in numerous power system applications, including power system protection. With regards to the research area of superconductivity, recent developments have been proposed using ML approaches to extract useful insights and discover hidden trends of superconducting materials such as tools to predict the critical temperature T_C of superconductors or more generally new potentially high-temperature superconducting materials [13]–[16]. Nevertheless, AI-based protection of SCs considering its dynamic behavior (i.e. variable resistance, reduced fault currents and quenching) has not been investigated and reported so far in the literature. To address such research gap, this paper exploits the potential of hybrid methods which composed of ML techniques, such as Artificial Neural Network (ANN) and Support Vector Machine (SVM), and signal processing techniques such as Wavelet Transform (WT), for fault detection on SCs integrated in systems with high penetration of converter-interfaced generation (CIG).

Several studies are reported in the literature which propose the combination of ML classifiers (e.g. ANN and SVM algorithms) with WT for fault detection and classification in distribution and transmission networks. In [17], a hybrid method is reported for fault detection on transmission lines, utilizing local currents from one end of the protected line. Specifically, Discrete Wavelet Transform (DWT) is used as a feature extraction tool to obtain high-frequency components of the two aerial modal currents. The detail coefficients are directly utilized as input to train the ANN classifier to perform fault detection as a classification problem. In [18], the combination of ANN and WT algorithms has been considered to address the challenge of detecting highly resistive faults in distribution feeders. Furthermore, an intelligent fault detection algorithm for series compensated lines is reported in [19]. Particularly, DWT technique is used to extract the detailed coefficients of pre-fault and post-fault signals of the three phase and ground fault currents at the sending end of a transmission line. The energy content of the detail coefficients form the training data set are fed the ANN classifier. Another widely used ML algorithm for fault diagnosis in power systems is the SVM, which has been proven to be a powerful tool for classification problems. In [20], a fault detection scheme for power distribution networks is proposed which uses DWT to extract the features of the transient fault current. The normalized energy content of the detail coefficients are fed to train the SVM classifier for fault detection and fault type classification. A hybrid method based on WT-SVM techniques is presented in [21] for fault detection and discrimination in microgrids, while in [22] the same approach is developed to discriminate highly resistive faults from other transient events (i.e., loading conditions, capacitor switching and load switching) in distribution networks. The results of the reviewed methods indicate that the combination of ML classifiers with the DWT technique can provide reliable and accurate fault detection for transmission and distribution systems, without being affected by varying fault parameters, accounting for fault resistance, fault type and fault location. However, the integration of SCs into power system has unlocked a new research path for the area of power systems protection. The unique electro-thermal properties of the SCs impose many challenges to the existing fault detection schemes, due to the quenching effect. Therefore, in the presented research the effectiveness of the aforementioned hybrid fault detection methods has been evaluated for the application of the SCs which has not been reported in the literature yet. Additionally, the practical implementation of the reported methods has not be tested and the time required for the fault to be detected have not been reported or examined thoroughly.

The remainder of the paper is organised as follows: Section II describes the modelling methodologies for the SC and the system under test and demonstrates initial results for the fault characterisation of the SC. Section III presents the limitations of a conventional over-current protection scheme to provide adequate protection for the SC and analyzes the steps of the proposed protection algorithms. The results of the simulation-based analysis and the validation of the proposed algorithms for real-time applications are

presented in Section IV. Finally conclusions are drawn in Section V.

II. NETWORK MODELLING AND FAULT ANALYSIS

A. SUPERCONDUCTING CABLE MODEL

A verified model of a SC with second-generation (2G) HTS tapes has been utilized for the purposes of this paper, considering both the electrical and the thermal features of the SC, (refer to [7] for detailed analysis and description of the modelling). The specifications of the SC are presented in Table 1.

TABLE 1. Specifications of 33 kV SC.

Symbol	Parameter	Value
n_{tap}	Number of tapes	15
w	Tape width	4 mm
th_{HTS}	YBCO layer thickness	1 μm
th_{Cu}	Copper layers thickness (in total)	40 μm
th_{Sub}	Substrate layer thickness	60 μm
th_{Silv}	Silver layer thickness	3.8 μm
T_C	Critical Temperature	92 K
T_{op}	Operating Temperature	70 K
I_{C0}	Critical current per tape (at 70 K and 0 mT)	250 A
l	Cable length	5 km
V	Rated Voltage	33 kV
S	Rated Capacity	202 MVA

The number of the HTS tapes was selected based on their critical current I_C and the rated current of the cable, while the geometric characteristics of the tapes have been determined based on the maximum quenching voltage [23]. The cable core consists of a copper former made of stranded copper wire, several conducting layers of HTS tapes, an insulation layer and the HTS shield layer, all of which are helically wound around the copper former. The employed tapes are composed of two copper stabilizer layers, one Yttrium Barium Copper Oxide (YBCO) layer, substrate and silver layers [24]. Fig. 1 presents the simplified structure diagram of the HTS tapes. The copper stabilizer layers along with the copper former provide an alternative parallel conducting path for transient current during the quenching. The effect of buffer layer is expected to be negligible and thus has not been considered in the model [25], [26]. Polypropylene Laminated Paper (PPLP) was applied on the HTS tapes and utilized as electric insulation, while a cryostat contains subcooled LN_2 at $65-70K$ was considered to keep SC in superconducting state. The structure of the cable is 3-in-One (triad cable configuration), considering the three phases contained in one cryostat, offering the advantage of reduced installation space and heat leak compared to other cable configurations.

The values of the self-field ($0\,mT$) critical current I_{C_0} for each of the HTS tapes, have been selected based on detailed measurements of the critical current for commercial 2G HTS wires [27]. The critical current I_C, the critical temperature T_C and the working magnetic field B are the main factors which affect the resistivity of the HTS tapes. As the temperature $T(t)$ increases during quenching, the value of the critical current density J_C and by extend the value of the critical current I_C decrease accordingly. The dependence of the critical current density J_C on the temperature can be seen from (1) and (2):

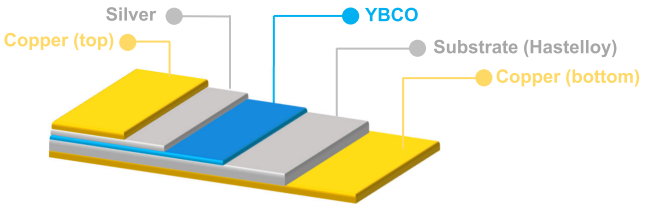

FIGURE 1. Cross section of the HTS tapes.

$$J_C(T) = \begin{cases} J_{C0}(B) \cdot \left(\dfrac{(T_C - T(t))^a}{(T_C - T_0)^a}\right) & \text{for} \quad T < T_C \\ 0 & \text{for} \quad T > T_C \end{cases} \tag{1}$$

$$J_{C_0} = \frac{I_{C_0} \cdot n_{tap}}{s_{HTS}} \tag{2}$$

where J_{C_0} is the critical current density (A/m^2) at initial operating temperature $T_0 = 70\,(K)$ and the working magnetic field $B\,(T)$, T_C is the critical temperature (K), a is the density exponent equal to 1.5 which is applicable to YBCO [28], I_{C0} is the self-field critical current per tape (A) at $T_0 = 70$, n_{tap} is the number of HTS tapes and s_{HTS} is the cross-sectional area of the superconductor. During the resistive state, when the temperature is above the critical value T_C the current density of the HTS layer is reduced to 0.

The non-linear relationship between the current and the voltage of the SC can be explained based on the $E-J$ law. The resistance of the HTS tapes is modeled as a variable resistance and their resistivity was calculated as a function of the critical current density J_C and the temperature T based on (3) [29]:

$$\rho_{HTS} = \frac{E_C}{J_C(T)} \cdot \left(\frac{J}{J_C(T)}\right)^{n-1} \tag{3}$$

where J_C is the critical current density, $E_C = 1\,\mu V/cm$ is the critical electric field and coefficient n has been set to 30 according to [27], [30]. During the superconducting state the resistivity of the HTS tapes is $\rho_{HTS} = 0$. When the applied current exceeds the critical value I_C, the HTS tapes start to quench and their resistance increases. As soon as the temperature exceeds the critical value T_C, the HTS tapes switch to normal resistive state and lose their superconducting properties.

The resistance of the SC during normal resistive mode is only determined by the resistance of the copper (i.e. the resistance of the HTS tapes becomes very high and is set to a maximum value obtained from experimental results), as the majority of the fault current has been diverted to the copper stabilizer layers and the copper former. The resistivity of the copper ρ_{Cu} is given as a function of the temperature based on (4) [31]:

$$\rho_{Cu} = (0.0084 \cdot T - 0.4603) \cdot 10^{-8}, \quad 250\,K > T \geq 70\,K \tag{4}$$

Considering the three distinct operation stages of the SC as the quenching phenomenon is evolving, the equivalent resistance of the SC is calculated as the equivalent resistance of

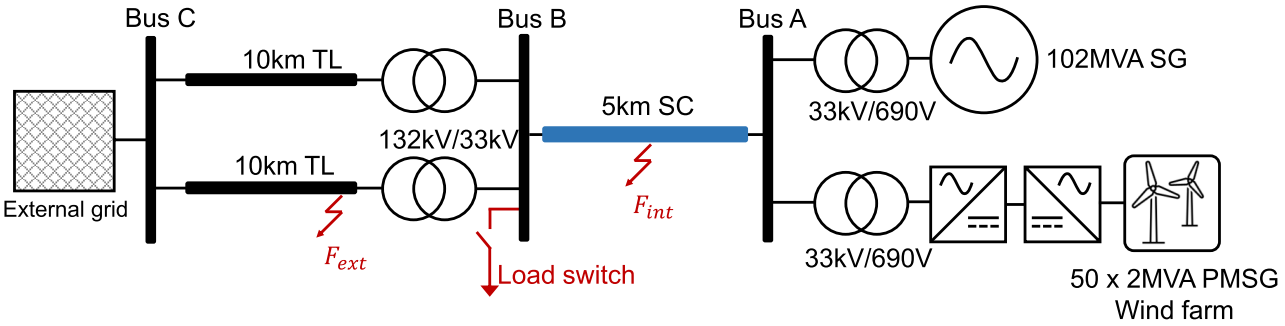

FIGURE 2. Test network.

parallel circuits, considering the current distribution between the HTS layers, the copper stabilizer layer and the copper former. The equivalent resistance R_{eq} of the SC is given in (5) for each operating stage:

$$R_{eq} = \begin{cases} R_{hts} & \text{for } T < T_C \text{ and } I < I_C \\ R_{hts}//R_{Cu} & \text{for } T < T_C \text{ and } I > I_C \\ R_{Cu} & \text{for } T > T_C \text{ and } I > I_C \end{cases} \quad (5)$$

In the presented research, during the quenching process the heat transfer with the external environment has been neglected. In this adiabatic regime, the heat generated by the superconductor is absorbed by itself (causing an increase in the superconductor temperature) and the LN_2 circulating system. The increase in the temperature can be obtained based on (6):

$$T(t) = T_0 + \frac{1}{C_p} \cdot \int_0^t P_{SC}(t)dt \quad (6)$$

where C_p denotes the is the heat capacity of each material and is calculated by the multiplication of the specific heat by the volume and the density of each material. The net power P_{SC} is calculated based on (7):

$$P_{SC}(t) = P_{diss}(t) - P_{cooling}(t) \quad (7)$$

where P_{diss} is the Joule heating produced by the superconducting during the quenching and the $P_{cooling}$ is the power transferred to the LN_2 coolant. The mathematical form of the P_{diss} and $P_{cooling}$ is given by (8) and (9), respectively:

$$P_{diss}(t) = I^2(t) \cdot R_{eq} \quad (8)$$

$$P_{cooling}(t) = h \cdot A \cdot (T(t) - 70) \quad (9)$$

where h denotes the heat transfer coefficient. The value of h is selected based on [32]. As A presented the surface area covered by the LN_2 cooling system.

Therefore, equations (1) to (9) describe the electro-thermal coupling in the SC's modelling procedure. The developed modelling process incorporated dynamic calculations of the electro-thermal conditions of the HTS tapes by including the temperature-dependence of the SC's physical parameters. In more specific during the quenching, the current flowing through the SC results in the generation of joule heating and variations in the temperature, which on their turn affect the physical properties of the SC. The physical parameters of the SC are updated at the end of each time step according to the current value of the temperature. The developed modelling process is depicted in Fig. 3.

B. POWER SYSTEMS MODEL

In order to evaluate the performance of the SC model under network faults and subsequent design and validation of the proposed protection scheme, a power systems model has been developed in Matlab/Simulink as illustrated in Fig. 2 and is utilized for the Electromagnetic Transient (EMT) type simulation studies. The network consists of a voltage source connected at Bus C with nominal voltage of 132 kV, which represents the equivalent transmission network. Two different generation units connected at Bus A have been considered accounting for a Synchronous Generator (SG) and an CIG unit (i.e. wind farm) [33]. The SG has been modelled as a standard salient-pole synchronous machine rated at 102 MVA, integrating automatic voltage regulator, a power system stabilizer and over-excitation limiters [34]. The wind farm has approximately equal rated capacity with the SG and consists of 50 × 2 MVA variable speed wind turbines, yielding a total of 100 MVA. A 5 *km* long SC has been installed between Bus A and Bus B to export the power from SG and wind farm to the transmission system.

C. SC FAULT CURRENT SIGNATURES

For the purposes of designing the proposed protection scheme, a systematic iterative transient simulation analysis was conducted, which aimed to investigate the performance of the SC under different fault types, by analyzing the stages of the quenching process and the resulting voltages and current signatures. The fault analysis considered all types of faults accounting for three-phase (LLL), three-phase to ground (LLL-G), phase-to-phase (LL), phase-to-phase to ground (LL-G) and phase-to-ground (L-G), with fault resistance up to 50 Ω and different fault positions along the SC.

Fig. 4 shows the fault current signatures of the SC under the influence a LLL-G solid fault occurring at 50% of the SC's length.

During the pre-fault conditions, the current flows only through the HTS layer (Fig. 4a). The fault occurs at $t = 3.06\,s$ and the phase currents at the HTS layer start increasing.

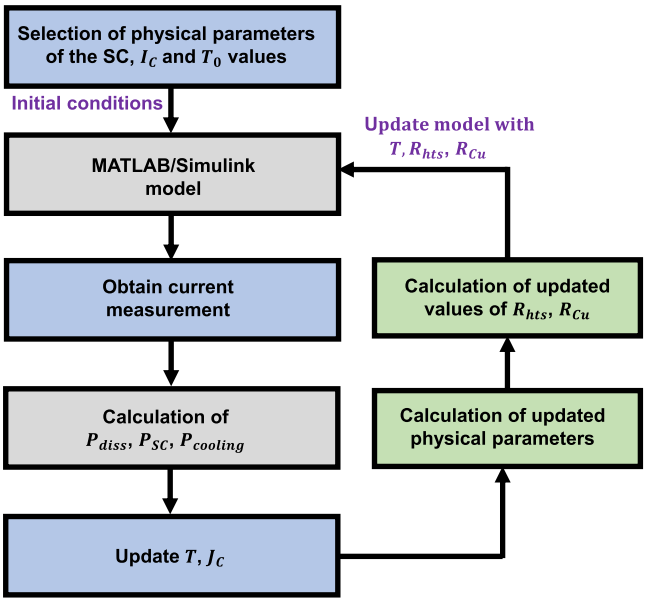

FIGURE 3. Modeling process.

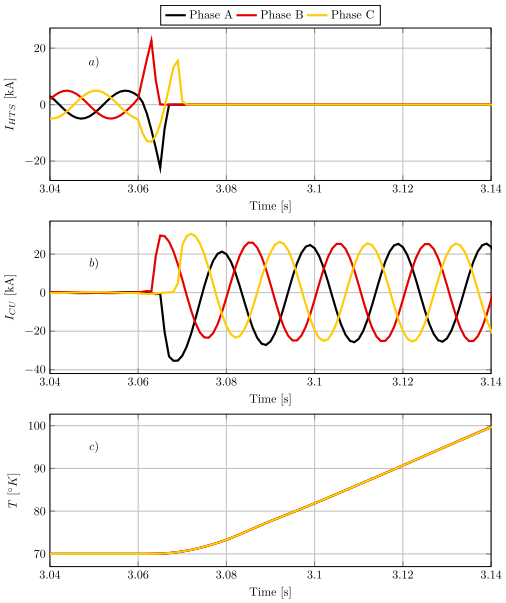

FIGURE 4. SC response to a LLL-G solid fault at 50% of SC's length: a) currents of HTS layer, b) currents of copper stabilizer layer, c) temperature of SC.

As soon as the fault current exceeds the value of the critical current I_C, the HTS tapes start quenching, the resistance of the HTS tapes and the temperature start increasing immediately and the fault current distribution changes. Specifically, as depicted in Fig. 4b, at $t = 3.064\ s$, most of the current diverts to the copper stabilizer layer since the resistance of the HTS layers is relatively high. The initial peak of the fault current flowing through the copper is 35.03 kA for Phase A, 29.69 kA for Phase B and 30.19 kA for Phase C.

Furthermore, the copper resistivity increases as a function of the temperature, which leads to the current being sustained at approximately 24.36 kA, 25.25 kA and 25.07 kA for Phase A, B and C respectively. Fig. 4c presents the increase in the temperature of the SC for each phase. As observed, the temperature exceeds the critical temperature T_C (i.e. 92 K) for the three phases, and the HTS tapes enter into the highly resistive state.

Fig. 5 provides a deeper insight of the effect of the fault resistance on the quenching process by presenting the fault current signatures under the influence of a LLL-G fault occurring at 50% of SC's length with fault resistance $R_f = 50\ \Omega$.

As depicted in Fig. 5a, when fault occurs at $t = 3.06\ s$, the current reaches peak values of approximately 5.12 kA, 5.14 kA and 5.15 kA for Phase A, B and C respectively (i.e. below critical current I_C). Effectively, there is no quenching phenomenon and therefore there is no current sharing between the HTS and copper stabilizer layers. Quenching depends on the value of the prospective fault current, which in turn depends on the value of the fault resistance and fault current contribution from the energy sources. Therefore, an increase in the value of the fault resistance leads to low prospective fault currents, even below the critical current I_C, preventing the SC from quenching and affecting its fault current limiting capability, while making the fault detection and discrimination aspect even more challenging. This effect in conjunction with penetration of ICG units in the future power grids, which result in reduced fault current magnitudes [33], make the faults on the SCs even more difficult to be detected.

III. PROPOSED ALGORITHMS

The proposed fault detection and discrimination scheme is primarily based on two distinctive tools namely SWT for real-time feature extraction and ML classifiers (i.e. ANN and SVM) for fault classification and discrimination.

A. LIMITATIONS OF EXISTING SCHEMES & NEED FOR ADVANCED SOLUTIONS

Prior to analyzing the proposed algorithms, it is of paramount importance to illustrate the limitations of existing solutions and subsequently highlight need for more advanced and efficient solutions.

For this purpose, a conventional over-current relay has been developed in Matlab/Simulink and its performance has been investigated in terms if its a sensitivity to internal faults as well as its stability against external faults and load switching events. The test cases (i.e. the fault current signatures) have been obtained by conducting a series of faults using the system in Fig. 2. The simulation studies contain internal (F_{int}) and external (F_{ext}) faults and load switching event. It shall be noted that external faults and load switching events can initiate the quenching of the HTS tapes so it is of utmost importance to ensure that the protection scheme remains stable (i.e. the protection scheme does not falsely indicate the presence of an internal fault).

The internal faults were simulated at every 10% of the SC's length, while external faults were considered at the adjacent transmission lines. All possible fault types were considered (i.e LLL-G, LLL, LL-G, LL and L-G) with fault resistance up to 50 Ω. Load switching events with different

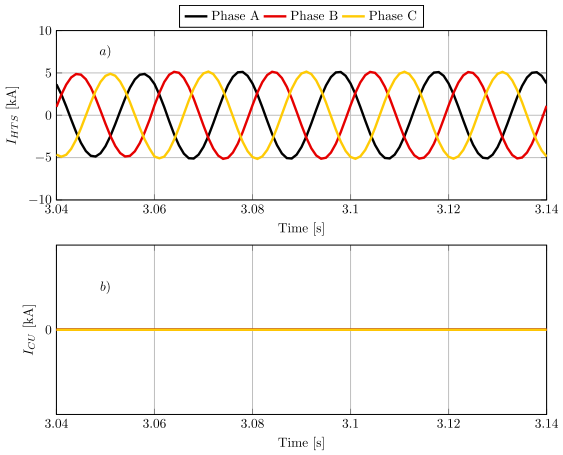

FIGURE 5. SC response to a LLL-G fault at 50% of SC's length with $R_f = 50\ \Omega$: (a) currents of HTS layer, (b) currents of copper stabilizer layer.

values of active and reactive power were simulated at the end of SC at Bus B. During the simulation process the three phase current signatures flowing through the SC for all the investigated transient events (i.e internal, external faults and load switching events) were captured at sampling frequency of 20 *kHZ*. The developed over-current scheme was tested in terms of its sensitivity to operate for the internal faults and its capability to remain stable during the external faults and the load switching events.

For the current setting of the developed relay, a wide range over-current threshold was considered starting from 1.05 *p.u.* to 2 *p.u.* (base value corresponds to the nominal current). The performance of the over-current relay can be evaluated based on the diagram presented in Fig. 6. The results indicate that for low overcurrent threshold (i.e 1.05 *p.u.*), approximately 84% of the total number of internal faults are successfully detected. However, for the same current setting, the over-current relay initiates a tripping signal for the external faults and the load switching events as well, presenting low degrees of stability. To obtain high margins of stability the threshold should be set to 1.4 *p.u.* and beyond, which would comprise the element of sensitivity.

Effectively, these results demonstrate that conventional protection techniques, such as the over-current relays, are not suitable to provide reliable solutions for SCs, combining both sensitivity and stability. In particular, it can be concluded that protection of SCs, is a complex problem, which cannot be solved with continental protection approaches (i.e. thresholds with time delays and grading), and more profound insights to the transient nature of SC faults should be considered. Therefore, this paper proposes the utilization of ML techniques which is anticipated to overcome the aforementioned limitations.

B. STAGES OF THE PROPOSED ALGORITHMS

The proposed algorithm, enabling fault detection and classification of SC, is a time-domain method, implemented in four discrete stages as illustrated in Fig. 7.

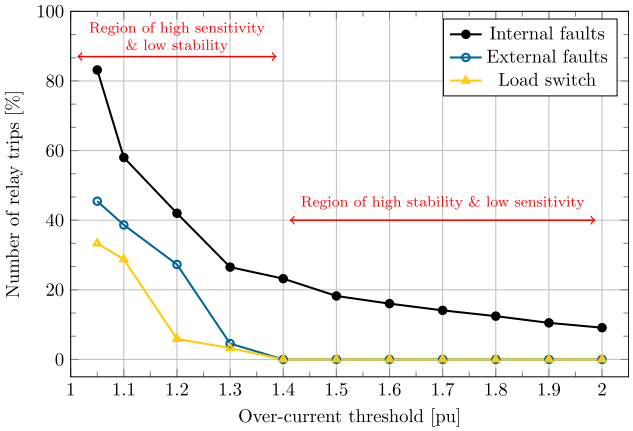

FIGURE 6. Performance of over-current relay under internal, external faults and load switching events.

1) STAGE 1 - SIGNAL ACQUISITION

At this stage, the three phase current and voltage signals (i.e. currents flowing through the SC, as well as voltage at Bus A) are captured at a sampling frequency of 20 *kHz*. These are then passed through anti-aliasing filters, normalized and packaged into appropriate windows to be processed by the SWT filters.

2) STAGE 2 - SWT

Wavelet Transform (WT) is a powerful tool for power system protection due to its capability to simultaneously analyze signals in time-frequency domains. One of the main appealing features of WT, is its inherent capability to detect signal singularities and disclose the useful information contained in measured quantities (e.g. voltages and currents) after a power system event. WT can be distinguished in two categories: (i) Continuous Wavelet Transform (CWT) and (ii) Discrete Wavelet Transform (DWT), the selection between them is a trade-off between the desired time resolution and processing requirements [35].

DWT has been widely used for power system protection applications due to its reduced complexity and computational efficiency [36]–[38]. However, one of the significant drawbacks of the DWT, is the effect of the downsampling process taking place at every decomposition level [39], leading to loss of information in the high frequency content of the analyzed signal. A potential solution to overcome this drawback, is the utilization of Stationary Wavelet Transform (SWT) algorithm, which does not downsample the signal, but instead it upsamples the filters by a factor of two at every decomposition level (by means of zero padding).

The output of the SWT at each decomposition level contains the same number of coefficients with the analyzed signal. Therefore, the main advantage of the SWT is the preservation of time information of the original signal at each level. SWT algorithm can be implemented by applying discrete convolution to the analyzed signal with the appropriate high-pass and low-pass filters, as in the case of DWT, but without downsampling. Fig. 8 illustrates the SWT procedure up to decomposition level of two.

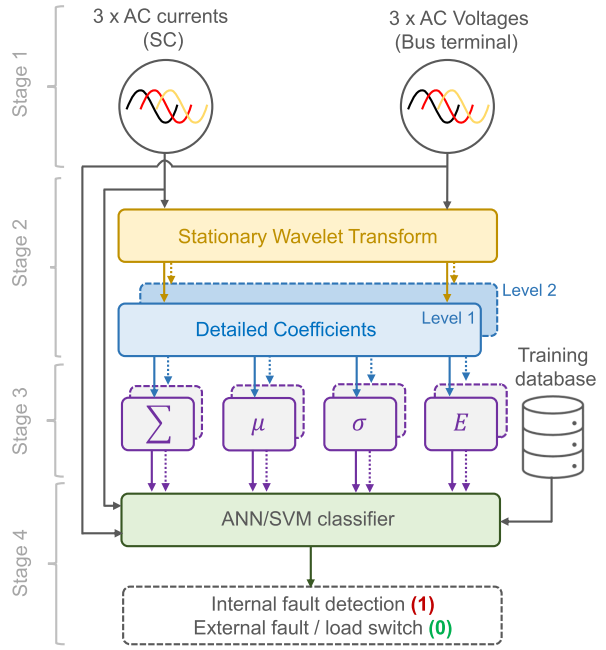

FIGURE 7. Schematic diagram of the proposed algorithm.

Specifically, $x[k]$ is the original signal, $h_j[k]$ and $g_j[k]$ are the high-pass and low-pass filters at $j-th$ level, and $A_j[k]$ and $D_j[k]$ are the approximation and detailed coefficients at $j-th$ level. For the decomposition level j, the filters $h_j[k]$ and $g_j[k]$ are obtained by upsampling the filters at level $j-1$ which are then convolved with the approximation coefficient at level $j-1$ to produce the approximation and detailed coefficient of level j. For each decomposition level j, the detailed coefficients are calculated based on (10).

$$D_j[k] = \sum_{l=0}^{L-1} A_{j-1}[n] \times h_j[k-n] \tag{10}$$

where A_j is the approximation coefficients at level j, k is the index of the sample and L the order of the high pass filter $h[n]$.

In the presented research, the monitored parameters are subjected to level 1 and 2 decomposition though the SWT technique. The selection of the most suitable decomposition levels is based on the frequency content of interest of the signal to be processed. Based on the literature, the *db*4 mother wavelet presents relatively high accuracy and reliability and therefore it was selected for the purposes of the proposed scheme [36], [39], [40]. It shall be highlighted that wavelet design can be considered a dedicated and separate research area and is subject to the application requirements; therefore detailed designed is beyond the scope of the presented research. Considering *db*4 mother wavelet and the required level of decomposition, the required number of the samples per iteration is eight.

3) STEP 3 - FEATURE EXTRACTION

A 30-sample moving data window with 29-sample overlap, has been applied on the monitored parameters and subsequent detail coefficients at level 1 and level 2. The numerical values

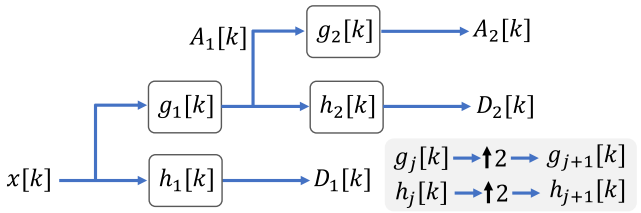

FIGURE 8. Stationary wavelet transform algorithm.

within those windows are used to calculate feature vectors such as the sum $\sum(D_j)$, mean $\mu(D_j)$, standard deviation $\sigma(D_j)$ and energy content $E(D_j)$ of the absolute values of detail coefficients at level 1 and 2, in order to unlock deeper insights in the nature and the evolution of faults. The feature vectors were calculated as presented in (11) to (14) below:

$$\sum(D_j) = \sum_{k=1}^{n_w} |D_j(k)| \tag{11}$$

$$\mu(D_j) = \frac{1}{2^j \cdot n_w} \sum_{k=1}^{n_w} |D_j(k)| \tag{12}$$

$$\sigma(D_j) = \sqrt{\frac{1}{2^j \cdot n_j} \sum_{k=1}^{n_w} (|D_j(k)| - \mu(D_j))^2} \tag{13}$$

$$E(D_j) = \sum_{k=1}^{n_w} [D_j(k)]^2 \tag{14}$$

where $D_j(k)$ is the $k-th$ detail coefficient for each decomposition level $j = 1, 2$ and n_w is the window size.

These feature vectors can represent effectively the state of the SC during the simulated transient events and form the basis for fault detection and discrimination. It is worth highlighting here that the feature vectors are normalized by removing the mean value and dividing by the standard deviation as presented in (15):

$$x(i)_{scaled} = \frac{x(i) - \overline{X}}{\sigma(X)} \tag{15}$$

where $x(i)$ is the value of the sample in the feature vector x, $\overline{X}$ is the mean value of each feature in the training set and $\sigma(X)$ is the standard deviation of each feature in the training set.

4) STAGE 4 - BINARY CLASSIFICATION

The normalized feature vectors are used as inputs to the ML-based binary classifiers, to discriminate between internal faults and external faults and disturbances. The classier will initiate at its output '1' for internal faults and '0' for external faults and other disturbances. Effectively, the output of the binary classifier is used as a tripping signal to initiate operation of the circuit breaker which protects the SC. Detailed analysis of the ML-based binary classifiers are presented in the following subsection. In principle, ANN and SVM algorithms have been proven to be robust and effective algorithms for fault detection, classification and location, providing fast and reliable fault diagnosis in power

systems [17], [19], [21], [22]. In the presented work their performance was evaluated for the fault detection on SCs.

C. ML-BASED BINARY CLASSIFIERS

1) ARTIFICIAL NEURAL NETWORKS

ANNs are decision-making algorithms which have been widely adopted for fault diagnosis studies, as they offer a variety of advantages and exhibit excellent qualities such as capability to incorporate with dynamic changes in power systems, ability to find the solution for complex non-linear equations, normalization and generalization capability, immunity to noise and robustness [41].

In order to select the most-suitable ANN architecture for fault detection and the best training model, a wide range of ANN network topologies have been tested. The optimum hyperparameters were set based on the grid search technique. For this purpose, hyperparameter tuning was performed, considering different combinations of hyperparameters. Specifically, the hyperparameters defined with the grid search process are the following: i) the number of hidden layers, ii) the learning rate, iii) the batch size and iv) the number of the neurons at each hidden layer. The performance of all the combinations was evaluated based on the K-fold cross-validation technique. Specifically, the dataset was divided into K subsets and the model was trained and tested on each hyperparameter combination K times. In each iteration, $K-1$ subsets were used for training, while the remaining 1 fold was used for validation. The optimum combination of the hyperparameters was determined based on the K-fold cross-validation score, which is the average of the scores obtained on each subset.

In this study, the 5-fold cross-validation technique was utilized, while F1-score was selected as the 5-fold cross-validation evaluation metric, in order to select the optimum hyperparameters for the ANN model. The optimum hyperparameters and subsequently the best ANN classifier are presented in Fig. 9.

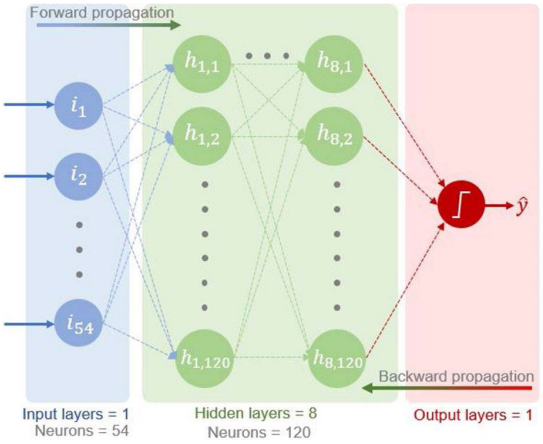

FIGURE 9. Architecture of the developed ANN classifier.

The developed ANN classifier is a fully-connected, multilayer model which consists of one input layer with fifty-four neurons (the number of the neurons in the input layer is equal to the length of the feature vectors) and eight hidden layers with one hundred twenty neurons in total. The grid search 5-fold cross-validation technique revealed that a deep ANN network is required in order to learn a robust data representation and present higher generalization capability. Furthermore, to improve the performance of the ANN classifier, the drop-out technique was used for the hidden neurons during the training process in order to reduce interdependent learning amongst the neurons and consequently minimize the over-fitting to the training data. The optimization method used is the Adam optimizer, the learning rate has been defined based on the grid search 5-fold cross-validation technique, while the rest of the parameters were used as defined within the Pytorch framework. The ANN model operates as a binary classifier, and therefore it has one neuron in the output layer. The output value varies from 0 to 1 due to the utilization of log-sigmoid function as activation function for the output layer. Specifically, the log-sigmoid function yields a probability value for each class. In this research in order to convert the predicted probability value to a class label (0 or 1), a decision threshold equal to 0.9 has been selected for both training and testing process. This means that any probability above the threshold 0.9 corresponds to output 1 and indicates the presence of an internal fault, generating a tripping signal.

2) SUPPORT VECTOR MACHINE

SVM is a supervised learning algorithm which is based on statistical theory and is widely used for solving linear and non-linear classification as well as regression problems. In recent years there has been a surge of interest in using SVM for fault detection and classification problems [41], [42]. SVM possess excellent features for binary and multi-class classification problems, such as capability to deal with arbitrarily structured data, over-fitting avoidance and not converge to local minima and generalization capability. In this work the detection of faults on SCs can be considered as a binary classification problem whose input vectors are not linearly separable.

The idea of SVM algorithm is to map non-linearly the input vectors into a high dimensional feature space, and define a decision boundary. For a given set of labeled training data, an optimal hyperplane is determined as a solution of an optimization problem.

The optimal hyperplane is the one that best-separates the features into to two classes. The selected data points from the training set which affect the position of the dividing hyperplane are called support vectors. By projecting the hyperplane into the initial dimensions, the desired decision boundary can be determined. The SVM algorithm can be explained as a Wolf's dual optimization problem based on [43]. The values of the SVM model parameters have been selected based on the combination of grid search and 5-fold cross-validation method and similarly to the ANN, F1-score was utilized as 5-fold cross-validation score. For the SVM classifier, the selected hyperparameters are the following: $C = 100$ and $\gamma = 1$, kernel function = Radial Basis Function (RBF).

D. SYSTEM TRAINING

For the purpose of the simulation-based training, the system depicted in Fig. 2 has been utilized and a series of systematic iterative simulations have been performed (similar to those conducted in III-A for the testing of the over-current relay). For each simulation, the waveforms of the current flowing through the SC's phases (measure at the end connected at Bus A), and the voltage at Bus A, were captured for five cycles (one pre-fault and four during fault). All the feature vectors presented in Subsection III-B3 were also extracted as part of the training process. Normalization technique was also applied to scale the feature vectors prior to the training process in order to improve the performance of the classifiers and accelerate the learning process. The monitored parameters and calculated feature vectors were used to create a Python-based training data base using the PyTorch open source machine learning library. A dataset of 415 transient events (faults and load switching events) has been created. From this dataset, 60% was used for training, 20% for validation, while the remaining 20% for testing.

E. ANTICIPATED TIME DELAYS OF THE PROPOSED SCHEME

It is important to ensure that the proposed time-domain method will operate correctly, despite delays expected in real life implementation. The anticipated operating time t_{op} of the proposed scheme, comprises of the delays associated with the window-based processing t_{dw}, the delays of the data processing t_{dt} (accounting for digitisation and transmission) and the time t_{ML} required by the ML algorithm to produce a binary decision:

$$t_{op} = t_{dw} + t_{dt} + t_{ML} \tag{16}$$

The delay t_{dw} associated with the window-based processing can be calculated as follows:

$$t_{dw} = (n_{w-fv} - n_{w-ov}) \cdot t_s \tag{17}$$

where n_{w-fv} is the length of the processing window for the feature vectors, n_{w-ov} is the window overlap and t_s is the sampling time. Considering a 30-sample window, with 29 samples overlap at 20 kHz, t_{dw} is 50 μs.

The proposed protection scheme requires six measurements to be digitised, concentrated and transmitted to the protection system for further processing. Considering a modern centralised system with merging units (MUs) and an Ethernet switch based on IEC-61850 to collect and transmit all measurements in real-time, the overall time delays for digitisation and transmission t_{dt} can be calculated as follows [36]:

$$t_{dt} = t_s + t_{MU} + t_{Eth} + t_{ps} \tag{18}$$

where t_s is the maximum delay due to the analogue sampling (i.e. $t_s = 1/f_s = 1/20\ kHz = 50\ \mu s$), t_{MU} is the processing time in the MU (i.e. time to encode the sampled values), t_{Eth} is the total maximum Ethernet network latency, and t_{ps} is the processing time for the protection system (i.e. the time to decode the sampled values). Assuming one Ethernet link and eight competing measurements, t_{Eth} can be estimated to be 6.34 μs [36]. t_{MU} and t_{ps} can be estimated as 12 μs and 9.5 μs, respectively, based on the work conducted in [44]. Therefore, the overall resulting t_{dt} is 77.84 μs.

The time required by the ML-based classifier (i.e. t_{ML}) to produce the tripping signal is subject to a number of variables such the algorithm complexity, the coding efficiency, the processing power of the system, etc. Therefore, t_{ML} cannot be assessed theoretically but will be evaluated experimentally in the following section.

IV. SIMULATION RESULTS AND VALIDATION

The performance of the proposed protection algorithms has been validated using widely-used evaluation metrics and time performance assessment. The robustness and the classification capability of the two classifiers were tested using as evaluation metric the classification accuracy, which is the ratio of the number of the correct predictions to the total number of input samples. A time performance assessment has been utilized to validate the suitability of the algorithms for real-time implementation (i.e. their ability to produce in real-time a binary tripping signal) using a real-time software in the loop (SIL) platform.

A. ACCURACY EVALUATION

The ANN and SVM classifiers were tested using the 20% of the pre-simulated dataset of 415 cases, which contain all types of events (i.e. internal faults, external faults and load switch events). Table 2 and Table 3 present the normalized confusions matrix produced for each binary classifier. The high percentage value of True Positive (TP) predictions indicates the capability of the classifiers to classify correctly the internal faults, while the high percentage value of the True Negative (TN) predictions show that both classifiers can predict correctly the external faults and the load switch events, preventing protection operation for these disturbances. Regarding the percentage value of False Positive (FP) and False Negative (FN) predictions, they must be in principle very low as they indicate incorrect predictions. Practically, these values would falsely flag the presence of an internal fault and the absence of external fault and load switch events, which would compromise the stability and sensitivity of the proposed scheme.

The results presented in Table 2 and 3 show that the percentage of the FP predictions for the ANN classifier is higher compared to those of the SVM classifier, which suggests that the SVM provides higher reliability and availability. Conversely, the percentage of FN predictions for the ANN is slightly lower compared to those of SVM, which highlights that ANN provides higher degree of dependability. Generally, from the protection perspective, there is clearly a trade-off between the reliability and the dependability. However, it shall be noted that undetected faults resulting from FN predictions, are in principle more hazardous for the

TABLE 2. ANN confusion matrix.

Actual / Predicted Condition	Predicted Negative	Predicted Positive
Actual Negative	TN=99%	FP=0.12%
Actual Positive	FN=0.41%	TP=99.6%

TABLE 3. SVM confusion matrix.

Actual / Predicted Condition	Predicted Negative	Predicted Positive
Actual Negative	TN=99%	FP=0.048%
Actual Positive	FN=0.56%	TP=97.5%

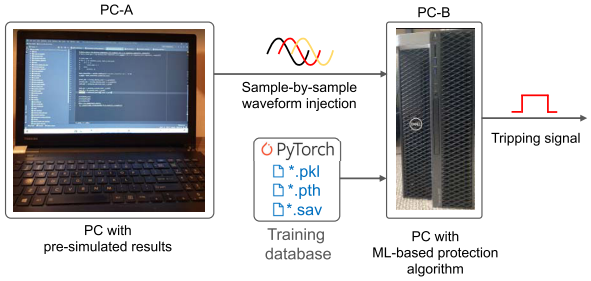

FIGURE 10. Overview of the testing environment.

system, compared to reduced availability resulting from FP predictions.

The selected evaluation metric used to asses the performance of the ANN and SVM classifiers on the testing dataset, is the accuracy ACC and it is derived from the confusion matrix based on (19):

$$ACC = \frac{TP + TN}{TP + TN + FP + FN} \tag{19}$$

Taking into account the value presented in Table 2 and Table 3, the resulting accuracy for ANN and SVM is 99.74% and 99.69%, respectively.

B. TESTING ENVIRONMENT FOR REAL-TIME VALIDATION

A diagram of the testing environment utilized for validation of the proposed scheme is shown in Fig. 10. A wide range of cases (i.e. internal faults, external faults and load switching events) were simulated using the Simulink-based model depicted in Fig. 2, and the resulting waveforms were stored externally for post-processing. Such pre-simulated results were loaded on PC-A and were subsequently injected (on a sample-by-sample basis) to PC-B though TCP/IP sockets. The specification of the PC-A and PC-B are shown in Table 4.

TABLE 4. PC specifications.

PC	Specifications
PC-A	i7-6500U, 2 cores, 4 threads, 2.4 GHz, 4 MB Cache
PC-B	i9-10980XE, 18 cores, 36 threads, 3/4.6 GHz, 24 MB Cache, GPU NVIDIA Quadro RTX 6000

The developed protection algorithm was loaded in PC-B and the training database was also fed to the PC for complementing the binary classifiers.

Effectively, the developed testing environment forms a real-time SIL platform for validating the proposed protection scheme. The results reported in the following subsections are based on this SIL set-up, assessing the capability of the proposed scheme to run in real-time taking into account realistic digital infrastructures. This will enable the in-depth,

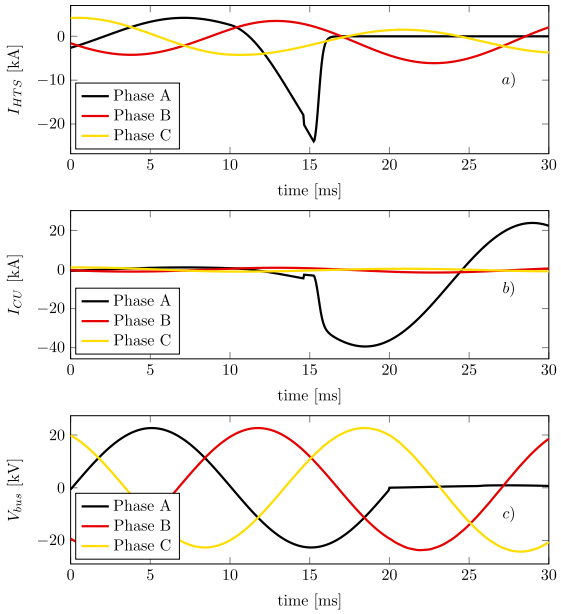

FIGURE 11. Current and voltage signatures for internal, L-G fault solid at 10% of the SC.

time-domain assessment of the ML-based protection schemes as opposed to the statistical accuracy metrics presented in Section IV-A.

C. TIME PERFORMANCE EVALUATION

The ANN and SVM classifiers were tested on a real-time basis on a wide range of fault scenarios and load switch events in order to assess their classification capability and time performance to initiate the corresponding tripping signals.

1) SENSITIVITY AND STABILITY OF THE PROPOSED SCHEME

Fig. 11, Fig. 12 and Fig. 13 present the simulations results of representative test cases, which quantify the overall performance of the proposed protection algorithms. Effectively, such cases demonstrate the feasibility of the algorithms to operate for internal solid and highly resistive faults and remain stable for external faults and load switch events (in all scenarios, the event is triggered at $t = 10\ ms$).

Fig. 11 and Fig. 12 illustrate the system response and protection algorithms feature vectors performance under an internal LG solid fault, occurring at 10% of SC's length. Fig. 11a, Fig. 11b and Fig. 11c, present the fault current signatures flowing through the HTS and copper stabilizer layers and the voltages for each phase respectively. At the time of the fault occurrence at $t = 10\ ms$, the HTS layer of Phase A starts quenching, reaching peak values of approximately 16 kA. Once the HTS tapes reach a highly resistive state, the current is diverted to the copper stabilizer layer (approximately 6 ms after the fault occurrence).

Fig. 12a illustrates the detailed coefficients for the first and second decomposition levels of the total current flowing through the Phase A of the SC. As it can be seen, the utilization of the SWT technique leads to unique peaks which indicate the presence of a transient (i.e. a fault at this

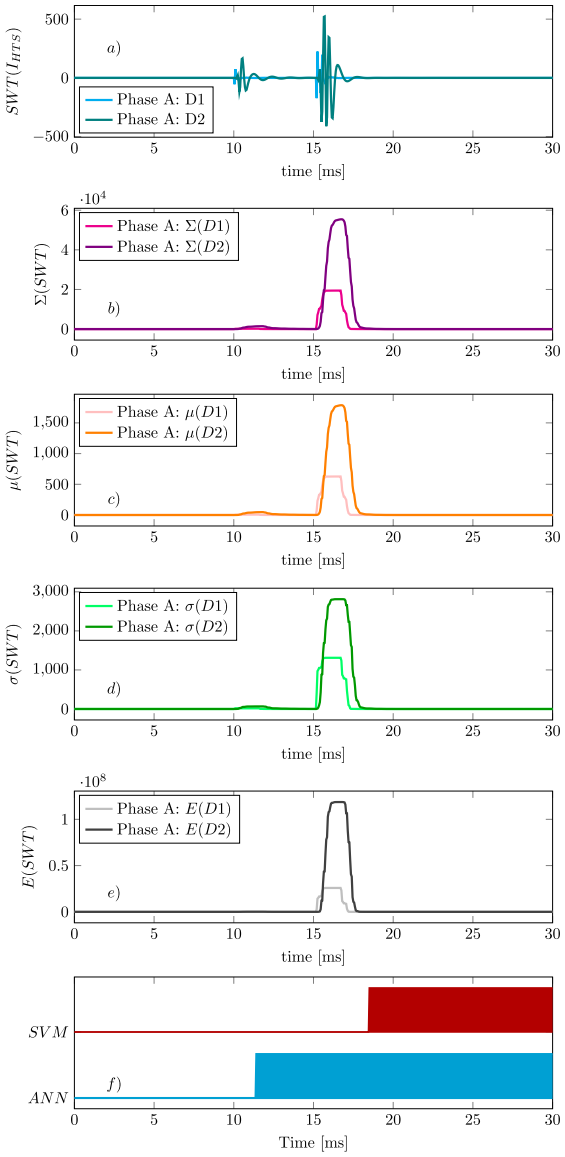

FIGURE 12. Feature vectors resulted from the SWT of the total current flowing through the SC for an internal, L-G solid fault at 10% of the SC.

occurrence). Fig. 12b to Fig. 12e, illustrate the magnitudes of selected features vectors extracted from the current signal flowing through the Phase A of the SC, which satisfies the feature extraction stage (fault detection) of the algorithms. In particular, Fig. 12b corresponds to the magnitude of the sum of the absolute values of detailed coefficients, Fig. 12c depicts the magnitude of the mean of the absolute values of the detail coefficients, Fig. 12d illustrates the standard deviation of detail coefficients and Fig. 12e presents the magnitude of the energy of the detail coefficients. The measurements and feature vectors presented in Fig. 11 and Fig. 12a to Fig. 12e (alongside the extracted feature from the non-faulted Phases B and C) were used as inputs to ANN and SVM classifiers in order to produce a tripping signal, as presented in Fig. 12f. The binary signals presented in Fig. 12f, demonstrate the capability of both classifiers to classify correctly the internal fault and initiate a tripping signal, validating the effectiveness of the proposed protection algorithms. Particularly, the ANN classifier initiates a tripping signal 1.38 *ms* after the fault occurrence, while SVM outputs the same signal after 8.45 *ms*. The total delay between the time instant of the fault occurrence and the initiation of the tripping signal is a sum of the measurement, collection, processing and transmission delays as discussed in Section III-E emanating from the realistic implementation of the proposed algorithm, as well as the time required by classifier's algorithm (ANN and SVM) to be executed and perform event classification.

Fig. 13 demonstrates the stability of the protection algorithms during external faults and load switch events and the discriminative capability of the algorithms to produce tripping signal for highly resistive internal faults. Specifically, an LLL-G fault with fault resistance $R_f = 50\ \Omega$ was applied at 10% of SC's length. The currents flowing through the HTS layers are depicted in Fig. 13a for the three phases and the currents of the copper stabilizers layers in Fig. 13d, respectively. It is evident that during the highly resistive fault, the current flowing through the HTS layer of Phase A is lower than the critical current I_c, preventing the SC from quenching. Therefore there is no current sharing between the HTS and copper stabilizer layer and at this case, the fault current is predominately limited by the high value of the fault resistance. Nevertheless, the proposed protection algorithms detect the internal fault and both classifiers produce a tripping signal as illustrated in Fig. 13g. Specifically, ANN initiates a tripping signal 1.43 *ms* after the fault occurrence and SVM after 7.94 *ms*. Based on these results it is evident that both classifiers have been trained well and are able to make accurate predictions, increasing the sensitivity of the protection algorithm.

Fig. 13b and Fig. 13c present the HTS current signatures for an LLL-G external solid fault applied at the adjacent 132 *kV* transmission line and a load switch event at Bus B respectively. As opposed to the highly resistive internal fault, both of such events force the SC to quench. Particularly, during the external fault, the current flowing through the HTS layers of the three phases, present a peak of 8.9 *kA* for Phase A, 10.5 *kA* for Phase B and 9.1 *kA* for Phase C, within the first 5 *ms* (Fig. 13b) and 10 *ms* after the fault occurrence the fault current has been diverted to the copper stabilizer layer (Fig. 13e).

For the load switching event (Fig. 13c) once the load is connected at Bus B, the SC starts to quench, as the current flows through the HTS layers of the three phases is higher than the critical current I_c. At $t = 15$ *ms*, the current started flowing through the copper stabilizer layers (Fig. 13e), as the HTS tapes have entered the highly resistive state. Although the SC quenches due to the presence of the external fault and the load switching event, as it can be seen from Fig. 13h and Fig. 13i, there is no tripping signal initiated for these scenarios. These results justify that the algorithms demonstrated high degree of stability during disturbances such as external faults and load switching events which cause the quenching of the SC.

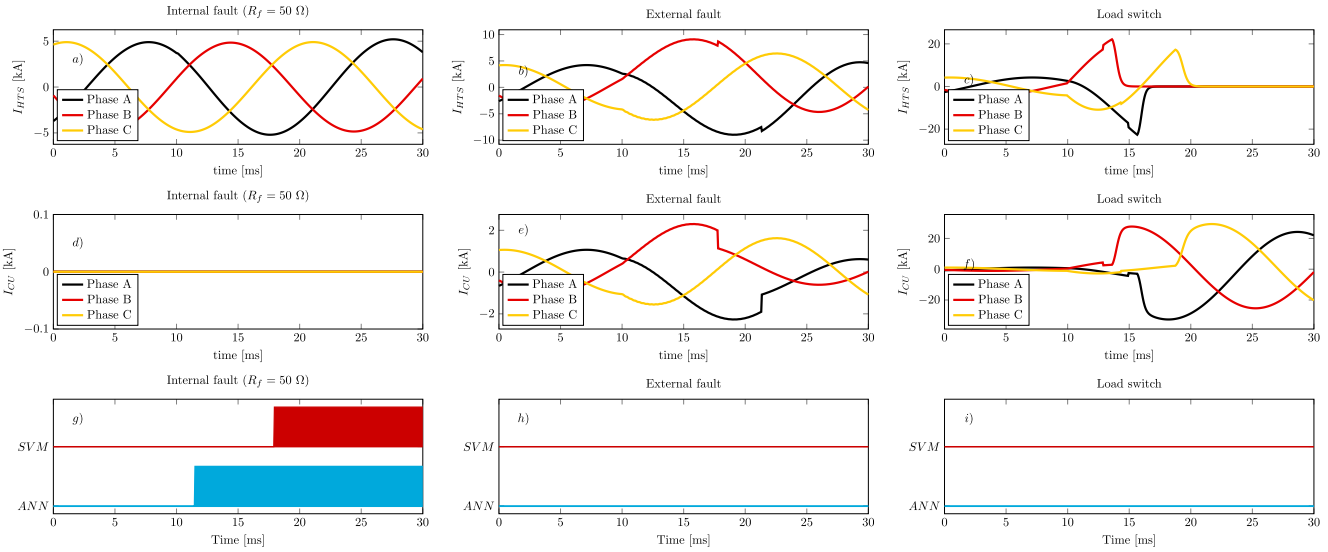

FIGURE 13. Simulation results for and ANN/SVM output for internal LLL-G fault with $R_f = 50\ \Omega$ at 90% of SC, external LLL-G solid fault and load switching event.

2) TIME PERFORMANCE OF BINARY CLASSIFIERS

The ANN and SVM classifiers were tested on 100 additional internal faults occurring at 5%, 15%, 25% and 95% of the SC's length for all types of faults. It shall be noted here that such locations were not part of the initial data set. Practically, this is the foreseen situation as any developed scheme is anticipated to accept inputs not necessarily similar to the trained cases. The results presented in Table 5, validate the effectiveness of the proposed algorithms, as both classifiers are capable of detecting the internal faults and initiating the corresponding tripping signal. In terms of the comparison between the two classifiers, it is noticeable that the ANN appears to initiate the tripping signal in shorter time scales.

Specifically, for the ANN classifier, the time required to produce a binary tripping signal lies within the range of 1.028 *ms* to 4.21 *ms*, with an average value of 1.49 *ms*. For the SVM classifier, a tripping signal can be initiated within the range of 7.57 *ms* to 8.21 *ms* with average a value of 7.92 *ms*. Therefore, the ANN classifier outperforms the SVM with respect to the speed operation. The time performance of the proposed algorithms were compared with the protection schemes for SCs proposed in [9], [10], [45], to demonstrate the superiority of both classifiers in terms of speed of operation, accounting for detection and discrimination.

D. EXECUTION OF THE PROPOSED SCHEME USING DIFFERENT HARDWARE CONFIGURATIONS

This section presents the feasibility of both ANN and SVM classifiers to provide fast and precise fault classification under different hardware configurations. The algorithm of both classifiers has been executed (for the same scenario) at different computers in order to evaluate their execution time in conjunction with anticipated hardware costs. Table 6 demonstrates the computer's hardware specifications.

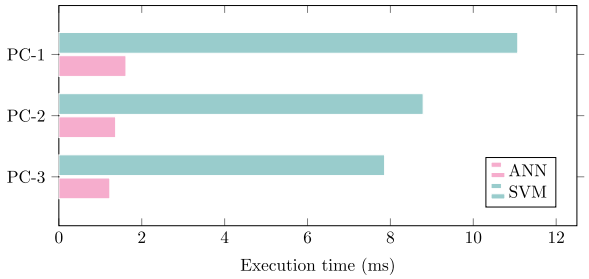

FIGURE 14. Execution time for ANN and SVM algorithms running in different computers.

Fig. 14 presents the execution time for ANN and SVM running at different computers. It can be seen that the execution time of ANN is relativity low, compared to that obtained for SVM. In overall, the execution time of both classifiers (considering all the anticipated delays introduced by the real implementation in Section III-E) is low, providing high level of confidence that the proposed protection algorithms is practical, considering realistic measurements and computation.

Another significant observation from this assessment, is that real-time implementation of the proposed scheme, can be achieved by relatively low-spec and cheap computers (i.e. PC-1) which could enable the wider adoption of the proposed scheme. Additionally, the utilization of high-spec computer (i.e. PC-3) could only result in very small improvement in terms of execution time, which can be considered negligible, especially in the case of ANN for which the execution time is practically very low.

V. CONCLUSION

In this paper, novel time-domain algorithms for protection of power systems which incorporate Superconducting Cables were proposed. A verified model of a SC with copper stabilizer layers was used to analyze the current and

TABLE 5. Time performance of ANN and SVM classifiers for previously unseen internal faults.

Internal fault			ANN	SVM	Internal fault			ANN	SVM
Location	Type	Rf [Ω]	Tripping time [ms]	Tripping time [ms]	Location	Type	Rf [Ω]	Tripping time [ms]	Tripping time [ms]
5%	LLL	0	1.507	7.692	25%	LLL	0	1.437	8.196
		2	1.443	7.982			2	1.468	7.838
		5	1.498	7.580			5	1.439	7.623
		15	1.477	8.077			15	1.521	7.968
		50	1.516	7.791			50	1.519	7.770
	LLLG	0	1.350	7.701		LLLG	0	1.445	8.006
		2	1.435	7.701			2	1.487	8.013
		5	1.028	7.933			5	1.030	7.839
		15	1.480	7.579			15	1.500	8.204
		50	1.764	7.792			50	1.501	7.938
	LL	0	1.441	8.133		LL	0	1.440	7.920
		2	1.425	7.890			2	1.450	7.620
		5	1.420	7.890			5	1.355	7.764
		15	1.520	8.100			15	1.473	8.077
		50	1.489	8.040			50	1.498	7.805
	LLG	0	1.476	8.037		LLG	0	1,461	8.033
		2	1.456	7.872			2	1.431	7.640
		5	1.471	8.147			5	1,460	8.009
		15	1.502	7.710			15	1,508	7.863
		50	1.499	8.190			50	1.470	7.850
	LG	0	1.438	7.780		LG	0	1.411	7.740
		2	1.440	8.210			2	1.462	8.059
		5	1.436	8.067			5	1.442	7.905
		15	1.513	8.099			15	1.488	8.088
		50	1.814	8.048			50	1.519	7.890
15%	LLL	0	1.455	7.877	95%	LLL	0	1.458	8.167
		2	1.442	8.038			2	1.436	7.605
		5	1.503	7.673			5	1.459	8.030
		15	1.506	8.048			15	1.469	8.050
		50	1.487	7.810			50	1.495	8.202
	LLLG	0	1.453	7.813		LLLG	0	1.470	8.080
		2	1.447	8.109			2	1.452	7.921
		5	1.448	8.005			5	1.445	8.048
		15	1.509	8.101			15	1.479	7.630
		50	1.471	7.786			50	1.487	8.077
	LL	0	1.427	7.630		LL	0	1.455	8.037
		2	1.473	7.771			2	1.456	7.812
		5	1.463	7.771			5	1.456	7.828
		15	1.469	8.161			15	1.484	7.980
		50	1.508	8.080			50	1.464	8.110
	LLG	0	4.210	7.761		LLG	0	1.460	7.640
		2	1.487	7.670			2	1.411	8.055
		5	1.790	8.000			5	1.440	7.875
		15	1.496	8.119			15	1.745	7.890
		50	1.496	7.799			50	1.494	8.190
	LG	0	1.498	7.810		LG	0	1.429	8.191
		2	1.468	8.208			2	1.435	8.179
		5	1.449	7.897			5	1.446	8.011
		15	1.480	7.690			15	1.493	7.680
		50	1.535	7.805			50	1.464	7.990

TABLE 6. PC specifications.

PC	Specifications
PC-1	i7-6500U, 2 cores, 4 threads, 2.4 GHz, 4 MB Cache
PC-2	R7 4800H, 8 cores, 16 threads, 2.9/4.2 GHz, 8 MB Cache, GPU NVIDIA RTX 2060
PC-3	i9-10980XE, 18 cores, 36 threads, 3/4.6 GHz, 24 MB Cache, GPU NVIDIA Quadro RTX 6000

voltage signatures during internal faults occurring on the SC, external faults occurring at adjacent lines and other disturbances. In an attempt to overcome the limitations of the conventional protection methods, the proposed algorithms utilize the principles of the SWT signal processing technique, to extract unique features from the resulting current and voltage signatures and ML-based classifiers (i.e. ANN and SVM) for fault detection and discrimination. The results revealed that the proposed algorithms can provide fast and discriminative protection for both solid and highly resistive internal faults at different fault positions along the SC. In terms of accuracy, results revealed that both classifiers are capable of classifying correctly the internal faults occurring on the SC, while remaining stable to external faults and other disturbances which cause the quenching of the SC. Specifically, results indicated that the accuracy of the proposed scheme reached values equal to 99.74% and 99.69% for ANN and SVM respectively.

The performance of proposed algorithms has been also scrutinised against its capability to run in real-time using a SIL testing environment, reflecting realistic digital infrastructures. Results demonstrated that both classifiers are capable of running correctly in real-time, highlighting the feasibility for a realistic implementation. In terms of the accuracy results and the prediction speed, ANN seems to outperform SVM, producing a decision in average time of 1.49 *ms*, while for the same decision the SVM would require average time of 7.92 *ms*. Further sensitivity analysis on hardware requirements, revealed that the proposed scheme can run in low-spec

computers, diminishing the needs for high costs, ultimately adopting its wider adoption for the protection of SCs.

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All results can be fully reproduced using the methods and data described in this paper and provided references.

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