# Analysis and Comparison of Series Resonant Converter With Embedded Filters for High Power Density DCX of Solid-State Transformer

**SHOTA OKUTANI**[ID], (Graduate Student Member, IEEE), **PIN-YU HUANG**[ID], (Member, IEEE), **RYO NISHIYAMA**, (Graduate Student Member, IEEE), **AND YUICHI KADO**[ID], (Member, IEEE)

Graduate School of Science and Technology, Kyoto Institute of Technology, Kyoto 606-8585, Japan

Corresponding author: Pin-Yu Huang (eins0620@gmail.com)

**ABSTRACT** A series resonant converter (SRC) operating as a DC transformer (DCX) is a candidate for the isolated bidirectional DC/DC converters of solid-state transformers (SSTs). However, the input/output current ripple of the SRC is relatively high, which requires bulky parallel capacitors and low-pass filters such as C/LC filters. These additional components reduce the power density. In addition, to operate an SRC as a DCX, a small resonant inductance is desired to reduce the voltage gain variation and achieve a faster transient response. To resolve these problems, a SRC with embedded filters is studied. Adding a clamping capacitor between split transformers not only significantly reduces current ripples and the harmonic components of the input/output currents but also connects resonant inductors in parallel to reduce the equivalent resonant inductance. In addition, dividing the resonant current into two split windings reduces the RMS current of the transformer. This paper presents a detailed analysis, a design methodology, and a comprehensive comparison with the conventional half-bridge CLLC converter with C/LC filters. 1-kW prototypes with a 600-V input voltage and 200-V output voltage demonstrate the superiority of the proposed converter; the second harmonic of the output current was significantly suppressed by 19.3 dB compared with that of the conventional converter with the same power density. The loss breakdown showed the proposed converter mitigated copper loss by 9.47% and eliminated the losses of the filter and DC-link capacitors. The prototype of the proposed converter had the highest efficiency of 95.4% at full-load among prototypes.

**INDEX TERMS** DC transformer, embedded filter, ripple-cancellation, high power density, series-resonant converter, soft-switching, solid-state transformer.

## I. INTRODUCTION

Solid-state transformers (SSTs) have attracted much attention in the past few decades and are considered to be alternative power-electronics technologies that can replace the line frequency transformers (LFTs) of middle-voltage (MV) applications in distribution systems, traction systems, renewable energy systems, shipboard distribution systems, and possibly even future electric aircraft systems [1]–[6].

A typical cascaded configuration for a single-phase AC/DC SST is shown in Fig. 1. The isolated bidirectional DC/DC converter (IBDC) is a core component of such a

The associate editor coordinating the review of this manuscript and approving it for publication was Vitor Monteiro[ID].

cascaded configuration. The basic concept of SST is reducing the volume/size by replacing LFTs with IBDCs. Therefore, an IBDC with a high-power density is required for an SST. There are mainly two candidates for the IBDC: a dual active bridge (DAB) converter [8]–[11] and a series resonant converter (SRC) [12]–[15]. The DAB features advanced voltage and power controllability and zero-voltage switching (ZVS) capability. However, the ZVS condition of a DAB depends on the load condition, and the ZVS fails especially under a light-load condition. In addition, the turn-off current of a DAB is the peak current; thus, the turn-off switching loss is large. The trapezoidal current of a DAB contains higher harmonic components, which cause a large amount of EMI. Furthermore, a closed-loop voltage control
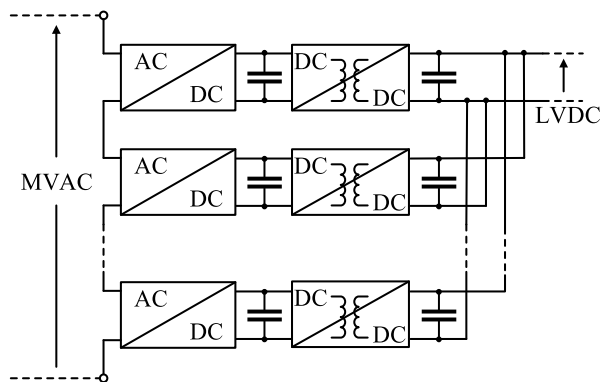
**FIGURE 1.** Typical cascaded configuration for single-phase AC/DC SST.

is required for a DAB [8]–[11], and an input voltage sharing control is also necessary in the AC/DC stage of a DAB-based cascaded SST [8], [9]. In comparison, the SRC features a load-independent ZVS and zero-current switching (ZCS) capability. The quasi-sinusoidal current of an SRC also leads to smaller harmonic components. In addition, the input/output voltage conversion gain can be set to unity without a closed-loop voltage control by operating the SRC at its resonant frequency. This operating mode is, therefore, regarded as a DC transformer (DCX) and is widely used in SST applications [12]–[15]. Although a DCX cannot regulate the output voltage, it is preferable for an input-series output-parallel configuration, as shown in Fig. 1, in terms of an automatic voltage-sharing capability without a closed-loop voltage control [14], [15]. For these reasons, an SRC-DCX is more suitable for the IBDC in a cascaded SST than a DAB.

In practice, however, the resonant components have some tolerance in mass production. In addition, the component values vary depending on the temperature and aging. Therefore, it is difficult to always operate the converter at the resonant frequency without a closed-loop voltage control. As a result, the automatic voltage-sharing capability will be lost. To solve the problem without a closed-loop voltage control, the ratio of magnetizing inductance $L_m$ to resonant inductance $L_r$, which is $L_m/L_r$, should be increased to planarize the voltage gain within the tolerance range of the resonant frequency. The magnetizing inductance $L_m$ is generally designed to satisfy the ZVS condition; therefore, a low resonant inductance design is desired in a DCX application [16]. From another perspective, the SRC in SSTs should work as if it were a real transformer, which means it requires a fast transient response. Small inductance is generally desired for a fast transient response. For these reasons, the resonant inductance of the SRC needs to be as small as possible.

Generally, the input/output current ripples of SRCs are high. Therefore, low-pass filters such as C or LC filters are required to reduce current ripple and harmonics [17]–[19]. When using a C filter, some of the high current ripple flows into a DC-link aluminum electrolytic capacitor. If a high current ripple flows into DC-link capacitors, the lifetime of the

capacitors becomes shorter. Therefore, a C filter with a large capacitance or bulky parallel DC-link capacitor configuration is required. When using an LC filter, an additional inductor is required. Both distributed and centralized filters are used for reducing the differential mode noise in a cascaded configuration [18], which means the number of filters increases as the number of cells increases. Thus, these low-pass filters decrease the power density of an SRC-SST.

Several methods have been proposed to solve this problem, including an interleaved converter [20]–[22], current-fed converter [23]–[26], and passive ripple-cancelling circuit [27]–[31]. Although an interleaved converter basically reduces current ripple, it has another current-imbalance problem when the resonant components have tolerance. In [20], an additional phase shift modulation is proposed. However, it is not suitable for the half-bridge topology, and it leads to more complex control. The voltage gains of the interleaved converter can be adjusted with an additional auxiliary circuit [21]; however, this adds weight and volume, which in turn results in decreasing the power density. The converter in [22] has an automatic current-balance characteristic by using the charge balance of flying capacitors. It solves the current-imbalance problem. However, the output current ripple cannot be suppressed. Current-fed converters are proposed in [23]–[26]. However, these converters require additional large filter inductors, which results in a low power density. The transient response of the current-fed converter is slower than that of voltage-fed converters due to the large filter inductance. To reduce the filter inductance, an interleaved technique is required, even with current-fed converters [25], [26]. Passive ripple-cancelling circuits are proposed in [27]–[31]. These circuits require additional magnetic components such as transformers or coupled inductors and capacitors. These auxiliary circuits can be used for cancelling ripple and cannot be used for transferring power. In addition, the circuits can cancel the current ripple of either the input or output currents. Therefore, they are not suitable for bidirectional applications.

To solve the above-mentioned problems, we previously proposed a ripple-cancellation technique for input/output currents [32], [33]. The proposed ripple-cancellation circuit just requires an additional clamping capacitor on each port for cancelling current ripple, which means the magnetic components play two roles, transferring power and cancelling ripple. In addition, the circuit has symmetry because the circuit can be used as both an inverter and rectifier. Thus, this proposed circuit can be easily applied to bidirectional converters. A bidirectional isolated ripple-cancellation converter based on this technique was proposed in [34], and a bidirectional built-in filter converter was proposed in [35]. On the basis of the converters in [34] and [35], converters for three-port and high-voltage applications were proposed in [36] and [37]. The converters in [34]–[37] are classified as being in the DAB family. However, the SRC-DCX is more suitable for SSTs than DAB, as mentioned above. Thus, a ripple-cancellation SRC-DCX converter was

proposed in [38]. According to [34]–[38], compared with conventional converters, ripple-cancellation converters do not require an input/output filter and can use a miniaturized EMI filter. In [34], [35], and [38], the operating principles of the ripple-cancellation converter and superiority against EMI are presented. However, a quantitative analysis of ripple-cancelling characteristics, the dynamics of the proposed converter, and a loss breakdown are not presented in detail. A detailed parameter design of the converter is not presented either, especially for the clamping capacitors. The power density may decrease when using clamping capacitors with a large capacitance. In addition, a comprehensive comparison with the conventional converters with filter circuits is not presented either.

This paper presents a detailed analysis of the proposed converter in [38] and a comprehensive comparison with the conventional SRC to verify the superiority of the proposed converter. An analysis of the proposed converter is shown in detail including a quantitative analysis of ripple-cancelling characteristics, component stress, and a dynamic model in section II. The tolerance of the resonant components is discussed in section III. Section IV explains the design methodology of the proposed converter. A loss breakdown among the proposed converter and conventional SRC with C/LC filter circuits is given in section V. A comprehensive comparison including voltage gain, harmonic components, power density, transient response, and efficiency are shown in section VI. Section VII is the conclusion.

## II. ANALYSIS OF PROPOSED CONVERTER

Circuit diagrams of a conventional half-bridge CLLC (HBCLLC) converter [39] and the proposed ripple-cancellation CLLC (RCCLLC) converter are shown in Fig. 2. The diagram of the proposed converter is the same as the bidirectional isolated ripple-cancellation converters proposed in [34] and [35]. However, the passive components work differently. Here, $L_1$, $L_2$, $L_3$, and $L_4$ are designed to be resonant inductors, and $C_1$, $C_2$, $C_3$, and $C_4$ are designed to be resonant capacitors. The proposed converter consists of two half-bridge switch pairs, $Q_1$-$Q_2$ and $Q_3$-$Q_4$, a split four-winding transformer, $S_1$, $S_2$, $S_3$, and $S_4$, the magnetizing inductance of the transformer, $L_m$, resonant inductors, $L_1$, $L_2$, $L_3$, and $L_4$, resonant capacitors, $C_1$, $C_2$, $C_3$, and $C_4$, clamping capacitors, $C_a$ and $C_b$, and two DC-link capacitors, $C_i$ and $C_o$. In DCX applications, no voltage regulation is required; the proposed converter can operate at a fixed switching frequency with a complementary 50% duty ratio. The switching frequency is set to a frequency slightly lower than the resonant frequency because the switching period equals the resonant conduction period plus deadtime period to achieve high efficiency operation [12]. In powering mode, the switch pair on the primary side, $Q_1$-$Q_2$, is complementarily operated as an inverter. The switch pair on the secondary side, $Q_3$-$Q_4$, is operated as a rectifier. In regenerating mode, the pair on the secondary side is complementarily operated as an inverter. The pair on the primary side is operated as a rectifier. Several assumptions are
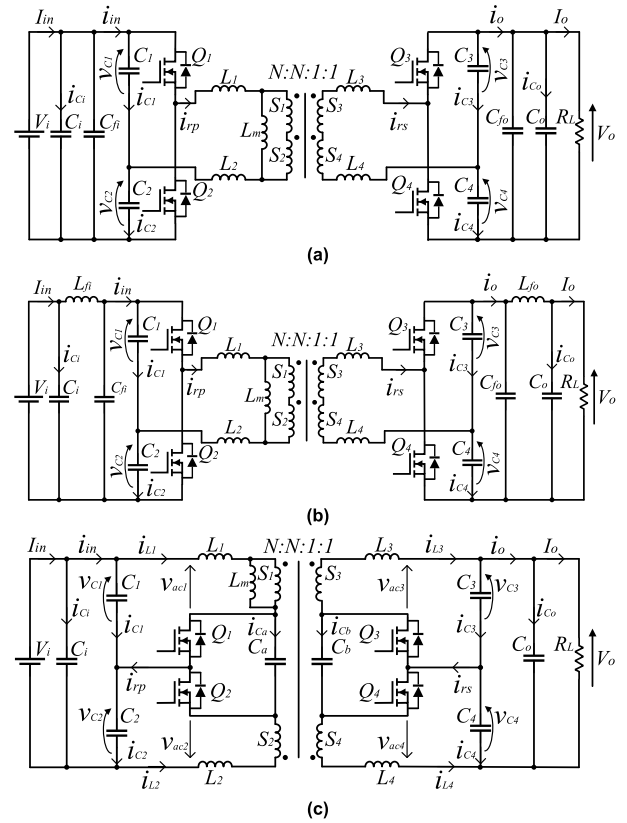


**FIGURE 2.** Circuit diagram of conventional half-bridge CLLC converter (a) with C filters, (b) with LC filters, and (c) proposed RCCLLC converter.

made to simplify the analysis. The semiconductors are ideal. The clamping capacitors, $C_a$ and $C_b$, and DC-link capacitors, $C_i$ and $C_o$, are large enough to not take part in resonance and are considered to be constant voltage sources.

### A. OPERATING PRINCIPLE
Fig. 3 shows the key waveforms of the proposed converter. There are six operating modes in one switching cycle. In modes 1 and 4, the converter operates resonantly and transfers power, while in modes 2 and 5, which are discontinuous current modes, the converter does not transfer power. Modes 3 and 6 are deadtime durations in which ZVS is achieved. Because the operating modes are similar, only the operating principles of the half-switching cycle during the powering operation are described. Fig. 4 shows the operating modes of the proposed converter during the cycle. Each operation stage is described in detail as follows.

*Mode 1*$[t_0-t_1]$ : As shown in Fig. 4(a), $Q_1$ is turned on with ZVS at $t_0$. In this mode, power is transferred from the primary to the secondary side through the transformer. The body diode of the $Q_3$ is conducted. The voltage across the transformer is clamped by $NV_o/2$. Therefore, the current of $L_m$ increases linearly. Resonant inductors $L_1$, $L_2$, $L_3$, and $L_4$ and resonant capacitors $C_1$, $C_2$, $C_3$, and $C_4$ participate in the resonant operation. During this mode, the voltages across $Q_2$ and $Q_4$ are clamped by $v_{Ca}(t)$ and $v_{Cb}(t)$, respectively. Because of
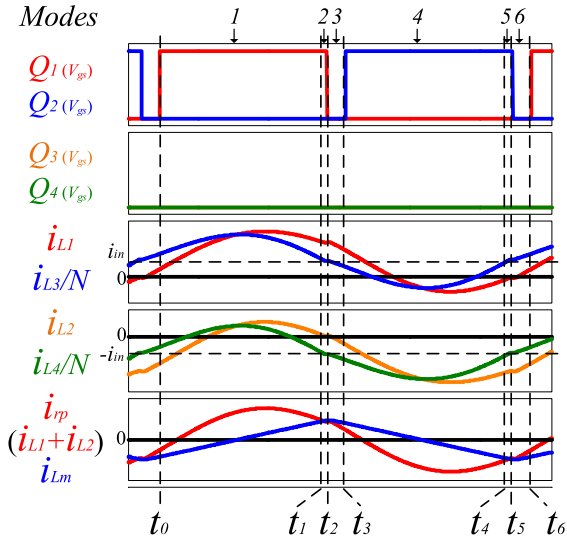
**FIGURE 3. Key waveforms of proposed converter.**



**FIGURE 4.** Operating modes of proposed converter: (a) Mode 1 [$t_0$-$t_1$], (b) Mode 2 [$t_1$-$t_2$], and (c) Mode 3 [$t_2$-$t_3$].

the reverse polarity of the transformer on each side, $S_1$-$S_2$ and $S_3$-$S_4$, the average voltages across $C_a$ and $C_b$ are the same as the input and output voltages, $V_i$ and $V_o$, respectively. Assuming $C_a$ and $C_b$ are large enough, the voltage stresses of $Q_2$ and $Q_4$ are represented in (1) and (2), respectively.
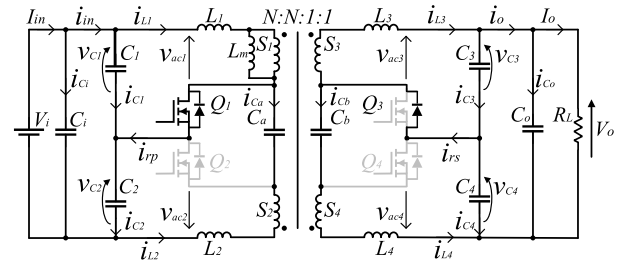
$$V_{ds\_Q2} = v_{Ca}(t) = V_i \qquad (1)$$
$$V_{ds\_Q4} = v_{Cb}(t) = V_o \qquad (2)$$

*Mode 2[$t_1$-$t_2$]:* As shown in Fig. 4(b), this mode starts when the magnetizing current reaches the resonant current $i_{rp}(t)$, which is the sum of the inductor currents $i_{L1}(t)$ and $i_{L2}(t)$. $Q_1$ is still conducted. When the switch current $i_{Q3}(t)$ is equal to zero, $Q_3$ is turned off. Thus, $Q_3$ is turned off with ZCS. In this mode, power is not transferred from the primary to the secondary side. Therefore, resonant current $i_{rp}(t)$ is equal to the magnetizing current. Because of the reverse polarity of the secondary-side transformer, $S_3$-$S_4$, the average voltage across $C_b$ is the same as the output voltage. The output current is mainly provided by $C_b$. Thus, $i_{c3}(t)$ and $i_{c4}(t)$ are nearly zero.
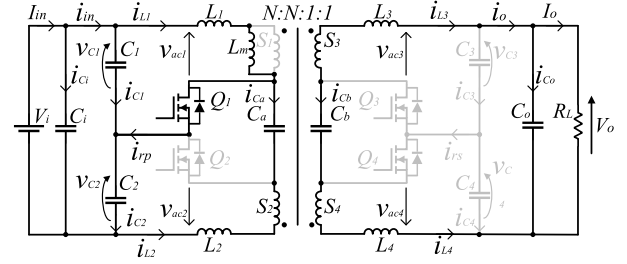
*Mode 3[$t_2$-$t_3$]:* This mode is a deadtime duration. As shown in Fig. 4(c), $Q_1$ is turned off with a low turn-off current. The current in $Q_1$ commutates through the body diode of $Q_2$; thus, it turns $Q_2$ on with ZVS at $t_3$. In this interval, $Q_4$ is conducted to transfer power from the primary to the secondary side. The voltage across the transformer is also clamped by $-NV_o/2$. During this mode, voltages across $Q_1$ and $Q_3$ are clamped by $v_{Ca}(t)$ and $v_{Cb}(t)$, respectively. Thus, the voltage stresses of $Q_1$ and $Q_3$ are similarly $V_i$ and $V_o$, respectively.

The intervals of Mode 2 and 3 and the magnetizing current in $L_m$ are ignored in the following time-domain analysis for simplification. The circuit equations in Mode 1 are derived by Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL) in (3)-(8).
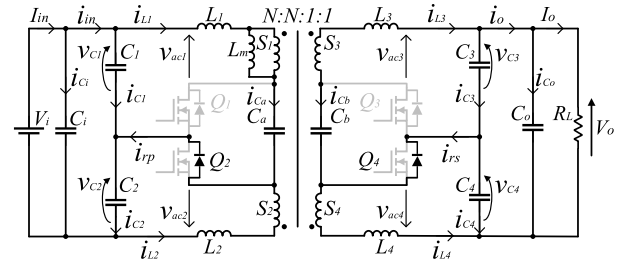
$$v_{C1}(t) - Nv_{C3}(t) = L_1\frac{di_{L1}(t)}{dt} + NL_3\frac{di_{L3}(t)}{dt} \qquad (3)$$

$$V_i = v_{C1}(t) + v_{C2}(t) = L_1\frac{di_{L1}(t)}{dt}$$
$$- L_2\frac{di_{L2}(t)}{dt} + v_{Ca}(t) \qquad (4)$$

$$V_o = v_{C3}(t) + v_{C4}(t) = -L_3\frac{di_{L3}(t)}{dt}$$
$$+ L_4\frac{di_{L4}(t)}{dt} + v_{Cb}(t) \qquad (5)$$

$$i_{rp}(t) = i_{L1}(t) + i_{L2}(t) = -i_{C1}(t) + i_{C2}(t) \qquad (6)$$

$$i_{rs}(t) = i_{L3}(t) + i_{L4}(t) = i_{C3}(t) - i_{C4}(t) \qquad (7)$$

$$Ni_{rp}(t) = i_{rs}(t) \qquad (8)$$

Since the clamping capacitors, $C_a$ and $C_b$, are assumed to be large enough, they can be considered as constant voltage sources $V_i$ and $V_o$, respectively. As a result, (4) and (5) are transformed to (9) and (10), respectively.

$$L_1\frac{di_{L1}(t)}{dt} = L_2\frac{di_{L2}(t)}{dt} \qquad (9)$$

$$L_3\frac{di_{L3}(t)}{dt} = L_4\frac{di_{L4}(t)}{dt} \qquad (10)$$

By substituting (6) into (9), the differentiation of resonant current $i_{rp}(t)$ is derived in (11).

$$\frac{di_{rp}(t)}{dt} = \frac{L_1 + L_2}{L_2} \frac{di_{L1}(t)}{dt} \tag{11}$$

Analogously, the differentiation of resonant current $i_{rs}(t)$ is derived in (12) by substituting (7) into (10).

$$\frac{di_{rs}(t)}{dt} = \frac{L_3 + L_4}{L_4} \frac{di_{L3}(t)}{dt} \tag{12}$$

By differentiating (4) and (5), the relationships of $i_{C1}(t)$ and $i_{c2}(t)$, and $i_{C3}(t)$ and $i_{C4}(t)$ are derived in (13) and (14), respectively.

$$\frac{1}{C_1} i_{C1}(t) + \frac{1}{C_2} i_{C2}(t) = 0 \tag{13}$$

$$\frac{1}{C_3} i_{C3}(t) + \frac{1}{C_4} i_{C4}(t) = 0 \tag{14}$$

By substituting (6) into (13), $i_{C1}(t)$ is represented in (15).

$$i_{C1}(t) = -\frac{C_1}{C_1 + C_2} i_{rp}(t) \tag{15}$$

Analogously, $i_{C3}(t)$ is represented in (16) by substituting (7) into (14).

$$i_{C3}(t) = \frac{C_3}{C_3 + C_4} i_{rs}(t) \tag{16}$$

By applying (8), (11), (12), (15), and (16) to (3), a time-domain equation for resonant current $i_{rp}(t)$ is derived in (17).

$$v_{C1}(t_0) - N v_{C3}(t_0) = L_r \frac{di_{rp}(t)}{dt} + \frac{1}{C_r} \int_{t_0}^{t} i_{rp}(t) \, d\tau, \tag{17}$$

where

$$L_r = (L_1 // L_2) + N^2 (L_3 // L_4),$$
$$C_r = (C_1 + C_2) // \frac{1}{N^2} (C_3 + C_4). \tag{18}$$

Here, $v_{C1}(t_0)$ and $v_{C3}(t_0)$ are initial voltages of $C_1$ and $C_3$ at $t_0$. The equivalent resonant frequency of the resonant tank is derived in (19).

$$f_r = \frac{1}{2\pi \sqrt{L_r C_r}} \tag{19}$$

The solution for (17) is expressed in (20).

$$i_{rp}(t) = \sqrt{2} I_{rp} \sin(2\pi f_r t) \tag{20}$$

Here, $I_{rp}$ is the RMS value of $i_{rp}(t)$. By applying KCL, $i_{L1}(t)$ and $i_{L2}(t)$ are derived in (21) and (22), respectively.

$$i_{L1}(t) = -i_{Ci}(t) - i_{C1}(t) + \frac{V_o}{NR_L} \tag{21}$$

$$i_{L2}(t) = i_{Ci}(t) + i_{C2}(t) - \frac{V_o}{NR_L} \tag{22}$$

Note that (21) and (22) hold independently of the operating modes. Currents through capacitors should be purely AC waveforms due to the capacitors' charge balance in the steady state. As a result, inductor currents consist of the two AC currents and a DC bias current that is the same as the average input current. By using (11) and (20), the AC component of the $i_{L1}(t)$ can be represented in (23).

$$i_{L1\_AC}(t) = \frac{\sqrt{2} L_2}{L_1 + L_2} I_{rp} \sin(2\pi f_r t) \tag{23}$$

By replacing the AC component of $i_{L1}(t)$ in (21) with (23), $i_{L1}(t)$ is represented in (24).

$$i_{L1}(t) = \frac{\sqrt{2} L_2}{L_1 + L_2} I_{rp} \sin(2\pi f_r t) + \frac{V_o}{NR_L} \tag{24}$$

Analogously, $i_{L2}(t)$ is derived in (25).

$$i_{L2}(t) = \frac{\sqrt{2} L_1}{L_1 + L_2} I_{rp} \sin(2\pi f_r t) - \frac{V_o}{NR_L} \tag{25}$$

To determine $I_{rp}$ in (24) and (25), the charge balance of $C_a$ during one switching cycle can be applied.

$$\frac{1}{C_a} \int_{t_0}^{t_0 + T_{sw}} i_{Ca}(t)$$
$$= -\frac{1}{C_a} \int_{t_0}^{t_0 + T_{sw}/2} i_{L2}(t) \, dt + \frac{1}{C_a} \int_{t_0 + T_{sw}/2}^{t_0 + T_{sw}} i_{L1}(t) \, dt$$
$$= \frac{T_{sw}}{C_a} \left( \frac{V_o}{NR_L} - \frac{\sqrt{2}}{\pi} I_{rp} \right) = 0 \tag{26}$$

By substituting (26) into (20), $i_{rp}(t)$ can be represented in (27).

$$i_{rp}(t) = \frac{\pi V_o}{NR_L} \sin(2\pi f_r t) \tag{27}$$

Note that the resonant current of the proposed converter is the same as that of the half-bridge SRC in [40]. Thus, the current stress of the semiconductors and voltage stress of the resonant capacitors in the proposed converter are the same as those of the conventional HBCLLC converter. $i_{L3}(t)$ and $i_{L4}(t)$ can be derived in (28) and (29) in the same manner.

$$i_{L3}(t) = \frac{L_4}{L_3 + L_4} i_{rs}(t) + \frac{V_o}{R_L} \tag{28}$$

$$i_{L4}(t) = \frac{L_3}{L_3 + L_4} i_{rs}(t) - \frac{V_o}{R_L} \tag{29}$$

As shown in (24), (25), (28), and (29), the resonant current is divided into two inductor currents on each side. The inductor currents consist of AC and DC components. Assuming that $L_1 = L_2$ and $L_3 = L_4$ for simple calculation, the RMS values of the inductor currents are derived in (30) and (31).

$$I_{L1} = I_{L2} = \frac{V_o}{NR_L} \sqrt{1 + \frac{\pi^2}{8}} < \frac{\pi V_o}{\sqrt{2} NR_L} = I_{rp} \tag{30}$$

$$I_{L3} = I_{L4} = \frac{V_o}{R_L} \sqrt{1 + \frac{\pi^2}{8}} < \frac{\pi V_o}{\sqrt{2} R_L} = NI_{rp} \tag{31}$$

Equations (30) and (31) indicate that the RMS values of the inductor currents of the proposed converter are smaller than

those of the conventional converter, which reduces the copper loss. A detailed loss breakdown is given in section V. In accordance with this analysis, a comparison of the component stresses between the conventional HBCLLC converter and the proposed RCCLLC converter is summarized in Table 1.

TABLE 1. Comparison of component stress.

| Topology | HBCLLC | RCCLLC |
|---|---|---|
| Pri. switch voltage stress | $V_i$ | |
| Sec. switch voltage stress | $V_o$ | |
| Pri. switch current stress | $I_{rp} = \dfrac{\pi V_o}{\sqrt{2} N R_L}$ | |
| Sec. switch current stress | $I_{rs} = \dfrac{\pi V_o}{\sqrt{2} R_L}$ | |
| Pri. inductor current stress | $I_{L1} = I_{L2} = \dfrac{\pi V_o}{\sqrt{2} N R_L}$ | $I_{L1} = I_{L2} = \dfrac{V_o}{N R_L}\sqrt{1+\dfrac{\pi^2}{8}}$ |
| Sec. inductor current stress | $I_{L3} = I_{L4} = \dfrac{\pi V_o}{\sqrt{2} R_L}$ | $I_{L3} = I_{L4} = \dfrac{V_o}{R_L}\sqrt{1+\dfrac{\pi^2}{8}}$ |
| Pri. capacitor voltage stress | $V_{C1} = V_{C2} = \dfrac{V_i}{2} + \dfrac{V_o}{4 N R_L f_r C_p}$ , $\left(C_p = C_1 = C_2\right)$ | |
| Sec. capacitor voltage stress | $V_{C3} = V_{C4} = \dfrac{V_o}{2} + \dfrac{V_o}{4 R_L f_r C_s}$ , $\left(C_s = C_3 = C_4\right)$ | |

## B. GAIN CHARACTERISTICS

To identify the gain characteristics of the proposed converter, a fundamental harmonic approximation (FHA) analysis is done. The resonant components are assumed to be $L_1 = L_2 = L_p$, $C_1 = C_2 = C_p$, $L_3 = L_4 = L_s$, and $C_3 = C_4 = C_s$ to simplify the analysis. The equivalent circuit of the proposed converter is shown in Fig. 5. Here, the voltages $v_{ac1}(t)$, $v_{ac2}(t)$, $v_{ac3}(t)$, and $v_{ac4}(t)$ are represented in (32)-(35).

$$v_{ac1}(t) = \begin{cases} v_{C1}(t) & (t_0 \le t \le t_0 + T_{sw}/2) \\ v_{C1}(t) - v_{Ca}(t) & (t_0 + T_{sw}/2 \le t \le t_0 + T_{sw}), \end{cases}$$
(32)

$$v_{ac2}(t) = \begin{cases} v_{Ca}(t) - v_{C2}(t) & (t_0 \le t \le t_0 + T_{sw}/2) \\ -v_{C2}(t) & (t_0 + T_{sw}/2 \le t \le t_0 + T_{sw}), \end{cases}$$
(33)

$$v_{ac3}(t) = \begin{cases} v_{C3}(t) & (t_0 \le t \le t_0 + T_{sw}/2) \\ v_{C3}(t) - v_{Cb}(t) & (t_0 + T_{sw}/2 \le t \le t_0 + T_{sw}), \end{cases}$$
(34)

$$v_{ac4}(t) = \begin{cases} v_{Cb}(t) - v_{C4}(t) & (t_0 \le t \le t_0 + T_{sw}/2) \\ -v_{C4}(t) & (t_0 + T_{sw}/2 \le t \le t_0 + T_{sw}). \end{cases}$$
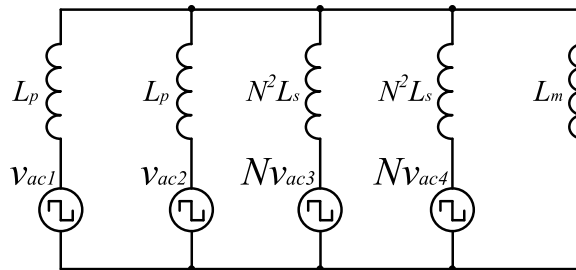(35)



FIGURE 5. Equivalent circuit of proposed converter.

Assuming that $C_a$ and $C_b$ are large enough, $v_{ca}(t)$ and $v_{cb}(t)$ can be considered as constant voltage sources $V_i$ and $V_o$, respectively. Thus, equations (36) and (37) are derived.

$$v_{ac1}(t) = v_{ac2}(t)$$
(36)

$$v_{ac3}(t) = v_{ac4}(t)$$
(37)

Because $v_{ac1}(t)$ equals $v_{ac2}(t)$, and $v_{ac3}(t)$ equals $v_{ac4}(t)$, the resonant inductors are connected in parallel. The configuration of the resonant capacitor is a general split capacitor one. The FHA model of the conventional converter [39] and the proposed converter are derived as shown in Fig. 6. Using these models, the transfer functions of the resonant tanks can be derived. Since the difference between two models is only the coefficient of the resonant inductance, the transfer functions can be summarized into one. Due to their symmetric resonant tank, the transfer function of the resonant tank $H_r(s)$ in powering mode is described only. Transfer function $H_r(s)$ is represented in (38).

$$H_r(s) = \frac{v_o(s)}{v_i(s)} = \frac{sL_m \parallel N^2 Z_o(s)}{Z_{in}(s)} \frac{2R_L}{\pi^2 Z_o(s)},$$
(38)

where

$$Z_{in}(s) = smL_p + \frac{1}{s2C_p} + sL_m \parallel N^2 Z_o(s),$$

$$Z_o(s) = smL_s + \frac{1}{s2C_s} + \frac{2}{\pi^2}R_L,$$

$$m = \begin{cases} 1/2 & (RCCLLC) \\ 2 & (HBCLLC). \end{cases}$$
(39)

Here, $Z_{in}(s)$ is the input impedance of the resonant tank, $Z_o(s)$ is the impedance of the output stage, and $m$ is the coefficient of the resonant inductance. By using (38) and (39), the voltage gains of the converters can be derived in terms of the normalized frequency $f_n$, (40) as shown at the bottom of the page, where

$$k = \frac{L_m}{L_p}, \quad a = \frac{N^2 L_s}{L_p}, \quad b = \frac{C_s}{N^2 C_p}, \quad f_n = \frac{f_{sw}}{f_r},$$

$$|H_r(f_n)| = \frac{1}{\sqrt{\left(\frac{m}{k} + 1 - \frac{m}{kf_n^2}\right)^2 + (mQ)^2 \left\{f_n\left(1 + \frac{am}{k} + a\right) - \frac{1}{f_n}\left(\frac{am}{k} + 1 + \frac{1}{b} + \frac{m}{bk}\right) + \frac{1}{f_n^3}\frac{m}{kb}\right\}^2}}$$
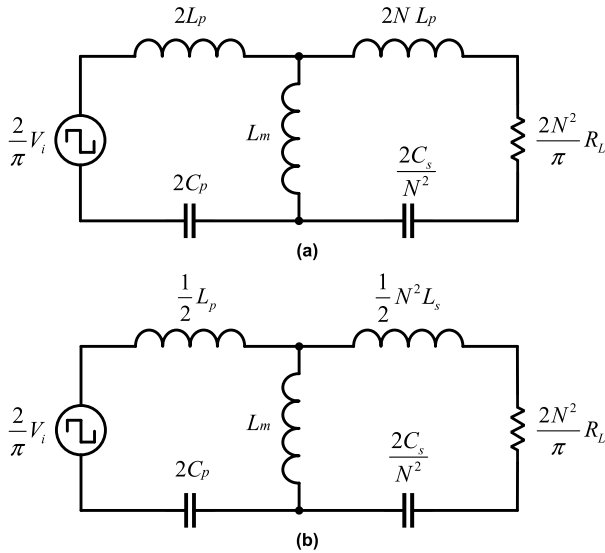(40)

**FIGURE 6.** FHA model of (a) conventional converter and (b) proposed converter.

$$f_r = \frac{1}{2\pi \sqrt{2mL_pC_p}},$$

$$Q = \frac{\pi^2}{2N^2R_L}\sqrt{\frac{L_p}{2mC_p}} = \frac{\pi^3 L_p f_r}{N^2 R_L}. \tag{41}$$

Here, $k$ and $Q$ are defined for comparison when utilizing the same resonant inductance. Fig. 7 shows the voltage gains of the proposed and conventional converters when $a = 1$, $b = 1$, $k = 5$, and $Q = 0.3$. Comparing between these two models, the gain deviation of the proposed converter is smaller than that of the conventional converter because the equivalent resonant inductance of the proposed converter is four times smaller than that of the conventional converter. To design the resonant converter as a DCX, a smaller resonant inductance is desired for planarizing the voltage gain and fast transient response as mentioned. Therefore, the proposed converter is more suitable for a DCX.
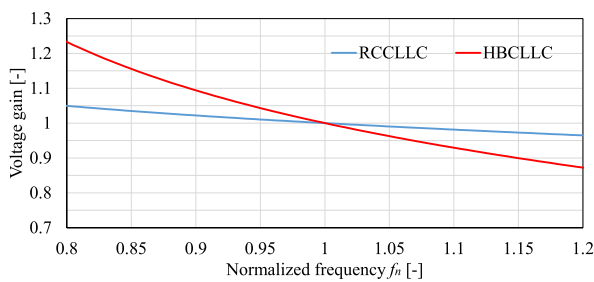


**FIGURE 7.** Voltage gains of conventional converter and proposed converter.

## C. RIPPLE-CANCELLING CHARACTERISTICS

In contrast to the conventional resonant converter, the input/output capacitors of the proposed converter have voltage and current ripple-cancelling characteristics. Because of
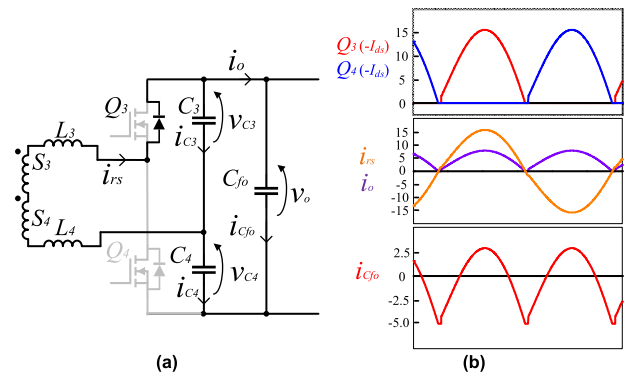


**FIGURE 8.** Operation of conventional converter during positive half-cycle: (a) current directions and voltage polarities on secondary side, (b) key waveforms of output current ripple.
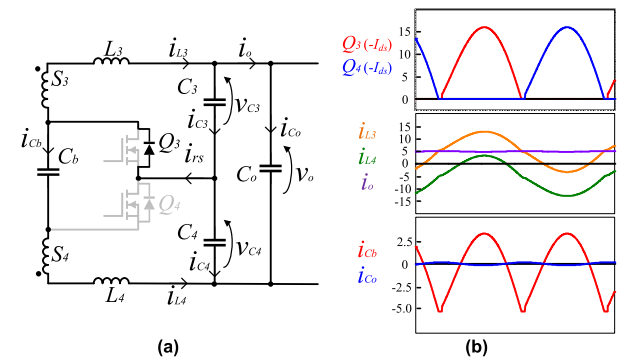


**FIGURE 9.** Operation of proposed converter during positive half-cycle: (a) current directions and voltage polarities on secondary side, (b) key waveforms of output current ripple.

their analogous operations, the ripple-cancelling characteristics on the secondary side during a positive half-cycle is described only. Fig. 8 shows the current directions, voltage polarities, and key waveforms of the current ripple of the conventional converter. Fig. 9 shows those of the proposed converter. The circuit equations of the conventional converter are derived by KVL in (42)-(44) based on Fig. 8(a).

$$\frac{1}{C_3}\int i_{C3}(t)\,dt + v_{C3}(0) + \frac{1}{C_4}\int i_{C4}(t)\,dt + v_{C4}(0)$$
$$= v_o(t) \tag{42}$$

$$i_{C3}(t) - i_{C4}(t) = i_{rs}(t) \tag{43}$$

$$i_o(t) = -i_{C4}(t) \tag{44}$$

Here, $v_{C3}(0)$ and $v_{C4}(0)$ are the initial values of the voltages of $C_3$ and $C_4$, respectively. When capacitor $C_{fo}$ is assumed to be large enough and considered as constant voltage source $V_o$, equation (45) holds by differentiating (42).

$$\frac{1}{C_3}i_{C3}(t) + \frac{1}{C_4}i_{C4}(t) = 0 \tag{45}$$

By (43)-(45), the output current $i_o(t)$ and the current ripple $i_{Cfo}(t)$ are represented in (46).

$$i_o(t) = \frac{C_4}{C_3 + C_4}i_{rs}(t)$$

$$i_{Cfo}(t) = \frac{C_4}{C_3 + C_4} i_{rs}(t) - \frac{V_o}{R_L} \quad (46)$$

Generally, $C_3$ and $C_4$ are designed to be the same; thus, the output current is half of the resonant current, and the output current ripple, whose amplitude is also half of the resonant current, flows into the filter capacitor in the conventional converter as shown in Fig. 8(b). The output current of the proposed converter and the output current ripple are derived in (47) by (16) and (29).

$$i_o(t) = i_{L3}(t) - i_{C3}(t) = \frac{L_4 C_4 - L_3 C_3}{(L_3 + L_4)(C_3 + C_4)} i_{rs}(t) + \frac{V_o}{R_L}$$

$$i_{Co}(t) = \frac{L_4 C_4 - L_3 C_3}{(L_3 + L_4)(C_3 + C_4)} i_{rs}(t) \quad (47)$$

As shown in (47), the output current ripple will be zero when $L_3 C_3 = L_4 C_4$. Practically, the resonant components should be designed to be identical for each port. Thus, the current ripple will be cancelled in the proposed converter as shown in Fig. 9(b).

According to the current ripple-cancelling characteristics of both input/output capacitors, the voltage ripple on both capacitors is also cancelled. Although the current ripples of the capacitors are moved to the clamping capacitors as shown in Fig. 9(b), film or ceramic capacitors with a small capacitance can be used as clamping capacitors. Because the output voltage ripple is cancelled, using a small clamping capacitance does not cause any voltage variations in the input/output. Therefore, the propagation noise is suppressed by this feature. In addition, the design of the input/output capacitors needs to consider only the energy transfer during the transient operation of the converter because input/output capacitors are free from large current ripples.

### D. EMBEDDED π FILTER

On the basis of the average DC current paths, the proposed converter has embedded π filters at both the input and output. Fig. 10(a) shows the average DC current paths of the proposed



**FIGURE 10.** Derivation of embedded π filter: (a) average DC current paths and (b) equivalent average switching model.

converter. In the steady state, the average current through the capacitor is zero. Accordingly, the mid-terminal average current is zero. Thus, the mid-terminal is open in the average switch model. As a result, switch pairs $Q_1$-$Q_2$ and $Q_3$-$Q_4$ can be replaced by rectifier current sources $i_{rect}$ and $Ni_{rect}$ as shown in Fig. 10(b). The rectifier current sources are in parallel to the clamping capacitors. Consequently, the clamping capacitor, resonant inductors, resonant capacitors, and DC-link capacitor compose a π filter to suppress differential mode noise on each side. The resonant inductors work for not only transferring power but also for filtering current ripple in this converter. Thus, an additional filter inductor is no longer necessary.

### E. DYNAMIC MODEL

Since voltage regulation is implemented in the part of the AC/DC converter in the SST, the dynamics of the proposed converter with open-loop control is of high interest because its output voltage is a control target of the part of the AC/DC converter. The proposed converter has the characteristics of the SRC and the embedded π filter as discussed in the previous sections. Therefore, the dynamics of the proposed converter is derived by combining two characteristics. The dynamics of the SRC has been accurately modeled by a passive equivalent circuit [41]. The equivalent circuit is derived by converting the total resonant inductor and total parasitic resistance to DC equivalent ones. The DC equivalent resistor $R_{dc}$ is derived on the basis of the energy consumption of the resistor. The energy consumption of the total resistor should be the same as the energy consumption of the DC equivalent resistor. Therefore, the relationship is derived from (48).

$$i_{dc}{}^2 R_{dc} = i_{rms}{}^2 R_{total} \Rightarrow R_{dc} = \beta^2 R_{total} \text{ with } \beta^2 = \left(\frac{i_{rms}}{i_{dc}}\right)^2 \quad (48)$$

The DC equivalent inductor $L_{dc}$ is derived on the basis of the stored energy of the inductor. The total stored energy of the resonant inductor should be the same as the stored energy of the DC equivalent inductor. Therefore, the relationship is derived from (49).

$$\frac{1}{2} L_{total} i_{peak}{}^2 = \frac{1}{2} L_{dc} i_{dc}{}^2 \Rightarrow L_{dc} = \alpha^2 L_{total} \text{ with } \alpha^2 = \left(\frac{i_{peak}}{i_{dc}}\right)^2 \quad (49)$$

Here, $R_{total}$ is the total parasitic resistor, $L_{total}$ is the total resonant inductor, $i_{rms}$ is the RMS current of the resonant current, $i_{peak}$ is the peak current of the resonant current, and $i_{dc}$ is the half-cycle average value of the resonant current.

By using this technique, the characteristics of the proposed converter as an SRC are derived as the DC equivalent circuit shown in Fig. 11(a). Here, $V_F$ is the equivalent voltage drop in rectifier diodes, i.e., $V_F = 2V_{diode}$ in the considered circuit. Fig. 11(b) shows the embedded π filter when considering parasitic resistors. Here, $R_{Lp}$ and $R_{Ls}$ are equivalent series resistors (ESRs) of each winding on the primary-side transformer and on the secondary-side transformer. $R_{Ci}$ and $R_{Co}$ are ESRs
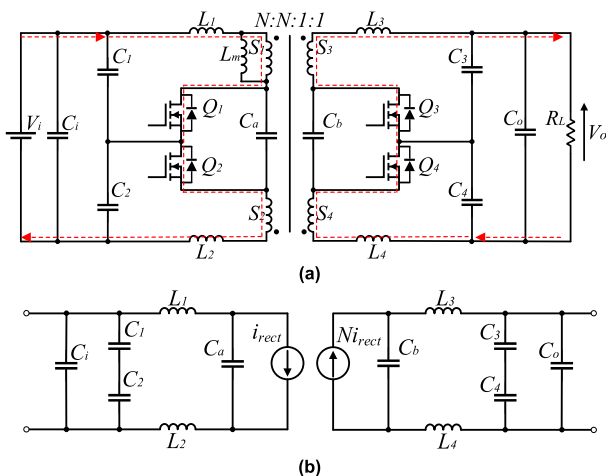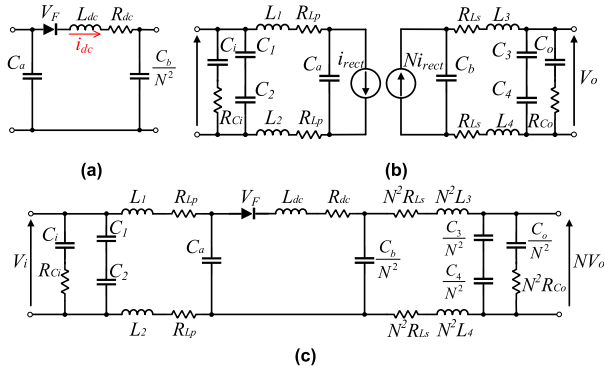
**FIGURE 11.** Dynamic model of proposed converter: (a) SRC characteristics, (b) embedded $\pi$ filter characteristics. (c) two combined characteristics.
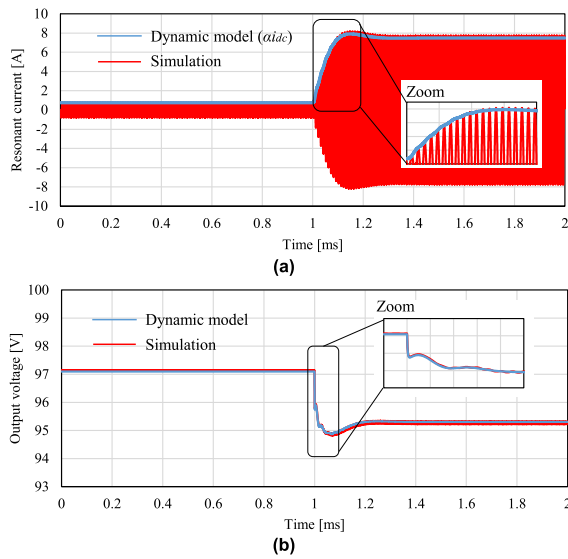


**FIGURE 12.** Simulation and dynamic model results of transient response of proposed converter: (a) resonant current and (b) output voltage.

**TABLE 2.** Simulation parameters.

| Parameters | Value |
|---|---|
| Input voltage $V_i$ | 300 V |
| Output voltage $V_o$ | 100 V |
| Turns ratio $N$ | 3 |
| Switching frequency $f_{sw}$ | 100 kHz |
| Resonant inductors $L_1, L_2, L_3, L_4$ | 30 µH, 30 µH, 3.3µH, 3.3µH |
| Resonant capacitors $C_1, C_2, C_3, C_4$ | 83.5 nF, 83.5 nF, 750 nF, 750 nF |
| Clamping capacitors $C_a, C_b$ | 220 nF, 2.2 µF |
| DC-link capacitors $C_i, C_o$ | 10µF, 40 µF |
| Load step $R_L$ | 400 Ω → 40 Ω |
| ESR of input capacitor $R_{Ci}$ | 2.6 Ω |
| ESR of output capacitor $R_{Co}$ | 660 mΩ |
| ESR of each winding on primary-side transformer $R_{Lp}$ | 520 mΩ |
| ESR of each winding on secondary-side transformer $R_{Ls}$ | 97 mΩ |
| On-resistance of switch $R_{on}$ | 65 mΩ |
| Equivalent voltage drop $V_F$ | 2.7 V |
| Total equivalent inductance $L_{total}$ | 30 µH |
| Total parasitic resistance $R_{total}$ | 762 mΩ |
| Coefficient $\alpha$ | $\pi$ |
| Coefficient $\beta$ | $\pi/\sqrt{2}$ |

are connected in parallel. Here, $R_{on}$ is the on-resistance of the switch. The copper loss derived by the DC bias current through the inductor can be represented by $R_{Lp}$ and $N^2 R_{Ls}$ in the embedded $\pi$ filter part. The proposed model coincides with the actual circuit simulation well during both steady state and transient period as shown in Fig. 12.

## III. TOLERANCE OF RESONANT COMPONENTS

The proposed converter was analyzed assuming that the resonant components on each side were identical to those in section II. However, it is difficult to accurately align the values of the resonant components on each side in mass production. In this section, the tolerance of the resonant components is discussed. Taking the secondary side resonant inductance as an example, the tolerance is discussed. As mentioned in sections II-A and B, the resonant inductors are connected in parallel. Therefore, the equivalent resonant inductance on the secondary side is derived in (50).

$$L_{s\_eq} = L_3 // L_4 = \frac{L_3 L_4}{L_3 + L_4} \tag{50}$$

Equation (50) indicates that the equivalent resonant inductance will be 0.5 $L_s$ when $L_3 = L_4 = L_s$. As the difference between $L_3$ and $L_4$ increases, $L_{s\_eq}$ also moves away from 0.5 $L_s$; however, even if the difference between $L_3$ and $L_4$ is $\pm 20\%$, $L_{eq\_s}$ will remain within a range of about $\pm 10\%$ for 0.5 $L_s$. Thus, the parallel connection mitigates the impact of the difference between resonant inductances on the equivalent resonant inductance, which means reducing the change in the resonant frequency and voltage gain curve. In addition, the currents through $L_3$ and $L_4$ are represented in (28) and (29) in section II. Equations (28) and (29) indicate that when the

of input and output DC-link capacitors, respectively. Since the ESRs of the resonant capacitors and clamping capacitors are small, they are ignored in the equivalent circuit. $i_{dc}$ in Fig. 11(a) is the same as the $i_{rect}$ in Fig. 11(b) because these two currents indicate the half-cycle average value of the resonant current. Therefore, these two equivalent circuits can be combined, and the developed DC equivalent circuit of the proposed converter is shown in Fig. 11(c). Fig. 12 shows the simulation results for the proposed dynamic model and an actual circuit simulation based on the parameters in Table 2. The load is changed in a step from 400 Ω to 40 Ω. $\alpha$ and $\beta$ can be calculated by (48) and (49). To decide $\alpha$ and $\beta$, the resonant current is assumed to be a sinusoidal current, and the switching frequency is assumed to be the resonant frequency. In this case, $\alpha$ and $\beta$ are calculated with $\pi$ and $\pi/\sqrt{2}$, respectively, with reference to (27). The total inductance can be calculated with $L_1//L_2 + N^2(L_3//L_4)$ with reference to (18). The total resistance $R_{total}$ can be calculated with $R_{Lp}/2 + N^2 R_{Ls}/2 + R_{on}$ because the resonant inductors on each side

resonant inductors are different, their current ripples become different. However, even if the difference between $L_3$ and $L_4$ is ±20%, the difference in the current ripple is about ±10%, which means one resonant inductor current ripple is 45%, and the other is 55% of the resonant current ripple. Therefore, this difference does not have a big impact on the copper loss. The output current ripple ratio is obtained with (51) in reference to (47).

$$\frac{\Delta i_o}{\Delta i_{rs}} = \frac{L_4 C_4 - L_3 C_3}{(L_3 + L_4)(C_3 + C_4)} \tag{51}$$

Fig. 13 shows the current ripple ratio $\Delta i_o / \Delta i_{rs}$ in accordance with the inductance ratio $L_4/L_3$. As is shown, even if the difference is ±20%, the output current ripple is about ±5% of the resonant current ripple. Therefore, even if the resonant parameter has tolerance, the ripple-cancelling characteristics are effective.
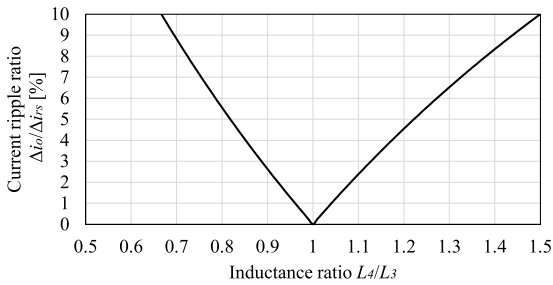


**FIGURE 13.** Current ripple ratio according to inductance ratio.

## IV. DESIGN METHODOLOGY OF PROPOSED CONVERTER

In this study, the specifications of the final target for the SST are an input voltage of 6.6 kVac, output voltage of 400 Vdc, and output power of 32 kW with 8 cells. Therefore, the specifications of each cell SRC are an input voltage of 1200 Vdc, output voltage of 400 Vdc, and output power of 4 kW. A prototype of the proposed circuit was fabricated as a scaled down version with an input voltage of 600 Vdc, output voltage of 200 Vdc, and output power of 1 kW. The selected resonant frequency was 100 kHz, and the turns ratio was set to 3:1. This section consists of three parts: 1) the design of the magnetizing inductance, 2) of the resonant tank, and 3) of the clamping capacitor.

### A. DESIGN OF MAGNETIZING INDUCTANCE

To achieve ZVS, the magnetizing inductance $L_m$ and dead-time $t_d$ have to be carefully chosen in order to charge and discharge the output capacitance of MOSFETs, $C_{oss}$, and the junction capacitance of diodes, $C_{jc}$. Generally, a small $L_m$ easily achieves ZVS. However, a small $L_m$ increases the RMS current. Extending the deadtime $t_d$ can give a large $L_m$, which would result in a low RMS current. However, this reduces the effective energy transfer and increases the RMS current when $td$ is excessively large. Both cause a high conduction loss. Considering the deadtime effect [12], [42], Equation (52)

represents the magnetizing inductance condition of the ZVS operation.

$$L_m \leq \frac{t_d (T_{sw} - 2t_d)}{16 \left(C_{oss} + \frac{C_{jc}}{N^2}\right)} \tag{52}$$

The primary-side resonant current shown in Fig. 14 can be expressed by (53).

$$i_{rp}(t) = \sqrt{2} I_{rp} \sin\left(\frac{2\pi}{T_{sw} - 2t_d}t + \phi\right) \tag{53}$$

Here, $I_{rp}$ is the RMS value of the primary current $i_{rp}(t)$, and

$$\phi = \sin^{-1}\left(-\frac{NV_o(T_{sw} - 2T_d)}{8\sqrt{2} L_m I_{rp}}\right). \tag{54}$$

The secondary-side resonant current can be expressed by (55) on the basis of KCL.

$$i_{rs}(t) = N\left(i_{rp}(t) - i_{Lm}(t)\right) \tag{55}$$

Here, $I_{Lm}(t)$ is the magnetizing current shown in Fig. 14 written as

$$i_{Lm}(t) = \frac{NV_o}{2L_m}t - \frac{NV_o(T_{sw} - 2t_d)}{8L_m}. \tag{56}$$

From (53)-(56), the average output current $I_o$ can be calculated as

$$I_o = \frac{V_o}{R_L} = \frac{2}{T_{sw}} \int_0^{(T_{sw}-2t_d)/2} \frac{1}{2}N\left(i_{rp}(t) - i_{Lm}(t)\right)dt$$

$$= \frac{N}{T_{sw}} \int_0^{(T_{sw}-2t_d)/2} \left(\sqrt{2}I_{rp}\sin\left(\frac{2\pi}{T_{sw} - 2t_d}t + \phi\right)\right.$$
$$\left. - \frac{NV_o}{2L_m}t + \frac{NV_o(T_{sw} - 2t_d)}{8L_m}\right)dt. \tag{57}$$

From (54) and (57), the RMS value of $i_{rp}(t)$ is obtained as

$$I_{rp} = \frac{I_o}{N}\sqrt{\frac{\pi^2}{2}\frac{T_{sw}^2}{(T_{sw} - 2t_d)^2} + \frac{N^4 R_L^2 (T_{sw} - 2t_d)^2}{128 L_m^2}}. \tag{58}$$

The RMS value of the secondary current $I_{rs}$ can be obtained as (59), shown at the bottom the of the next page. Generally,
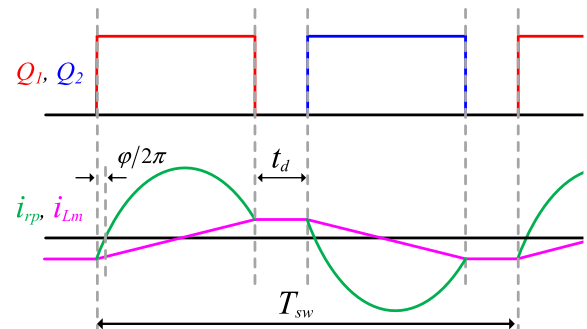


**FIGURE 14.** Picture of primary-side resonant current and magnetizing current with deadtime.

conduction loss on the secondary side is a large concern due to its high RMS current and the forward voltage drops of the diodes. The relationship between $L_m$ and $I_{rs}$ at various deadtimes from (52) and (59) is plotted as shown in Fig. 15. As is shown, a large $L_m$ leads to a low RMS current. However, when it is excessively large, the RMS current increases again. $L_m$ and $t_d$ values were selected to be 200 $\mu$H and 300 ns, respectively, on the basis of Fig. 15.
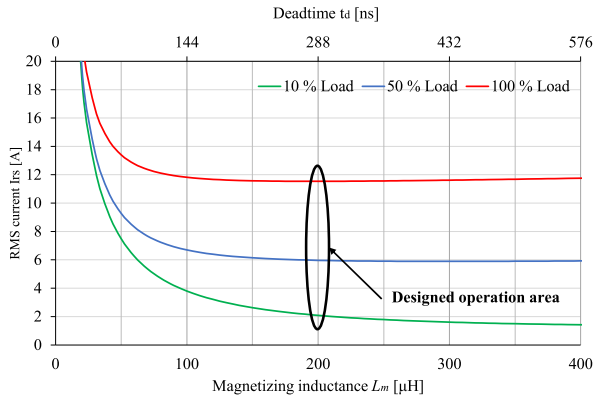


**FIGURE 15. Relationship between magnetizing inductance and secondary-side RMS resonant current at various deadtimes.**

### B. DESIGN OF RESONANT TANK

It is desirable for the DCX to make the leakage inductance as small as possible for a flat voltage gain and faster response. This section discusses designing the value of $k$ to be satisfied so that the voltage gain is flat within the tolerance range of the resonant frequency. Resonant components might generally have ±20% parameter deviations; consequently, the resonant frequency $f_r$ may vary from $0.8 f_r$ to $1.2 f_r$. Thus, the voltage gain of the DCX should be unity from $0.8 f_n$ to $1.2 f_n$. From (41), the relationship between $k$ and $Q$ is derived in (60).

$$kQ = \frac{\pi^3 L_m f_r}{N^2 R_L} = (\text{constant}) \qquad (60)$$

Equation (60) indicates that a large $k$ leads to a small $Q$. Both a large $k$ and small $Q$ contribute to planarizing the voltage gain. Fig. 16 shows the voltage gains under a full-load condition with several $k$ values. The value of $k$ should be greater than five to keep the voltage gain variation range within 5% as based on Fig. 16.
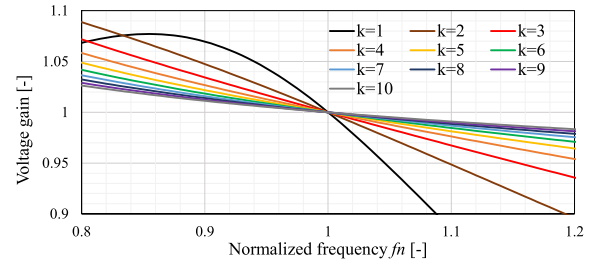


**FIGURE 16. Voltage gains under full-load condition with several k values.**

### C. DESIGN OF CLAMPING CAPACITOR

To avoid the clamping capacitor from participating in the resonant operation, the easiest way is using a capacitor with a large capacitance. However, this can reduce the power density. This section discusses designing the minimum value of the clamping capacitor to be satisfied so that it will not participate in the resonant operation. For the clamping capacitor not to participate, the voltage ripple of the clamping capacitor should be sufficiently smaller than that of the resonant capacitor as shown in (61).

$$\Delta v_{Ca} \ll \Delta v_{Cp} \qquad (61)$$

To simplify the calculation, the magnetizing current and deadtime are ignored here. The resonant current of the proposed converter is divided into two resonant capacitors. Thus, the voltage ripple of the resonant capacitor is written as

$$\Delta v_{Cp} = \frac{\sqrt{2}}{2\pi f_r C_p} I_{rp} = \frac{V_o}{2NR_L f_r C_p}. \qquad (62)$$

The voltage ripple of the clamping capacitor is written as

$$\Delta v_{Ca} = \frac{V_o}{\pi f_r C_a N R_L} \left[ \sin^{-1}\left(\frac{2}{\pi}\right) - \frac{\pi}{2}\left\{ 1 - \sqrt{1 - \left(\frac{2}{\pi}\right)^2} \right\} \right]. \qquad (63)$$

From (62) and (63), the clamping capacitor should satisfy (64).

$$C_a \gg \frac{2C_p}{\pi} \left[ \sin^{-1}\left(\frac{2}{\pi}\right) - \frac{\pi}{2}\left\{ 1 - \sqrt{1 - \left(\frac{2}{\pi}\right)^2} \right\} \right] = 0.211\, C_p \qquad (64)$$

Generally, it is necessary for satisfying the condition of being enough large as in (61) to be ten times or more. Fig. 17 shows

$$I_{rs} = \sqrt{\frac{2}{T_s} \int_0^{(T_{sw}-2t_d)/2} \left[ N\left(i_{rp}(t) - i_{Lm}(t)\right) \right]^2 dt}$$

$$= \frac{V_o}{R_L} \sqrt{\frac{T_{sw} - 2t_d}{T_{sw}} \left( \frac{\pi^2}{2} \frac{T_{sw}^2}{(T_{sw} - 2t_d)^2} + \left(\frac{5\pi^2 - 48}{384}\right)\left( \frac{N^4 R_L^2 (T_{sw} - 2t_d)^2}{\pi^2 L_m^2} \right) \right)} \qquad (59)$$
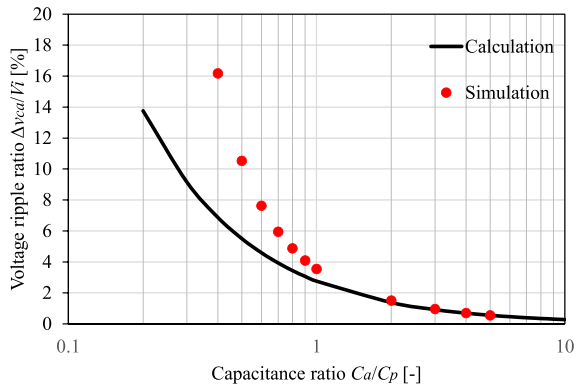
**FIGURE 17.** Voltage ripple ratio according to capacitance ratio.

the clamping capacitor voltage ripple ratio $\Delta v_{ca}/V_i$ in accordance with the capacitance ratio $C_a/C_p$. As shown in Fig. 17, the calculation result for (63) coincides with the simulation result in the range where the capacitance ratio is more than two. Therefore, the clamping capacitor should be greater than $2C_p$ to avoid it from taking part in the resonant operation.

## V. LOSS BREAKDOWN AMONG PROPOSED CONVERTER AND CONVENTIONAL CONVERTER WITH C/LC FILTERS

Taking the operation in powering mode as an example, the loss breakdown of three different structures, the proposed RCCLLC converter, the conventional HBCLLC converter with C filters, and one with LC filters, is investigated in this section. Since the ESRs of the resonant capacitors and filter capacitors are small, the ESR losses are ignored.

### A. SWITCHING LOSS AND CONDUCTION LOSS

Although the resonant current of the proposed converter is divided into two resonant inductors, the current through the switch is the sum of them. Therefore, the switch currents of the three structures are considered to be the same. Therefore, the switching loss and conduction loss of each structure are estimated to be the same. Since both the proposed and conventional converters have turn-on ZVS on the primary side and turn-on and turn-off ZCS on the secondary side, switching loss occurs only at the turn-off on the primary side. The turn-off loss is represented by (65), and the conduction losses on the primary side and the secondary side are represented by (66) and (67).

$$P_{turn\_off} = E_{off} f_{sw} \tag{65}$$

$$P_{pri\_cond} = R_{on} I_{rp}^2 \tag{66}$$

$$P_{sec\_cond} = V_F I_{rs} \tag{67}$$

Here, $E_{off}$ is the turn-off switching energy, $R_{on}$ is the on-resistance of the switch, and $V_F$ is the forward voltage drop of the diode rectifier.

### B. TRANSFORMER CORE LOSS

As the polarities of the transformer winding $S_1$ and $S_2$ are the reverse, DC magnetic fluxes caused by DC bias currents are

cancelled. Therefore, the design of the magnetic core for the HBCLLC converter can be applied to the proposed RCCLLC converter. The magnetic flux density of the HBCLLC converter $B_{HBCLLC}$ and that of the proposed converter $B_{RCCLLC}$ are written as follows.

$$B_{HBCLLC} = \frac{NV_o}{8f_{sw}\left(N_{S1\_HBCLLC} + N_{S2\_HBCLLC}\right)A_e} \tag{68}$$

$$B_{RCCLLC} = \frac{NV_o}{4f_{sw}\left(N_{S1\_RCCLLC} + N_{S2\_RCCLLC}\right)A_e} \tag{69}$$

Here, $N_{S1\_HBCLLC}, N_{S2\_HBCLLC}, N_{S1\_RCCLLC},$ and $N_{S2\_RCCLLC}$ are the number of turns for each transformer winding $S_1$ and $S_2$, respectively. $A_e$ is the effective cross-sectional area of the magnetic core. (68) and (69) indicate that the two converters have the same magnetic flux density when the total number of turns in the HBCLLC is half the number of turns in the RCCLLC. In that case, the transformer core loss of each structure is estimated to be the same.

### C. TRANSFORMER AND INDUCTOR COPPER LOSS

Since the currents through the transformer windings and the resonant inductors are the same, these copper losses are calculated together in this section. The copper loss of the conventional converter on the primary side is represented in (70).

$$P_{S1\_HBCLLC} + P_{S2\_HBCLLC} = 2I_{rp}^2 R_{Sp\_HBCLLC} \tag{70}$$

Here, $R_{Sp\_HBCLLC}$ is the ESR of each primary-side transformer winding of the conventional converter. In comparison, the primary-side total copper loss of the proposed converter is represented in (71) in reference to (24) and (25).

$$P_{S1\_RCCLLC} + P_{S2\_RCCLLC} = 2\left(I_{in}^2 + \frac{1}{4}I_{rp}^2\right)R_{Sp\_RCCLLC} \tag{71}$$

Here, $I_{in}$ is the input source current and $R_{Sp\_RCCLLC}$ is the ESR of each primary-side transformer winding of the proposed converter. As mentioned in section V-B, the winding resistances of the proposed converter are estimated to be twice as large as those of the conventional converter because the total turn numbers are double. When the magnetizing current and deadtime are ignored for simple calculation, (70) and (71) are calculated in (72) and (73).

$$P_{S1\_HBCLLC} + P_{S2\_HBCLLC} = \pi^2 I_{in}^2 R_{Sp\_HBCLLC}, \tag{72}$$

$$P_{S1\_RCCLLC} + P_{S2\_RCCLLC} = \left(2 + \frac{\pi^2}{4}\right)I_{in}^2 R_{Sp\_RCCLLC}$$

$$= \left(4 + \frac{\pi^2}{2}\right)I_{in}^2 R_{Sp\_HBCLLC}. \tag{73}$$

Comparing (72) and (73), it can be seen that the primary-side total copper loss of the proposed converter is estimated to be 9.47% smaller than that of the conventional converter. The secondary side is the same.

### D. FILTER LOSS AND DC-LINK CAPACITOR ESR LOSS

Thanks to the ripple-cancelling characteristics and embedded $\pi$ filter, the current through the DC-link capacitor of the proposed converter becomes zero. Therefore, the proposed converter has no DC-link capacitor ESR loss. In comparison, in the case of the conventional converter, the current flows thorough the DC-link capacitor when using C filters. Therefore, the structure has DC-link capacitor ESR loss. The current through the input DC-link capacitor is calculated as follows.

$$i_{C_i}(t) = \frac{\frac{\sqrt{2}}{2} I_{rp} |\sin(2\pi f_{sw}t)| - \frac{I_o}{N}}{\sqrt{\left(1 + \frac{C_{fi}}{C_{i\_2fsw}}\right)^2 + \left(4\pi f_{sw}C_{fi}R_{C_i}\right)^2}}$$
$$\simeq \frac{\sqrt{2}\, I_{rp}\sin(4\pi f_{sw}t)}{4\sqrt{\left(1 + \frac{C_{fi}}{C_{i\_2fsw}}\right)^2 + \left(4\pi f_{sw}C_{fi}R_{C_i}\right)^2}} \quad (74)$$

Here, $C_{fi}$ is the input filter capacitor, $C_{i\_2fsw}$ is the capacitance of the input DC-link capacitor at twice the switching frequency, and $R_{C_i}$ is the ESR of the input DC-link capacitor. The input DC-link capacitor ESR loss is written as follows.

$$P_{C_i} = \frac{I_{rp}{}^2 R_{C_i}}{16\left(\left(1 + \frac{C_{fi}}{C_{i\_2fsw}}\right)^2 + \left(2\omega_{sw}C_{fi}R_{C_i}\right)^2\right)} \quad (75)$$

When using LC filters, additional filter inductors are required. Therefore, additional copper loss of the filter inductor occurs in the structure. The filter inductor copper loss on the primary side is written as follows.

$$P_{Lfi} = I_{in}{}^2 R_{Lfi} \quad (76)$$

Here, $R_{Lfi}$ is the ESR of the input filter inductor. Although copper loss of the additional filter inductor occurs in the structure, the current through the DC-link capacitor becomes zero in the structure. The secondary side is the same.

## VI. EXPERIMENTAL RESULTS

Three hardware prototypes, the proposed RCCLLC converter, a conventional HBCLLC converter with C filters, and one with LC filters, were implemented to demonstrate the feasibility of the proposed converter and compare their operation characteristics in experiments. The specifications and circuit parameters are listed in Table 3. According to Table 3, the resonant frequency of the prototype RCCLLC converter was 97.5 kHz in reference to (19), and that of the HBCLLC converter was 93.7 kHz. This difference is due to an error of the resonant components. Since an SRC has the highest efficiency at a frequency slightly lower than the resonant frequency, the normalized switching frequency of the proposed converter was set to 95 kHz, and that of the conventional converter was set to 90 kHz in the experiments for fair comparison. The filter components of the conventional converters were designed on the basis of the embedded

**TABLE 3.** Specifications and electrical parameters.

| Specification/ Component | HBCLLC parameters | RCCLLC parameters |
|---|---|---|
| Rated power $P$ | 1 kW | 1 kW |
| Input voltage $V_i$ | 600 V | 600 V |
| Output voltage $V_o$ | 200 V | 200 V |
| Turns ratio N | 3 | 3 |
| Resonant inductor $L_1, L_2, L_3, L_4$ | 7.82 μH, 7.86 μH, 1.04 μH, 1.06μH | 30.4 μH, 30.1 μH, 3.69 μH, 3.74 μH |
| Resonant capacitor $C_1, C_2, C_3, C_4$ | 83.5 nF, 83.6 nF, 750 nF, 749 nF | 83.5 nF, 83.6 nF, 760 nF, 749 nF |
| Magnetizing inductor $L_m$ | 198 μH | 198 μH |
| Clamping capacitor $C_a, C_b$ | None | 220 nF, 2.2 μF |
| Filter capacitor $C_{fi}, C_{fo}$ | 220 nF, 2.2 μF | None |
| Filter inductor $L_{fi}, L_{fo}$ | 60.0 μH, 6.57 μH | None |
| DC-link capacitor $C_i, C_o$ | 10 μF, 40 μF | 10 μF, 40 μF |

filter characteristics shown in Fig. 10(b). Only a powering mode test was conducted in the experiments. 900-V SiC-MOSFETs, C3M0065090D, were used as the primary-side inverter switching devices, and 650-V SiC-Schottky diodes, CVFD20065A, were used as the secondary-side rectifier. The three hardware prototypes are shown in Fig. 18. The power densities of the three structures are summarized in Table 4. Since clamping capacitors are used for ripple-cancelling characteristics in the proposed converter instead of filter capacitors, the number of components is the same in the proposed converter and the conventional converter with C filters. Thus, the cross-sectional areas of the prototypes are decided by the presence or absence of the filter inductors, and the heights of the prototypes depend on the transformer core size as shown in Fig. 18. As shown in (68) and (69), if the magnetic flux densities of the two converters are designed to be the same, the cross-sectional area of the core or the total number of turns of the HBCLLC converter can be halved compared with those of the proposed converter. If the cross-sectional area of the core is halved, the power density will be improved, but the copper loss in the winding will be increased. Therefore, the same cores are used in their transformers in this research. As a result, the power densities of the proposed converter and the conventional converter with C filters are the same, and that of the conventional converter with LC filters is the lowest among the three structures because it requires additional filter inductors.

### A. SOFT-SWITCHING OPERATIONS

Primary-side ZVS and secondary-side ZCS soft-switching operations are shown in Fig. 19 and 20, respectively. The proposed converter achieved primary-side ZVS and secondary-side ZCS under 10% load (100 W) and full-load (1 kW) conditions. Therefore, it had load-independent soft-switching characteristics like those of conventional converters.
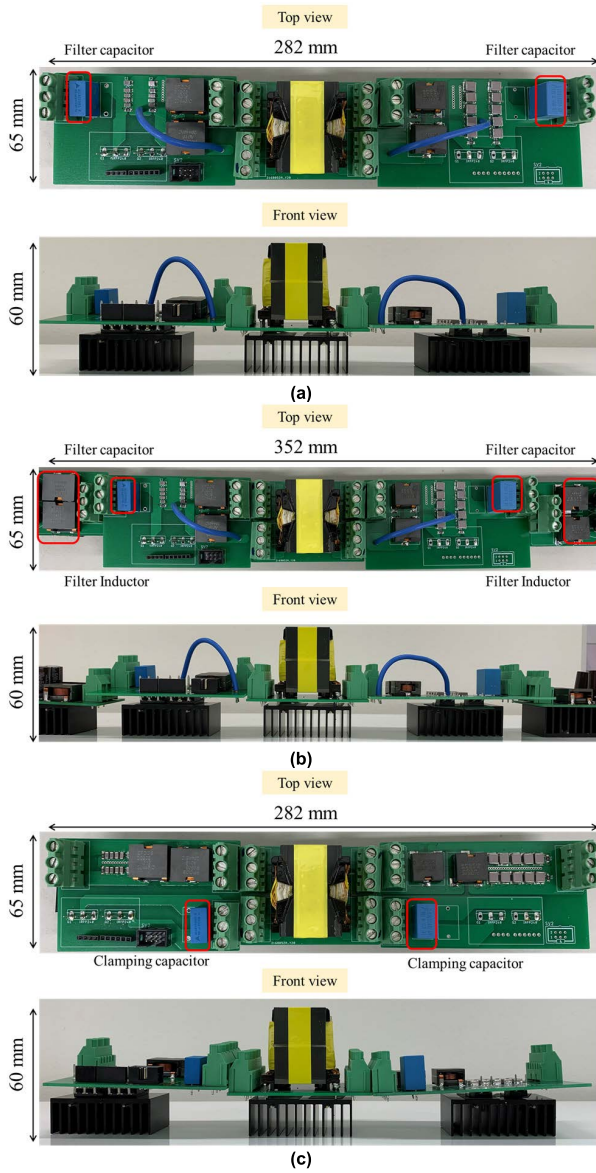
**FIGURE 18.** Three hardware prototypes: (a) HBCLLC converter with C filters, (b) HBCLLC converter with LC filters, and (c) RCCLLC converter.

**TABLE 4.** Power densities of three hardware prototypes.

|  | HBCLLC converter with C filters | HBCLLC converter with LC filters | RCCLLC converter |
|---|---|---|---|
| Power density | 0.91 kW/L | 0.73 kW/L | 0.91 kW/L |

## B. VOLTAGE GAIN

Fig. 21 shows the voltage gains of the three structures versus the normalized frequency and output power, respectively. The theoretical and experimental gains were close and flat within the operating range. The voltage gains of the three structures had close values because the resonant inductors of the conventional converters were designed to be four times as small as that of the proposed converter. Therefore, this
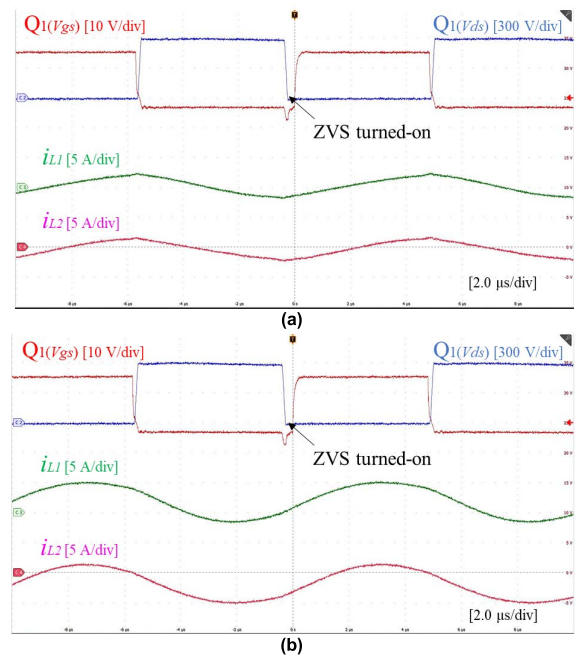


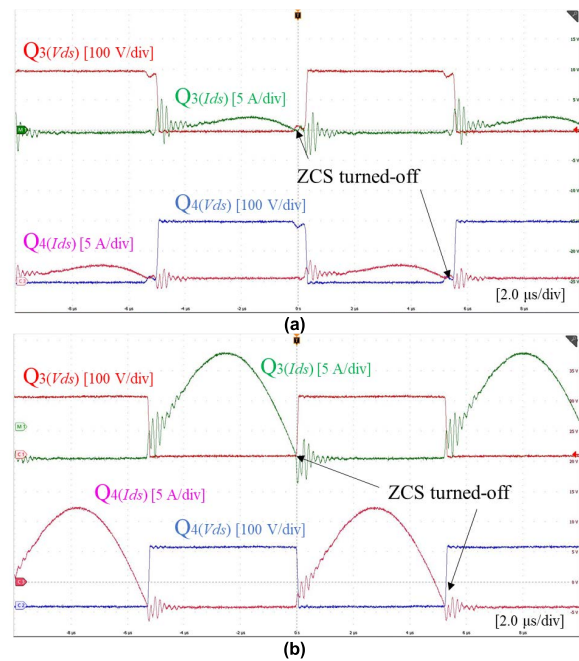**FIGURE 19.** ZVS operation of proposed converter: (a) 10% load (100 W) and (b) full load (1 kW).



**FIGURE 20.** ZCS operation of proposed converter: (a) 10% load (100 W) and (b) full load (1 kW).

indicates that the voltage gain of the proposed converter is more constant than those of the conventional converters if the resonant inductors are the same.

## C. TRANSIENT RESPONSE

To verify the proposed dynamic model, the load step response of the prototype proposed converter is compared with the
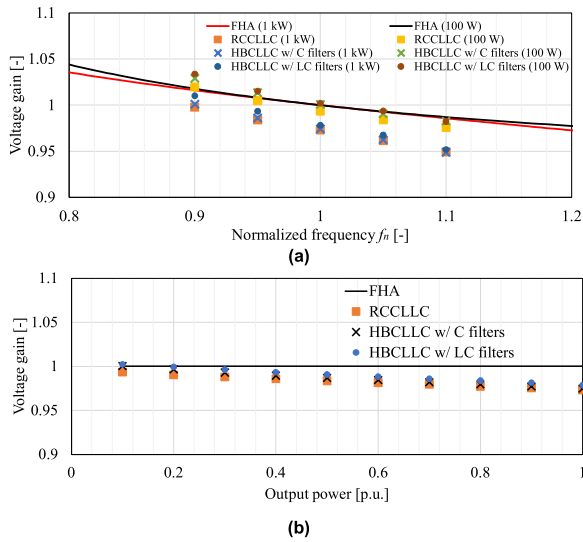
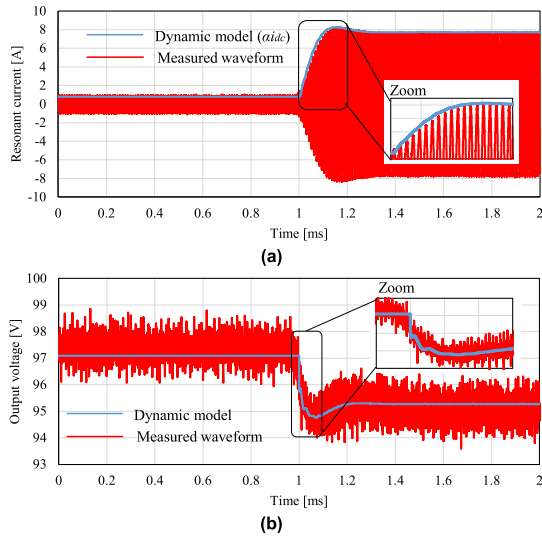**FIGURE 21.** Voltage gains of three structures versus (a) normalized frequency and (b) output power.



**FIGURE 22.** Comparison of measured transient response and proposed dynamic model of proposed converter: (a) resonant current and (b) output voltage.

proposed model. The circuit parameters of the prototype are given in Table 3, and the parameters of parasitic resistances are given in Table 2. In the experiment, the input voltage was set to 300 V. The load was changed in a step from 400 Ω to 40 Ω. The forward voltage drop of the diode was 1.35 V, i.e., $V_F = 2.7$ V. The resonant current can be assumed to be a piecewise sinusoidal current because $f_{sw}$ is lower than $f_r$. Referring to (48) and (49), $\alpha$ and $\beta$ can be calculated as $\alpha = \pi f_r / f_{sw} = 3.22$ and $\beta = \pi \sqrt{f_r / 2 f_{sw}} = 2.25$, respectively. From the above, the DC equivalent parameters can be calculated as $L_{dc} = 330~\mu$H and $R_{dc} = 3.86$ Ω. Fig. 22 shows the transient response of the proposed converter and corresponding result from the proposed model. The experimental result verifies the accuracy of the proposed dynamic model and the fact that the proposed converter
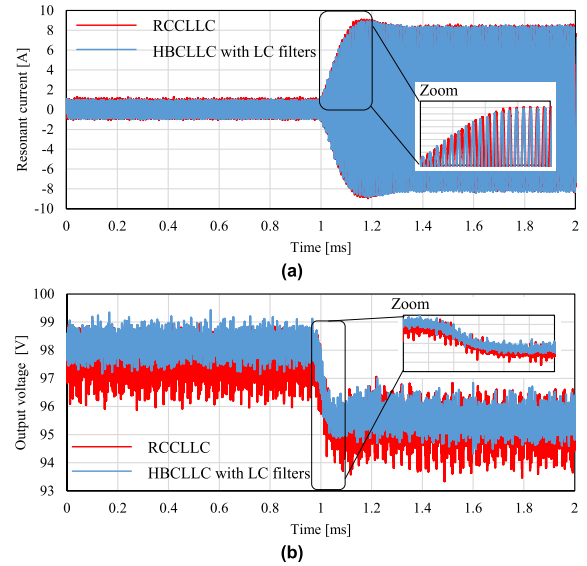


**FIGURE 23.** Comparison of measured transient responses between proposed and conventional converters: (a) resonant current and (b) output voltage.

comprises the characteristics of an SRC and embedded $\pi$ filter. From this result, the proposed dynamic model can be used for the controller design of future SSTs. Furthermore, the load-step responses of the proposed converter and conventional converter with LC filters are compared in Fig. 23. The circuit parameters of the two converters are given in Table 3. Note that the resonant inductor of the conventional converter is designed to be four times smaller than that of the proposed converter. The experimental conditions are the same as the above. As shown in Fig. 23, the response speeds of both were almost the same. Therefore, it is verified that the transient response of the proposed converter is faster than that of the conventional converter with LC filters if the resonant inductors are the same.

### D. CURRENT RIPPLE COMPARISON

The key waveforms of the resonant currents and ripple-cancelling characteristics are shown in Fig. 24 under a full-load (1 kW) condition. The currents after passing through filters, which are $I_o + i_{co}$ for each structure, were measured as output currents to compare how well each filter mitigates current ripples. The output current ripple of the conventional HBCLLC converter with C filters was 3.73 A, whereas the conventional HBCLLC converter with LC filters and the proposed converter had almost no output current ripple even though the resonant current amplitudes of the three structures are almost the same.

The output current spectra up to the 20th harmonic component are compared in Fig. 25. The output current spectrum of the proposed converter was suppressed by 19.3 dB compared with that of the conventional converter with C filters and was larger by 0.8 dB compared with that of the conventional converter with LC filters at a frequency of $2 f_{sw}$. In addition, the
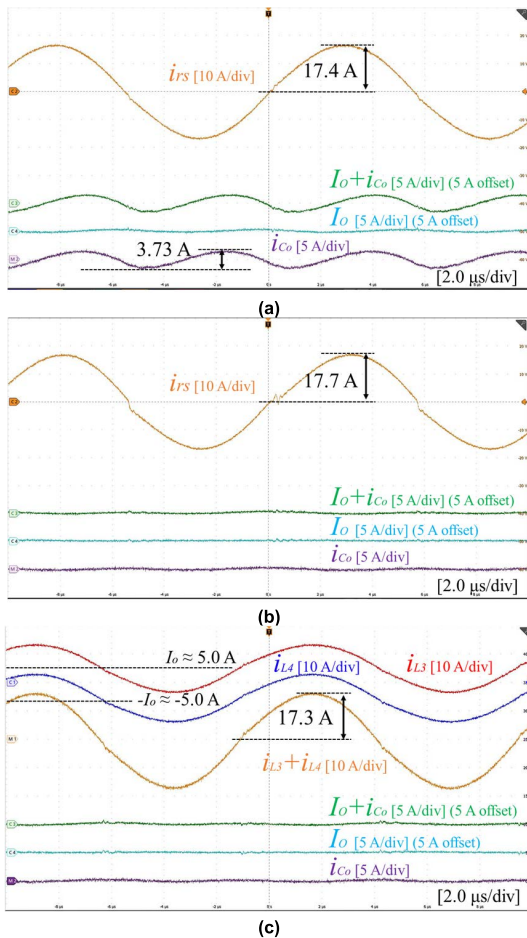
**FIGURE 24.** Key waveforms of resonant current and ripple-cancelling characteristics under 1-kW full load condition: (a) HBCLLC converter with C filter, (b) HBCLLC converter with LC filter, and (c) RCCLLC converter.
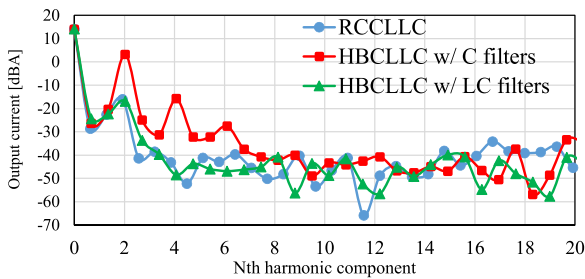


**FIGURE 25.** Experimental output current spectra up to 20th harmonic component of three different structures.

proposed converter is as effective as the LC filters in reducing the current ripple in the higher harmonic components.

From the results, the filter capacitor needs more capacitance in the conventional converter with C filters to suppress the output current ripple. As a result, the power density will be decreased. In addition, although the conventional converter with LC filters suppressed the output current the most, the structure sacrifices power density, and the proposed converter already sufficiently suppresses output current ripple. Thus, this result shows that the proposed converter suppresses EMI most effectively without sacrificing power density.

## E. EFFICIENCY COMPARISON

The measured efficiencies of the three structures are shown in Fig. 26. Among the three structures, the efficiencies were almost the same. However, the proposed converter had a slightly higher efficiency compared with the other two structures. Fig. 27 shows the loss breakdown of the three structures under a 1-kW full-load condition. As discussed in section V, the conduction loss is estimated to be the same. Since the normalized frequencies of the two converters are different, the switching loss and the transformer core loss were slightly different. The switching loss of the conventional converter
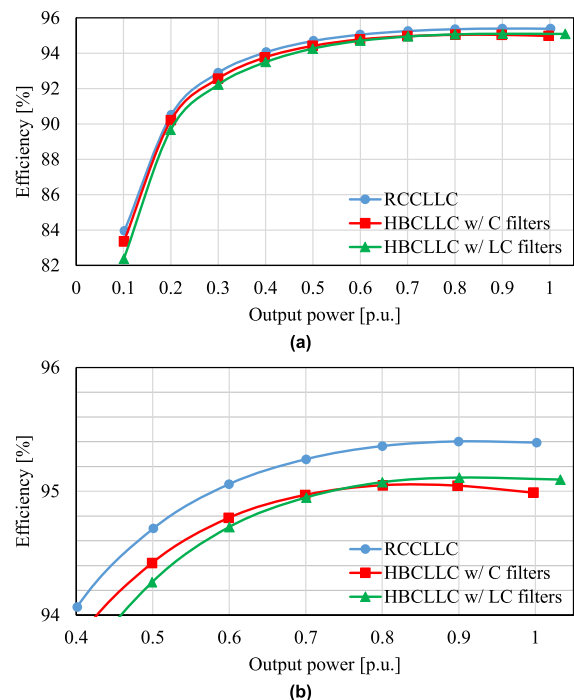


**FIGURE 26.** Measured efficiency of three structures: (a) overall efficiency and (b) zoom-in from 0.4 p.u. to 1.0 p.u.
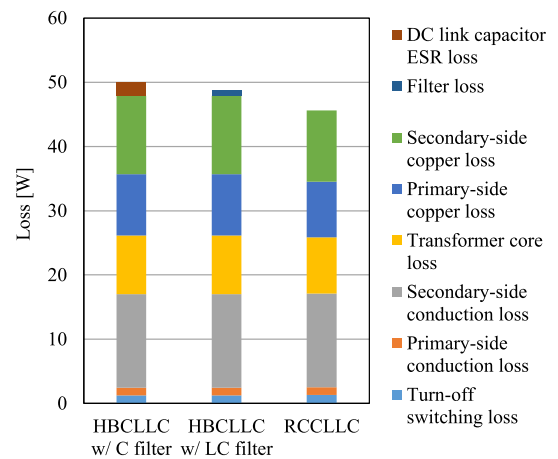


**FIGURE 27.** Loss breakdown of three structures under full-load (1 kW) condition.

was 0.07 W less than that of the proposed converter, and the transformer core loss of the conventional converter is 0.38 W more than that of the proposed converter. Since these differences account for a small proportion of the total losses, they do not have a significant impact on the efficiency comparison. In comparison, the transformer and resonant inductor copper loss of the proposed converter was estimated to be smaller than that of the conventional converter structures by 9.47%. In addition, the ESR loss of the DC-link capacitor and copper loss of the filter inductor additionally occurred for the conventional converters with C and LC filters, respectively. For these reasons, the proposed converter had the highest efficiency among the three structures. Furthermore, since these losses increase as the power rating increases, it is expected that the efficiency of the proposed converter will be further improved compared with the conventional converter with C/LC filters at full-scale.

## VII. CONCLUSION

This paper comprehensively discussed the characteristics and design methodology of a proposed converter and compared the converter with a conventional half-bridge CLLC converter with C/LC filters. The equivalent resonant inductor of the proposed converter is four times as small as that of the conventional converters. Therefore, a more constant voltage gain and faster transient response are possibly achieved when the resonant inductors have the same values. In addition, the proposed converter has ripple-cancelling characteristics and an embedded $\pi$ filter. Consequently, it is superior to the conventional converters in its ability to reduce EMI. Experimental results showed that the proposed converter significantly suppressed the second harmonics of the output current by 19.3 dB compared with that of the conventional converter with C filters while maintaining the same power density, and it improved the power density compared with the conventional converter with LC filters while maintaining almost the same ripple mitigation. Thus, it enables the power density to be increased. It also inherits the advantages of the conventional SRC, such as load-independent soft-switching characteristics. Furthermore, a loss breakdown showed that the proposed converter reduced the copper loss of the transformer windings by 9.47% and eliminated the losses of filter inductors and DC-link capacitors. As a result, the proposed converter had the highest efficiency of 95.4% under a full-load condition among three structures.

These results indicate that the efficiency and power density of the proposed converter are expected to be further improved compared with the conventional converters when they are implemented at full-scale. These features allow a conventional converter to be quickly replaced with the proposed converter for high-power-density DCX-SST.

## REFERENCES

[1] A. Q. Huang, "Medium-voltage solid-state transformer: Technology for a smarter and resilient grid," *IEEE Ind. Electron. Mag.*, vol. 10, no. 3, pp. 29–42, Sep. 2016.

[2] A. Q. Huang, M. L. Crow, G. T. Heydt, J. P. Zheng, and S. J. Dale, "The future renewable electric energy delivery and management (FREEDM) system: The energy internet," *Proc. IEEE*, vol. 99, no. 1, pp. 133–148, Jan. 2011.

[3] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 186–198, Sep. 2013.

[4] J. E. Huber and J. W. Kolar, "Solid-state transformers: On the origins and evolution of key concepts," *IEEE Ind. Electron. Mag.*, vol. 10, no. 3, pp. 19–28, Sep. 2016.

[5] F. Wang, Z. Zhang, T. Ericsen, R. Raju, R. Burgos, and D. Boroyevich, "Advances in power conversion and drives for shipboard systems," *Proc. IEEE*, vol. 103, no. 12, pp. 2285–2311, Dec. 2015.

[6] M. A. Hannan, P. J. Ker, M. S. H. Lipu, Z. H. Choi, M. S. A. Rahman, K. M. Muttaqi, and F. Blaabjerg, "State of the art of solid-state transformers: Advanced topologies, implementation issues, recent progress and improvements," *IEEE Access*, vol. 8, pp. 19113–19132, 2020.

[7] J. E. Huber and J. W. Kolar, "Volume/weight/cost comparison of a 1MVA 10 kV/400 V solid-state against a conventional low-frequency distribution transformer," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2014, pp. 4545–4552.

[8] T. Isobe, R. A. Barrera-Cardenas, Z. He, Y. Zou, K. Terazono, and H. Tadano, "Control of three-phase solid-state transformer with phase-separated configuration for minimized energy storage capacitors," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 3014–3028, Sep. 2020.

[9] T. Zhao, G. Wang, S. Bhattacharya, and A. Q. Huang, "Voltage and power balance control for a cascaded H-bridge converter-based solid-state transformer," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1523–1532, Apr. 2013.

[10] H. Shi, H. Wen, J. Chen, Y. Hu, L. Jiang, G. Chen, and J. Ma, "Minimum-backflow-power scheme of DAB-based solid-state transformer with extended-phase-shift control," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3483–3496, Jul./Aug. 2018.

[11] J. Huang, Y. Wang, Z. Li, and W. Lei, "Unified triple-phase-shift control to minimize current stress and achieve full soft-switching of isolated bidirectional DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4169–4179, Jul. 2016.

[12] Q. Zhu, L. Wang, A. Q. Huang, K. Booth, and L. Zhang, "7.2-kV single-stage solid-state transformer based on the current-fed series resonant converter and 15-kV SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1099–1112, Feb. 2019.

[13] G. Ortiz, M. G. Leibl, J. E. Huber, and J. W. Kolar, "Design and experimental testing of a resonant DC–DC converter for solid-state transformers," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7534–7542, Oct. 2017.

[14] J. E. Huber, D. Rothmund, L. Wang, and J. W. Kolar, "Full-ZVS modulation for all-SiC ISOP-type isolated front end (IFE) solid-state transformer," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2016, pp. 1–8.

[15] J.-I. Itoh, K. Aoyagi, K. Kusaka, and M. Adachi, "Development of solid-state transformer for 6.6-kV single-phase grid with automatically balanced capacitor voltage," *IEEJ J. Ind. Appl.*, vol. 8, no. 5, pp. 795–802, Sep. 2019.

[16] M. Ngo, Y. Cao, D. Dong, and R. Burgos, "Design of 500 kHz, 18 kW low leakage inductance intraleaved litz wire transformer for bi-directional resonant DC–DC converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Jun. 2021, pp. 1153–1161.

[17] S.-M. Park, D.-H. Kim, D.-M. Joo, M.-J. Kim, and B.-K. Lee, "Design of output filter in LLC resonant converters for ripple current reduction in battery charging applications," in *Proc. 9th Int. Conf. Power Electron. ECCE Asia (ICPE-ECCE Asia)*, Jun. 2015, pp. 2050–2056.

[18] T. Lamorelle, Y. Lembeye, and J.-C. Crebier, "Handling differential mode conducted EMC in modular converters," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5812–5819, Jun. 2020.

[19] J.-M. Choe, C.-S. Yeh, O. Yu, M. Lee, H. Wen, J.-S. Lai, and L. Zhang, "Controller and EMI filter design for modular front-end solid-state transformer," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2018, pp. 188–192.

[20] K. Murata and F. Kurokawa, "An interleaved PFM LLC resonant converter with phase-shift compensation," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2264–2272, Mar. 2016.

[21] H. Chen, X. Wu, and S. Shao, "A current-sharing method for interleaved high-frequency LLC converter with partial energy processing," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1498–1507, Feb. 2020.

[22] O. Kirshenboim and M. M. Peretz, "Combined multilevel and two-phase interleaved LLC converter with enhanced power processing characteristics and natural current sharing," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5613–5620, Jul. 2018.

[23] P. Xuewei and A. K. Rathore, "Novel bidirectional snubberless naturally commutated soft-switching current-fed full-bridge isolated DC/DC converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2307–2315, May 2014.

[24] W. Qin, X. Wu, and J. Zhang, "A family of DC transformer (DCX) topologies based on new ZVZCS cells with DC resonant capacitance," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2822–2834, Apr. 2017.

[25] D. Moon, J. Park, and S. Choi, "New interleaved current-fed resonant converter with significantly reduced high current side output filter for EV and HEV applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4264–4271, Aug. 2015.

[26] X. Sun, Y. Shen, Y. Zhu, and X. Guo, "Interleaved boost-integrated LLC resonant converter with fixed-frequency PWM control for renewable energy generation applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4312–4326, Aug. 2015.

[27] S.-J. Kim and H.-L. Do, "Soft-switching step-up converter with ripple-free output current," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5618–5624, Aug. 2016.

[28] Y.-M. Chen, Y.-C. Liu, and F.-Y. Wu, "Multiinput converter with power factor correction, maximum power point tracking, and ripple-free input currents," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 631–639, May 2004.

[29] C.-T. Pan, M.-C. Cheng, C.-M. Lai, and P.-Y. Chen, "Current-ripple-free module integrated converter with more precise maximum power tracking control for PV energy harvesting," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 271–278, Jan. 2015.

[30] M. J. Schutten, R. L. Steigerwald, and J. A. Sabate, "Ripple current cancellation circuit," in *Proc. 18th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Feb. 2003, pp. 464–470.

[31] Y. Gu, D. Zhang, and Z. Zhao, "Input current ripple cancellation technique for boost converter using tapped inductor," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5323–5333, Oct. 2014.

[32] C. S. Leu and P. Y. Huang, "Near zero current-ripple inversion or rectification circuits," U.S. Patent 8 665 616 B2, Mar. 4, 2014.

[33] C. S. Leu and P. Y. Huang, "Near zero current-ripple inversion or rectification circuits," Taiwan Patent TWI 479 795 B, Apr. 1, 2015.

[34] P.-Y. Huang, T. Ohta, M. Fujii, and Y. Kado, "Bidirectional isolated ripple cancel dual active bridge DC–DC converter," in *Proc. IEEE 3rd Int. Conf. DC Microgrids (ICDCM)*, Shimane, Japan, May 2019, pp. 1–6.

[35] S. Inoue, M. Ishigaki, A. Takahashi, and T. Sugiyama, "Design of an isolated bidirectional DC–DC converter with built-in filters for high power density," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 739–750, Jan. 2021.

[36] T. Ohta, P.-Y. Huang, and Y. Kado, "Bidirectional isolated ripple cancel triple active bridge DC–DC converter," in *Proc. 22nd Eur. Conf. Power Electron. Appl. (EPE ECCE Europe)*, Lyon, France, Sep. 2020, p. 1.

[37] J. Sugimoto, P.-Y. Huang, S. Okutani, and Y. Kado, "Bidirectional isolated ripple cancel dual active bridge modular multile vel DC–DC converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, New Orleans, LA, USA, Mar. 2020, pp. 1081–1088.

[38] S. Okutani, P.-Y. Huang, R. Nishiyama, and Y. Kado, "Series resonant converter with embedded filters for DCX of solid-state transformer," in *Proc. 47th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Oct. 2021, pp. 1–7.

[39] S. Zou, J. Lu, A. Mallik, and A. Khaligh, "Bi-directional CLLC converter with synchronous rectification for plug-in electric vehicles," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 998–1005, Mar. 2018.

[40] D. Rothmund, J. E. Huber, and J. W. Kolar, "Operating behavior and design of the half-cycle discontinuous-conduction-mode series-resonant-converter with small DC link capacitors," in *Proc. IEEE 14th Workshop Control Model. Power Electron. (COMPEL)*, Jun. 2013, pp. 1–9.

[41] J. E. Huber, J. Miniböck, and J. W. Kolar, "Generic derivation of dynamic model for half-cycle DCM series resonant converters," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 4–7, Jan. 2018.

[42] Y. Liu, "High efficiency optimization of LLC resonant converter for wide load range," M.S. thesis, College Eng., Virginia Tech, Blacksburg, VA, USA, Dec. 2007. Accessed: Jan. 5, 2022. [Online]. Available: https://vtechworks.lib.vt.edu/handle/10919/30990/

**SHOTA OKUTANI** (Graduate Student Member, IEEE) was born in Kyoto, Japan, in 1995. He received the B.S. and M.S. degrees in electrical engineering from the Kyoto Institute of Technology, Kyoto, in 2018 and 2020, respectively, where he is currently pursuing the Ph.D. degree. His current research interests include modeling and control of dc–dc converters, high power-density dc–dc converters, and high voltage dc–dc converters.

**PIN-YU HUANG** (Member, IEEE) was born in Taipei, Taiwan, in 1985. He received the M.S. and Ph.D. degrees in electrical engineering from the National Taiwan University of Science and Technology, Taipei, in 2011 and 2015, respectively.

In 2013, he was a Visiting Scholar with the Center for Power Electronics (CPES), Virginia Polytechnic Institute and State University, USA. From 2015 to 2018, he was a Postdoctoral Researcher at the Power Electronic Laboratory, Tokyo Metropolitan University, Japan. He has been an Assistant Professor with the Kyoto Institute of Technology, since 2018. His current research interests include voltage multipliers, high power density dc–dc converter design, multi-level converters, passive components characteristics measurement of capacitors and inductors, and three-port power routers for renewable energy dc microgrids.

**RYO NISHIYAMA** (Graduate Student Member, IEEE) was born in Osaka, Japan, in 1997. He received the B.S. degree in electrical engineering from the Kyoto Institute of Technology, Kyoto, Japan, in 2021, where he is currently pursuing the M.S. degree.

His current research interests include resonant converters and high power-density dc–dc converters.

**YUICHI KADO** (Member, IEEE) received the M.S. and Ph.D. degrees in electronics from Tohoku University, Miyagi, Japan, in 1983 and 1998, respectively.

In 1983, he joined the Electrical Communication Laboratories of Nippon Telegraph and Telephone Public Corporation (now NTT), Kanagawa, Japan, where he was engaged in research on SOI structure formation by hetero-epitaxial growth. From 1989 to 1998, he worked on the development of fully depleted CMOS/SIMOX LSIs and ultra-low-power CMOS circuits. From 1999, he was engaged in Research and Development on compact network appliances using ultra-low-power CMOS circuit technologies for ubiquitous communications. He led research and development projects on ultra-low-power network appliances, sub-terahertz-wave wireless communication, and intra-body communication as the Director of the Smart Devices Laboratory at NTT Microsystem Integration Laboratories, from 2003 to 2010. In July 2010, he joined the Department of Electronics, Kyoto Institute of Technology, Kyoto, Japan. His current research interest includes multi-port power routers to build energy interchanging systems.

• • •