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# Multiphase Traction Inverters: State-of-the-Art Review and Future Trends

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**ABSTRACT** Multiphase inverters (MPIs) continue to increase in popularity owing to their compelling features that include enhanced fault-tolerance capability, improved per-phase power handling, and reduced dc-bus capacitor sizing. This article presents a comprehensive review on MPIs and their application in transportation electrification. More specifically, voltage source inverter (VSI) and nine-switch inverter (NSI) are the two MPI topologies reviewed herein, due to their popularity and potential for employment as traction inverters. The state-of-the-art review covers modeling and control techniques, dc-capacitor sizing, modulation strategies, inverter losses, and cost. Promising future trends of MPIs in terms of topologies, switching devices and integrated design are also investigated.

**INDEX TERMS** Automotive, dc-ac converters, electric vehicles, inverters, power electronics, pulse width modulated power converters, transportation electrification, vector control.

## I. INTRODUCTION

Recent years have seen an uptake of electrification in all sectors of transportation: road, sea, and air [1]–[3]. In 2020, we witnessed many original equipment manufacturers (OEMs) releasing electric vehicles extending beyond the standard passenger vehicle to include sports cars [4]. This uptake is only expected to grow into the future; it is projected that more than 50% of the global sales of passenger vehicles will be electric by 2040 [5]. This is driven by the need for clean, reliable, inexpensive and sustainable transportation system as global warming concerns continue to rise [6].

The driving power of all electrified powertrains is one or more electric machines (EMs) operating either solely, or in conjunction with an internal combustion engine (ICE) [6]. Driving and controlling the EM is achieved by a traction inverter which converts the dc power drawn from the battery to a variable frequency ac power in motoring mode. Vice versa, in generation mode the inverter acts as a rectifier to transfer the kinetic energy from the vehicle back to the battery. Extensive efforts are being invested in optimizing the efficiency, power density, and cost of traction inverters. Such efforts are in line with the next-generation framework of electrified transportation that includes increased voltage and power ratings [7] and employment of wide bandgap (WBG) devices [8].

At the heart of traction inverters are power semiconductor devices, whose ratings might be limited in the face of the aforementioned trends. When voltage is a limiting factor, multilevel inverters (MLIs) constitute a viable solution [9]. MLIs are able to utilize switching devices with lower voltage ratings for the same or higher DC-link voltages when compared to two-level inverters. Thereby, their application in powertrains rated at and beyond 800 V is gaining a a significant attention [10]. On the other hand, when current is a limiting factor for the semiconductor devices, discrete device paralleling is the industry-accepted solution; multiple devices are connected in parallel to withstand the output current of the inverter. Tesla's Model 3 (2018), for example, employs four SiC discrete MOSFET devices per switch [11]. However, device paralleling poses design challenges pertaining to static and dynamic current sharing among the paralleled devices [12]–[15]. Mismatches between the paralleled devices lead to current unbalance, which in turn causes hot spots [14].

Alternatively, multiphase drives (MPDs), beyond three phases, thrive in delivering high-power, owing to their improved per-phase current handling [16]. With more phases to share the required output power, device paralleling issues are alleviated, or eliminated altogether [17]. Besides improved current handling, MPDs offer improved fault

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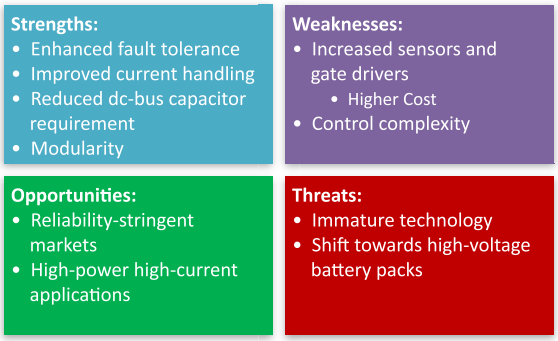


**FIGURE 1.** Strengths, weaknesses, opportunities, and threats (SWOT) analysis of multiphase inverters (MPIs).

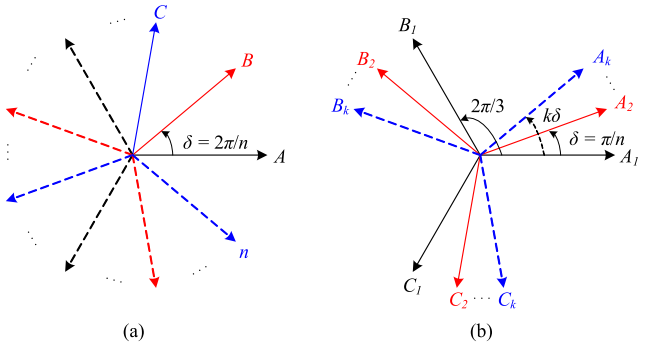


**FIGURE 2.** General phase distribution in $n$-phase inverters for different spatial displacement configurations. (a) Symmetric: $\delta = 2\pi/n$. (b) Asymmetric: $\delta = \pi/n$, $k = (n-3)/3$ for $n$ multiples of 3.

tolerance capability, lower torque pulsations, better noise characteristics, and modularity [16], [18].

Whether to use a multilevel inverter or a multiphase drive is a subtle question, and rather application-oriented. Increasing the powertrain voltage rating is attractive for electric vehicles (EVs) as it enables fast charging and reduces cabling footprint. On the other hand, it compounds insulation requirements. Improper insulation leads to partial discharge, which in turn causes machine failures [19]. This poses a serious threat for more electric aircrafts (MEA), for example, where reliability is of utmost importance. In such applications, meeting high power demand can be achieved by increasing the current supply at a relatively low voltage, around 400 V [20]. Heavy-duty vehicles resemble another example of high-power electrified powertrain. In such cases, MPDs are more suitable, thanks to their reduced per-phase current requirements. From another perspective, electrified aircrafts can also exploit MPDs to leverage reliability as multiphase drives have superior fault-tolerance capabilities. Fig. 1 summarizes the pros and cons of MPIs.

Both technologies, MLI and MPI, have been widely investigated in literature. Application of MLIs in transportation electrification was recently reviewed in [9]. MPDs for traction applications was reviewed [16], with a focus on six-phase drives. A little attention, though, has been paid to multiphase inverters (MPIs). This arises from the notion that conventional three-phase inverters are extendable to MPIs by simply adding additional switching legs to the existing ones [21]. Another reason is the modularity of six-phase machines with two isolated neutrals, which can be treated as two three-phase sets, commonly known as *dual three-phase* machines [22]. In principle, for $n$-phase machine with $n$ multiples of three, the system can be decomposed into $n/3$ three-phase systems [23]. Thus, as far as hardware implementation is concerned, these machines can be driven by multiple three-phase inverters. While such reasoning is valid, the resulting MPI is usually oversized with switches rated at twice the rated current and two dc-bus capacitors, in the case of six-phase drives.

Proper considerations invested in MPI design can yield improved inverter design. Along with addressing the aforementioned device paralleling issues, input parasitic can be made smaller, thanks to improved current handling in MPIs. Therefore, a higher power density can be achieved. To this end, this paper presents an in-depth review of MPIs for traction applications. More specifically, two MPI topologies are reviewed: voltage source inverter (VSI) and nine-switch inverter (NSI). The selection of those topologies is based on their potential for the applications listed in Fig. 1.

This paper is organized as follows. Modeling techniques for MPIs are discussed in Section II. Sections III and IV review multiphase VSI and NSI, respectively. Section V investigates the future trends for MPIs and the challenges hindering their adoption. Finally, Section VI concludes the paper.

## II. MODELING OF MULTIPHASE INVERTERS

The spatial displacement between the phases, $\delta$ can be symmetric or asymmetric. For symmetric systems, each two consecutive phases are $\delta = 2\pi/n$ apart. Asymmetric distribution is exclusive to $n$-phase system where $n$ is a multiple of three. In this case, the system is composed of $n/3$ multiples of three-phase systems with a displacement of $\delta = \pi/n$ between each three-phase set. Fig. 2 depicts the general phase distribution for symmetric and asymmetric MPIs.

Modeling of MPIs is an $n$-dimensional problem. There are two main methods to model $n$-phase inverters, namely vector space decomposition (VSD) and multiple $dq$. The two modeling approaches are reviewed in this section for multiphase inverters, in addition to the general structure of the current control loop based on such approaches.

### A. VECTOR SPACE DECOMPOSITION (VSD)

The VSD technique is applicable to any $n$-phase system and any spatial displacement configuration. It decomposes the $n$-dimensional system into multiple orthogonal 2D planes or subspaces [24]. For example, the vectors in six-phase inverter—six-dimensional—are mapped into three two-dimensional subspaces, namely $\alpha$–$\beta$, $x$–$y$, and $0_1$–$0_2$.

**TABLE 1. Harmonic mapping into different planes using VSD transformation for multiphase systems ($k = 0, 1, 2, 3 \ldots, m = 1, 3, 5 \ldots$).**

| Plane | 5-Phase | 6-Phase | 7-Phase | 9-Phase |
|---|---|---|---|---|
| $\alpha-\beta$ | $10k \pm 1$ (1,9,11...) | $12k \pm 1$ (1,13,25...) | $14k \pm 1$ (1,13,15...) | $18k + 1$ (1,19,37...) |
| $x_1-y_1$ | $10k \pm 3$ (3,7,13...) | $6m \pm 1$ (5,7,17...) | $14k \pm 5$ (5,9,19...) | $18k + 17$, $8m \pm 4$ (5,13,17...) |
| $x_2-y_2$ | — | — | $14k \pm 7$ (3,11,17...) | $9k \pm 2$ (7,11,25...) |
| Zero sequence | $5(2k + 1)$ (5,15,25...) | $3(2k + 1)$ (3,9,15...) | $7(2k + 1)$ (7,21,35...) | $3(2k + 1)$ (3,9,15...) |

Clarke's transformation is extended to $n$-phase to yield a single transformation matrix for the multiphase space. The VSD transformation is equally applicable for symmetric and asymmetric MPIs. The power-invariant VSD transformation, in the complex vector form, for symmetric $n$-phase MPI is given in (1), as shown at the bottom of the page, where $f_{-\alpha-\beta} = f_\alpha + jf_\beta$ and $f$ can be any $n$-phase variable, e.g. voltage or current. Similarly, $f_X$, $X \in \{A, B, \ldots, n\}$ is the $X$-phase variable in the stationary $ABC \ldots n$ frame.

The vector mapping is selected in such a way that the fundamental component is mapped into the $\alpha$–$\beta$ plane, whereas low order harmonics and zero-sequence components are mapped into the $x$–$y$ and $0_1$–$0_2$ planes, respectively. Applying the VSD transformation to MPIs with $n > 6$ yields multiple $x_k$–$y_k$ planes, $k \in [1, 2, ..]$. A general formulation for $k$ in terms of $n$ cannot be established. Five- and Six-phase MPIs have a single $x$–$y$ plane, while seven- and nine-phase MPIs have two $x$-$y$ planes [25], [26]. Additionally, applying VSD transformation to MPIs with odd number of phases, $n$, produces a single zero-sequence component ($0_2 = 0$), whereas two zero sequence components are produced in inverters with $n$ even phases [27]. A special case, however, is asymmetric MPIs with $3j, j \in [1, 2, \ldots]$ isolated neutrals. In such a configuration, all the vectors in $0_1$–$0_2$ are mapped at the origin, thus, nullifying the zero-sequence subspace [28]. Table 1 summarizes the harmonic mapping of the VSD transformation in the 2D orthogonal subspaces for five-, six-, seven-, and nine-phase MPIs.

### B. MULTIPLE D–Q

Known in the literature as double $d$–$q$ for six-phase inverters [16], the notion is extended herein to *multiple* $d$–$q$ for MPIs with $n$ multiples of three. Alternative to the VSD modeling, which treats the $n$-dimensional space as one, the multiple $d$–$q$ decomposes the system into multiples of three-phase systems [29]. While multiple $d$–$q$ is applicable to symmetric and asymmetric spatial distributions, it is only famous for the latter in the literature.

Each three-phase set is transformed using Clarke's and Park's transformation. The stationary frames, $\alpha_k$–$\beta_k$ obtained from Clarke's transformation are transformed into the rotational frame using Park's transformation with a phase shift of $k\delta$, $k \in [1, 2, \ldots, (n-3)/3]$. In this case, the same Clarke's transformation is used for all $\alpha_k$–$\beta_k$ frames. Thus, the transformations can be defined as:

$$\begin{aligned}
[f_{\alpha 1} \quad f_{\beta 1}]^T &= \mathbf{T_3}\,[f_{A1} \quad f_{B1} \quad f_{C1}]^T \\
[f_{\alpha 2} \quad f_{\beta 2}]^T &= \mathbf{T_3}\,[f_{A2} \quad f_{B2} \quad f_{C2}]^T \\
&\vdots \\
[f_{\alpha k} \quad f_{\beta k}]^T &= \mathbf{T_3}\,[f_{Ak} \quad f_{Bk} \quad f_{Ck}]^T,
\end{aligned} \tag{2}$$

$$\begin{aligned}
f_{-d1-q1} &= e^{j\theta} f_{-\alpha 1-\beta 1} \\
f_{-d2-q2} &= e^{j(\theta+\delta)} f_{-\alpha 2-\beta 2} \\
&\vdots \\
f_{-dk-qk} &= e^{j(\theta+k\delta)} f_{-\alpha k-\beta k},
\end{aligned} \tag{3}$$

$$\mathbf{T_3} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \tag{4}$$

where $\theta \in [0, 2\pi]$ is the angular position. The resulting $d$-$q$ frame is considered to be the sum of all $d_i$-$q_i$ components, i.e. $f_{d,q} = f_{d1,q1} + f_{d2,q2} + \cdots + f_{dk,qk}$.

### C. VECTOR-ORIENTED CONTROL

Fig. 3 depicts the general structure for the current control of MPIs using VSD and multiple $d$-$q$ modeling techniques. In VSD (Fig. 3a), the $n$-phase currents are transformed into the stationary frame using $\mathbf{T_{VSD}}$ in (1). Only the $\alpha$-$\beta$ frame is transformed to the synchronous $d$-$q$ frame using Park's transformation, whereas current components in the $x_i$-$y_i$, $i = 1, 2, \ldots, k$ are controlled in the stationary frame. Since the latter components carry the undesired harmonics, they are controlled to zero. The employed controllers can be proportional-integral (PI), proportional-resonant (PR), a combination of both [30], or model predictive controller (MPC) [31]. The output of the current controllers, i.e. reference voltages, are mapped back to phasor quantities using inverse transformations. The reference phase voltages are

$$\begin{bmatrix} f_{-\alpha-\beta} \\ f_{-x_1-y_1} \\ \vdots \\ f_{-x_k-y_k} \\ f_{-0_1-0_2} \end{bmatrix} = \frac{2}{n} \underbrace{\begin{bmatrix} 1 & a & a^2 & a^3 & \cdots & a^{(n-1)} \\ 1 & a^2 & a^4 & a^6 & \cdots & a^{2(n-1)} \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ a^{(k+1)} & a^{2(k+1)} & a^{3(k+1)} & a^{4(k+1)} & \cdots & a^{(k+1)(n-1)} \\ b & b^7 & b & b^7 & \cdots & b \end{bmatrix}}_{\mathbf{T_{VSD}}} \begin{bmatrix} f_A \\ f_B \\ \vdots \\ f_n \end{bmatrix}, \quad \begin{aligned} a &= e^{j2\pi/n} \\ b &= e^{j\pi/4} \end{aligned} \tag{1}$$

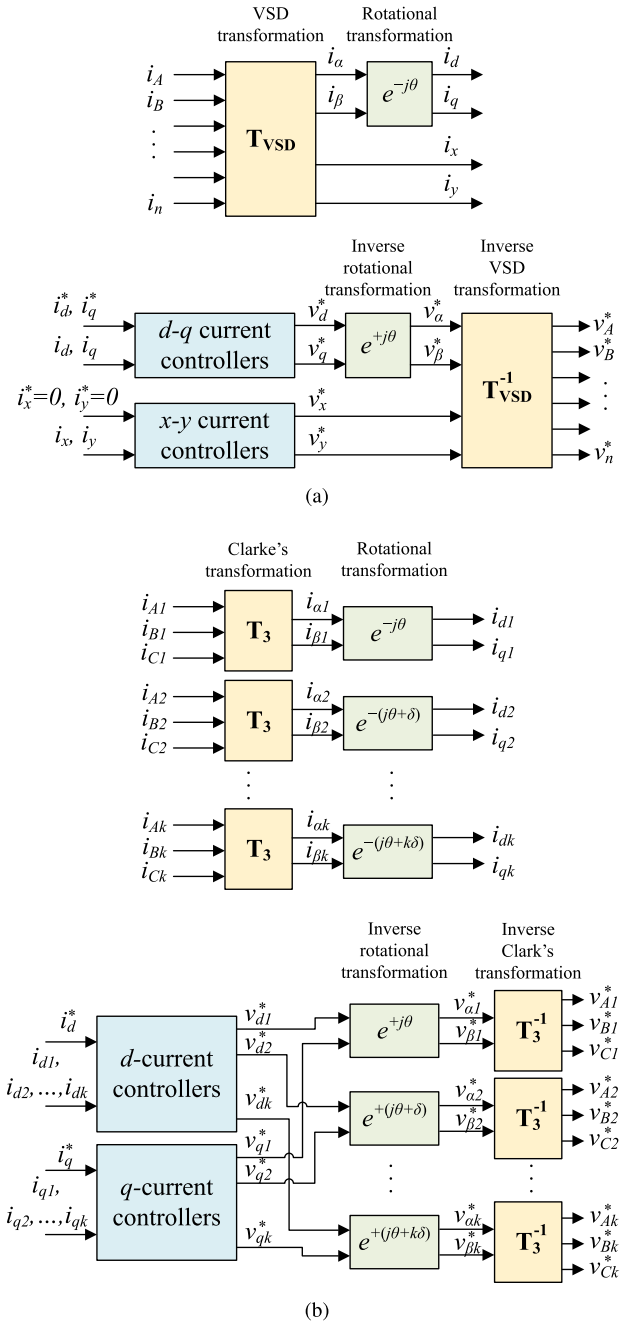


**FIGURE 3.** General current control structure of MPIs using the two different modeling techniques. (a) VSD modeling: $\mathbf{T_{VSD}}$ is given in (1). (b) Multiple $d$–$q$ modeling: $\mathbf{T_3}$ is Clarke's transformation, $\delta = \pi/n$ and $k = (n-3)/3$ for $n$ multiples of 3.

then used to generate the switching pulses. Note that an additional zero-sequence controller(s) is required when the $n$-phase inverter is connected to a single neutral point [32].

Current control in multiple $d$–$q$ (Fig. 3b) is straightforward. Currents are transformed into multiple $d$-$q$ frames using Clarke's and Park's transformations given in (2) and (3), respectively. Each $i_{di,qi}$ ($i \in [1, 2, \ldots, k], k = (n-3)/3$) is controlled to a reference $d$- and $q$-axis current, $i^*_{d,q}$.

**TABLE 2.** Comparison between VSD and multiple $d$–$q$ modeling for MPIs.

| Modeling Technique | VSD | Multiple d–q |
|---|---|---|
| **Applicable to** | any $n$ | $n$ multiple of 3 |
| **Physical interpretation of subspaces** | Fund. & low-order harmonics | Contributions of fund. component from each 3-ph set |
| **Asymmetry compensation** | Yes | No |
| **Integration of 3-ph control techniques** | Simple | Complex |
| **Specific modulation schemes** | $n$-dimensional SVPWM | Vector classification |

The number of required controllers in both modeling techniques is usually the same, regardless of spatial distribution (Fig. 2). For example, for a six-phase inverter with two isolated neutrals, four PI controllers are required in the VSD to control $d$-, $q$-, $x$-, and $y$-currents. In multiple $d$–$q$, the same controllers regulate $d_1$-, $q_1$-, $d_2$-, and $q_2$-currents. A similar performance can be achieved using both modeling techniques when the system is balanced [29]. However, multiple $d$–$q$ is unable to correct for system asymmetries such as magnitude unbalance or inverter dead-time compensation. This is because the contribution of each $d$–$q$ subspace to such asymmetries is usually undetermined. In this case, current control in VSD is superior as $xy$-currents can be exploited to correct for system asymmetries [30]. Furthermore, from drives perspective, integration of existing three-phase controls, such as flux-weakening, is seamless in VSD since the MPD is treated as a single system in the synchronous $dq$-frame [33], [34]. For such attributes, in addition to generality, VSD modeling is favored over multiple $d$–$q$. Table 2 summarizes the comparison between VSD and multiple $d$–$q$ modeling.

After establishing the modeling techniques and the general vector control structure of MPIs, the most relevant MPI topologies are reviewed next.

## III. MULTIPHASE VOLTAGE SOURCE INVERTER

Owing to its simplicity, high efficiency and low cost, voltage source inverter (VSI) is the most commonly used inverter topology in transportation electrification applications [35]. This holds true irrespective of the number of phases, $n$ or the type of the load machine [21]. Nevertheless, multiphase VSIs have distinctive attributes that distinguish them from their conventional three-phase counterpart, such as dc-bus capacitor sizing and modulation techniques. The remainder of this section reviews such features.

### A. TOPOLOGY

Fig. 4 depicts the two-level (2L) multiphase VSI topology with $n$ number of phases. For traction applications, Si IGBT and SiC MOSFET are the two most commonly used devices, with a breakdown voltage range of 600 V – 1700 V [36], [37]. The dc-link capacitor is an indispensable component in VSI

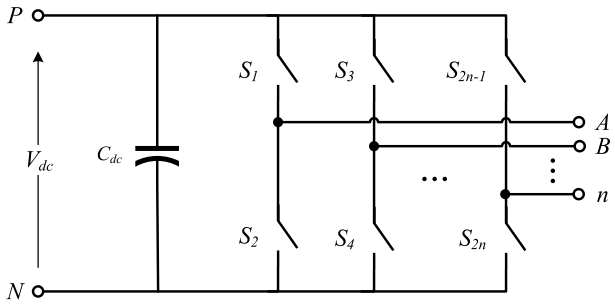


**FIGURE 4.** Multiphase voltage source inverter (VSI).

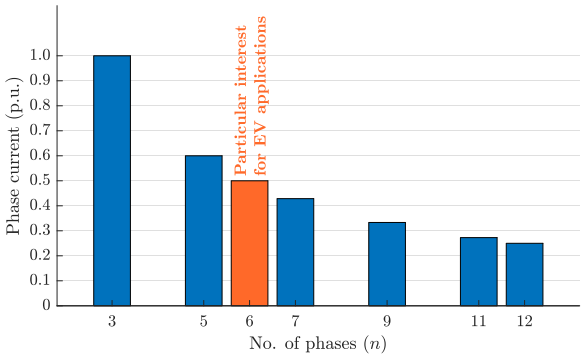


**FIGURE 5.** Reduced per-phase current requirement in MPIs.

as it reduces voltage fluctuations and current ripples [38]. The VSI is known for its high efficiency and low cost, however, it suffers some drawbacks. Firstly, the VSI exhibits a buck behavior where the output voltage level is lower than the dc-link voltage. Secondly, for high power applications, multiple power semiconductor devices are usually paralleled per switch, which poses design challenges as will be discussed next. Thirdly, the dc-bus capacitor is bulky and has a limited operating temperature range. In fact, it is the bottleneck in the face of achieving higher power densities as it occupies up to two thirds of the total volume of the inverter [16], [39]. While the first drawback is inherent in the VSI topology, multiphase VSIs alleviate the foregoing challenges as discussed next.

### B. PER-PHASE REQUIREMENTS

One of the most notable features of MPIs is the reduced per-phase current. The phase current of MPIs can be defined with respect to their three-phase counterpart as:

$$I_{n-\phi} = \frac{3}{n} I_{3-\phi}, \quad n \geq 3 \tag{5}$$

The reduction in per-phase current in MPIs with respect to three-phase VSI is depicted in Fig. 5. The higher the number of phases the lower the per-phase current requirement is. However, this trend exhibits a diminishing return where at a certain point the reduction in per-phase current is no longer appreciated in the face of increased complexity. On the other hand, $n$-phase MPIs have, in large part, the same cost, owing to the same volt-ampere (VA) rating. The inverter VA rating reflects the power rating of the semiconductor switches, which in turn drives the cost in large part [40], [41]. The VA rating is given based on the per-unit voltage stress, $E$ and the per-unit current stress, $I$, multiplied by the total number of switches, $k$. Note that $E$ is the rated blocking voltage of the switches and is equal to $V_{dc}$ for 2L MPIs. Since there are two switches per leg in an $n$-phase VSI (i.e. $k = 2n$), the VA rating can be defined as:

$$VA = (2n) \times E \times I_{n-\phi} \tag{6}$$

Substituting (5) in (6) yields $6EI$, irrespective of $n$.

The significance of the reduction in per-phase requirements is twofold. Firstly, it enables the use of smaller and lighter cables. The considerable reduction in cable size outweighs the increase in number of cables rendering a lower cost overall. This is demonstrated in Table 3, where AC cable sizing and pricing is calculated based on a 100 kW, 0.8 PF, and 230 V system for MPIs with $n \geq 3$. Compared to the conventional three-phase VSI, a six-phase VSI yields a 21% reduction in cabling cost.

**TABLE 3.** AC cable sizing and cost for MPIs to deliver 100 kW at 230 VAC and 0.8 PF (length ≤ 10 m).

| $n$ | Per-Phase Current (A) | Cable Size (AWG)† | Cable Unit Price (USD/m)‡ | Total Price (USD/m) |
|---|---|---|---|---|
| 3 | 181 | 1 | 36.9 | 110.8 |
| 5 | 109 | 4 | 21.2 | 105.8 |
| 6 | 91 | 6 | 14.6 | 87.4 |
| 7 | 78 | 6 | 14.6 | 101.9 |
| 9 | 60 | 8 | 10.1 | 91.2 |

†Calculated using the online tool in [42] based on IEC 60364-5-52 standard for Copper conductor

‡Based on shielded single-core motor cables from Igus® [43]

Secondly, the reduction in per-phase current mitigates the current limitation of the employed power semiconductor devices, especially SiC MOSFET. As of this writing, the maximum current rating of commercially available, automotive-grade discrete SiC MOSFETs is around a 100 A (see Table 7 in [37]). This limitation renders paralleling of multiple discrete devices in three-phase inverters inevitable. Tesla's Model 3 (2018), for example, employs four discrete SiC MOSFET devices per switch [11], [44]. Device paralleling makes the design of gate drivers more challenging to ensure proper dynamic and static current sharing among the paralleled devices [13]–[15]. Mismatches among the paralleled devices lead to current unbalance, which in turn causes localized over-temperature [14]. According to [15], $R_{ON}$, pinch-off voltage (which determines at what gate voltage the device enters forward conduction mode), reverse breakdown voltage of the gate, transconductance, and device placement on the circuit are all factors that should be carefully monitored/designed to ensure proper operation of the paralleled devices.

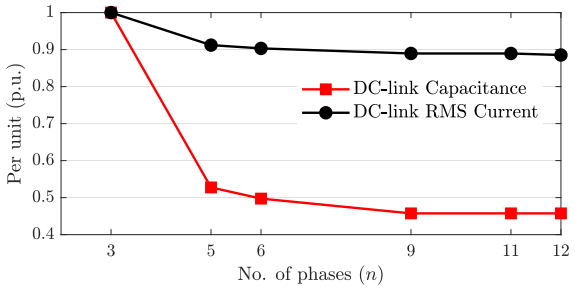


**FIGURE 6.** Normalized dc-link capacitor requirements for multiphase VSI with different phase number, $n$ in terms of capacitance and RMS current using SPWM [39].

### C. DC CAPACITOR REQUIREMENT REDUCTION

Multiphase VSIs offer reduced capacitor requirements in terms of capacitance and physical volume [39]. The capacitance, $C_{dc}$ is determined based on the allowable dc-voltage ripple (typically 5%) [45]. It was shown in [39] that the required $C_{dc}$ decreases with increasing phase number. A 50% capacitance reduction can be achieved in six-phase VSI. Additionally, the dc-voltage ripple is inversely proportional with $C_{dc}$ and switching frequency. This means that the same voltage ripple can be achieved with a lower $C_{dc}$ and higher switching frequency using SiC devices. The volume of the dc-bus capacitor, on the other hand, is dictated by the dc-link RMS current [23], [45]–[48], which depends on a couple of factors including modulation technique, modulation index, and power factor (PF). Similarly, the increased number of phases can decrease the dc-link RMS current, but the reduction is not as appealing. Yet, since the dc-bus capacitor can take up to two thirds of the total volume of the traction inverter [16], even a small reduction is appreciated nonetheless. A 10% reduction in the dc-link RMS current for $n \geq 6$ was demonstrated in [39]. Fig. 6 illustrates the reduction in the $C_{dc}$ and dc-link RMS current for multiphase VSI with different $n$, with respect to three-phase VSI.

### D. MODULATION

The basic PWM modulation techniques of three-phase systems are extendable to multiphase inverters. The majority of available techniques, irrespective of inverter topology, can be classified into two groups: carrier-based PWM (CBPWM) and space vector PWM (SVPWM) [49], which are discussed in this subsection. Fig. 8 depicts the classification of the most common modulation techniques for multiphase VSI.

#### 1) CBPWM

CBPWM is the most favorable technique for multiphase inverters. This is due to the high number of permissible states in SVPWM that incurs a heavy computational burden. Furthermore, a comparison between CBPWM and SVPWM in 2L seven-phase VSI in [50], in terms of voltage and current THD, concluded that both techniques exhibit a similar performance. Hence, CBPWM is deemed a simpler yet effective technique for multiphase systems. Similar to three-phase inverters, the carrier is either a periodic triangular or sawtooth signal that control the gating signals when compared to $n$ number of modulating sinusoidal signals, for multiphase VSI with $n$-phases. The CBPWM with a single carrier is commonly known as sinusoidal PWM (SPWM). Unlike three-phase VSIs, the additional legs in multiphase inverters provide an additional degree of freedom to address PWM-associated issues. For example, CBPWM techniques that reduce the common-mode voltage (CMV) in five-phase VSI were suggested in [51] and [52].

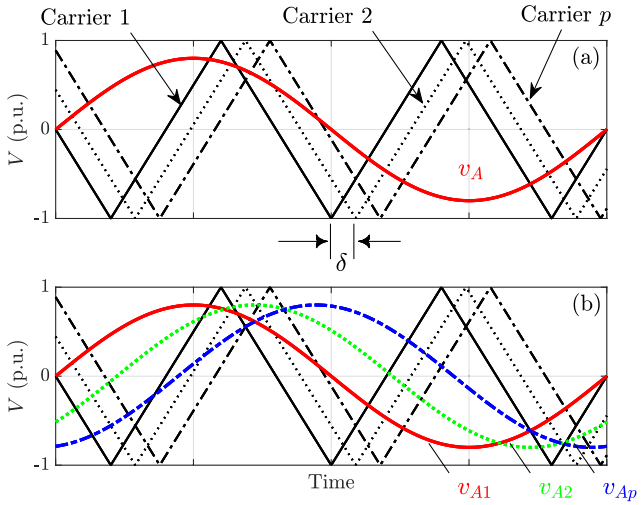


**FIGURE 7.** Interleaved CBPWM techniques for $n$-phase inverter where $n = p \cdot m$ is a multiple of three and $m = 3$. (a) Three-phase modulating signals, $m = 3$ with $p$ carriers. (b) $n$-phase modulating signals, $p \cdot m = n$ and $p$ carriers.

Extension beyond the traditional SPWM to interleaved multi-carrier techniques for multiphase inverters have been suggested for $n$ multiples of three. In interleaved multi-carrier PWM, the $n$ phases are divided into $p$ groups of $m$ phases, $n = p \cdot m$. A multiple of $p$ carriers, shifted by $\delta$ degrees, can be used to modulate $m = 3$ signals to generate the gate pulses for $n$ switches, as shown in Fig. 7a. This strategy was implemented and reported in [53] on a 15-phase inverter. Implementation of such interleaving technique in [54] resulted in a 60% volume reduction in the dc-bus capacitor for a 55 kW six-phase inverter. However, this strategy is only limited to a segmented MPD[1] and reduces the $n$-dimensional control to 3-dimensional. In other words, some degrees of freedom are lost. Alternatively, the same $p$ carriers can be used to modulate the $n$ phases, as shown in Fig. 7b. Furthermore, phase-shifted PWM (PS-PWM) with $n$ number of carriers, with $\delta$ phase shift between two consecutive carriers, was proposed in [55] for five- and six-phase 2L VSI in order to reduce the CMV. However, the high number of carriers increases the computational time dramatically.

Despite its simple implementation, CBPWM suffers low dc-link voltage utilization. The maximum level of dc-link

[1]Motor drive segmentation is to segment inverter switches and motor windings to form multiple parallel connected three-phase drive units.

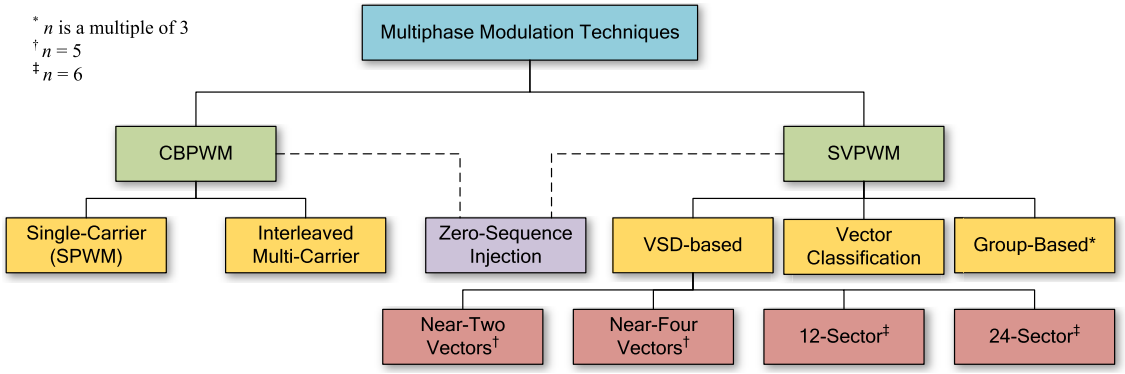


**FIGURE 8.** Classification of modulation techniques for multiphase inverters.

utilization is determined by the modulation index, $M$. The $M$ is defined as the ratio of the peak fundamental-component of the phase voltage, $\hat{V}_1$ to one half of $V_{dc}$:

$$M = \frac{\hat{V}_1}{0.5V_{dc}} \tag{7}$$

In linear modulation region, the maximum output voltage is $0.5V_{dc}$ (i.e. $M_{max} = 1$), regardless of the number of phases [50]. CBPWM techniques in conjunction with zero-sequence injection (ZSI) were proposed for multiphase inverters in order to improve the dc-link utilization [56], increase the torque density [57], and reduce output distortion [58]. Analogous to third-harmonic injection in three-phase VSI, $n^{\text{th}}$ harmonic injection for multiphase VSI with $n$ odd phases was suggested in [56]. The $M_{max}$ for $n$ odd number of phases is defined as [59]:

$$M_{max} = \frac{1}{\cos\left(\pi/2n\right)}, \quad n \in \{3, 5, 7, \dots\} \tag{8}$$

For example, 5$^{\text{th}}$ harmonic injection in CBPWM for five-phase 2L VSI results in 5.15% increase in output fundamental voltage, making it equal to that of SVPWM. A special case is $n = 6$, where (8) is only applicable when the load has asymmetric windings with a single neutral point [60]. Alternatively, multiple ZSIs can be applied to achieve a 15.4% dc-link voltage utilization, similar to SVPWM, when $n$ is a multiple of three and the neutral points are isolated [61]. For example, six-phase VSI with dual ZSIs was demonstrated in [62]. Table 4 summarizes the maximum attainable $M_{max}$ in multiphase inverters with single and multiple ZSI for symmetric and asymmetric loads.

### 2) SVPWM

In spite of its complexity, SVPWM is yet attractive in multiphase traction inverters owing to its improved dc-bus voltage utilization, lower harmonic components, and improved fault tolerance owing to the redundant switching states for the same voltage vectors. This redundancy also provides the designer with an additional degree of freedom to optimize the performance based on a desired criterion.

**TABLE 4.** Percentage increase in maximum modulation index in multiphase inverters using single and multiple zero sequence injections (ZSIs).

| No. Phases | Phase Spatial Displacement | Single ZSI | Multiple ZSI |
|---|---|---|---|
| 3 | Symmetric | 15.4 | — |
| 5 | Symmetric | 5.15 | — |
| 6 | Symmetric<br>Asymmetric | —<br>3.53 | 1.54 |
| 7 | Symmetric | 2.57 | — |
| 9 | Symmetric<br>Asymmetric | 1.54 | 1.54 |

Numerous SVPWM techniques have been proposed in the literature for MPIs. The different techniques vary in the applied vectors and/or switching sequence. Consequently, different maximum modulation indices are derived. Nonetheless, many of the proposed techniques are based on the VSD approach discussed in Section II-A.

The $\alpha$–$\beta$ and $x$–$y$ subspaces are commonly referred to as torque-producing subspace and harmonic-producing subspace, respectively. Put otherwise, the vectors in $\alpha$–$\beta$ subspace contain the fundamental components of the machine that produce a rotating magnetomotive force, while the vectors in $x$–$y$ subspace only produce losses. Hence, modulation techniques usually focus on minimizing the $x$–$y$ subspace contribution. While completely eliminating its effect is impossible, using the volt–second principle alternating vectors in $x$–$y$ subspace can be chosen to produce a zero average of those components. Note that for multiphase inverters with $n > 6$ there exist more than one $x$–$y$ subspaces (see Table 1).

VSD-based SVPWM for $n = 5$ decomposes the 5D space into two orthogonal subspaces, $\alpha$–$\beta$ and $x$–$y$. In general, for any $n$ odd number of phases, voltage and current vectors are mapped into $(n-1)/2$ orthogonal subspaces. Fig. 9 depicts the voltage vectors in 2L five-phase VSI, where the vectors form two concentric decagons. In VSI, there exist $2^5 = 32$ voltage vectors, of which 30 are active [63]. Those vectors are categorized in three groups: large, medium, and small vectors. SVPWM techniques for 2L five-phase VSI

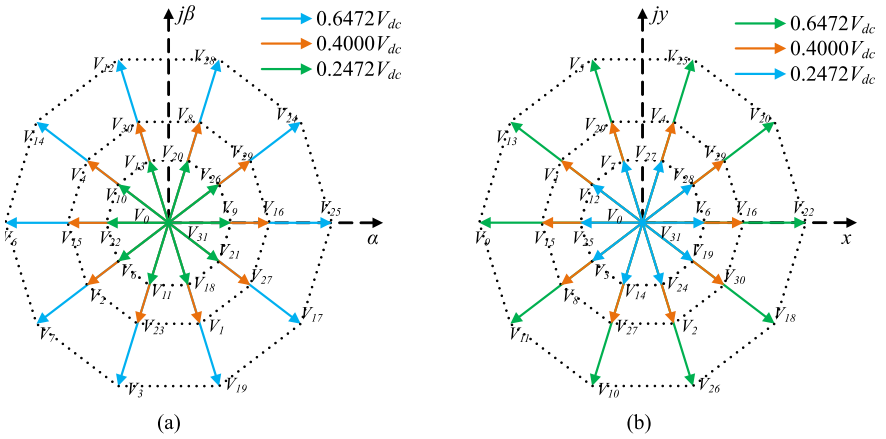


**FIGURE 9.** All possible voltage vectors in five-phase 2L VSI and their projection on (a) $\alpha$–$\beta$ subspace, and (b) $x$–$y$ subspace.

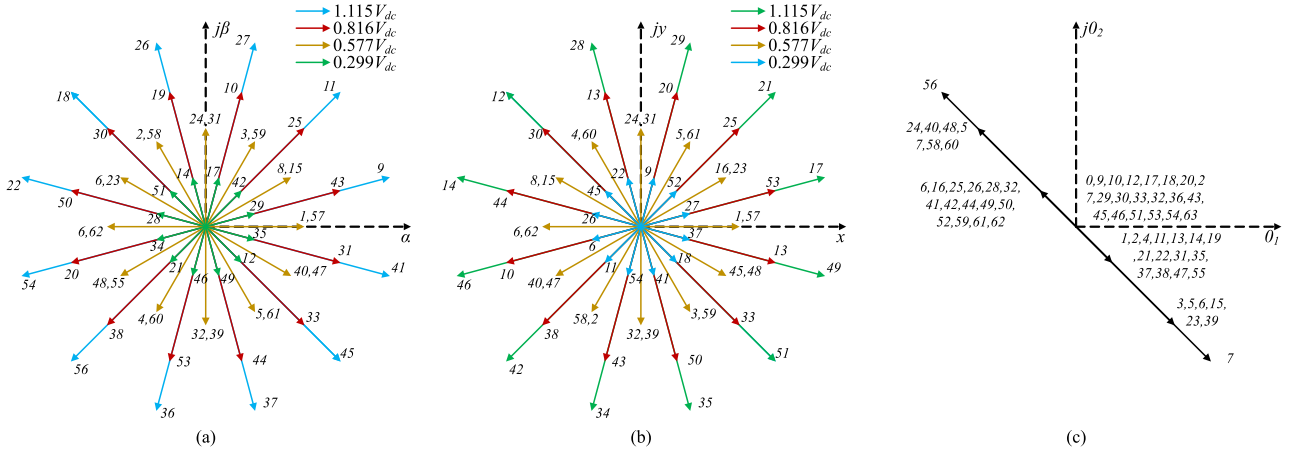


**FIGURE 10.** All possible voltage vectors in six-phase 2L VSI and their projection on (a) $\alpha$–$\beta$ subspace, (b) $x$–$y$ subspace, and (c) $0_1$–$0_2$ subspace.

are normally classified, based on voltage vectors selection, as near-two vectors (NTV) and near-four vectors (NFV) [64]. While NTV techniques enjoy a superior maximum modulation index, NFV techniques are preferred for their 3rd harmonic suppression capability.

VSD-based SVPWM for $n = 6$ can be classified as 12-sector based [24], [58], [65], [66] and 24-sector based techniques [67]–[69]. The latter is digitally easier to implement and yields reduced current harmonic distortion. However, two transitions belonging to two or more inverter legs occur at the same time during a sampling period [67]. As a result, asymmetric PWM waveforms are expected. On the other hand, the digital implementation of 12-sector modulation techniques is challenging since inverter legs can switch more than once in a switching period. In both schemes, the vectors are categorized in four groups: large, medium-large, medium, and small vectors, as shown in Fig. 10. The switching sequence and the applied zero vector yields continuous or discontinuous (DPWM) modulation [65], [69], [70]. In continuous modulation, all switching legs change their on/off state within one switching period at least once, whereas one (or more) leg(s) is clamped to $+V_{dc}$ or $-V_{dc}$ for at least one sector in DPWM. Discontinuous SVPWM techniques can reduce the implementation complexity at the cost of higher distortions [70], [71].

Numerous VSD-based SVPWM techniques for MPIs are invested in the reduction of CMV, induced by the high-frequency modulated inverters. The CMV excites a common-mode current, which is detrimental for many applications including motor drives and PV systems [81], [82]. The excited common-mode current contributes to motor aging rate by causing a bearing damage, insulation breakdown and electromagnetic interference (EMI) [83]. For $n$-phase VSI, the CMV varies in the range of $\pm 0.5V_{dc}$, regardless of $n$. However, the number of levels in CMV increases with $n$. Figs. 11 demonstrates the CMV in 2L VSI with $n \in \{3, 5, 6, 7\}$ when conventional SVPWM is employed. Hence, the higher the phase count the higher the degrees of freedom are to be exploited to reduce the CMV. CMV reduction based on SVPWM techniques for five-phase VSI was investigated in [72]–[76], [83]. The conventional SVPWM technique for five-phase VSIs employs large, medium and zero vectors.

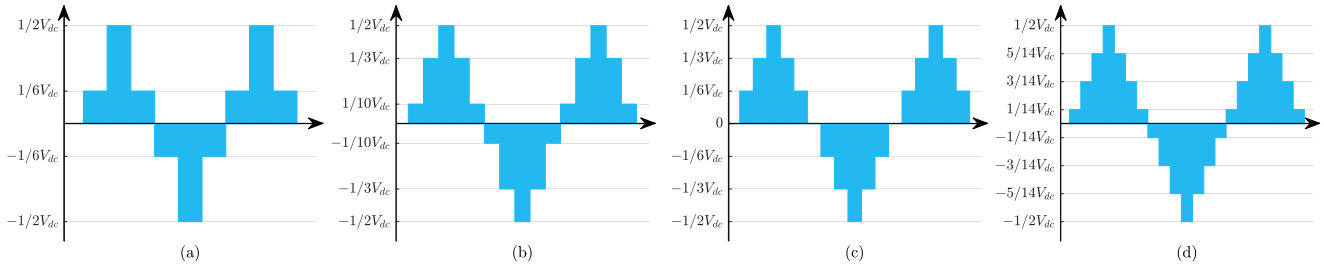


**FIGURE 11.** Common-mode voltage (CMV) waveform in 2-level multiphase VSIs as a function of dc-bus voltage. (a) $n = 3$. (b) $n = 5$. (c) $n = 6$. (d) $n = 7$.

**TABLE 5.** Survey on SVPWM techniques for common mode voltage (CMV) reduction in multiphase VSI.

| $n$ | Ref. | Vector Selection | ΔCMV | Voltage THD | Current THD | SW Loss | Modulation Range |
|---|---|---|---|---|---|---|---|
| 5 | [72] | (Conventional) Large, Medium & Zero | $\pm 0.5V_{dc}$ | Good | Good | Good | $0 \le M \le 1.05$ |
| | [72] | Large, Medium & Phase-Opposed | $\pm 0.3V_{dc}$ | Poor | Good | Good | $0 \le M \le 1.05$ |
| | [72] | Large, Adjacent Large & Phase-Opposed | $\pm 0.1V_{dc}$ | Poor | Medium | Poor | $0 \le M \le 1.05$ |
| | [73] | 10 Larges | $\pm 0.1V_{dc}$ | Poor | Poor | Good | $0 \le M \le 1.05$ |
| | [73] | Large & Medium | $\pm 0.4V_{dc}$ | Good | Good | NR | $0 \le M \le 1.05$ |
| | [74] | 5 Mediums | 0 | NR | Good | NR | $0 \le M \le 0.55$ |
| | [74] | 10 Mediums | $\pm 0.3V_{dc}$ | NR | NR | NR | $0 \le M \le 0.65$ |
| | [74] | 5 Larges | 0 | NR | Medium | NR | $0 \le M \le 0.89$ |
| | [75] | 5 near-state Larges | $\pm 0.1V_{dc}$ | Poor | Poor | Medium | $0.88 \le M \le 1.05$ |
| | [76] | Large, Medium & Phase-Opposed, but Odd or Even vectors only | $\pm 0.2V_{dc}$ | Medium | NR | Poor | $0 \le M \le 0.89$ |
| | [77] | 4 Larges | $\pm 0.1V_{dc}$ | Medium | Good | Poor | $0 \le M \le 1.05$ |
| 6 | [24] | (Conventional) Large, Medium-large & Zero | $\pm 0.5V_{dc}$ | Good | Good | Good | $0 \le M \le 1.035$ |
| | [70] | Large, Medium-large, Medium & Small | $\pm 0.2V_{dc}$ | Good | Good | NR | $0 \le M \le 0.667$ |
| | [78] | Large, Medium-large, Small & Zero | 0 | Good | Medium | NR | $0 \le M \le 0.911$ |
| | [79] | Large, Medium-large & Small | 0 | Medium | Medium | Poor | $0 \le M \le 0.928$ |
| 7 | [50] | (Conventional) Large, Medium-large & Zero | $\pm 0.5V_{dc}$ | Good | Good | Good | $0 \le M \le 1.026$ |
| | [80] | 5 Larges | $\pm 0.1V_{dc}$ | Medium | Good | NR | $0 \le M \le 1.026$ |

NR: Not Reported.

The latter are responsible for the highest level of CVM (i.e. $\pm 0.5V_{dc}$). Hence, the suggested techniques in [72]–[76], [83] offer alternative switching techniques and patterns that eliminate the need for zero vectors, thus reducing the CMV. However, the reduction of CMV comes at the expense of performance deterioration in either voltage THD, current THD, switching loss, modulation range, or a combination of them.

Utilization of only medium vectors or only large vectors were suggested in [74]. Such techniques yield a constant CMV (i.e. $\Delta$CMV$= 0$). On the other hand, the RMS value of the CMV was still high. A competitive technique using only a combination of large vectors was suggested in [72] and employed in [83] for motor drives applications. This technique results in a CMV of $\pm 0.1V_{dc}$ while maintaining an adequate current THD. Its switching loss can also be improved when combined with the method suggested in [75] at high $M$. A MPC controller was proposed in [77] to improve the current performance while simultaneously reducing the CMV to $\pm 0.1V_{dc}$ and maintaining a full modulation range. This, however, is achieved at the expense of increased switching frequency.

Similarly, CMV reduction by SVPWM for $n = 6$ [70], [78], [79] and $n = 7$ [80] have been proposed. In [70], [79], and [80], zero vectors are avoided to reduce, and even eliminate, the variations in CMV at the expense of reduced modulation range. In [78], a phase shifting strategy for the PWM signals of a six-phase VSI supplying a dual three-phase asymmetric machine was proposed. The shifting strategy leads to two CMVs (from each three-phase set) that are 180° out of phase. As a result, the total CMV, which is the sum of both, is zero. Table 5 summarizes the VSD-based SVPWM techniques for for CMV reduction in multiphase VSIs.

Besides VSD, other SVPWM techniques have been investigated for 2L multiphase VSIs such as group-based and vector classification. When $n$ is a multiple of 3, the $n$-dimensional space can be treated as $n/3$ independent three-phase systems, given that the load has $n/3$ isolated neutrals. Such an approach is known as a group-based SVPWM. In [23] and [39], group-based SVPWM techniques were applied to 2L nine-phase VSI. An improved performance, in terms of voltage and current harmonics, was reported when compared to VSD-based SVPWM techniques. Additionally, it was demonstrated in [39] that group-based SVPWM can reduce dc-link capacitor requirements. More specifically, it was found that $C_{dc}$ in a nine-phase VSI with group-based SVPWM has to handle only one third of the dc-link RMS current when compared to a three-phase VSI modulated via

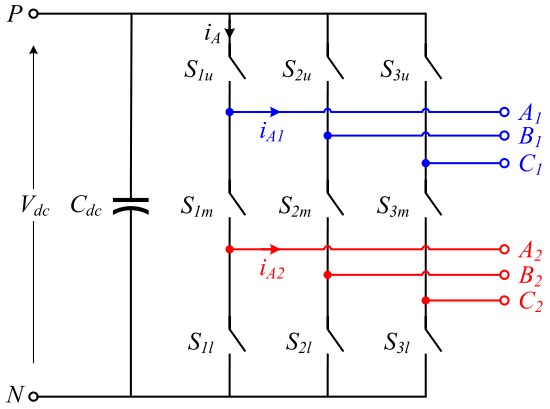


**FIGURE 12.** Nine-switch inverter (NSI) topology for six-phase machines ($S_u$, $S_m$, and $S_l$ are upper, middle, and lower switches, respectively).

SPWM. Hence, the modulation technique can play a key role in achieving a higher power density in multiphase inverters.

Vector classification (VC)-SVPWM was investigated in 2L six-phase VSI in [84]–[86]. The VC-SVPWM is based on the double $d$–$q$ modeling theory for multiphase systems. He *et al.* [86] compared VC-SVPWM to 12-sector VSD-based SVPWM techniques. They concluded that VC-SVPWM achieves a higher dc-bus voltage utilization with a simpler implementation, at the expense of higher output harmonics.

## IV. NINE-SWITCH INVERTER

Nine-switch inverter (NSI) is a special VSI topology. Originally conceived in the late 2000's to independently drive two three-phase machines with reduced switch count [87], NSI was later adopted for six-phase machines [88]–[93]. This section reviews the NSI topology and compares it to the six-phase VSI in terms of cost, control, and efficiency.

### A. TOPOLOGY

The NSI topology is depicted in Fig. 12, where a six-phase inverter is realized by three legs only, each comprising three switches. Instead of the twelve switches needed for six-phase machines in the traditional 2L VSI topology (Fig. 4), NSI utilizes only nine switches. The middle switches of the NSI, $S_m$ are controlled via an exclusive OR (XOR) logic gate to prevent a leg short-circuit, as detailed in the next subsection. The NSI topology is also extendable to any $(3n + 3)$-switch inverter, where $n$ is the number of three-phase sets [87]. For example, a 12-switch inverter can be developed for nine-phase applications with four switches per leg, in contrast to the 18 switches in nine-phase VSI.

While NSI employs reduced switch count, the current rating of its switches is relatively larger than their counterparts in six-phase VSI. Fig. 13 depicts the relationship between input leg current and output phase currents of the NSI for leg A, when connected to an asymmetric load (i.e. $\delta = 30°$). The input leg current is the vector summation of the two output phase currents as illustrated in Fig. 14. Its magnitude for an

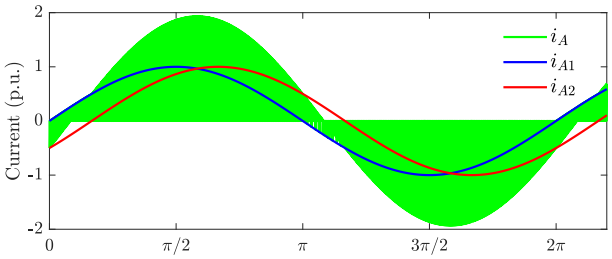


**FIGURE 13.** Current waveforms of leg A, $i_{legA}$ and associated phase currents, $i_{A1}$ and $i_{A2}$ of the NSI in Fig. 12 for asymmetric six-phase load (switching frequency: 30 kHz).

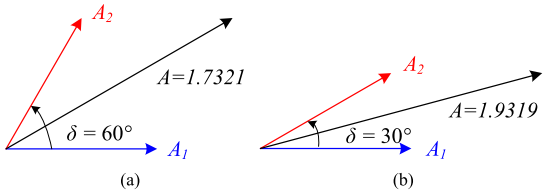


**FIGURE 14.** Input and output current vectors of leg A in six-phase NSI. (a) Symmetric. (b) Asymmetric.

arbitrary $\delta$, defined in Fig. 2, can be generally defined as:

$$I_A = \sqrt{2(1 + \cos\delta)} \cdot I_{A1} \tag{9}$$

where $I_A$ and $I_{A1}$ are the magnitude of leg and phase currents, respectively, as depicted in Fig. 12.

A fair comparison of inverter cost can be evaluated using the volt-ampere (VA) rating of the inverter, as discussed in Section III. Table 6 compares the inverter VA ratings of the NSI and VSI for the different load configurations. The values in Table 6 assumes three-phase VSI for base values. Since the discussion is limited to 2L inverters, the switches in both, VSI and NSI, are rated at $E$, irrespective of number of phases. The per-unit current rating, $I$ of the switches in VSI for $n$ phases is given in (5), whereas for NSI it is defined as:

$$\begin{aligned} I &= (3/n) \cdot I_A / I_{A1} \\ &= (3/n) \cdot \sqrt{2(1 + \cos\delta)}, \quad n = \{6, 9, \ldots\} \end{aligned} \tag{10}$$

From the VA rating comparison, it is evident that NSI has a higher cost compared to six-phase VSI. The total VA rating for VSI is always 6 p.u., as discussed in the previous section. Considering six-phase asymmetric machine as a load, the cost ratio of NSI to VSI is three to two. Power semiconductors dictate around 40% and 70% of the total cost of traction inverters in the case of Si IGBT and SiC MOSFET, respectively [94], [95]. Hence, the NSI topology could be more expensive than VSI. It also follows that the reduced switch count in NSI does not necessarily mean reduced cost.

At the expense of increased cost, NSI has the potential for higher power density owing to its reduced switch count and associated gate drivers. Furthermore, because the commutation time of the inverter legs is relatively larger, to supply two phase currents, the stress on the dc-bus capacitor is alleviated. In other words, there exists a current path from the switching

**TABLE 6.** VA rating comparison between VSI and NSI.

| No. Phases | Config. | VSI | | | NSI / 12-Switch Inverter | | |
|---|---|---|---|---|---|---|---|
| | | Switch Rating | Amount | Total | Switch Rating | Amount | Total |
| 6 | Symm. | $E \times 0.5I$ | 12 | $6EI$ | $E \times 0.87I$ | 9 | $8EI$ |
| | Asymm. | $E \times 0.5I$ | 12 | $6EI$ | $E \times 0.97I$ | 9 | $9EI$ |
| 9 | Symm. | $E \times 0.3I$ | 18 | $6EI$ | $E \times 0.63I$ | 12 | $8EI$ |
| | Asymm. | $E \times 0.3I$ | 18 | $6EI$ | $E \times 0.66I$ | 12 | $8EI$ |

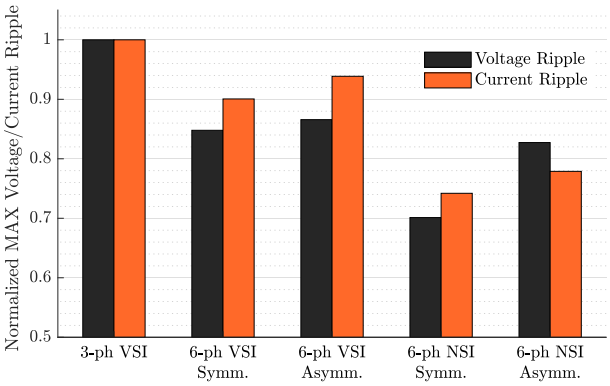


**FIGURE 15.** Normalized dc-link capacitor requirements for NSI compared to six-phase VSI for symmetric and asymmetric load configurations.

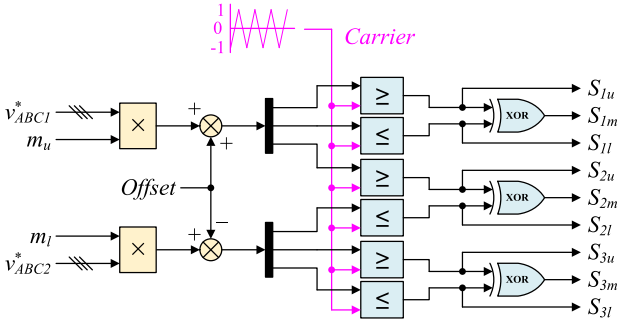


**FIGURE 16.** CBPWM scheme for NSI. $m_u$ and $m_l$ denote the modulation index for the upper and lower three-phase sets, respectively.

pole to the load for a longer time within one switching cycle, when compared to VSI. Therefore, less commutation spikes are experienced by the dc-capacitor in NSI. Fig. 15 compares the normalized maximum stress on the dc-link capacitor in VSI and NSI topologies. Judging by the maximum current stress, NSI can achieve dc-capacitor size reduction by approximately 16% when compared to its six-phase VSI counterpart, or 26% with respect to the conventional three-phase VSI.

One of the main drawbacks of the NSI, however, is the low dc-link voltage utilization by the established modulation techniques [16]. The NSI requires 20% or 33% higher input voltage with respect to its VSI counterpart in order to produce the same output power when the winding of the load machine is asymmetric or symmetric, respectively [88]. A NSI topology with a boosting feature has been recently proposed in [96] to overcome this issue. With the help of input inductor and diodes the boosting NSI yields a higher dc-link voltage utilization.

### B. MODULATION

Similar to the VSI topology, the modulation techniques of the NSI can generally be categorized into CBPWM and SVPWM techniques. Additionally, the operation of the NSI can be divided into common-frequency (CF) and different-frequency (DF) modes [97]. In CF mode, both three-phase sets (upper and lower sets in Fig. 12) operate at the same frequency, whereas in DF mode each of the two sets is operated at different frequency. Again, when the NSI is utilized to drive a six-phase machine, it is desired to have all sets operating at the same frequency, thus only CF mode is considered for multiphase drives applications. The CBPWM and SVPWM techniques of the CF mode of the NSI are reviewed in this subsection.

#### 1) CBPWM

Similar to the VSI, the reference voltages of the NSI are compared with a carrier waveform to produce the gating signals of the switches in CBPWM [88]–[90], [92]. However, there are three distinct differences in CBPWM for the NSI. Firstly, each three-phase set can be controlled independently, and as such, has its own modulation index. Secondly, to guarantee that each of the two three-phase sets supply the same power, the modulating signals of the two sets must not overlap. Consequently, a vertical offset in the positive and negative directions is added to the upper and lower three-phase sets, respectively. While the modulation index and the offset values can be different for each three-phase set, they are chosen to be the same when supplying a single six-phase machine [88]. Thirdly, as mentioned earlier, the gate signals of the middle switches are generated by XOR-ing the gate signals of the upper and lower switches to prevent a short-circuit. Fig. 16 depicts the CBPWM technique for the NSI.

As mentioned in the previous subsection, the modulation index of the NSI in CBPWM is influenced by the winding configuration of the six-phase machine. The maximum modulation index for the NSI topology, as a function of the spatial displacement between the two three-phase sets, $\delta$ is defined as [92]:

$$M_{max} = \frac{1}{1 + \sin \delta/2} \tag{11}$$

**TABLE 7. Comparison between modulation schemes for the NSI topology.**

| Modulation Technique | Ref. | Voltage THD | Max Modulation Index | | Thermal Distribution Among Switches | Switching Loss | Complexity |
|---|---|---|---|---|---|---|---|
| | | | Symm. | Asymm. | | | |
| CBPWM | [87] | High | 0.6667 | 0.7944 | Not balanced | High | Low |
| | [90] | Medium | 0.7694 | 0.9167 | Not balanced | High | Low |
| | [97] | Medium | 0.7694 | 0.9167 | Top and bottom | Medium | Medium |
| | [98] | Low | 0.6667 | 0.7944 | All switches | Low | High |
| SVPWM | [99] | Medium | 0.7694 | 0.9167 | Not balanced | High | High |
| | [100] | Low | 0.7694 | 0.9167 | Not balanced | High | High |
| | [101] | Low | 0.7694 | 0.9167 | Not balanced | Medium | High |

Using (11), the $M_{max}$ is 0.667 and 0.794 for symmetric ($\delta = \pi/3$) and asymmetric ($\delta = \pi/6$) machines, respectively. Therefore, the NSI topology is deemed more competitive when utilized in asymmetric six-phase drives. Sinusoidal modulating signals with proper offsets are used in [87]. Although the method is simple, it suffers from uneven thermal distribution among the three switches of the same leg and high switching loss. Additionally, shifting the modulating signals vertically leads to unsymmetrical switching profiles of the positive and negative half cycles which in return increases the voltage THD. Modifying the modulating signals by ZSI is investigated in [90]. The addition of the third order harmonic increases $M_{max}$ by 15.4%, similar to SVPWM technique [99]. However, the method in [90] could not reduce the switching loss.

In order to reduce the switching loss of NSI, DPWM was in [97], where one modulating signal is shifted vertically and the other one remains symmetric along the time axis, which is the modulating signal of higher magnitude. The method in [97] reduces the THD and the switching loss of the top and bottom switches. This method is extended in [98] to include the middle switch as well, achieving a minimum switching loss at the expense of complexity. Table 7 summarizes the comparison between those different modulation techniques.

#### 2) SVPWM

Based on the surveyed literature, SVPWM techniques are not as common when compared to CBPWM techniques, although they enjoy the potential of improved dc-link voltage utilization and reduced switching commutation [89], [99]. This is mainly attributed to the simplicity of the CBPWM. Conversely, the SVPWM scheme for NSI is not as involved as its six-phase VSI counterpart. For the NSI, the SVPWM scheme is found upon the hexagon of the conventional 2L three-phase VSI. However, each voltage vector of the hexagon can be generated by two redundant switching states in the NSI [91]. Hence, there are a total of 14 switching states in the SVPWM of the NSI. Nevertheless, Li *et al.* [91] argue that not all switching states are necessary to generate the desired output. In [91], a six-mode SVPWM switching sequence was proposed, which resulted in improved efficiency at the expense of slightly higher output voltage harmonics. Authors in [100] and [101] developed an SVM that provides a decoupled control for the NSI similarly as it is two 2-level 6-switch VSIs. The decoupled control in [100] and [101] eliminates the need for XOR gate to generate the PWM signals for the middle switches. In [101], the selection of voltage vectors to reduce the switching loss is considered which was not in [100].

### C. INVERTER LOSSES

Based on the foregoing relative VA ratings of VSI and NSI, the efficiency of both multi-phase inverter topologies can be evaluated by comparing the power losses incurred by the switches. For this analysis, the considered switch is SiC MOSFET (1200V/115A) by Cree (C3M0016120D). Also, the modulators used for both topologies is SPWM.

The device switching loss is determined by the rated voltage and current stress and switching frequency, while the conduction loss is determined by the average current and on-state resistance, $R_{DS(ON)}$, from the datasheet. All operating conditions including junction temperature, gate resistance and switching frequency, along with modulation index, are assumed the same. Normalized power loss with respect to the switching loss is adopted to yield a generalized comparison. Put otherwise, the rated switching loss of the SiC MOSFET is set to 1 p.u. It follows that the total per-leg switching loss for six-phase VSI is 2 p.u. The switching loss of the upper and lower switches ($S_u$ and $S_l$) in NSI is similar to that of the VSI, i.e. 1 p.u. However, the switching frequency for the middle switch ($S_m$) is twice as that of $S_u$/$S_l$. Thus, the total per-leg switching loss of NSI is 4 p.u.

The conduction loss of the SiC MOSFET can be determined by the average current and $R_{DS(ON)}$ from the datasheet. For a duty cycle $D = 0.6$, the conduction loss is found to be 0.6 p.u. per switch, or 1.2 p.u. per-leg in six-phase VSI. In NSI, the average current is higher than that of the VSI and can be determined by using (10). For $n = 6$, $I = 1.73$ and 1.93 for symmetric and asymmetric loads, respectively. Therefore, the conduction loss ratio between $S_u$ and $S_l$ to that of the VSI is $I^2$. The difference in duty cycle for $S_u$ and $S_l$ due to the modulation offset in Fig. 16 balance out when considering per-leg losses. It follows that the conduction loss for ($S_u + S_l$) is (0.6 p.u. $\times$ $2I^2$) or 3.6 p.u. and 4.5 p.u. for symmetric and asymmetric loads, respectively. Lastly, $S_m$ is only on for a fraction of $D$ equal to the modulation offset value, which is considered 0.2 herein. It follows that the conduction loss of $S_m$ is (0.6 p.u. $\times$ 0.2 $\times$ $I^2$). Thus, the

**TABLE 8. Per-unit inverter loss comparison between six-phase VSI and NSI using SiC MOSFET.**

| Type of Losses | 6-phase VSI | Symm. NSI | Asymm. NSI |
|---|---|---|---|
| Inverter VA Rating | $6EI$ | $8EI$ | $9EI$ |
| Switching Loss | 12.0 | 12.0 | 12.0 |
| Conduction Loss | 7.1 | 12.0 | 14.7 |
| **Total Loss (p.u.)** | **19.1** | **24.0** | **26.7** |

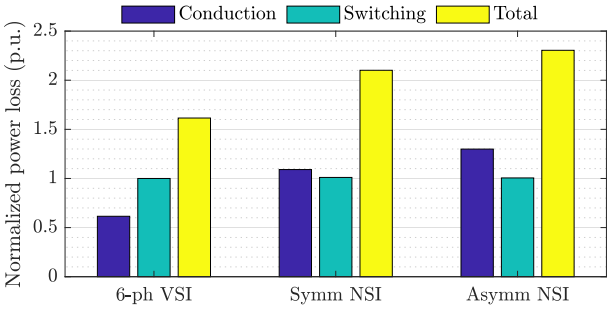


**FIGURE 17. Normalized power losses of six-phase VSI and NSI using SiC MOSFET for symmetric and asymmetric loads ($V_{dc}$ = 800 V, $f_1$ = 50 Hz, $f_s$ = 10 kHz, $M$ = 0.6, $PF$ = 1).**

total per-leg conduction loss in NSI is 4 p.u. and 4.9 p.u. for symmetric and asymmetric loads, respectively.

Table 8 summarizes the total inverter loss of NSI and VSI based on the respective VA rating of each topology. Based on this analysis, NSI is inferior to VSI in terms of inverter efficiency, and it is at its worst when supplying an asymmetric load/machine due to high $I$ rating. VSI enjoys approximately 25% and 40% higher efficiency when compared to NSI with symmetric and asymmetric loads, respectively. The same analysis was verified numerically using the thermal model of the SiC MOSFET in PLECS by Plexim. Fig. 17 depicts the normalized losses of VSI and NSI, which are in line with those tabulated in Table 8.

## V. FUTURE TRENDS

To further advance the viability and commercial feasibility of MPIs, some recent research trends have been noticed in literature. Such trends focus on improving efficiency, power density, and reliability of the MPIs. This section reviews such trends and highlights the challenges that must be addressed prior to their adoption.

### A. TOPOLOGIES

#### 1) MULTIPHASE CURRENT SOURCE INVERTER

By principle of duality, the current source inverter (CSI), shown in Fig. 18, constitute an alternative family of inverter topologies [125]. The CSI offers inherent advantages that are unavailable in VSI, such as a voltage boosting capability which enables an extended range of operation [102]–[104]. Additionally, the bulky and volatile dc-bus capacitor in the VSI is replaced with a choke input inductor, which can improve the power density of the inverter and

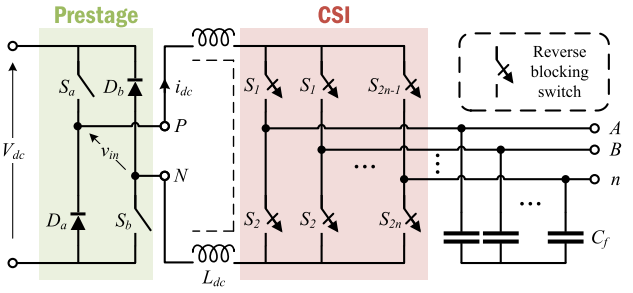


**FIGURE 18. Multiphase current source inverter (CSI) topology with prestage buck converter for voltage-to-current source conversion.**

reduce maintenance cost. Unlike the dc-bus capacitor, the input inductor is not temperature-limited and its size can be reduced by increasing the switching frequency [126]. This in turn gives way for wider operating temperatures and higher power density. Last but not least, the CSI output is PWM currents and not voltages as in VSI. Therefore, the high $dv/dt$ issue associated with VSI is non-existent in CSI [116]. The CSI requires switches with reverse blocking (RB) capability, which has conventionally been realized using Si controlled rectifiers (SCRs) or Si IGBT with a diode in series.

On the other hand, CSI suffers a relatively low efficiency and increased control complexity. Consequently, it has traditionally been considered inferior to VSI. However, with the emergence of WBG devices, as will be discussed in the next subsection, the employment of CSI drives for automotive and MEA applications has been revisited [113]–[116]. WBG devices with RB or bidiretional (BD) capabilities, such as SiC MOSFET and Gallium Nitride high electron mobility transistors (GaN HEMT), yield superior efficiency performance and reduce the size of the input inductor, thus improving the power density. An efficiency of 97.2% was reported in [113] for a three-phase CSI with RB SiC MOSFETs. Further efficiency improvement using BD GaN HEMT devices over RB SiC MOSFET was demonstrated in [114] and [115]. Extension to multiphase CSI has been reported in literature, albeit limited to five phases. In [120]–[124], five-phase CSI-fed drive operation, modulation, and fault tolerance techniques were investigated.

Nevertheless, the bottleneck for CSI in battery-powered applications is the need for a prestage converter to be installed between the battery and the CSI to provide a controlled dc-current [108], as shown in Fig. 18. The prestage is normally set to operate in continuous conduction mode, thus incurring high conduction loss [116]. The future of CSI traction inverter is promising, yet its commercialization is contingent upon overcoming its inherent drawbacks. For example, inclusion of a seventh switch (in addition to the six switches in three-phase systems), in different topologies, was proposed in [105], [106], [109] to reduce CMV. In [107], an $LC$ resonant circuit across the input inductor was proposed to enable soft-switching, and therefore, improve the inverter efficiency.

**TABLE 9.** Future trends on multiphase inverters and the challenges associated with them.

| Research Trend | Sub-category | Potential | Challenges |
|---|---|---|---|
| **Topologies** | Multiphase current source inverters | • Boosting capability<br>• Improved reliability<br>• Higher operating temperature | • High conduction loss by prestage converter<br>• Control complexity |
| | Multiphase multilevel inverters (MPMLIs) | • Higher voltage<br>• Improved EMC | • Higher complexity<br>• Increased cost |
| **WBG Devices** | SiC MOSFET | • Miniaturization<br>• High efficiency | • High EMI<br>• Oxide layer failures |
| | GaN HEMT | • High operating temperature<br>• High efficiency | • Limited breakdown voltage<br>• Gate driver design |
| **Multiphase Integrated Motor Drives** | | • Higher power density<br>• Reduced cost<br>• Improved EMC | • Complex cooling system<br>• Mechanical stress on electronics<br>• Limited space |

**TABLE 10.** Recent studies on CSI topology from different perspectives.

| Topic | Reference | Highlights |
|---|---|---|
| Inverter topology | [102]–[104] | Basic CSI topology and control for traction applications |
| Advanced topologies | [105]–[109] | Inclusion of additional switches and resonant circuits |
| Control schemes | [102], [103], [110]–[112] | Control schemes for CSI drives |
| WBG devices | [113]–[115] | Employment of SiC and GaN devices |
| Machine design | [116], [117] | CSI-specific machine design |
| Over-lap time | [118], [119] | New techniques to compensate over-lap time effects |
| Multiphase CSI | [120]–[124] | Modulation and control of multiphase CSI (predominantly 5-phase) |

A summary of recent research related to CSI from various perspectives is listed in Table 10.

#### 2) MULTIPHASE MULTILEVEL INVERTER (MPMLI)

As mentioned in Section I MLIs have been proposed for higher efficiency, reduced harmonic distortion, lower electromagnetic compatibility (EMC) requirements, and improved fault tolerance [9]. With the trend in the automotive industry to upgrade powertrains from 400 V to 800 V and beyond [7], [127], MLI is expected to compete with the dominant 2L VSI, let alone supersede it.

Multiphase MLIs (MPMLIs) have been studies in [128]–[132]. Five-, six- and seven-phase 3L neutral-point-clamped (NPC) inverters were investigated in [131], [132], and [129] and [133], respectively. The 3L T-type was examined in [128]–[130] for asymmetric six-phase drives.

Currently, the high complexity and cost associated with the high part count, make MPMLIs feasible only for MV and HV applications. However, as the market share of 800 V powertrains is expected to grow [134], [135], MPMLIs will become more feasible.

### *B. WBG DEVICES*

A paradigm shift from conventional Si IGBT to WBG devices has been noticed over the past decade, thanks to their superior material properties [136]–[138]. Normally, the term WBG is synonym to SiC MOSFET and GaN HEMT semiconductor switches as they dominate the market share of WBG devices. However, other devices such SiC junction field effect transistor (JFET) [139] and vertical GaN [138] are under development.

In terms of technology, GaN semiconductors are considered superior to SiC as they enjoy higher breakdown field, higher switching frequency, and lower $R_{DS(ON)}$ [138], [140]. In contrast, device packaging, gate driver design, and EMC are deemed more challenging for GaN HEMT due to gate and parasitics ringing arising from ultra-fast switching [37]. Yet the main shortcoming of GaN HEMT is its low voltage rating ($\leq$ 650 V). Hence, GaN devices are not applicable in traction inverters, but rather limited to on-board chargers and dc-dc converters. Fig. 19 shows the power–frequency envelope of the most famous Si, SiC and GaN power semiconductor devices, highlighting the suitability for traction inverters and on-board chargers in the automotive industry.

SiC MOSFETs enjoy a multitude of features that can be exploited to produce traction inverters with a significantly higher power density [8]. Currently, the cost premium associated with SiC is challenging its wide adoption. Despite the compelling advantages of SiC switching devices over Si counterparts, they suffer reliability issues due to the thinner gate oxide layer (typically 50 nm for SiC versus 100 nm for Si) [141]–[143]. The thinner oxide layer can introduce degradation to the gate and body diode. Since SiC switching devices experience higher stress of electric field, it has been concluded that applying positive gate voltage for a long time causes a change in the threshold voltage (i.e. the minimum voltage required to turn on the device) and vice-versa for applying a negative gate voltage. This can be explained by moving the trapped electrons or holes when a gate voltage

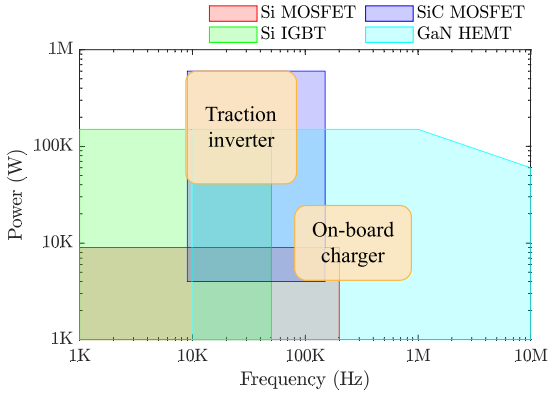


**FIGURE 19.** Power–frequency envelope of power semiconductor devices and application to the automotive industry [140].

is applied causing a shift to the threshold voltage [144]. Although this phenomenon has been reduced in the second generation of the SiC MOSFETs, still 0.25 V variation is expected. This change can be limited when applying positive and negative gate voltages [142]. The gate leakage current is another concern for SiC switching devices. MOSFETs should be capable of withstanding a short-circuit current for small periods, where these currents are usually tenfold the rated value. When MOSFET experiences short-circuit current, the entire dc-link voltage is applied across the MOSFET terminals. This introduces a high electric field that causes a leakage current from the gate to the source of the MOSFET, depending on the thickness of the gate oxide layer (which is relatively thin in SiC compared to the Si devices) and the applied electric field. This leakage current causes degradation to the gate oxide layer [145].

### C. MULTIPHASE INTEGRATED MOTOR DRIVES

The integrated motor drive (IMD) is a structural integration of the electric motor and the driving power electronics in a single unit. As a result of the physical integration, cost cutting is possible by the elimination of shielded cables and separate inverter housing [146]–[148]. The elimination of such components leads to 20%–40% volume reduction [149]. Furthermore, enhanced EMC is achieved, thanks to the direct connection between the two components. Researchers have been interested in combining the merits of IMDs with the merits of multiphase drives, such as higher torque density, lower torque ripple and improved fault tolerance, to yield a highly competitive motor drive for traction applications [53], [150]–[152]. A five-phase IMD with a disk-shaped, air-cooled inverter was proposed in [151]. The authors reported a reduced volume when compared to its three-phase counterpart, thanks to the reduction in the dc-bus capacitor. Another disk-shaped, nine-phase inverter in an IMD structure was reported in [150]. A high power density of 35 kW/L was achieved by exploiting the reduced per-phase power handling of the MPI. In [152], a six-phase IMD drive for 48 V belt starter-generators (BSGs) was suggested for mild hybrid vehicles. The six phases were divided into three direct bonded copper (DBC) modules with air-cooling.

On the contrary, thermal management and mechanical design of IMD is very challenging [147]. Such challenges are compounded in multiphase IMD due to increased electronic components, such as sensors and gate drivers [146]. A potential solution for thermal management is the employment of WBG devices that can intrinsically operate at higher temperatures when compared to Si-based counterparts. The employment of GaN HEMT in IMD is currently a hot topic of research as reported in [115], [147], [148], and [114].

## VI. CONCLUSION

This paper reviewed the state-of-the-art of multiphase (beyond three) inverters and their application in transportation electrification. Two main topologies were reviewed: voltage source inverter and nine-switch inverter. While the former is extendable to any number of phases the latter is only limited to multiples of three phases. The benefits reaped from multiphase inverters in terms of improved per-phase current handling, reduced cabling cost, dc-capacitor sizing, control flexibility were reviewed in detail and benchmarked against the conventional three-phase inverter. Comparing six-phase to three-phase inverters for example, the former employs lighter AC cables whose total cost is lower than that of the later by around 20%. Also, the volume of the dc-bus capacitor can be reduced by up to 10% or 25% when utilizing a voltage source inverter or a nine-switch inverter, respectively. Furthermore, while multiphase voltage source inverters employ a higher number of switches when compared to three-phase counterparts, both systems have the same volt-ampere rating, thus incurring similar cost in terms of power semiconductors. Such benefits make multiphase inverters suitable for high-power traction and aerospace applications.

It was found in this paper that voltage source inverter is more competitive than nine-switch inverter in terms of efficiency, fault tolerance, dc-bus voltage utilization, and cost. Although the latter employs a fewer number of switches (nine versus twelve for six-phase systems), it exhibits a higher volt-ampere rating due to the reduced number of legs, which in turn increases the current stress on the switches.

Despite the foregoing merits of multiphase inverters, they require increased number of sensors and gate driver circuitry. Additionally, design for electromagnetic compatibility can be more complex. This is due to the higher switch count, which means more sources of electromagnetic noise.

## REFERENCES

[1] B. Bilgin, P. Magne, P. Malysz, Y. Yang, V. Pantelic, M. Preindl, A. Korobkine, W. Jiang, M. Lawford, and A. Emadi, "Making the case for electrified transportation," *IEEE Trans. Transport. Electrific.*, vol. 1, no. 1, pp. 4–17, Jun. 2015.

[2] A. J. Sorensen, R. Skjetne, T. Bo, M. R. Miyazaki, T. A. Johansen, I. B. Utne, and E. Pedersen, "Toward safer, smarter, and greener ships: Using hybrid marine power plants," *IEEE Electrific. Mag.*, vol. 5, no. 3, pp. 68–73, Sep. 2017.

[3] E. Sayed, M. Abdalmagid, G. Pietrini, N.-M. Sa'adeh, A. D. Callegaro, C. Goldstein, and A. Emadi, "Review of electric machines in more-/hybrid-/turbo-electric aircraft," *IEEE Trans. Transport. Electrific.*, vol. 7, no. 4, pp. 2976–3005, Dec. 2021.

[4] L. Ulrich, "Top 10 tech cars: The trend towards all-electric is accelerating," *IEEE Spectr.*, vol. 58, no. 4, pp. 44–53, Apr. 2021.

[5] C. McKerracher, A. Izadi-Najafabadi, A. O'Donovan, N. Albanese, N. Soulpolous, D. Doherty, M. Boers, R. Fisher, C. Cantor, J. Frith, S. Mi, A. Grant, A. Zamorano-Cadavid, A. T. Abraham, K. Ampofo, N. Kou, W. Edmonds, I. Berryman, J. Landess, and J. Lyu, "Electric vehicle outlook 2020," BloombergNEF, New York, NY, USA, Tech. Rep. EVO2020, 2020. [Online]. Available: https://about.bnef.com/electric-vehicle-outlook/

[6] D.-D. Tran, M. Vafaeipour, M. El Baghdadi, R. Barrero, J. Van Mierlo, and O. Hegazy, "Thorough state-of-the-art analysis of electric and hybrid vehicle powertrains: Topologies and integrated energy management strategies," *Renew. Sustain. Energy Rev.*, vol. 119, Mar. 2020, Art. no. 109596.

[7] I. Aghabali, J. Bauman, P. J. Kollmeyer, Y. Wang, B. Bilgin, and A. Emadi, "800-V electric vehicle powertrains: Review and analysis of benefits, challenges, and future trends," *IEEE Trans. Transport. Electrific.*, vol. 7, no. 3, pp. 927–948, Sep. 2021.

[8] A. K. Morya, M. C. Gardner, B. Anvari, L. Liu, A. G. Yepes, J. Doval-Gandoy, and H. A. Toliyat, "Wide bandgap devices in AC electric drives: Opportunities and challenges," *IEEE Trans. Transport. Electrific.*, vol. 5, no. 1, pp. 3–20, Mar. 2019.

[9] A. Poorfakhraei, M. Narimani, and A. Emadi, "A review of modulation and control techniques for multilevel inverters in traction applications," *IEEE Access*, vol. 9, pp. 24187–24204, 2021.

[10] W. Taha, B. Nahid-Mobarakeh, and J. Bauman, "Efficiency evaluation of 2L and 3L SiC-based traction inverters for 400 V and 800 V electric vehicle powertrains," in *Proc. IEEE Transp. Electrific. Conf. Expo (ITEC)*, Chicago, IL, USA, Jun. 2021, pp. 625–632.

[11] J. Jenkins. (2020). *Here's Why Tesla Transitioned to a Semi-Custom Power Module Design in Model 3 Inverter. CHARGED Electric Vehicles Magazine*. [Online]. Available: https://chargedevs.com/features/heres-why-tesla-transitioned-to-a-semi-custom-power-module-design-in-model-3-inverter/

[12] C. Zhao, L. Wang, X. Yang, F. Zhang, and Y. Gan, "Comparative investigation on paralleling suitability for SiC MOSFETs and SiC/Si cascode devices," *IEEE Trans. Ind. Electron.*, vol. 69, no. 4, pp. 3503–3514, Apr. 2022.

[13] Y. Wen, Y. Yang, and Y. Gao, "Active gate driver for improving current sharing performance of paralleled high-power SiC MOSFET modules," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1491–1505, Feb. 2021.

[14] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, and F. Wang, "Active compensation of current unbalance in paralleled silicon carbide MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Fort Worth, TX, USA, Mar. 2014, pp. 1471–1477.

[15] D. Peftitsis, R. Baburske, J. Rabkowski, J. Lutz, G. Tolstoy, and H. P. Nee, "Challenges regarding parallel connection of SiC JFETs," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1449–1463, Mar. 2013.

[16] A. Salem and M. Narimani, "A review on multiphase drives for automotive traction applications," *IEEE Trans. Transport. Electrific.*, vol. 5, no. 4, pp. 1329–1348, Dec. 2019.

[17] L. Jin, S. Norrga, H. Zhang, and O. Wallmark, "Evaluation of a multiphase drive system in EV and HEV applications," in *Proc. IEEE Int. Electr. Mach. Drives Conf. (IEMDC)*, Coeur d'Alene, ID, USA, May 2015, pp. 941–945.

[18] E. Levi, F. Barrero, and M. J. Duran, "Multiphase machines and drives—Revisited," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 429–432, Jan. 2016.

[19] V. Madonna, P. Giangrande, W. Zhao, H. Zhang, C. Gerada, and M. Galea, "Electrical machines for the more electric aircraft: Partial discharges investigation," *IEEE Trans. Ind. Appl.*, vol. 57, no. 2, pp. 1389–1398, Mar./Apr. 2021.

[20] M. Alnajjar and D. Gerling, "Six-phase electrically excited synchronous generator for more electric aircraft," in *Proc. Int. Symp. Power Electron., Electr. Drives, Autom. Motion (SPEEDAM)*, Jun. 2016, pp. 7–13.

[21] S. Karugaba and O. Ojo, "A carrier-based PWM modulation technique for balanced and unbalanced reference voltages in multiphase voltage-source inverters," *IEEE Trans. Ind. Appl.*, vol. 48, no. 6, pp. 2102–2109, Nov. 2012.

[22] W. Liao, M. Lyu, S. Huang, Y. Wen, M. Li, and S. Huang, "An enhanced SVPWM strategy based on vector space decomposition for dual three-phase machines fed by two DC-source VSIs," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9312–9321, Aug. 2021.

[23] Z. Nie, M. Preindl, and N. Schofield, "SVM strategies for multiphase voltage source inverters," in *Proc. 8th IET Int. Conf. Power Electron., Mach. Drives (PEMD)*, Glasgow, U.K., 2016, pp. 1–6.

[24] Y. Zhao and T. A. Lipo, "Space vector PWM control of dual three-phase induction machine using vector space decomposition," *IEEE Trans. Ind. Appl.*, vol. 31, no. 5, pp. 1100–1109, Sep. 1995.

[25] E. Levi, "Multiphase electric machines for variable-speed applications," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 1893–1909, May 2008.

[26] I. Subotic, N. Bodo, E. Levi, and M. Jones, "Onboard integrated battery charger for EVs using an asymmetrical nine-phase machine," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3285–3295, May 2015.

[27] Z. Liu, Z. Zheng, L. Xu, K. Wang, and Y. Li, "Current balance control for symmetrical multiphase inverters," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4005–4012, Jun. 2016.

[28] J. Taylor, D. F. V. Garcia, W. Taha, M. Mohamadian, D. Luedtke, B. Nahid-Mobarakeh, B. Bilgin, and A. Emadi, "Dynamic modelling of multiphase machines based on the VSD transformation," SAE Tech. Paper 2021-01-0774, 2021.

[29] R. Bojoi, M. Lazzari, F. Profumo, and A. Tenconi, "Digital field-oriented control for dual three-phase induction motor drives," *IEEE Trans. Ind. Appl.*, vol. 39, no. 3, pp. 752–760, May/Jun. 2003.

[30] H. S. Che, E. Levi, M. Jones, W.-P. Hew, and N. A. Rahim, "Current control methods for an asymmetrical six-phase induction motor drive," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 407–417, Jan. 2014.

[31] W. Agnihotri, D. F. Valencia, W. Taha, and B. Nahid-Mobarakeh, "Virtual-flux finite control set model predictive control of dual-three phase IPMSM drives," in *Proc. 47th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Toronto, ON, Canada, Oct. 2021, pp. 1–6.

[32] H. M. Eldeeb, A. S. Abdel-Khalik, and C. M. Hackl, "Dynamic modeling of dual three-phase IPMSM drives with different neutral configurations," *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 141–151, Jan. 2019.

[33] Y. Hu, Y. Li, X. Ma, X. Li, and S. Huang, "Flux-weakening control of dual three-phase PMSM based on vector space decomposition control," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 8428–8438, Jul. 2021.

[34] W. Taha, D. F. Valencia, Z. Zhang, B. Nahid-Mobarakeh, and A. Emadi, "Adaptive flux weakening controller for dual three-phase PMSM drives in vector space decomposition," in *Proc. 47th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Toronto, ON, Canada, Oct. 2021, pp. 1–6.

[35] A. Emadi, *Advanced Electric Drive Vehicles*. Boca Raton, FL, USA: CRC Press, 2014.

[36] J. Reimers, L. Dorn-Gomba, C. Mak, and A. Emadi, "Automotive traction inverters: Current status and future trends," *IEEE Trans. Veh. Technol.*, vol. 68, no. 4, pp. 3337–3350, Apr. 2019.

[37] I. López, E. Ibarra, A. Matallana, J. Andreu, and I. Kortabarria, "Next generation electric drives for HEV/EV propulsion systems: Technology, trends and challenges," *Renew. Sustain. Energy Rev.*, vol. 114, Oct. 2019, Art. no. 109336.

[38] M. Eull, M. Preindl, and A. Emadi, "Analysis and design of a high efficiency, high power density three-phase silicon carbide inverter," in *Proc. IEEE Transp. Electrific. Conf. Expo (ITEC)*, Dearborn, MI, USA, Jun. 2016, pp. 1–6.

[39] Z. Nie and N. Schofield, "Multi-phase VSI DC-link capacitor considerations," *IET Electr. Power Appl.*, vol. 13, no. 11, pp. 1804–1811, Nov. 2019.

[40] K. Ha, C. Lee, J. Kim, R. Krishnan, and S. G. Oh, "Design and development of low-cost and high-efficiency variable-speed drive system with switched reluctance motor," *IEEE Trans. Ind. Appl.*, vol. 43, no. 3, pp. 703–713, May/Jun. 2007.

[41] P. Azer and J. Bauman, "An asymmetric three-level T-type converter for switched reluctance motor drives in hybrid electric vehicles," in *Proc. IEEE Transp. Electrif. Conf. Expo (ITEC)*, Detriot, MI, USA, Jun. 2019, pp. 1–6.

[42] (2021). *Eland Cables Calculator*. [Online]. Available: https://www.elandcables.com/cable-calculator

[43] (2021). *Flexible Motor Cables for Movement*. [Online]. Available: https://www.igus.com/chainflex/motor-cable

[44] E. Barbarini. (2018). STMicroelectronics SiC module in Tesla model 3 inverter. SYSTEMPlus Consulting. [Online]. Available: https://www.systemplus.fr/wp-content/uploads/2018/06/SP18413-STM_SiC_Module_Tesla_Model_3_Inverter_sample-2.pdf

[45] H. Wen, W. Xiao, X. Wen, and P. Armstrong, "Analysis and evaluation of DC-link capacitors for high-power-density electric vehicle drive systems," *IEEE Trans. Veh. Technol.*, vol. 61, no. 7, pp. 2950–2964, Sep. 2012.

[46] X. Lyu, Y. Li, and D. Cao, "DC-link RMS current reduction by increasing paralleled three-phase inverter module number for segmented traction drive," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 171–181, Mar. 2017.

[47] A. Rodionov, X. Huang, and Y. Liu, "Analysis of DC link current and voltage stress for motor drive application in dual three-phase configuration," in *Proc. 46th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Singapore, Oct. 2020, pp. 1267–1272.

[48] A. Safayet, M. Islam, and T. Sebastian, "Sizing of DC-link capacitor considering voltage and current ripple requirements for a 3-phase voltage source inverter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Detriot, MI, USA, Oct. 2020, pp. 1512–1518.

[49] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ, USA: Wiley, Sep. 2003.

[50] M. A. Al-Hitmi, S. Moinoddin, A. Iqbal, K. Rahman, and M. Meraj, "Space vector vs. Sinusoidal carrier-based pulse width modulation for a seven-phase voltage source inverter," *CPSS Trans. Power Electron. Appl.*, vol. 4, no. 3, pp. 230–243, Sep. 2019.

[51] C. Tan, D. Xiao, J. E. Fletcher, and M. F. Rahman, "Carrier-based PWM methods with common-mode voltage reduction for five-phase coupled inductor inverter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 526–537, Jan. 2016.

[52] Z. Liu, P. Wang, W. Sun, Z. Shen, and D. Jiang, "Sawtooth carrier-based PWM methods with common-mode voltage reduction for symmetrical multiphase two-level inverters with odd phase number," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 1171–1183, Jan. 2021.

[53] L. Verkroost, J. Van Damme, D. V. Bozalakov, F. De Belie, P. Sergeant, and H. Vansompel, "Simultaneous DC-link and stator current ripple reduction with interleaved carriers in multiphase controlled integrated modular motor drives," *IEEE Trans. Ind. Electron.*, vol. 68, no. 7, pp. 5616–5625, Jul. 2021.

[54] G.-J. Su and L. Tang, "A segmented traction drive system with a small DC bus capacitor," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Raleigh, NC, USA, Sep. 2012, pp. 2847–2853.

[55] Z. Liu, Z. Zheng, S. D. Sudhoff, C. Gu, and Y. Li, "Reduction of common-mode voltage in multiphase two-level inverters using SPWM with phase-shifted carriers," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6631–6645, Sep. 2016.

[56] A. Iqbal, E. Levi, M. Jones, and S. N. Vukosavic, "Generalised sinusoidal PWM with harmonic injection for multi-phase VSIs," in *Proc. 37th IEEE Power Electron. Spec. Conf.*, Jeju, South Korea, Jun. 2006, pp. 1–7.

[57] R. Lyra and T. Lipo, "Torque density improvement in a six-phase induction motor with third harmonic current injection," *IEEE Trans. Ind. Appl.*, vol. 38, no. 5, pp. 1351–1360, Sep./Oct. 2002.

[58] P. R. Rakesh and G. Narayanan, "Investigation on zero-sequence signal injection for improved harmonic performance in split-phase induction motor drives," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2732–2741, Apr. 2017.

[59] E. Levi, D. Dujic, M. Jones, and G. Grandi, "Analytical determination of DC-bus utilization limits in multiphase VSI supplied AC drives," *IEEE Trans. Energy Convers.*, vol. 23, no. 2, pp. 433–443, Jun. 2008.

[60] D. Dujic, E. Levi, and M. Jones, "DC bus utilisation in multiphase VSI supplied drives with a composite stator phase number," in *Proc. IEEE Int. Conf. Ind. Technol.*, Via del Mar, Chile, Mar. 2010, pp. 1495–1500.

[61] A. G. Yepes and J. Doval-Gandoy, "Extension to symmetrical and asymmetrical n-phase AC drives of simple carrier-based PWM for prolonged high DC-link utilization," in *Proc. 46th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Singapore, Oct. 2020, pp. 2733–2740.

[62] T. Zhao, Y. Zhang, H. Xu, X. Gui, and D. Xu, "DTP-PMSM drive with proportional resonant regulator and dual zero injection PWM control method," in *Proc. 21st Int. Conf. Electr. Mach. Syst. (ICEMS)*, Jeju, South Korea, Oct. 2018, pp. 1628–1633.

[63] G. Carrasco and C. A. Silva, "Space vector PWM method for five-phase two-level VSI with minimum harmonic injection in the overmodulation region," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 2042–2053, May 2013.

[64] C. Yong and H. Qiu-Liang, "Four-dimensional space vector PWM strategy for five-phase voltage source inverter," *IEEE Access*, vol. 7, pp. 59013–59021, 2019.

[65] J. Prieto, F. Barrero, M. Jones, and E. Levi, "A modified continuous PWM technique for asymmetrical six-phase induction machines," in *Proc. IEEE Int. Conf. Ind. Technol.*, Vina del Mar, Chile, Mar. 2010, pp. 1489–1494.

[66] Y. Zhu, W. Gu, K. Lu, and Z. Wu, "Vector control of asymmetric dual three-phase PMSM in full modulation range," *IEEE Access*, vol. 8, pp. 104479–104493, 2020.

[67] C. Wang, K. Wang, and X. You, "Research on synchronized SVPWM strategies under low switching frequency for six-phase VSI-fed asymmetrical dual stator induction machine," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 6767–6776, Nov. 2016.

[68] S. M. Suhel and R. Maurya, "Realization of 24-sector SVPWM with new switching pattern for six-phase induction motor drive," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5079–5092, Jun. 2019.

[69] S. M. Suhel and R. Maurya, "Modified SVPWM techniques for six-phase asymmetrical induction motor drives," in *Proc. IEEE 1st Int. Conf. Energy, Syst. Inf. Process. (ICESIP)*, Chennai, India, Jul. 2019, pp. 1–6.

[70] J. Zheng, F. Rong, P. Li, S. Huan, and Y. He, "Six-phase SVPWM with common-mode voltage suppression," *IET Power Electron.*, vol. 11, no. 15, pp. 2461–2469, Dec. 2018.

[71] M. Ippisch and D. Gerling, "Calculation of active and passive component stress of multiphase inverters with single frequency output," in *Proc. IEEE Transp. Electrific. Conf. Expo (ITEC)*, Chicago, IL, USA, Jun. 2020, pp. 420–426.

[72] M. J. Durán, J. Prieto, F. Barrero, J. A. Riveros, and H. Guzman, "Space-vector PWM with reduced common-mode voltage for five-phase induction motor drives," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4159–4168, Oct. 2013.

[73] W. N. W. A. Munim, M. F. Ismail, A. F. Abidin, and H. C. M. Haris, "Multi-phase inverter space vector modulation," in *Proc. IEEE 7th Int. Power Eng. Optim. Conf. (PEOCO)*, Langkawi, Malaysia, Jun. 2013, pp. 149–154.

[74] A. Iqbal, R. Alammari, M. Mosa, and H. Abu-Rub, "Finite set model predictive current control with reduced and constant common mode voltage for a five-phase voltage source inverter," in *Proc. IEEE 23rd Int. Symp. Ind. Electron. (ISIE)*, İstanbul, Turkey, Jun. 2014, pp. 479–484.

[75] S. M. Dabour, A. S. Abdel-Khalik, A. M. Massoud, and S. Ahmed, "Analysis of scalar PWM approach with optimal common-mode voltage reduction technique for five-phase inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1854–1871, Sep. 2019.

[76] M. Fernandez, A. Sierra-Gonzalez, E. Robles, I. Kortabarria, E. Ibarra, and J. L. Martin, "New modulation technique to mitigate common mode voltage effects in star-connected five-phase AC drives," *Energies*, vol. 13, no. 3, p. 607, Jan. 2020.

[77] B. Yu, W. Song, J. Li, B. Li, and M. S. R. Saeed, "Improved finite control set model predictive current control for five-phase VSIs," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 7038–7048, Jun. 2021.

[78] Z. Shen, D. Jiang, Z. Liu, D. Ye, and J. Li, "Common-mode voltage elimination for dual two-level inverter-fed asymmetrical six-phase PMSM," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3828–3840, Apr. 2020.

[79] M. Pulvirenti, G. Scarcella, G. Scelba, and M. Cacciato, "Space vector modulation technique for common mode currents reduction in six phase AC drives," in *Proc. 15th Eur. Conf. Power Electron. Appl. (EPE)*, Lille, France, Sep. 2013, pp. 1–10.

[80] H.-C. Vu and H.-H. Lee, "Model-predictive current control scheme for seven-phase voltage-source inverter with reduced common-mode voltage and current harmonics," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 3610–3621, Jun. 2021.

[81] M. S. Hassan, A. Abdelhakim, M. Shoyama, J. Imaoka, and G. M. Dousoky, "Three-phase split-source inverter-fed PV systems: Analysis and mitigation of common-mode voltage," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9824–9838, Sep. 2020.

[82] G. Zhang, H. Wang, Y. Yang, M. Su, C. Zhang, and F. Blaabjerg, "Common-mode voltage reduction with improved output voltage for three-to-five-phase indirect matrix converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2918–2929, Sep. 2020.

[83] U. R. Muduli, B. Chikondra, and R. K. Behera, "Space vector PWM based DTC scheme with reduced common mode voltage for five-phase induction motor drive," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 114–124, Jan. 2022.

[84] D. Yazdani, S. A. Khajehoddin, A. Bakhshai, and G. Joos, "A generalized space vector classification technique for six-phase inverters," in *Proc. IEEE Power Electron. Spec. Conf.*, Orlando, FL, USA, Jun. 2007, pp. 2050–2054.

[85] D. Yazdani, S. A. Khajehoddin, A. Bakhshai, and G. Joos, "Full utilization of the inverter in split-phase drives by means of a dual three-phase space vector classification algorithm," *IEEE Trans. Ind. Electron.*, vol. 56, no. 1, pp. 120–129, Jan. 2009.

[86] Y. He, Y. Wang, J. Wu, Y. Feng, and J. Liu, "A comparative study of space vector PWM strategy for dual three-phase permanent-magnet synchronous motor drives," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Palm Springs, CA, USA, Feb. 2010, pp. 915–919.

[87] T. Kominami and Y. Fujimoto, "Inverter with reduced switching-device count for independent AC motor control," in *Proc. 33rd Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Taipei, Taiwan, Nov. 2007, pp. 1559–1564.

[88] E. C. dos Santos, C. B. Jacobina, and O. I. da Silva, "Six-phase machine drive system with nine-switch converter," in *Proc. 37th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Melbourne, VIC, Australia, Nov. 2011, pp. 4204–4209.

[89] G. N. Goyal and M. V. Aware, "A comparative performance of six-phase nine switch inverter operation with SPWM and SVPWM," in *Proc. IEEE Int. Conf. Power Electron., Drives Energy Syst. (PEDES)*, Bengaluru, India, Dec. 2012, pp. 1–6.

[90] N. Jarutus and Y. Kumsuwan, "A carrier-based phase-shift space vector modulation strategy for a nine-switch inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3425–3441, May 2017.

[91] X. Li, L. Qu, B. Zhang, G. Zhang, and H. Liao, "A simplified modulation strategy of nine-switch inverter to cut off half of switching modes," *IEEE Access*, vol. 6, pp. 7254–7261, 2018.

[92] M. S. Diab, A. A. Elserougi, A. S. Abdel-Khalik, A. M. Massoud, and S. Ahmed, "A nine-switch-converter-based integrated motor drive and battery charger system for EVs using symmetrical six-phase machines," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5326–5335, Sep. 2016.

[93] R. Wang, C. Li, C. Liu, C. Lu, and W. Wang, "Control strategy for four-leg nine-switch inverter under unbalanced loads," *IEEE Access*, vol. 8, pp. 50377–50389, 2020.

[94] *Electrical and Electronics Technical Team Roadmap*, U.S. DRIVE Partnership, Washington, DC, USA, Oct. 2017.

[95] Z. Zeng, X. Zhang, F. Blaabjerg, H. Chen, and T. Sun, "Stepwise design methodology and heterogeneous integration routine of air-cooled SiC inverter for electric vehicle," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3973–3988, Apr. 2020.

[96] M. K. Pinjala and R. Bhimasingu, "Improving the DC-link utilization of nine-switch boost inverter suitable for six-phase induction motor," *IEEE Trans. Transport. Electrific.*, vol. 6, no. 3, pp. 1177–1187, Sep. 2020.

[97] F. Gao, L. Zhang, D. Li, P. C. Loh, Y. Tang, and H. Gao, "Optimal pulsewidth modulation of nine-switch converter," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2331–2343, Sep. 2010.

[98] F. C. de Andrade, F. Bradaschia, L. R. Limongi, and M. C. Cavalcanti, "A reduced switching loss technique based on generalized scalar PWM for nine-switch inverters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 38–48, Jan. 2018.

[99] S. M. D. Dehnavi, M. Mohamadian, A. Yazdian, and F. Ashrafzadeh, "Space vectors modulation for nine-switch converters," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1488–1496, Jun. 2010.

[100] L. Pan, J. Zhang, J. Zhang, Y. Pang, B. Wang, K. Wang, and D. Xu, "A novel space-vector modulation method for nine-switch converter," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1789–1804, Feb. 2020.

[101] J. Zhang, Y. Pang, K. Wang, D. Xu, and L. Pan, "Modulation method for nine-switch converter based on equivalent mechanism between nine-switch converter and dual six-switch converters," *IEEE Trans. Ind. Electron.*, vol. 68, no. 4, pp. 2845–2855, Apr. 2021.

[102] L. Tang and G.-J. Su, "Boost mode test of a current-source-inverter-fed permanent magnet synchronous motor drive for automotive applications," in *Proc. IEEE 12th Workshop Control Modeling Power Electron. (COMPEL)*, Boulder, CO, USA, Jun. 2010, pp. 1–8.

[103] G.-J. Su and L. Tang, "A current source inverter based motor drive for EV/HEV applications," in *Proc. SAE World Congr. Exhib.*, Detroit, MI, USA, Apr. 2011, pp. 1–10.

[104] G.-J. Su and P. Ning, "Loss modeling and comparison of VSI and RB-IGBT based CSI in traction drive applications," in *Proc. IEEE Transp. Electrif. Conf. Expo (ITEC)*, Detroit, MI, USA, Jun. 2013, pp. 1–7.

[105] W. Wang, F. Gao, Y. Yang, and F. Blaabjerg, "Operation and modulation of H7 current-source inverter with hybrid SiC and Si semiconductor switches," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 1, pp. 387–399, Mar. 2018.

[106] E. Lorenzani, F. Immovilli, G. Migliazza, M. Frigieri, C. Bianchini, and M. Davoli, "CSI7: A modified three-phase current-source inverter for modular photovoltaic applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5449–5459, Jul. 2017.

[107] M. J. Mauger, P. Kandula, and D. Divan, "Soft-switching current source inverter for next-generation electric vehicle drivetrains," in *Proc. IEEE Transp. Electrific. Conf. Expo (ITEC)*, Chicago, IL, USA, Jun. 2020, pp. 651–658.

[108] W. Taha and M. Narimani, "A modified current source inverter fed drive for electric vehicle applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Phoenix, AZ, USA, Jun. 2021, pp. 822–828.

[109] F. Akbar, H. Cha, and D.-T. Do, "CSI7: Novel three-phase current-source inverter with improved reliability," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9170–9182, Aug. 2021.

[110] Z. Wu and G.-J. Su, "High-performance permanent magnet machine drive for electric vehicle applications using a current source inverter," in *Proc. 34th Annu. Conf. IEEE Ind. Electron.*, Orlando, FL, USA, Nov. 2008, pp. 2812–2817.

[111] G.-J. Su, L. Tang, and Z. Wu, "Extended constant-torque and constant-power speed range control of permanent magnet machine using a current source inverter," in *Proc. IEEE Vehicle Power Propuls. Conf.*, Dearborn, MI, USA, Sep. 2009, pp. 109–115.

[112] R. A. Torres, H. Dai, W. Lee, T. M. Jahns, and B. Sarlioglu, "A simple and robust controller design for high-frequency WBG-based current-source-inverter-fed AC motor drive," in *Proc. IEEE Transp. Electrific. Conf. Expo (ITEC)*, Chicago, IL, USA, Jun. 2020, pp. 111–117.

[113] H. Dai, T. M. Jahns, R. A. Torres, M. Liu, B. Sarlioglu, and S. Chang, "Development of high-frequency WBG power modules with reverse-voltage-blocking capability for an integrated motor drive using a current-source inverter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Portland, OR, USA, Sep. 2018, pp. 1808–1815.

[114] H. Dai, R. A. Torres, W. Lee, T. M. Jahns, and B. Sarlioglu, "Integrated motor drive using soft-switching current-source inverters with SiC- and GaN-based bidirectional switches," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Detroit, MI, USA, Oct. 2020, pp. 2372–2378.

[115] R. A. Torres, H. Dai, W. Lee, B. Sarlioglu, and T. Jahns, "Current-source inverter integrated motor drives using dual-gate four-quadrant wide-bandgap power switches," *IEEE Trans. Ind. Appl.*, vol. 57, no. 5, pp. 5183–5198, Sep. 2021.

[116] V. Madonna, G. Migliazza, P. Giangrande, E. Lorenzani, G. Buticchi, and M. Galea, "The rebirth of the current source inverter: Advantages for aerospace motor design," *IEEE Ind. Electron. Mag.*, vol. 13, no. 4, pp. 65–76, Dec. 2019.

[117] F. Chen, H. Ding, S. Lee, W. Feng, T. M. Jahns, and B. Sarlioglu, "Current source inverter based large constant power speed ratio SPM machine drive for traction applications," in *Proc. IEEE Transp. Electrific. Conf. Expo (ITEC)*, Chicago, IL, USA, Jun. 2020, pp. 216–221.

[118] Y. Geng, R. Deng, W. Dong, K. Wang, H. Liu, and X. Wu, "An overlap-time compensation method for current-source space-vector PWM inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3192–3203, Apr. 2018.

[119] W. Suroso and T. Noguchi, "Overlap-time compensation technique for current-source power inverter," *IET Power Electron.*, vol. 13, no. 4, pp. 854–862, Mar. 2020.

[120] M. A. Elgenedy, A. S. Abdel-Khalik, A. M. Massoud, and S. Ahmed, "Indirect field oriented control of five-phase induction motor based on SPWM-CSI," in *Proc. Int. Conf. Electr. Mach. (ICEM)*, Berlin, Germany, Sep. 2014, pp. 2101–2106.

[121] M. A. Elgenedy, A. Massoud, A. S. Abdel-Khalik, A. Elserougi, and S. Ahmed, "Fault-tolerant control of five-phase current source inverter for medium-voltage drives," in *Proc. 7th IET Int. Conf. Power Electron., Mach. Drives (PEMD)*, Manchester, U.K., 2014, p. 181.

[122] M. A. Elgenedy, A. A. Elserougi, A. S. Abdel-Khalik, A. M. Massoud, and S. Ahmed, "A space vector PWM scheme for five-phase current-source converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 562–573, Jan. 2016.

[123] J. He, Y. Lyu, Q. Li, P. Guo, J. Han, H. Jia, and C. Wang, "A fault-tolerant operation approach for grid-tied five-phase current-source converters with one-phase supplying wire broken," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6200–6218, Jul. 2019.

[124] J. He, Y. Lyu, J. Han, and C. Wang, "An SVM approach for five-phase current source converters output current harmonics and common-mode voltage mitigation," *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 5232–5245, Jul. 2020.

[125] B. Wu and M. Narimani, *High-Power Converters and AC Drives*, 2nd ed. Hoboken, NJ, USA: Wiley, 2017.

[126] H. Dai and T. M. Jahns, "Comparative investigation of PWM current-source inverters for future machine drives using high-frequency wide-bandgap power switches," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, San Antonio, TX, USA, Mar. 2018, pp. 2601–2608.
[127] C. Jung, "Power up with 800-V systems: The benefits of upgrading voltage power for battery-electric passenger vehicles," *IEEE Electrific. Mag.*, vol. 5, no. 1, pp. 53–58, Mar. 2017.
[128] S. Bhattacharya, D. Mascarella, G. Joós, J. M. Cyr, and J. Xu, "A dual three-level T-NPC inverter for high-power traction applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 668–678, Jun. 2016.
[129] Z. Wang, X. Wang, M. Cheng, and W. Hua, "Direct torque control of T-NPC three-level inverter fed dual three-phase PMSM drives based on double SVM strategy," in *Proc. 19th Int. Conf. Electr. Mach. Syst.*, Chiba, Japan, 2016, pp. 1–7.
[130] X. Wang, Z. Wang, M. Cheng, and Y. Hu, "Remedial strategies of T-NPC three-level asymmetric six-phase PMSM drives based on SVM-DTC," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 6841–6853, Sep. 2017.
[131] L. Gao and J. E. Fletcher, "A space vector switching strategy for three-level five-phase inverter drives," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2332–2343, Jul. 2010.
[132] E. A. R. E. Ariff, O. Dordevic, M. Jones, and E. Levi, "Space vector PWM technique for a three-level asymmetrical six-phase drive," in *Proc. 43rd Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Beijing, China, Oct. 2017, pp. 3872–3877.
[133] O. Dordevic, E. Levi, and M. Jones, "A vector space decomposition based space vector PWM algorithm for a three-level seven-phase voltage source inverter," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 637–649, Feb. 2013.
[134] Lucid Motors. (Sep. 2020). *Lucid Motors' Proprietary Electric Drive Train Technology Powers Record-Setting Performance and Industry-Leading Efficiency in the Lucid Air*. [Online]. Available: https://www.lucidmotors.com/media-room/lucid-motors-proprietary-electric-drivetrain-technology-powers-record-setting-performance/
[135] Vitesco Technologies. (Mar. 2021). *Vitesco Technologies Wins Major Order for 800-Volt SiC-Technology in Electric Vehicles*. [Online]. Available: https://vitesco-technologies.com/en/Home/Press/21-03-24
[136] A. Bindra, "Wide-bandgap-based power devices: Reshaping the power electronics landscape," *IEEE Power Electron. Mag.*, vol. 2, no. 1, pp. 42–47, Mar. 2015.
[137] X. She, A. Q. Huang, Ó. Lucía, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017.
[138] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016.
[139] J. Bendel, "Overview of united silicon carbide normally-on JFETs," United SiC, Princeton, NJ, USA, Tech. Rep. USCi_AN0003, 2014. [Online]. Available: https://unitedsic.com/appnotes/USCi_AN0003-Overview-of-United-Silicon-Carbide-Normally-On-JFETs.pdf
[140] N. Keshmiri, D. Wang, B. Agrawal, R. Hou, and A. Emadi, "Current status and future trends of GaN HEMTs in electrified transportation," *IEEE Access*, vol. 8, pp. 70553–70571, 2020.
[141] D. Okamoto, H. Yano, K. Hirata, T. Hatayama, and T. Fuyuki, "Improved inversion channel mobility in 4H-SiC MOSFETs on Si face utilizing phosphorus-doped gate oxide," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 710–712, Jul. 2010.
[142] F. Richardeau, F. Boige, and S. Lefebvre, "Gate leakage-current, damaged gate and open-circuit failure-mode of recent SiC power MOSFET : Overview and analysis of unique properties for converter protection and possible future safety management," in *Proc. IEEE Int. Conf. Electr. Syst. for Aircr., Railway, Ship Propuls. Road Vehicles Int. Transp. Electrific. Conf. (ESARS-ITEC)*, Nottingham, U.K., Nov. 2018, pp. 1–6.
[143] Z. Ni, X. Lyu, O. P. Yadav, B. N. Singh, S. Zheng, and D. Cao, "Overview of real-time lifetime prediction and extension for SiC power converters," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7765–7794, Aug. 2020.
[144] B. Nel and S. Perinpanayagam, "A brief overview of SiC MOSFET failure modes and design reliability," *Proc. CIRP*, vol. 59, pp. 280–285, Jan. 2017.
[145] Z. Wang, X. Shi, Y. Xue, L. M. Tolbert, F. Wang, and B. J. Blalock, "Design and performance evaluation of overcurrent protection schemes for silicon carbide (SiC) power MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5570–5581, Oct. 2014.
[146] R. Abebe, G. Vakil, G. Lo Calzo, T. Cox, S. Lambert, M. Johnson, C. Gerada, and B. Mecrow, "Integrated motor drives: State of the art and future trends," *IET Electr. Power Appl.*, vol. 10, no. 8, pp. 757–771, Sep. 2016.
[147] W. Lee, S. Li, D. Han, B. Sarlioglu, T. A. Minav, and M. Pietola, "A review of integrated motor drive and wide-bandgap power electronics for high-performance electro-hydrostatic actuators," *IEEE Trans. Transport. Electrific.*, vol. 4, no. 3, pp. 684–693, Sep. 2018.
[148] A. H. Mohamed, H. Vansompel, and P. Sergeant, "An integrated modular motor drive with shared cooling for axial flux motor drives," *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 10467–10476, Nov. 2021.
[149] D. Throne, F. Martinez, R. Maguire, and D. Arnes, "Integrated motor/drive technology with rockwell connectivity," Rexroth, Bosch Group, Lohr a. Main, Germany, Tech. Rep. [Online]. Available: https://www.cmafh.com/enewsletter/PDFs/IntegratedMotorDrives.pdf
[150] P. Brockerhoff, W. Schon, P. Blaha, P. Vaclavek, and Y. Burkhardt, "Disc inverter in highly integrated 9-phase drivetrain for E-mobility," in *Proc. 17th Eur. Conf. Power Electron. Appl. (EPE ECCE-Europe)*, Geneva, Switzerland, Sep. 2015, pp. 1–9.
[151] H. Yoshida, H. Nakayama, Y. Mizukoshi, and Y. Asahara, "Study on miniaturization of an air-cooled inverter integrated with motor," in *Proc. SAE World Congr. Exhib.*, Detroit, MI, USA, 2014, pp. 1–5.
[152] J. Seong, S. Park, M. K. Kim, J. Lim, H. Han, J. Jeon, and S. W. Yoon, "DBC-packaged inverter power module for integrated motor-inverter design used in 48 V mild hybrid starter-generator (MHSG) system," *IEEE Trans. Veh. Technol.*, vol. 68, no. 12, pp. 11704–11713, Dec. 2019.

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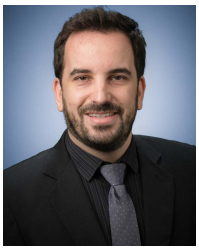

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