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# FPGA-Based Hardware-in-the-Loop Simulation of User Selection Algorithms for Cooperative Transmission Technology Over LOS Channel on Geosynchronous Satellites

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**ABSTRACT** Distributed satellite clusters and cooperative transmission technology have been used to improve the communication capability of the geosynchronous orbit (GEO) satellites in recent years. To validate the effectiveness of distributed cooperative technology, the authors designed an information transmission system using FPGA-based hardware-in-the-loop simulation. The focus of this paper is to complete the implementation of the link layer user selection algorithm to verify that cooperative transmission techniques are feasible. This system uses a Xilinx ML605 FPGA for simulating the synchronization and exchange of data during coordinated transmission in a GEO window. The authors assumed a dual-satellite scenario in the simulation used to validate the efficacy of the satellite system. After testing the system optimized with pipelining technology, the number of clock cycles was reduced by 66%. Furthermore, tests showed the system can process multi-user channel data with signal-to-noise ratios ranging from 110dB to 195dB and could select the optimal channel. Additionally, in a case study with 10 users and 2 collocated satellites, this optimized system's operation speed is approximately 2000 times faster -after hardware acceleration- than general-purpose processors, which verifies the efficacy of using distributed cooperative transmission algorithms. Because of this, the low-cost, and the low-power features, this system is a promising candidate for an embedded real-time simulation platform for GEO satellites.

**INDEX TERMS** Distributed, GEO satellite, hardware-in-the-loop, FPGA, cooperative transmission.

## I. INTRODUCTION

As a scarce ''natural resource'', GEO can only contain a limited number of satellites. Satellite constellation is a group of satellites working together as a system. Compared with a single satellite, satellite constellation can provide wider coverage and better communication performance [1]. In order to improve the capability of the GEO satellite communication system, one solution is to use a satellite transponder with higher power and higher bandwidth to improve the spectrum efficiency. But manufacturing and maintaining these powerful and complex satellite platforms would be very difficult [2], [3]. To address the shortcomings of the above conventional schemes, Visher [4] proposed distributed satellite clusters with collaborative transmission which exchanges data through an inter-satellite link. The multi-satellite configuration allows multiple satellites to operate within a single GEO window.

Nevertheless, due to its low spectrum efficiency and transmission capacity, the multi-satellite configuration technology needs to be further improved. To mitigate these two problems discussed above, multiple-input multiple-output (MIMO) techniques have been proposed as a promising approach to improve the performance of wireless communication. MIMO technique has shown its advantages of improved throughput, spatial gain, diversity, as well as interference reduction when applied in communication systems [5], [6]. Some preliminary research has been conducted on the feasibility of MIMO application in GEO satellite configuration (GEOSC).

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Sakarellos and Panagopoulos [7] evaluated the outage performance of a cooperative hybrid satellite-terrestrial LMS system and found that in most cases, the cooperative system outperforms the single satellite system. Zuo *et al.* [8] researched polarized modulation and spatial multiplexing schemes by conducting a fair comparison of the performance of a single and a dual-satellite system, and proposed a polarized modulation scheme for dual-polarization MIMO mobile satellite broadcasting systems. Kourogiorgas and Panagopoulos [9] used analytical expressions to compute the outage capacity statistics for a MIMO satellite system. Research shows that a $2 \times 2$ MIMO system outperformed both a single satellite and a dual combining diversity scheme system. Schwarz *et al.* [10] modeled the line of sight (LOS) satellite channel, which allows the study of the optimal capacity of satellite-based MIMO communication links. Base on previous work, Dou *et al.* [11] proposed a user selection strategy for cooperative transmission in a LOS satellite channel collocation system. Their study shows that the system achieved a cooperative gain compared to non-cooperative systems and high-power single satellite systems in terms of transmission rate. Xiao *et al.* [12] experimented on applying cooperative transmission to low earth orbiting satellite communication systems. The result shows that cooperative transmission improves the previous probability of communication and system performance, and the terminal's power is also reduced. Bai *et al.* [13] proposed a more realistic cooperative transmission scheme which has taken multipath components into consideration, in addition to, LOS components. User selection strategy with opportunistic beamforming is studied in an attempt to optimize the system capacity.

In MIMO satellite communication systems, the cooperative transmission scheme measures the user channel capacity and makes user selection based on the capacity, then the scheme allows matching user stations to start the transmission. So far, the work on cooperative transmission has only been carried out theoretically [11], [13].

With the increase of the user set, the speed of simulating the cooperative transmission mechanism in MIMO satellite communication systems using pure software algorithms can no longer meet the real-time requirements, and the software simulation cannot visually simulate the operation of the system. To address the above limitations, this paper implements the simulation of GEO collocated satellites system by hardware-in-the-loop (HIL) technology. Hardware-in-the-loop (HIL) simulation technique is a real-time simulation technique that includes hardware components, which allows us to test real systems under different realistic workloads and conditions, and can use hardware instead of some critical and complex mathematical models [14], [15].

FPGAs have the advantage of low latency, low power consumption, and powerful parallel processing capability, which is a significant advantage for multi-channel data processing, and its parallel processing capability and high speed are particularly suitable as an ideal operating platform for MIMO communication systems [16]–[18]. However, the hardware implementation of the channel capacity solution has not been discussed in existing research. Moreover, the HIL simulation of cooperative transmission in GEO collocated satellites communication systems still needs further research.

In this paper, we propose a HIL simulation platform that can perform the verification of distributed GEO satellite cooperative transmission system. The simulation platform is based on a HOST PC, a network switch, and the ML605 development kit from Xilinx. The HOST PC simulates the relaying of user signals by the satellite, and the FPGA in the ML605 implements the cooperative transmission algorithm to process the signals and match the combination of users with the optimal channel capacity in the set of satellite point beams. At the same time, the design process uses pipelining technology to optimize the hardware structure, so that the operation time of the cooperative transmission algorithm under multiple users is reduced to about 34% of the original, which greatly improves the simulation efficiency of the system.

Reviews of current researches can confirm that theoretically, cooperative transmission can improve the performance of GEO satellite communication systems in terms of channel capacity and spectrum utilization. And this improvement does not rely on the upgrading of satellite hardware. Therefore, cooperative transmission has great application potential by deploying in the existing GEO satellite communication system at a relatively low cost. Before the technology can be used in the application, a dedicated experimental platform is needed to evaluate the operation of the cooperative transmission in a hardware circuit. However, so far, very limited research has been done on actual hardware circuits. In response to the above problems, the main contributions of this research include:

(1) Demonstrate the technical details of implementing a cooperative transmission on an FPGA, including the RTL circuit implementation of algorithms, the connection of internal modules, and the timing of data input and output. Furthermore, an effective application of pipelining technology to optimize the hardware structure of the core module, which shortens the runtime of key algorithms in the strategy. Hardware resources and clock cycles of the core algorithm have also been discussed, which provides a reference for any future research.

(2) Provide a novel design of a cooperative transmission scheme simulation platform for GEO satellite communication. And base on the design, we built a dedicated HIL platform using an FPGA and a PC. The complete process of the cooperative transmission has been successfully simulated.

(3) Set up a demonstration scenario for actual applications using the HIL simulation platform. The experiments validated the theoretical derivation of the cooperative transmission scheme, and proved its effectiveness in practical applications.

The rest of this paper is organized as follows: Section II reviews the system model of the cooperative collocated satellites. Section III explains the design of cooperative transmission system. Section IV presents the timing optimization

of distributed cooperative algorithm verification system. Section V discusses the experiment results of the system. Section VI concludes the paper and identifies important future work.

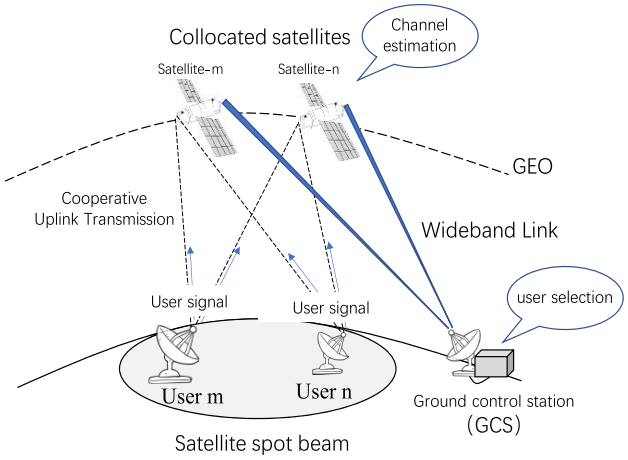


**FIGURE 1.** System model for cooperative juxtaposition of satellites and ground users. Collocated satellites are located in GEO and receive the user signals from the same spot beam. User signals are sent collocated satellites using cooperative transmission. Satellites forward the received signals to the GCS through wideband link.

## II. SYSTEM MODEL OF COOPERATIVE COLLOCATED SATELLITES

The system model of the cooperative collocated satellites is shown in Figure 1. For simplicity, Figure 1 shows only the case of two satellites and two users, with an assumption that each user and satellite within a point beam is equipped with a single antenna [10]. In this paper, we focus on uplinks with a cooperative transmission strategy, where, in general, the ground control center assigns a specific frequency and time slot to two selected users, using a specific selection strategy for cooperative transmission. The selected users then simultaneously transmit signals to the juxtaposed geostationary orbit satellites, while the satellite located in the same geographical window forwards the received signals to the ground control station for signal processing via another wideband link. The Ground control station (GCS) takes care of signal processing and allocates transmission resources to the selected users following the user selection algorithm. Channel estimation is performed before the signal is transmitted through a wideband link.

### A. POSITION MODEL OF SATELLITE AND GROUND USERS

In order to build a mathematical model of the cooperative collocated satellites, a description of the position relationship between the ground user and the satellite is required. In this paper, we use a Cartesian coordinate system to determine a location on the Earth as shown in Figure 2. The longitude of the *m-th* satellite is represented by $\theta_{s,m}$, and the position vector of the *m-th* satellite in the Cartesian coordinate system is shown in (1) [10].

$$\alpha_{s,m} = [R_s \cos\theta_{s,m}, R_s \sin\theta_{s,m}, 0]^T \tag{1}$$

where $R_s$ denotes the distance from the satellite to the center of the Earth. The geographic location of the ground user is denoted by $(\theta_u, \varphi_u)$, $\theta_u$ is longitude, and $\varphi_u$ is dimensionality. Therefore, the midpoint location between two ground users can be given by (2).

$$\alpha_{uc} = \begin{pmatrix} R_e \cos(\varphi_{uc})\cos(\theta_{uc}) \\ R_e \cos(\varphi_{uc})\sin(\theta_{uc}) \\ R_e \sin(\varphi_{uc}) \end{pmatrix} \tag{2}$$

where $R_e = 6378.1$km, denotes the radius of the Earth. Since GEO is 35,786km above ground level, $R_s = R_e + 35,786$km.

According to the literature [11], the position vector of two ground users in any direction can be represented by (3).

$$\alpha_{u,m} = \begin{pmatrix} x_{uc} - kd(\sin\theta_{uc}\cos\delta_{uc} + \sin\varphi_{uc}\cos\theta_{uc}\sin\delta_{uc}) \\ y_{uc} - kd(\cos\theta_{uc}\cos\delta_{uc} + \sin\varphi_{uc}\sin\theta_{uc}\sin\delta_{uc}) \\ z_{uc} - kd(\cos\varphi_{uc}\sin\delta_{uc}) \end{pmatrix} \tag{3}$$

where $d$ denotes the distance from the ground user to the middle position. where $k$ represents the *m-th* user on the ground. When $k = 1$, $m = 1$; when $k = -1$, $m = 2$. the distance from the *m-th* satellite to the *n-th* user is denoted as (4).

$$r_{m,n} = \left\| \alpha_{s,m} - \alpha_{u,n} \right\| \tag{4}$$

where $m = 1, 2$; $n = 1, 2$.

### B. CHANNEL CAPACITY

According to the literature [11], it is known that the GEO to ground terminal channel model usually contains both LOS components and multipath signal components. For the satellite radio channel, the main radio wave consists mainly of the LOS signal component because the power of the LOS signal is larger than that of the NLOS signal. Therefore, it is feasible for the satellite channel model to ignore the multipath component. According to the free-space propagation model, each element of the channel matrix can be given by (5).

$$\mathbf{H}_{m,n} = \rho_{m,n} \exp(-j2\pi f_c \frac{r_{m,n}}{c_0}) \tag{5}$$

where $f_c$ is the central frequency point, $c_0$ is the speed of light, and $\rho_{m,n}$ is the complex envelope. When the carrier phase angle is $\phi_0$, $\rho_{m,n} = (c_0 e^{j\phi_0}/4\pi f_c r_{m,n})$. Since the distance from the satellite to the ground user is long, p can be treated as a constant [13].

According to Shannon's theory, the capacity of a conventional single-input single-output (SISO) satellite communication system can be derived from (6).

$$C_{SISO} = \log_2(1 + SNR_{SISO} \cdot |h_{SISO}|^2) \tag{6}$$

$h_{SISO}$ is the channel gain between the transmitter and receiver, and $SNR_{SISO}$ is the signal-to-noise ratio of the transmitter.

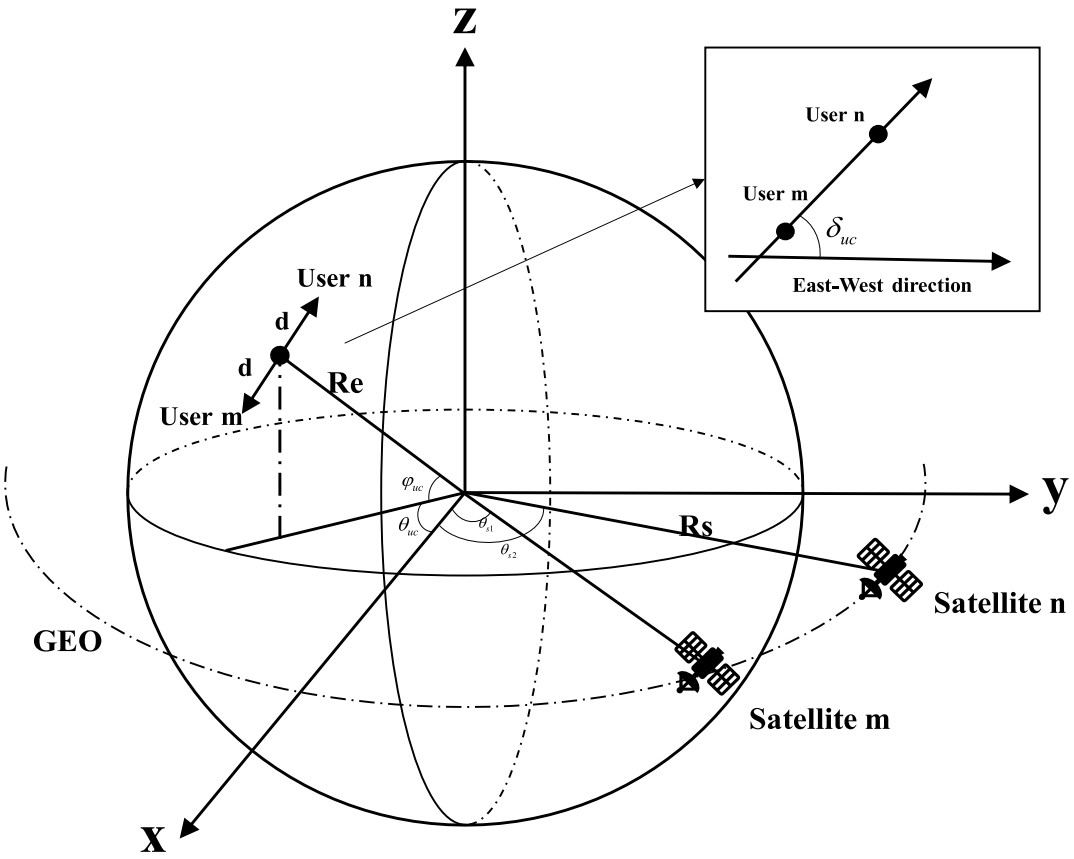


**FIGURE 2.** Location of ground users and satellites in the system. $\delta_{uc}$ is the angle between the east-west direction and the direction of the straight line connecting two arbitrary ground users. The positive direction of the z-axis is the north pole of the earth.

Since the cooperative collocated satellite system can be considered as a MIMO system, the channel capacity can be derived from (7) [11], [13].

$$C_{MIMO} = \log_2\{\det(I_m + SNR_{MIMO}{}^{*}\mathbf{H}\mathbf{H}^H)\} \tag{7}$$

where $\mathbf{H}$ is the channel matrix, $\mathbf{H}^H$ is the conjugate transpose of the channel matrix, and $SNR_{MIMO}$ is the signal-to-noise ratio of each transmitting antenna. Since the scenario set in this paper is that two satellites receive signals from two users at the same time, the channel matrix is two rows and two columns.

The elements in the channel matrix are obtained by channel estimation. In a multi-user MIMO system, the signal received by the receiver can be expressed as (8).

$$\mathbf{Y} = \mathbf{H}\mathbf{X} + n \tag{8}$$

During the coding process, the pilot sequence has been inserted into the user signal, and the least squares algorithm solves the channel response according to the variation law of the pilot. The pilot signal is located in the physical layer. It carries a combination of signals on a specific frequency carrier. Our effort is to realize the algorithm on the link layer, and does not involve verification of the communication standard and protocol. Therefore, we can preset the number and combination of pilots in the physical layer. In this paper, channel estimation with 4 pilot carrier points is used, and the results of LS channel estimation are given by (9).

$$\hat{\mathbf{H}}_{LS} = \mathbf{X}^{-1}\mathbf{Y} \tag{9}$$

where $\mathbf{Y} = \{y_1, y_2, y_3, y_4\}$ is the demodulated user signal at the receiver, $\mathbf{X} = \{x_1, x_2, x_3, x_4\}$ is the known pilot signal, and $\hat{\mathbf{H}}_{LS} = \{h_1, h_2, h_3, h_4\}$ is the channel response solved by the least squares algorithm. In order to make the channel estimation results more accurate, the channel response should also be averaged. The final channel estimation result is given by (10).

$$\hat{H} = \frac{h_1 + h_2 + h_3 + h_4}{4} \tag{10}$$

### C. USER SELECTION STRATEGY

The user selection strategy in the cooperative transmission is able to select the combination of communication pairs in

**Algorithm 1** User Selection Algorithm for Cooperative Transmission

**Initialize:** $SNR_{MIMO}$: the signal-to-noise ratio of each transmitting antenna; $H_{m,n}$: channel response of *m-th* satellite to the *n-th* user; $N$: amount of users; **H**: channel matrix.
**Step 1:** The *i*-th terrestrial user sends a cooperative transmission request to the satellite.
**Step 2:** $1 \le i \le N$, $i \le j \le N$;
$\mathbf{H}(1,1) \leftarrow H_{1,i}$; $\mathbf{H}(1,2) \leftarrow H_{1,j}$;
$\mathbf{H}(2,1) \leftarrow H_{2,i}$; $\mathbf{H}(2,1) \leftarrow H_{2,j}$;
$C_{MIMO} \leftarrow \log_2\{\det(I_m + SNR_{MIMO} * \mathbf{H}\mathbf{H}^H)\}$;
**Step 3:**
**If** All possible user combination pairing methods have been completed. **then**
Proceed to Step 4.
**else**
Return to Step 2.
**Step 4:** The user group corresponding to the maximum channel capacity is selected as the final user group for this communication.
**Step 5:** The serial number of the selected user group is returned to the computer and this round of the algorithm ends.

the current set of users that maximizes the system capacity according to some rule in the set. The multi-user selection algorithm design steps are generally, first construct the user data channel matrix or set, and select the data one by one to maximize the system capacity according to some rule that applies to that data set, and then store and return the optimal solution to the system to improve the throughput of the communication system. Our user selection algorithm is designed based on the previous work of Dou *et al.* [11] and described as follows.

In this paper, we simulate the channel capacity of single-satellite and two-satellite cooperative systems using MATLAB, and discuss the results in Section V.

Data precision is an important design consideration when accelerating an algorithm using an FPGA. Generally, lower data precision can save on hardware resources and computation time at the cost of degrading accuracy. 16-bit fixed-point numbers are used to calculate the optimal channel capacity, the relative error in comparison to the results from 32-bit floating-point numbers are plotted in Figure 3. Figure 3 (a) and (b) show the relative errors when the two different data precisions are used in a single satellite system and a dual cooperative satellites system, respectively. It is observed that at lower SNR, using 16-bit fixed-point numbers leads to a relative error peak of 0.72536 at 120dB, however, at high SNR, the relative error is close to 0. The key contributor to these results is the low channel capacity at low SNR which receives a significant impact from the reduction of data precision. Nevertheless, the data precision has little influence on the large channel capacity at high SNR. Due to the fact that low SNR is an important scenario to be considered for the cooperative transmission algorithm, a high precision data type: 32-bit floating-point numbers are selected for the hardware implementation.

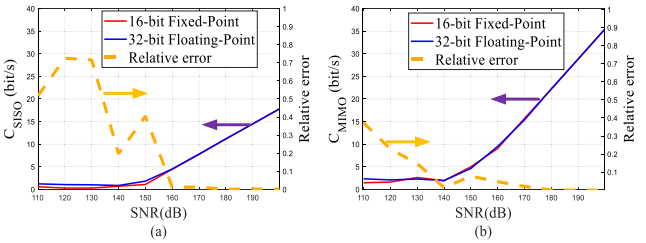


**FIGURE 3.** Relative error due to reduced data precision. (a) Relative errors of the single satellite system. (b) Relative errors of the dual cooperative satellites system.

## III. DESIGN OF COOPERATIVE TRANSMISSION SYSTEM

The simulation platform consists of a HOST PC and an ML605 FPGA board. They are connected and exchange data through an Ethernet interface. The schematic diagram of the simulation platform is shown in Figure 4. The HOST PC simulates the process of the satellite transferring user signals to GCS. The HOST PC used in this experiment is configured with an Intel Core i7-5500U processor at 2.40 GHz, 8 GB of DDR3 memory, Gigabit Ethernet. It runs Windows 10 Professional 64-bit operating system. We developed the HOST Software using Visual Studio. It controls the HOST PC's Gigabit Ethernet for sending and receiving data which is encapsulated in a MAC frame format. HOST Software and Virtual Channel are deployed on the HOST PC. HOST Software is used to (1) configure the MAC addresses of HOST PC and ML605, (2) send user signal (Y) processed by Virtual Channel and a pilot signal (X), and (3) collect and display the results returned by ML605. The above three functions correspond to the Parameter, Source, and Statistics in Figure 4, respectively. The modulation and scrambling of the original source are done through Virtual Channel. It is worth noticing that the Virtual Channel is not integrated into the HOST Software. One advantage of this is that the channel environment and modulation simulated by the platform can be easily changed. The distributed cooperative algorithm verification system is deployed on the ML605 to simulate the execution process of GCS making user selection in a cooperative collocated satellites system. In order to recover the user signal (Y) and pilot signal (X) before modulation and scrambling, the distributed cooperative algorithm verification system also performs Demodulate and Channel Estimation.

The source on HOST PC includes user signal (Y) and pilot signal (X), both of which are stored in Gray code. After the original source is sent to the Virtual Channel, it undergoes 16-QAM modulation and scrambling, in particular, superimposing Gaussian white noise to the source. The channel model is the Line-of-Sight channel. We superimposed Gaussian white noise without considering channel fading due to that

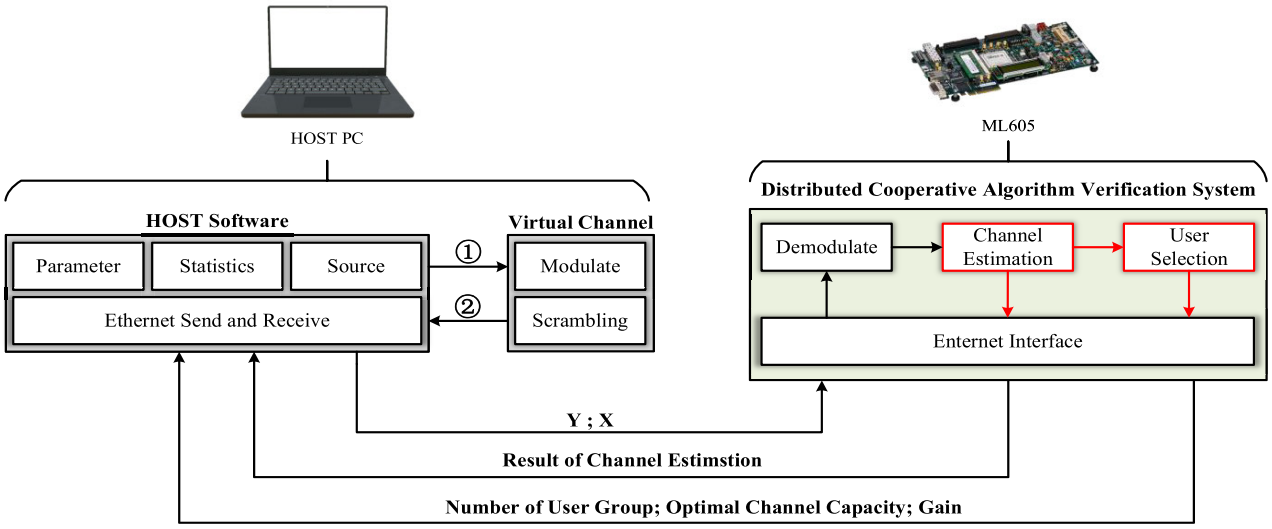


**FIGURE 4.** Schematic diagram of the hardware-in-the-loop simulation platform for distributed cooperative algorithms. ①: The original Source is output to the virtual channel, ②: HOST Software reads the modulated and scrambled Source.

our focus is on the implementation of the data link layer algorithm. The channel model building and channel impairment emulation are based on MATLAB. No additional toolbox was used in the emulation. The MATLAB functions that can generate Gaussian white noise include *wgn*, *awgn*, and *randn*. In this paper, the *awgn* function is used to superimpose Gaussian white noise to the signal. Then the channel data output by the Virtual Channel is stored in text format on the HOST PC. HOST Software reads the channel data and sends it to ML605 through the Ethernet interface. The distributed cooperative algorithm verification system deployed on ML605 demodulates the received channel data first, and then performs channel estimation. The result of channel estimation is the user-to-satellite channel information, which will be used as the input data of user selection. At the same time, the output result of the channel estimation module of the distributed cooperative algorithm verification system will also be returned to the HOST PC through the Ethernet interface and displayed on the HOST Software user interface. The user selection module returns the user combination, the optimal channel capacity, and the capacity gain compared to a single satellite system to the HOST PC. In Figure 4, the red-colored annotated blocks in the distributed cooperative algorithm verification system are Channel Estimation and User Selection modules, which are implemented in hardware in Section A and B later in this chapter.

According to the mathematical analysis of the channel data in Section II, if there are $N$ users in the beam at the current user point, the length of the user signal and the guide signal data at the 4 pilot carrier points are $4 \times N$. With the aid of the pilot carrier, the original channel information, i.e., the input data for the user selection algorithm, is recovered using the channel estimation algorithm in Section II. This data is of length $N$ and has two sets containing the elements of the channel matrix. One set is the channel information from each user in each user set to *m-th satellite*, denoted by *Satellite-m*, abbreviated as *S_m*. The other set is the

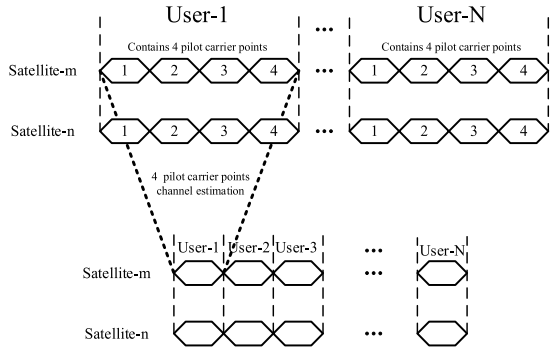


**FIGURE 5.** Data processing process of user signal Y and pilot carrier X after channel estimation to get the channel matrix.

channel information from each user to satellite n, denoted by *Satellite-n*, abbreviated as *S_n*. The data processing process of the demodulated user signal and the guide frequency signal to obtain the channel matrix elements after channel estimation is shown in Figure 5 which will be further elaborated in Section III-A hardware implementation of the channel estimation algorithm.

The reasoning in Section II shows that the data in the system calculation process are all complex data. In order to ensure the calculation accuracy, both the real and imaginary parts of the above complex data are 32-bit single-precision floating-point numbers. Xilinx's Floating-Point Operator IP core can perform 15 common mathematical operations related to floating-point numbers, which can simplify the complexity of FPGA design. Therefore, this IP core is mainly used in the design process to complete the mathematical operations of floating-point numbers.

### A. HARDWARE IMPLEMENTATION OF CHANNEL ESTIMATION ALGORITHM

From (9), it is clear that the core operation of the channel estimation algorithm is the user signal divided by the pilot carrier signal. Due to the limitation of the hardware

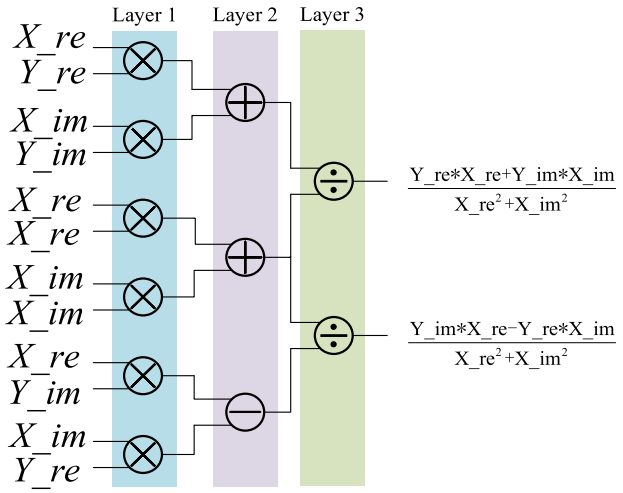


**FIGURE 6.** Hardware structure of complex division. The first layer is the multiplication layer, the second layer is the addition layer, and the third layer is the division layer.

description language, the complex data in the operation needs to be split into two parts, the real part and the imaginary part, for representation. The results of dividing the real and imaginary parts of the user signal and the structure of the complex divider are shown in Figure 6.

The hardware implementation of the channel estimation module is shown in Figure 7. The real and imaginary parts of the user signal (Y) and the pilot carrier signal (X) are input to the channel estimation module and are first cached in an internal register set. After all of them are cached, each set of data is entered into the complex division module in turn for operation. The real and imaginary parts of the quotient are stored in their respective buffer register groups in order. According to (10), it is also necessary to average the data of the four adjacent quotients. In order to reduce the computational time consumption, the averaging of the least-squares channel estimation results for $N$ users with 4 pilot carrier points is performed in parallel. The channel estimation module has two outputs, the real part and the imaginary part of the channel estimation result. To ensure the reliability of data interaction and transmission, the real and imaginary parts of the final channel estimation result are first stored in the output buffer register.

### B. HARDWARE IMPLEMENTATION OF THE USER SELECTION ALGORITHM

According to the user selection strategy in Section II. it can be known that the purpose of the user selection algorithm is to find a pair of users in the current set of users and the channel capacity under that user combination is the maximum. The core of the user selection algorithm is to calculate the channel capacity under different user channel combinations by (7).

Under a single satellite, it is equivalent to the SISO communication system. Its channel capacity is calculated by (6). The hardware architecture in Figure 8 implements the solution of the channel capacity under a single satellite. It is important to note that the Floating-Point Operator IP core provides only the logarithmic operation with base $e$. To calculate, it is necessary to obtain the logarithm by using the $e$. If $\log_2 a$ is calculated, it needs to be obtained by $(\ln a/\ln 2)$.

The cooperative parallel satellite system in this paper is equivalent to the $2 \times 2$ MIMO system. Therefore the channel matrix is two rows and two columns. Each row represents a different satellite and each column represents a different user selected. The *i-th* user in the set of users is defined as $User - m$ and the *j-th* user is defined as $User - n$, where $1 \le i \le N, i \le j \le N$. Figure 9 shows a schematic diagram of the composition of the channel matrix.

Under the MIMO communication system, the channel capacity is calculated by (7). Each element in the channel matrix is a complex number and the matrix operation in Eq. is an obstacle due to the limitation of the Verilog language. Therefore, in this paper, a hardware structure is designed to calculate $\mathbf{HH}^H$.

Suppose the real part of $S\_m$ is $S\_m\_re = \{a_1, a_2, \cdots, a_N\}$; the imaginary part of $S\_m$ is $S\_m\_im = \{b_1, b_2, \cdots, b_N\}$; the real part of $S\_n$ is $S\_n\_re = \{A_1, A_2, \cdots, A_N\}$; the imaginary part of $S\_n$ is $S\_n\_im = \{B_1, B_2, \cdots, B_N\}$. Taking $i = 1$ and $j = 2$ as examples, the $\mathbf{H}$-matrix at this time is given by (11).

$$\mathbf{H} = \begin{bmatrix} a1 + b1i & a2 + b2i \\ A1 + B1i & A2 + B2i \end{bmatrix} \tag{11}$$

The corresponding $\mathbf{H}^H$ matrix is given by (12).

$$\mathbf{H}^H = \begin{bmatrix} a1 - b1i & A1 - B1i \\ a2 - b2i & A2 - B2i \end{bmatrix} \tag{12}$$

Then $\mathbf{HH}^H(1,1)$ is $a1 \cdot a1 + b1 \cdot b1 + a2 \cdot a2 + b2 \cdot b2$; the real part of $\mathbf{HH}^H(1,2)$ and $\mathbf{HH}^H(2,1)$ is $a1 \cdot A1 + b1 \cdot B1 + a2 \cdot A2 + b2 \cdot B2$; the imaginary part of $\mathbf{HH}^H(1,2)$ and $\mathbf{HH}^H(2,1)$ is $-(a1 \cdot B1 - b1 \cdot A1 + a2 \cdot B2 - b2 \cdot A2)$; and $\mathbf{HH}^H(2,2)$ is $A1 \cdot A1 + B1 \cdot B1 + A2 \cdot A2 + B2 \cdot B2$. Based on the above results, the hardware structure of matrix multiplication as shown in Figure 10 is implemented.

According to (7) and the user selection strategy introduced in Section II, the hardware of the user selection module is implemented as shown in Figure 11. The algorithm is performed in two ways, the first being the solution of the single-satellite channel capacity $C_{SISO}$. The second way is the solution of the channel capacity $C_{MIMO}$ for all user combinations in the two-satellite cooperative system. When the $C_{MIMO}$ is calculated for all user combinations, the maximum value $C_{MIMO-\max}$ is found by a comparator, and the user combination corresponding to $C_{MIMO-\max}$ is used as the final communication combination. At the same time, the module also calculates the gain of $C_{MIMO-\max}$ with respect to $C_{SISO}$ and one of the most final outputs.

### C. LATENCY STATISTICS FOR HARDWARE DESIGN OF KEY OPERATIONS IN DISTRIBUTED COOPERATIVE ALGORITHM VERIFICATION SYSTEM

The operations in the algorithm are performed by the Floating-Point Operator IP cores, and the runtime of the hardware design depends on the clock cycles spent by the IP cores

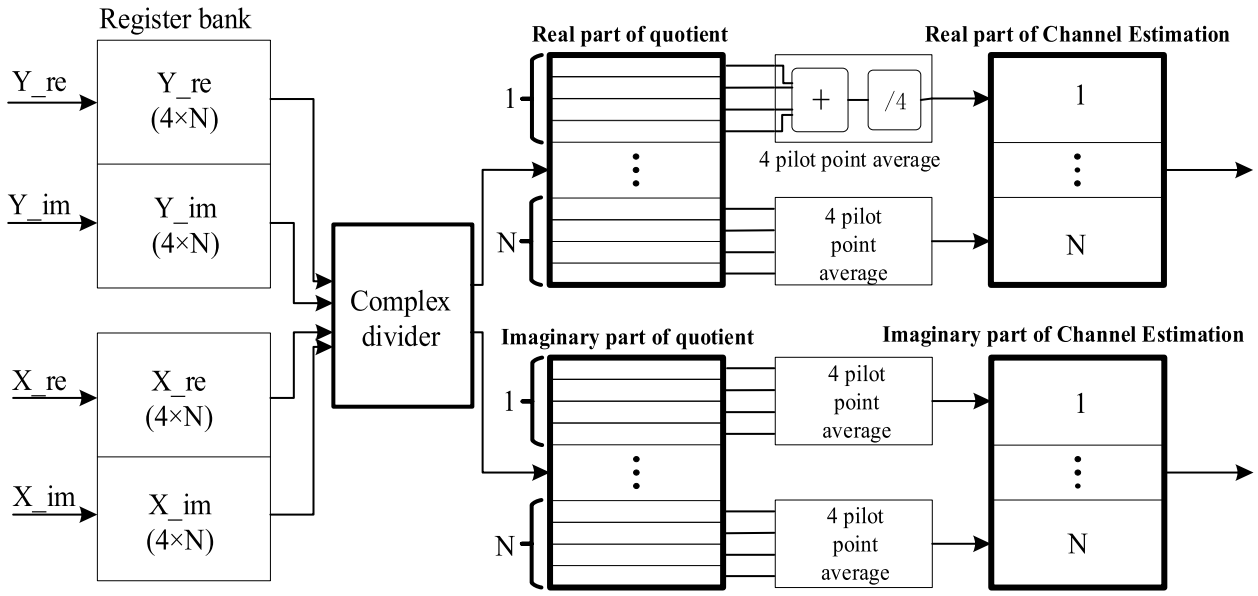


**FIGURE 7.** Hardware structure of the 4 pilot carrier points-based channel estimation algorithm.

**TABLE 1.** Clock cycles required for the operation of key hardware modules in the algorithm.

| Algorithm | Design | Operation (Maximum latency of each step) | DSP | Latency (Cycle) | Total Latency (Cycle) |
|---|---|---|---|---|---|
| Channel Estimation | Complex division | multiply | 2 | 8 | 44 |
| | | add(subtract) | - | 8 | |
| | | divide | 3 | 28 | |
| | Mean of 4 | add | - | 8 | 44 |
| | | add | - | 8 | |
| | | divide | 3 | 28 | |
| | $\log_2$ | ln | 13 | 28 | 56 |
| | | divide | 3 | 28 | |
| User Selection | $C_{SISO}$ | multiply | 2 | 8 | 96 |
| | | add | - | 8 | |
| | | add | - | 8 | |
| | | multiply | 2 | 8 | |
| | | add | - | 8 | |
| | | $\log_2$ | 16 | 56 | |
| | $HH^H$ | multiply | 2 | 8 | 24 |
| | | add(subtract) | - | 8 | |
| | | add | - | 8 | |
| | $\det(I + SNR * HH^H)$ | multiply | 2 | 8 | 32 |
| | | multiply(add) | 2 | 8 | |
| | | multiply(add) | 2 | 8 | |
| | | subtract | - | 8 | |
| | Gain | subtract | - | 8 | 36 |
| | | divide | 3 | 28 | |

to perform the mathematical operations. During the design process, the invoked Floating-Point Operator IP cores are set in Non-Block mode. The Floating-Point Operator IP cores require 8 clock cycles for addition, subtraction, and multiplication, and 28 clock cycles for division and logarithm.

In the hardware design scheme of this paper, the clock cycles spent by the core part of the algorithm to complete one operation are shown in Table 1.

## IV. TIMING OPTIMIZATION OF DISTRIBUTED COOPERATIVE ALGORITHM VERIFICATION SYSTEM

A detailed description of the hardware design of the two core algorithms in the distributed cooperative algorithm verification system has been made in Section III. The user selection algorithm under the cooperative collocated satellites is more complex, and the hardware implementation of (7) is a difficult

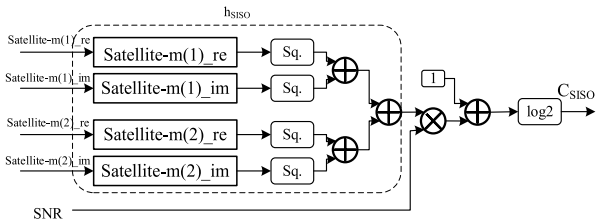


**FIGURE 8.** Hardware architecture for single-satellite channel capacity calculation.

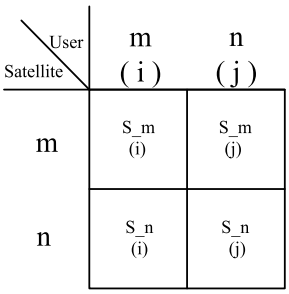


**FIGURE 9.** Schematic diagram of channel matrix composition.

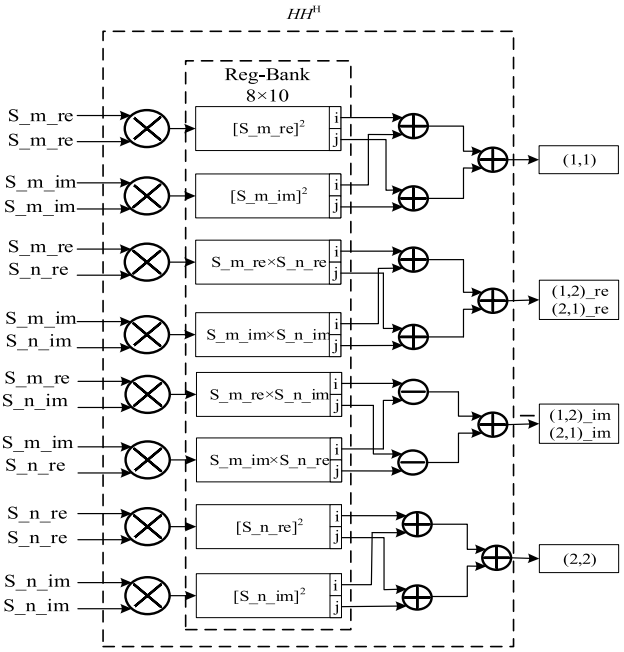


**FIGURE 10.** Hardware architecture of the channel matrix and its conjugate transpose multiplication.

point. Together with Figure 11, we can find that during the design process, we disassemble the formula into three parts, and each part is designed as a separate hardware module. These three parts complete the calculation of $\mathbf{HH}^H$, the calculation of $\det(I + SNR^* \mathbf{HH}^H)$, and finally the logarithmic operation of the second part, respectively. Each part reads and writes data from buffer registers, and let the clock cycles each part needs to spend be $T_{\mathbf{HH}^H}$, $T_{\det}$ and $T_{\log}$, respectively, and the time spent to complete a complete computation task is $T_{task}$. If there are n user combinations in the user set, the time taken to compute the channel capacity of all user combinations under the cooperative collocated satellites system is $T_{sum}$. The total time taken without pipeline structure optimization is shown in (13).

$$T_{sum} = n \times T_{task} = n \times (T_{\mathbf{HH}^H} + T_{\det} + T_{\log}) \tag{13}$$

After the introduction of the 3-stage pipeline structure. The total elapsed time is shown in (14), and it is clear that $T_{P\_sum} < T_{sum}$.

$$\begin{aligned} T_{P\_sum} = {} & T_{\mathbf{HH}^H} + \max(T_{\mathbf{HH}^H}, T_{\det}) \\ & + \max(T_{\mathbf{HH}^H}, T_{\det}, T_{\log}) \times (n-2) \\ & + \max(T_{\det}, T_{\log}) + T_{\log} \end{aligned} \tag{14}$$

As an example, we set the number of user combinations to 3, and the comparison of the computation timings of the conventional and optimized pipeline structures is shown in Figure 12. It can be found that the computation time of (7) can be significantly reduced by using pipeline optimization.

Based on Table 1 and the simulation timings, 112 clock cycles are required to calculate $C_{MIMO}$ for one user combination. At user combinations of 3, the functional simulation is performed for the $C_{MIMO}$ calculation module without pipeline structure optimization. Since there is no sub-module splitting, the next calculation can only be performed after the previous user combination is finished, so it takes 3 full calculation cycles to complete the above simulation, totaling 342 clock cycles. The simulation timing of the behavior of the $C_{MIMO}$ computational module without pipeline structure optimization is shown in Figure 13.

If the computation process of $C_{MIMO}$ is split, the sub-computation processes of different user combinations can be executed in parallel. After the pipeline optimization, part of the computation process of each user combination can be performed in parallel, which greatly reduces the overall computation time. When the number of user combinations is 3, the functional simulation of the $C_{MIMO}$ computing module with the optimized pipeline structure is carried out, and the process takes a total of 116 clock cycles to complete after the optimization. It can be found that the overall computation time is significantly reduced, and the optimized structure of the pipeline will be more significant with more user combinations. The simulation timings of the behavior of the $C_{MIMO}$ calculation module under flowline structure optimization are shown in Figure 14.

## V. EXPERIMENT RESULTS

An FPGA-based HIL simulation platform reflecting the schematic shown in Figure 4 has been developed to validate the design. The HOST PC is a Personal Computer equipped with a general-purpose CPU and an Ethernet interface. The ML605 evaluation board has a Virtex-6 series FPGA model number XC6VLX240T-1FFG1156. ML605 utilizes

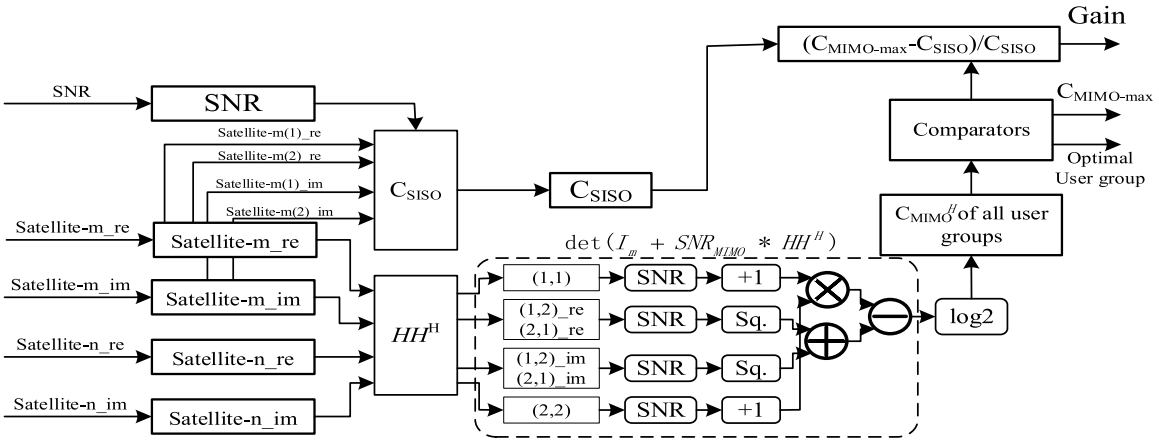


**FIGURE 11.** Hardware architecture of the user selection algorithm. The input data of this architecture is the result of channel estimation. The capacity of a single satellite system is calculated by $C_{SISO}$. The capacity of a dual cooperative satellite system is calculated by $HH^H$, $det(I_m+SNR_{MIMO}*HH^H)$, and log2.

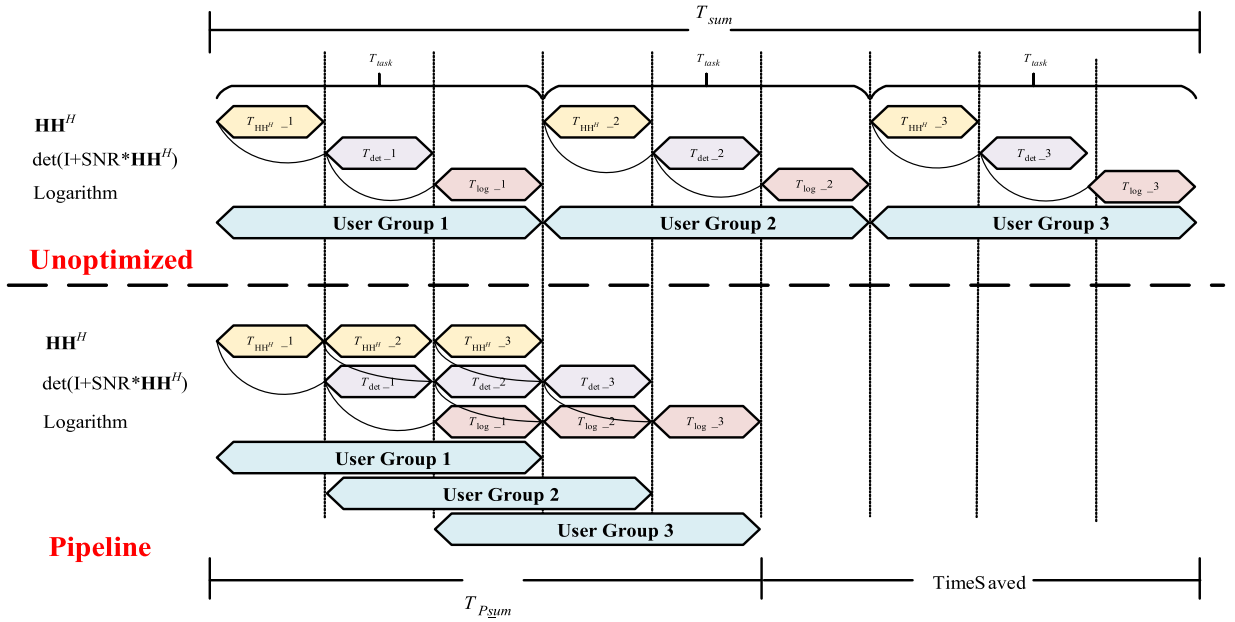


**FIGURE 12.** Timing optimization of the streamline structure for complex formula calculations.

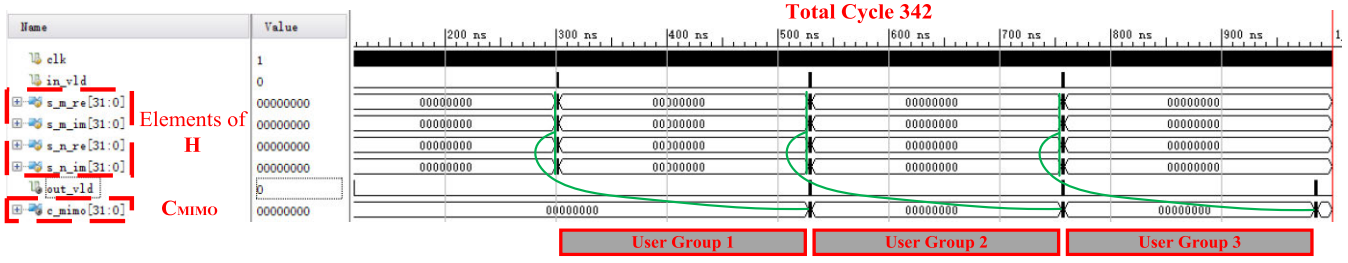


**FIGURE 13.** Simulation time for the behavior of the $C_{MIMO}$ computational module without pipeline structure optimization.

the onboard Marvell Alaska PHY device to do Ethernet communication at speeds of 10, 100 or 1000 Mb/s. The board supports MII, GMII, RGMII and SGMII interfaces from FPGA to PHY. In our implementation, the HOST PC communicates with ML605 on 1000 Mb/s, and the PHY interface mode is RGMII.

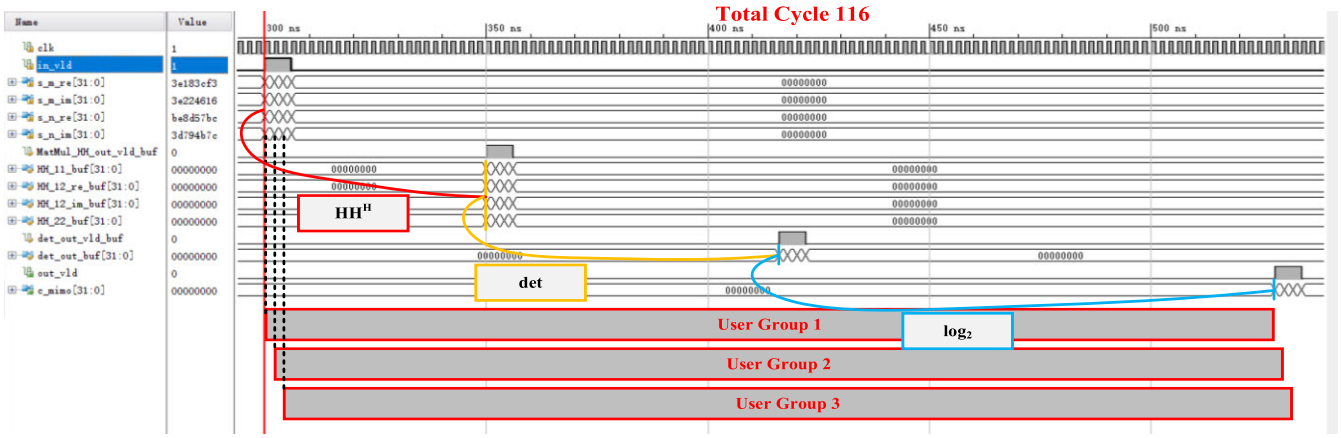


**FIGURE 14.** Timing of the simulation of the behavior of the $C_{MIMO}$ calculation module with pipeline structure.

The HOST PC and ML605 are connected using an Ethernet cable on which data exchange is carried out. First, we start the HOST Software on the HOST PC, and download the bitstream file of verification system hardware design to the FPGA on the ML605 board through the USB JTAG interface. Then we can configure the MAC addresses of the HOST PC and ML605 in the software. When using the HIL simulation platform to test the user selection strategy for cooperative transmissions, the channel data processed by the Virtual Channel should first be loaded in the HOST Software. Then the HOST Software will send the channel data to ML605 through the Ethernet interface. For the distributed cooperative algorithm verification system running on ML605, the calculated results will be returned to the HOST PC via Ethernet and displayed on the user interface of HOST Software. The designed software interface displays two main areas: source and statistics.

In the source area, channel data with different signal-to-noise ratios can be loaded for transmission. Channel data is generated by Virtual Channel and stored in the HOST PC. The statistics area is used to display the result of channel estimation module and user selection module returned by the Ethernet interface. As discussed in Section III A and B, the channel estimation results include *satellite-m_re, satellite-m_im, satellite-n_re, satellite-n_im*. The results from the user selection module include Number of User Group, Optimal Channel Capacity and Gain. The output result of the Channel Estimation module will be displayed on the left side of the statistics area, and the results from the user selection module will be displayed on the right side.

Table 2 lists the resource consumption. The resources used are LUT, FF and BRAM. The optimization with the pipeline structure does not significantly increase the resource consumption. Only the FF consumption is increased by 0.04%.

We compared the channel capacity of a single satellite and dual cooperative satellite systems using MATLAB. Figure 15 shows their channel capacity under different SNRs. The dual cooperative satellite system presents an overall higher channel capacity than the single satellite system. The results of the software algorithm will be used as a reference for the simulation and test results of the hardware acceleration to follow.

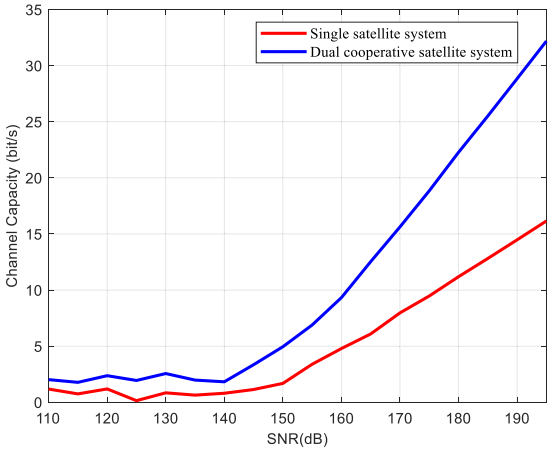


**FIGURE 15.** Comparison of optimal channel capacity for single-satellite system and dual-satellite system.

**TABLE 2.** Resource consumption.

| Resource | Pipeline | | Without Pipeline | |
|---|---|---|---|---|
| | Used | Utilization(%) | Used | Utilization(%) |
| LUT | 126242 | 61.94 | 126242 | 61.94 |
| LUTRAM | 5040 | 7.88 | 5040 | 7.88 |
| FF | 214776 | 52.69 | 214614 | 52.65 |
| BRAM | 399 | 89.66 | 399 | 89.66 |
| DSP | 79 | 9.40 | 79 | 9.40 |
| IO | 34 | 6.80 | 34 | 6.80 |
| BUFG | 8 | 25.00 | 8 | 25.00 |
| MMCM | 2 | 20.00 | 2 | 20.00 |

Behavioral simulation of the distributed cooperative algorithm verification system with a user set of 10. One of the core functions of the distributed cooperative algorithm verification system is to perform channel estimation on the user channel data from the Virtual Channel to solve the channel response.

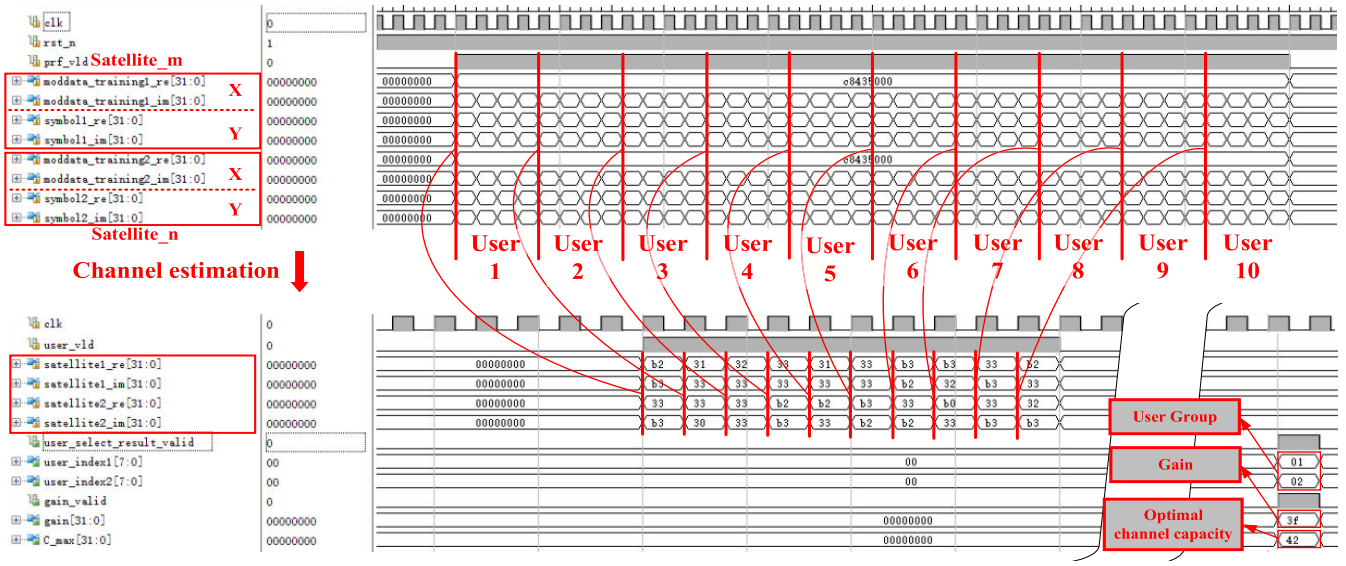


**FIGURE 16.** Input and output timing diagram for the behavioral simulation of the channel estimation module. Output timing diagram for the simulation of the user selection module behavior.

For the channel estimation module, its input data are the pilot carrier (X) and user signals (Y) of the two satellites with all users. The output of the channel estimation module is the final channel response. This result will be used as input to the module selected by the user for further processing.

Another core function of the distributed cooperative algorithm verification system is to match the combination of users within the set of users that results in the optimal channel capacity by means of a user selection algorithm. The final output for the user selection module is the two user numbers in the user combination, the optimal channel capacity, and the channel capacity gain relative to the single-satellite system. The timing diagram of the channel estimation module simulation and the output timing of the user selection module simulation are shown in Figure 16.

The test results for the hardware-in-the-loop simulation system are shown in Figure 17. A total of 18 sets of typical channel data are shown at different SNRs. The final test results show that the optimal channel capacity increases with the increase of SNR under the dual-satellite cooperative operation. At low SNRs, the gain of the optimal channel capacity under the dual-satellite cooperative operation is larger than that of the single-satellite optimal channel capacity. It can be seen that the cooperative transmission algorithm significantly improves the channel capacity at low SNRs and also at high SNRs.

In the simulation system, the FPGA's clock frequency is 200MHz, and it takes 2251 clock cycles to finish a complete round of the cooperative algorithm in the scenario set in this paper, which takes about 11.255$\mu$s. In the same test scenario, a complete round of cooperative algorithm with MATLAB on a computer with an Intel i7 5500U processor takes about 22000$\mu$s. The simulation platform with FPGA is

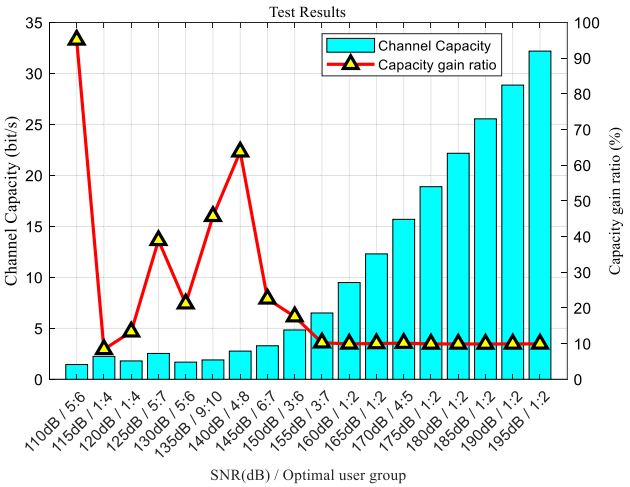


**FIGURE 17.** Optimal channel capacity test results on the hardware-in-the-loop platform.

about 2000 times faster than the general-purpose processor platform and takes significantly less time than the general-purpose computer.

## VI. CONCLUSION

This research was undertaken to design a novel FPGA-based platform to simulate cooperative transmission for the GEO satellite communication systems. We demonstrated the technical details of implementing such a design. This research is the first investigation of hardware-based verification of cooperative transmission technology and confirmed its effectiveness in increasing channel capacity and improving communication performance. The hardware acceleration makes

our simulation platform approximately 2000 times faster compared with a Core i7-5500U general-purpose processor in certain experimental scenarios. By using pipeline optimization, the simulation system has gained the real-time processing capability of the cooperative transmission algorithm. Our FPGA-based HIL simulation system will prove useful in expanding to future satellite communication systems by simulating the process of data processing in real-time at a much lower cost than experimenting on real multi-satellite systems.

A natural progression of this work is to adapt the system to simulate multi-user cooperative transmission in different scenarios, such as different channel conditions, a larger number of satellites, or a larger user set. A further study could assess the signal transmission with different noise models and explore applying noise reduction technology in cooperative transmission systems.

## REFERENCES


[1] W. Hasbi, "Tracking capability and detection probability assessment of space-based automatic identification system (AIS) from equatorial and polar orbiting satellites constellation," *IEEE Access*, vol. 8, pp. 184120–184136, 2020, doi: 10.1109/ACCESS.2020.3029093.

[2] A. Winterstein and L. A. Greda, "An adaptive calibration and beamforming technique for a GEO satellite data relay," *Int. J. Satell. Commun. Netw.*, vol. 36, no. 2, pp. 207–219, May 2017.

[3] A. Mengali *et al.*, "Ground-to-GEO optical feeder links for very high throughput satellite networks: Accent on diversity techniques," *Int. J. Satell. Commun. Netw.*, pp. 1–22, 2020. [Online]. Available: https://onlinelibrary.wiley.com/doi/10.1002/sat.1372, doi: 10.1002/sat.1372.

[4] P. S. Visher, "Satellite clusters," *Satell. Commun.*, vol. 5, pp. 22–24, 1979.

[5] E. Rohani, J. Xu, T. Che, M. Rahman, G. Choi, and M. Lu, "Asynchronous baseband processor design for cooperative MIMO satellite communication," in *Proc. IEEE 57th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2014, pp. 833–836, doi: 10.1109/MWSCAS.2014.6908544.

[6] M. Rahman, E. Rohani, J. Xu, and G. S. Choi, "An improved soft decision based MIMO detection using lattice reduction," *Int. J. Comput. Commun. Eng.*, vol. 3, no. 4, pp. 264–268, 2014.

[7] V. K. Sakarellos and A. D. Panagopoulos, "Outage performance of cooperative land mobile satellite broadcasting systems," in *Proc. 7th Eur. Conf. Antennas Propag. (EuCAP)*, Gothenburg, Sweden, 2013, pp. 473–476.

[8] B. Zuo, K. Zhao, W. Li, and N. Zhang, "Polarized modulation scheme for mobile satellite MIMO broadcasting," in *Proc. IEEE Int. Wireless Symp. (IWS)*, Mar. 2015, pp. 1–4, doi: 10.1109/IEEE-IWS.2015.7164605.

[9] C. I. Kourogiorgas and A. D. Panagopoulos, "Multi satellite MIMO systems at Ka band and above: Outage capacity analysis using bivariate IG distribution," in *Proc. 8th Eur. Conf. Antennas Propag. (EuCAP)*, The Hague, The Netherlands, Apr. 2014, pp. 1031–1034.

[10] R. T. Schwarz, A. Knopp, B. Lankl, D. Ogermann, and C. A. Hofmann, "Optimum-capacity MIMO satellite broadcast system: Conceptual design for LOS channels," in *Proc. 4th Adv. Satell. Mobile Syst.*, Bologna, Italy, 2008, pp. 66–71, doi: 10.1109/ASMS.2008.19.

[11] S. Dou, L. Bai, J. Xie, and Z. Xiao, "Cooperative transmission for geostationary orbiting satellite collocation system," in *Proc. IEEE Global Commun. Conf.*, Austin, TX, USA, Dec. 2014, pp. 2880–2885.

[12] X. Jie, F. Shaodong, Z. Gengxin, and W. Fan, "Research on amplify-and-forward strategy of cooperative diversity in low Earth orbiting satellite mobile communication system," in *Proc. Int. Conf. Comput. Sci. Service Syst. (CSSS)*, Nanjing, China, Jun. 2011, pp. 1583–1586, doi: 10.1109/CSSS.2011.5974514.

[13] L. Bai, L. Zhu, J. Choi, F. Liu, and Q. Yu, "Cooperative transmission over Rician fading channels for geostationary orbiting satellite collocation system," *IET Commun.*, vol. 11, no. 4, pp. 538–547, Sep. 2017.

[14] F. Wang, S. J. Zhang, and X. B. Cao, "Research and semi physical simulation for the compensation observer of wheel low speed friction," *J. Syst. Simul.*, vol. 17, no. 3, pp. 613–616, 2005.

[15] F. Wang, X. Cao, Y. Yang, and D. Gao, "Small satellite large angle attitude maneuver hardware-in-the-loop simulation based on three-axis air bearing table," in *Proc. AIAA Modeling Simulation Technol. Conf. Exhib.*, Keystone, CO, USA, Aug. 2006, p. 6733.

[16] S. Sharma, S. Kulkarn, V. Pujari, M. Vanitha, and P. Lakshminarsimhan, "FPGA implementation of M-PSK modulators for satellite communication," in *Proc. Int. Conf. Adv. Recent Technol. Commun. Comput.*, Kottayam, India, Oct. 2010, pp. 136–139.

[17] L. Guo-dong and R. Jian, "The spatial MIMO channel implement on FPGA," in *Proc. Int. Conf. Electr. Control Eng.*, Wuhan, China, Jun. 2010, pp. 2443–2446.

[18] H. Zhang, J. Chen, and W. Wu, "An FPGA-based MIMO-OFDM with golden decoding," in *Proc. IET Int. Commun. Conf. Wireless Mobile Comput. (CCWMC)*, Shanghai, China, 2011, pp. 355–358.


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